(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
02 May 2024 (02.05.2024)

(10) **International Publication Number**
WO 2024/091819 A1

(51) **International Patent Classification:**
H10N 97/00 (2023.01) *H01L 21/02* (2006.01)
H10B 53/30 (2023.01) *H01L 21/285* (2006.01)

(21) **International Application Number:** PCT/US2023/077120

(22) **International Filing Date:** 17 October 2023 (17.10.2023)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) **Priority Data:**
17/976,689 28 October 2022 (28.10.2022) US

(71) **Applicant: KEPLER COMPUTING INC.** [US/US]; 180 Steuart Street #192524, San Francisco, California 94105 (US).

(72) **Inventors: MANIPATRUNI, Sasikanth**; 16335 NW Rossetta Street, Portland, Oregon 97229 (US). **MUKHERJEE, Niloy**; 2586 Tamworth Lane, San Ramon, California 94582 (US). **SATO, Noriyuki**; 845 Altaire Walk, Palo Alto, California 94303 (US). **GOSAVI, Tanay**; 10997 NW Ironwood Lane, Portland, Oregon 97124 (US). **MANFRINI, Mauricio**; Geldenaaksebaan 173, 3001 Heverlee (BE). **RATHI, Somilkumar J.**; 1703 Bevin Brook Drive, San Jose, California 95112 (US). **CLARKSON, James David**; 1264 Kilcrease Circle, El Sobrante, California 94083 (US). **DOKANIA, Rajeev Kumar**; 16889 NW Desert Canyon Drive, Beaverton, Oregon 97006 (US). **OLAOSEBIKAN, Debo**; 403 Main Street #308, San Francisco, California 94105 (US). **MATHURIYA, Amrita**; 16335 NW Rossetta Street, Portland, Oregon 97229 (US).

(74) **Agent: MUGHAL, Usman**; MUGHAL GAUDRY & FRANKLIN PC, 1500 NW Bethany Blvd., Suite 200, Beaverton, Oregon 97006 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV,

(54) **Title:** ITERATIVE METHOD OF MULTILAYER STACK DEVELOPMENT FOR DEVICE APPLICATIONS

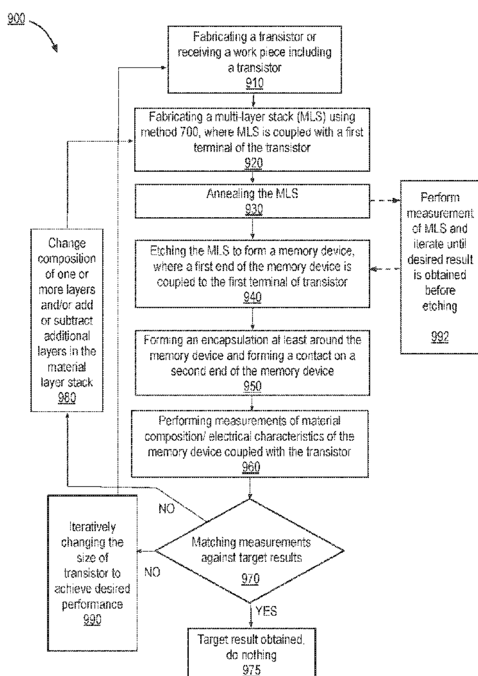


FIG. 9

(57) **Abstract:** A method to deposit a multi-layer stack for device applications includes implementing a model driven target selection for deposition. One or more targets may be procured with an initial stoichiometric composition or elemental purity. The targets may be utilized to form the multi-layer stack, and measurements may be made of chemical composition and electrical properties of the multi-layer stack. The measurements may be compared to reference target values and if measurement results are not within tolerance, the composition of the targets can be changed to yield a successive multi-layer stack. The process can be iterated until measurement results are within tolerance of target results. Additional experimentation with post deposition thermal anneal can be performed to optimize multi-layer stack properties.

WO 2024/091819 A1

[Continued on next page]

GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

ITERATIVE METHOD OF MULTILAYER STACK DEVELOPMENT FOR DEVICE APPLICATIONS

CLAIM FOR PRIORITY

[0001] This application claims priority to U.S. Patent Application No. 17/976,689, filed on October 28, 2022, titled "ITERATIVE METHOD OF MULTILAYER STACK DEVELOPMENT FOR DEVICE APPLICATIONS," and which is incorporated by reference in entirety.

BACKGROUND

[0002] Fabrication of multilayer stack including a ferroelectric material for memory applications is challenging.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The material described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Also, various physical features may be represented in their simplified "ideal" forms and geometries for clarity of discussion, but it is nevertheless to be understood that practical implementations may only approximate the illustrated ideals. For example, smooth surfaces and square intersections may be drawn in disregard of finite roughness, corner-rounding, and imperfect angular intersections characteristic of structures formed by nanofabrication techniques. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0004] **Figure 1** is a flow diagram of a method of iteratively developing a multilayer stack for application to memory devices, in accordance with an embodiment of the present disclosure.

[0005] **Figure 2A** is a representative tri-layer stack, in accordance with an embodiment of the present disclosure.

[0006] **Figure 2B** schematically illustrates a perovskite crystal structure of a polar layer of the material layer stack in **Figure 2A**, in accordance with an embodiment of the present disclosure.

[0007] **Figure 3A** is a flow diagram of a method illustrating iterations in a multilayer stack deposition as performed utilizing one or more targets in a tool, in accordance with an embodiment of the present disclosure.

[0008] **Figure 3B** is a flow diagram of a method illustrating iterations in a multilayer stack deposition as performed utilizing one or more targets in a tool, in accordance with an embodiment of the present disclosure.

[0009] **Figure 4** is a polarization vs. electric field plot for a representative multi-layer stack including a ferroelectric material.

[0010] **Figure 5** is a flow diagram of a method of iteratively developing a multilayer stack for application to memory devices, where the method further includes annealing the multilayer stack, in accordance with an embodiment of the present disclosure.

[0011] **Figure 6** is a cross-sectional illustration of a multi-layer stack including a ferroelectric material, deposited in accordance with the flow diagram in **Figure 1**, in accordance with an embodiment of the present disclosure.

[0012] **Figure 7** is a flow diagram of a method of iteratively developing a memory device, in accordance with an embodiment of the present disclosure.

[0013] **Figure 8A** is a cross-sectional illustration of a memory device obtained by patterning the multi-layer stack obtained in **Figure 7**.

[0014] **Figure 8B** is a cross-sectional illustration of a plurality of memory devices, where individual memory devices are at least laterally surrounded by an encapsulation layer.

[0015] **Figure 9** is a flow diagram of a method of iteratively developing a memory device coupled with transistor, in accordance with an embodiment of the present disclosure.

[0016] **Figure 10** is a cross-sectional illustration of a 1T-1C transistor device, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0017] At least one embodiment describes an iterative method of multi-layer stack development for device applications. While various embodiments are described with reference to ferroelectric random-access memory (FeRAM) or paraelectric random-access memory (RAM), capacitive structures formed herein can be used for any application where a capacitor is desired. For example, the capacitive structure can be used for fabricating ferroelectric based or paraelectric based majority gate, minority gate, and/or threshold gate. In the following description, numerous specific details are set forth, such as structural schemes and detailed fabrication methods to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as process equipment and device operations, are

described in lesser detail to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0018] In some instances, in the following description, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present disclosure. Reference throughout this specification to "an embodiment" or "one embodiment" or "some embodiments" means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrase "in an embodiment" or "in one embodiment" or "some embodiments" in various places throughout this specification are not necessarily referring to the same embodiment of the disclosure. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0019] As used in the description and the appended claims, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses all possible combinations of one or more of the associated listed items.

[0020] The terms "coupled" and "connected," along with their derivatives, may be used herein to describe functional or structural relationships between components. These terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical, optical, or electrical contact with each other. "Coupled" may be used to indicated that two or more elements are in either direct or indirect (with other intervening elements between them) physical, electrical or in magnetic contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause an effect relationship).

[0021] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one component or material with respect to other components or materials where such physical relationships are noteworthy. For example, in the context of materials, one material or material disposed over or under another may be directly in contact or may have one or more intervening materials. Moreover, one material disposed between two materials may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first material "on" a second material is in direct contact with that second material.

Similar distinctions are to be made in the context of component assemblies. As used throughout this description, and in the claims, a list of items joined by the term “at least one of” or “one or more of” can mean any combination of the listed terms.

[0022] The term “adjacent” here generally refers to a position of a thing being next to (e.g., immediately next to or close to with one or more things between them) or adjoining another thing (e.g., abutting it).

[0023] The term “signal” may refer to current signal, voltage signal, magnetic signal, or data/clock signal.

[0024] The term “device” may generally refer to an apparatus according to the context of the usage of that term. For example, a device may refer to a stack of layers or structures, a single structure or layer, a connection of various structures having active and/or passive elements, etc. Generally, a device is a three-dimensional structure with a plane along the x-y direction and a height along the z direction of an x-y-z Cartesian coordinate system. The plane of the device may also be the plane of an apparatus which comprises the device.

[0025] Unless otherwise specified in the explicit context of their use, the terms “substantially equal,” “about equal” and “approximately equal” mean that there is no more than incidental variation between two things so described. In the art, such variation is typically no more than +/-10% of a predetermined target value.

[0026] The terms “left,” “right,” “front,” “back,” “top,” “bottom,” “over,” “under,” and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. For example, the terms “over,” “under,” “front side,” “back side,” “top,” “bottom,” “over,” “under,” and “on” as used herein refer to a relative position of one component, structure, or material with respect to other referenced components, structures, or materials within a device, where such physical relationships are noteworthy. These terms are employed herein for descriptive purposes only and predominantly within the context of a device z-axis and therefore may be relative to an orientation of a device. Hence, a first material “over” a second material in the context of a figure provided herein may also be “under” the second material if the device is oriented upside-down relative to the context of the figure provided. Similar distinctions are to be made in the context of component assemblies.

[0027] The term “between” may be employed in the context of the z-axis, x-axis or y-axis of a device. A material that is between two other materials may be in contact with one or both of those materials. In another example, a material that is between two or other material may be separated from both of the other two materials by one or more intervening materials. A

material "between" two other materials may therefore be in contact with either of the other two materials. In another example, a material "between" two other materials may be coupled to the other two materials through an intervening material. A device that is between two other devices may be directly connected to one or both of those devices. In another example, a device that is between two other devices may be separated from both of the other two devices by one or more intervening devices.

[0028] Capacitors with a wide variety of materials are implemented for memory applications such as RAM applications. Nonlinear polar materials offer a wide array of technologically important properties, including ferroelectricity, piezoelectricity, metal-like electrical conductivity, semiconduction, pyroelectricity, etc. Perovskites are an example of non-linear polar material (i.e., materials with the chemical formula ABO_3). Perovskite materials are implemented in capacitors for high density FeRAM applications owing to their low power consumption and high on/off ratio. Perovskite FeRAM devices (herein FeRAM devices) may be desirable over other forms of memory, such as magnetic tunnel junction (MTJ)memory device for fabrication advantages. The MTJ can include a stack of 10 or more layers. In contrast, a perovskite based FeRAM device may include three layers for functionality. The ferroelectric dielectric is typically contained between two electrode layers independent of device geometry. The electrode layers may also include perovskite materials to enable lattice matching and reduction in electrical resistance. Introduction of lead-free perovskite materials offer additional environmental benefits without sacrificing device performance.

[0029] However, integration of nonlinear polar materials into silicon semiconductor chip fabrication processes can be challenging. From fabrication of a multi-layer stack to patterning devices, and integrating one or more devices with one or more transistors, iterations in experimentation can be technically challenging and extremely time consuming.

[0030] Challenges in iterations in experimentation for thin film development begins with material selection and engineering. Film with thickness of less than 100 nm may be considered to be sufficiently thin. While individual layers can be deposited in controlled amounts and stoichiometry of films can be tuned with careful experimentation, deposition of multiple layers in a multi-layer stack is even more challenging. Depositing an individual layer in a multi-layer stack involves forming with correct stoichiometry, crystallinity, crystal structure templating, thickness, and surface roughness to facilitate device functionality. Depositing layers in a multi-layer stack is expected to have the same requisite chemical and electrical properties as single layers, but also be compatible with each other to fabricate a

functional memory device. Lattice matching between layers, preserving surface roughness of layers so as to not amplify effects of roughness on upper layers, and avoiding interdiffusion of elements while depositing are some challenges. Conductive layers to be implemented as electrodes are expected to have the correct work function and the dielectric layer is expected to have appropriate polarization and polarization charge density (above 0.1 micro coulomb/cm^2). Additionally the multi-layer stack is expected to provide operational capability at adequately low operational voltage (such as below 2V) and devices formed from the multi-layer stack are expected to have an endurance of at least e15 for commercial viability.

[0031] In at least one embodiment, obtaining a multi-layer stack with requisite layer properties begins with targeting the deposition process for individual layers. Depending on the embodiments, the deposition process can be physical vapor deposition (PVD) or atomic layer deposition (ALD) based. PVD deposition uses adequate targets for sputter deposition and atomic layer deposition uses appropriate pre-cursors for nucleation. For PVD deposition, targets can be elemental alloys or compounds. In at least one embodiment, modeling of correct charge/mass or magnetic moment to mass for elements in the target and other variables and estimating the correct deposition conditions (e.g., power, pressure, temperature, etc.) is used to form layers with appropriate stoichiometry. Such modeling can enable substantially accurate prediction of sputter yield, a useful parameter in PVD deposition. The iterative nature of experimentation is sequentially and carefully based on results from one or more previous experiments.

[0032] When a multi-layer stack is patterned to form a device, the chemical and mechanical properties can be altered during the fabrication process. Air breaks can introduce additional oxygen and/or hydrogen (among other contaminants) leading to chemical reactions at interfaces and formation of undesirable residual layers. Such residual layers may cause increased circuit resistance. Furthermore, interdiffusion of elements in the residual layers can adversely impact parameters such as remnant polarization. Performing thermal anneal can mitigate potential grain size and defect issues as well as device patterning related issues. Thermal anneal can provide hydrogen terminations of dangling bonds. However, implementation of thermal anneal post stack deposition/and or post device fabrication may use careful consideration of thermal budget.

[0033] In at least one embodiment, integrating one or more devices with transistors involves experimentations to engineer multi-layer stack to address asymmetry in 1T-1C (one transistor, one capacitor) bit-cell operational voltage characteristics. Other aspects of

experimentation involves addressing integration issues associated with fabricating a memory device on a same substrate as a transistor, but post transistor fabrication. Yet other experimentation involves determining appropriate device layout and density requirements to form a useful memory chip. Size of memory devices and transistors may be matched for optimal integrated memory performance. A high operational capacitor voltage may necessitate a transistor that can provide a high current or operate at sufficiently high voltages. Furthermore, where the sequence of fabrication involves fabricating a transistor prior to multi-layer stack deposition, thermal budget for performing an anneal can be an important factor for material selection. Thus, experimentation around a total thermal flux is used for integrated 1T-1C device fabrication.

[0034] **Figure 1** is a flow diagram of method 100 of iteratively developing a multilayer stack for application to memory devices, in accordance with an embodiment of the present disclosure. In at least one embodiment, method 100 begins at operation 110 with determining a target multi-layer stack, where the initial material layer stack comprises an initial ferroelectric material of a form $AA'BB'O_3$. In at least one embodiment, the initial material layer stack comprises an initial ferroelectric material of a form $AA'BB'O_3N_XF_Y$. In at least one embodiment, method 100 continues at operation 120 by implementing a model driven target selection based on charge:mass ratio and a magnetic moment:mass ratio, and other variables, that enable accurate prediction of sputter yield. In at least one embodiment, method 100 continues at operation 130 by procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition. In at least one embodiment, the method to procure targets uses communication with external parts suppliers to request targets that include alloys with certain stoichiometric properties as referenced by operation 132. Such targets can use fabrication lead time from third parties if they are not readily available.

[0035] In at least one embodiment, method 100 continues at operation 140 by depositing a multi-layer stack using an initial one or more targets to form the initial multi-layer stack. In at least one embodiment, method 100 continues at operation 150 by performing measurements of chemical composition and electrical properties of the initial multi-layer stack. In at least one embodiment, method 100 continues at operation 160 by matching measurements of chemical composition and electrical properties of the initial multi-layer stack against target results and determining whether the measurements are within a tolerance level of the target results. In at least one embodiment, method 100 may end at operation 170 if measurements are within a tolerance level (e.g., within 5%) of the target results. In at least

one embodiment, the method continues at operation 180 by making modifications in response to determining that the measurements are not within the tolerance level. In at least one embodiment, modifications include changing composition of one or more layers in the initial multi-layer stack to form a successive multi-layer stack by implementing a model driven selection, modifying the single elements or the combination of elements in a successive one or more targets to comprise a respective second stoichiometric composition, and procuring the successive one or more targets. In at least one embodiment, method 100 iterates (denoted by arrow 190) by implementing a model driven selection, modifying stoichiometric composition of the one or more targets in the successive one or more targets, procuring the successive one or more targets, and depositing successive multi-layer stacks, performing compositional and electrical measurements, matching measurements with target values, and determining whether measurement results are within the tolerance level of target values, until target results are obtained.

[0036] While **Figure 1** is an iterative methodology to fabricate a multi-layer stack, in at least one embodiment, one or more operations (such as operations 110-180) can be further broken down in to sub operations as will be discussed below.

[0037] In at least one embodiment, beginning with operation 110, choosing an intended composition of a target multilayer stack includes material selection for least a pair of electrodes for a capacitor and a dielectric material that includes ferroelectric, paraelectric or anti-ferroelectric properties.

[0038] In at least one embodiment, dashed box 100A defines operations that are conducted by a first entity and fabrication of target 132 may be carried out by a second entity such as external suppliers, where the second entity is different from the first entity.

[0039] **Figure 2A** is representative stack 200, in accordance with an embodiment of the present disclosure. In at least one embodiment, stack 200 includes conductive layer 202, dielectric 204 that includes a polar material and conductive layer 206 on dielectric 204. Conductive layer 202 is on substrate 208. In at least one embodiment, substrate 208 includes silicon, silicon-germanium, or germanium.

[0040] In at least one embodiment, conductive layer 202 is deposited on substrate 208. In at least one embodiment, conductive layer 202 and conductive layer 206 include a conductive oxide. In at least one embodiment, the conductive oxide includes one of non-Pb perovskite metal oxides, such as but not limited to $(La,Sr)FeO_3$, $(La,Sr)CoO_3$, $(La,Ca)MnO_3$, $(La,Sr)MnO_3$, $SrRuO_3$, Sr_2RuO_4, $(Ba,Sr)RuO_3$, $SrMoO_3$, $(La,Sr)MnO_3$, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir_2O_x, Ru,

RuO_x, Mo, MoO_x, or WO_x. In other embodiments, conductive layer 202 and conductive layer 206 include a metal such as but not limited to Ir, Ru or W.

[0041] In at least one embodiment, dielectric 204 comprises a polar layer comprising a base polar material substitutionally doped with a dopant. In least one embodiment, dielectric 204 comprises a crystalline polar layer. In at least one embodiment, the base polar material can include one or more metal elements and one or both of oxygen and nitrogen. In at least one embodiment, the dopant can include a metal element of one of 4d series, 5d series, 6d series, 4f series or 5f series.

[0042] In at least one embodiment, dielectric 204 is a ferroelectric dielectric layer that includes non-Pb based perovskite material in the form ABO_3, where A and B are two cations of different sizes and O is Oxygen. In at least one embodiment, A is generally larger than B in size. In at least one embodiment, non-Pb perovskites can also be doped, e.g., by La or Lanthanides. In at least one embodiment, the non-Pb perovskite material can include one or more of: La, Sr, Co, Cr, K, Nb, Na, Sr, Ru, Y, Fe, Ba, Hf, Zr, Cu, Ta, Bi, Ca, Ti, or Ni. In at least one embodiment, dielectric 204 includes bismuth ferrite (BFO) with a doping material, wherein the doping material is one of lanthanum, elements from the lanthanide series of the periodic table, or elements of the 3d, 4d, 5d, 6d, 4f, or 5f series of the periodic table.

[0043] In at least one embodiment, dielectric 204 includes low voltage ferroelectric (FE) material sandwiched between conductive layer 206 and conductive layer 202. In at least one embodiment, these low voltage FE materials can be of the form $AA'BB'O_3$, where A' is a dopant for atomic site A and can be an element from the Lanthanides series, where B' is a dopant for atomic site B and can be an element from the transition metal elements such as Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, or Zn. A' may have the same valency of site A, with a different ferroelectric polarizability. In at least one embodiment, voltage below 2-Volts is sufficiently low to be characterized as low voltage. In at least one embodiment, dielectric 204 is of the form $AA'BB'O_3$.

[0044] In at least one embodiment, dielectric 204 includes a paraelectric material, the paraelectric material comprises $SrTiO_3$, $Ba_{(x)}Sr_{(y)}TiO_3$, $HfZrO_2$, Hf-Si-O, La-substituted $PbTiO_3$, or a PMN-PT based relaxor ferroelectrics. In at least one embodiment, x is -0.05, and y is 0.95 for $Ba_{(x)}Sr_{(y)}TiO_3$.

[0045] In at least one embodiment, dielectric 204 includes an anti-ferroelectric material. In at least one embodiment, the antiferroelectric material may include one of: PZT with > 30% Zr doping or Sn doping >25%, La-doped PZT with >30% Zr doping and/or Sn doping > 20%, $HfSiO_2$ and $HfZrO_x$ with >30% Si and >30% Zr doping, ZrO_2, $NaNbO_3$, or >5% K

doped $NaNbO_3$. In at least one embodiment, the choice of materials depends on a variety of factors. In at least one embodiment, factors include electrical results, fabrication of devices, and integrability with a transistor.

[0046] In at least one embodiment, conductive layer 202 may be deposited to a thickness T_1 between 3nm and 30 nm (inclusive). In at least one embodiment, conductive layer 206 may be deposited to a thickness T_3 between 3nm and 30 nm (inclusive). In at least one embodiment, dielectric 204 may be deposited to thickness T_2 between 1 nm and 30 nm (inclusive).

[0047] **Figure 2B** schematically illustrates a perovskite crystal structure of a polar layer of the material layer stack in **Figure 2A**, in accordance with an embodiment of the present disclosure. In at least one embodiment, the crystalline polar layer has a perovskite structure 204A. In at least one embodiment, perovskite structure 204A represents a crystalline oxide in a paraelectric state, which may have a chemical formula ABO_3, where each of A and B represent one or more metal cations and O represents an oxygen anion. In at least one embodiment, the crystalline polar layer can have more than one element represented by A(e.g., A1, A2, ... AN) and/or more than one element represented by B (e.g., B1, B2, ... BN), and can be doped with one or more dopants represented by A' (e.g., A'1, A'2, ... A'N) and/or one or more dopants represented by B' (e.g., B'1, B'2, ... B'N), as described above. Here, A-site cations occupy the corners, while B-site cations sit in the body center of the perovskite structure 204A. In at least one embodiment, three oxygen atoms per unit cell rest on the faces of the perovskite structure 204A. In at least one embodiment, various perovskite structures have, without limitation, a lattice constant close to approximately [[4A]]4 Angstroms due to the rigidity of the oxygen octahedra network and the well-defined oxygen ionic radius of 1.35 [[A]]Angstroms. In at least one embodiment, many different cations can be substituted on both the A and B sites as dopants to achieve the various advantageous properties described herein while maintaining the overall crystal structure. According to various embodiments, a dopant atom can occupy A or B sites to form substitutionally doped solid solutions. In at least one embodiment, a dopant occupying the A sites can have a very different effect on the base polar material than a dopant occupying the B sites.

[0048] In at least one embodiment, for a polar layer comprising barium titanate ($BaTiO_3$), which may be a paraelectric material having a cubic perovskite structure, the A sites are occupied by Ba atoms while Ti atoms occupy the B sites and are surrounded by octahedra of O atoms, and the O atoms are located at the center of each face of the unit cell. In at least one embodiment, for $BaTiO_3$, in the paraelectric phase, perovskite structure 204A may be cubic

or tetragonal above the Curie temperature (which may be about 130 degrees Celsius). In at least one embodiment, in the paraelectric phase, the O atoms may occupy a mid-position with respect to each pair of O atoms on opposing faces of the unit cell. In at least one embodiment, below the Curie temperature, in the ferroelectric phase, the perovskite structure 204A may have a tetragonal structure in which the B sub lattice (e.g., Ti sub lattice in $BaTiO_3$) and O atoms may shift in opposite direction with respect to the Ba atoms, taken as reference. In at least one embodiment, these atomic shifts may be accompanied by a small relaxation of the unit cell that becomes tetragonal (when the paraelectric phase is cubic) or further elongated tetragonal (when the paraelectric phase is tetragonal) and produce a stable polarization (e.g., about 26 $\mu C/cm^2$). In at least one embodiment, in the tetragonal phase, the cubic symmetry is broken, resulting in six symmetry equivalent variants with polarization along the [100], [010] and [001] directions.

[0049] **Figure 3A** is a flow diagram of method 300A illustrating iterations in a multilayer stack deposition as performed utilizing one or more targets 302 in deposition tool 304, in accordance with an embodiment of the present disclosure. In at least one embodiment, deposition tool 304 is a physical vapor deposition tool. In at least one embodiment, one or more targets 302 includes individual targets T_i. In at least one embodiment, T_i includes an element E_i or an $alloy_i$, where subscript "i" corresponds to the number of targets 302, such as for example 1, 2, 3, 4, etc. In at least one embodiment, the number of individual targets T_i depends on a material that is to be deposited, i.e., N refers to a last target. In at least one embodiment, the number of individual targets T_i can depend on the number of elements present in the material deposited. In at least one embodiment, where individual targets T_i are alloys or compounds (A_i), A_i can be binary alloys or compounds of the form F_xG_y, or ternary alloys or compounds of the form $F_xG_yH_z$, where F and G can be metals and H can be a non-metal like O.

[0050] In at least one embodiment, for a polar material such as $BiFeO_3$, the number of elements is 3. In at least one embodiment, Bi and Fe can be available as >99% pure elemental sputtering targets. In at least one embodiment, oxygen may be inserted into the sputtering environment as a gas or be part of a compound with iron in a binary compound. In at least one embodiment, for sputtering $BiFeO_3$ the total number of targets can be 1 or 2 (i.e., N can range from 1 to 2).

[0051] In at least one embodiment, for a polar material such as $BiFeO_3$, the number of elements is 3. In at least one embodiment, while Bi and Fe can be available as >99% pure elemental sputtering targets. In at least one embodiment, oxygen may be inserted into the

sputtering environment as a gas or be part of a compound with iron in a binary compound. In at least one embodiment, for sputtering $BiFeO_3$ the total number of targets can be 1 or 2 (i.e., N can range from 1 to 2).

[0052] In at least one embodiment, sputtering targets including multi-elemental compounds can be fabricated by arc-melting or radio-frequency melting of a mixture of metals in a vacuum or gas atmosphere. In at least one embodiment, the gas can be inert or include O, N, H, or F. In at least one embodiment sputtering targets including multi-elemental compounds can be fabricated by mixing the constituent binary oxides in the stoichiometric ratio, followed by Hot Isostatic Pressing (HIP). In at least one embodiment sputtering targets including multi-elemental compounds can be fabricated by mixing the constituent binary oxides in the stoichiometric ratio, followed by cold pressing the powder mixture into a ceramic compact using a pneumatic press, followed by sintering of the ceramic compact at high temperatures to obtain the desired chemistry and density of the target.

[0053] In at least one embodiment, the density of target is between 85 and 95% of theoretical material density.

[0054] In at least one embodiment, model 306 that utilizes information about charge/mass ratio and magnetic moment/mass ratio of ions (elemental or ionized alloys) can be implemented to estimate sputtering coefficients and rates within a PVD tool. In at least one embodiment, charge/mass ratio and magnetic moment/mass ratio are used in enabling an accurate prediction of sputter yield, deposition rates and composition of a deposited layer in deposition systems that utilize magnetic fields. In at least one embodiment, the computational model further utilizes operational parameters of tool 304 to calculate deposition rates on a substrate. In at least one embodiment, operational parameters may include radio frequency (RF) magnetron deposition power, chamber operational pressure, sputtering time, temperature of chamber, and/or substrate, and types and concentration of gases flowing during deposition. In at least one embodiment, the gas utilized for deposition can be inert such as Ar and/or include other gases such as such as O_2, N_2, H_2, Kr, and Ne.

[0055] In at least one embodiment, the deposition process to form stack 200 may include deposition of all layers without an air break. In at least one embodiment, air break may be avoided to prevent interfacial layers from forming between electrode layers and the dielectric layer. In at least one embodiment, interfacial layers can provide additional source of oxygen during cycling of devices fabricated from stack 200. In at least one embodiment, additional sources of oxygen may not be controllable and may lead to instability or loss of endurance during device cycling. In at least one embodiment, for a certain combination of targets A_i, the

deposition process may yield dielectric 204 in stack 200. In at least one embodiment, stack 200 has properties of stack 200 described in association with **Figure 2A**. In at least one embodiment, properties of stack 200 may be determined by a series of measurement methods outlined in **Table 1**. In at least one embodiment, dielectric 204 may not have the desired properties of a target dielectric layer, such as correct stoichiometry, thickness, uniformity, etc.

[0056] In at least one embodiment, same targets 302 may be utilized to deposit a new stack 200'. In at least one embodiment, tool deposition conditions can be changed based on inputs to model 306. In at least one embodiment, a new set of operational parameters power', chamber operational pressure', sputtering time', temperature', and gases' may be implemented to achieve stack 200'. In at least one such embodiment, stack 200', comprising a dielectric 204', may have the desired properties of a target dielectric layer, such as correct stoichiometry, thickness, uniformity, etc.

[0057] In at least one embodiment, the process to alter PVD tool parameters can be iteratively changed based on inputs from measurements and model 306 until stack 200' achieves target values that are within tolerance of results that are desired. In at least one embodiment, power' can range between 5 Watts per square inch and 75 Watts per square inch, chamber operational pressure' can range between 0.5 milli Torr and 30 milli Torr, and temperature' of chamber and or substrate can range between room temperature to 650 degrees Celsius.

[0058] In at least one embodiment, it may be deduced that, because of the methodology in **Figure 3A**, target results can be substantially within reach if one or more individual targets T_i are changed. In at least one embodiment, this method is illustrated in **Figure 3B**. In at least one embodiment, after initial experimentation and obtaining stack 200, a new one or more targets 308 may be implemented, in accordance with method 300B.

[0059] In at least one embodiment, targets 308 includes one or more individual targets T_i', that include one or more new compounds A_i'{$(F_xG_y)_i$', $(F_xG_yH_z)_i$'}. In at least one embodiment, individual stoichiometry within the compounds including Bi, Fe, and O can be different by 5% from compounds including Bi, Fe, O in the first one or more targets. In at least one embodiment, individual stoichiometry within the compounds including Bi, Fe, and O can be different by 10% from compounds including Bi, Fe, and O in the first one or more targets. In at least one embodiment, elemental targets E_i may have the same purity as before, or the purity can be changed in other embodiments. In at least one embodiment, a new purity can range from 99% to 99.5% in some examples.

[0060] In at least one embodiment, model 306 may be implemented on new targets T_i' to compute tool parameters. In at least one embodiment, the tool parameters may be non-different than those utilized to fabricate stack 200. In the illustrative embodiment, one or more properties of dielectric 204 is altered with an iteration in modification in one or more targets. In at least one embodiment, due to differences in targets T_i', dielectric layer 204" in stack 200" may have useful properties, such as stoichiometry, thickness, uniformity, etc. Stack 200' and 200" comprising dielectric 204' and 204", respectively, may have the desired properties of a target dielectric layer that are substantially matched and within tolerance of target results.

[0061] In at least one embodiment, while experimentation with emphasis on a $BiFeO_3$ dielectric 204 has been described, methods 300A and 300B may be generalized to apply to the variety of material choices described above for dielectric 204. In at least one embodiment, when $BiFeO_3$ may also be doped with other materials such as a metal element of one of the 3d, 4d, 5d, 6d, 4f or 5f series of the periodic table.

[0062] While experimentation with emphasis on dielectric 204 has been described, method 300A or 300B may be utilized to iteratively fine tune chemical and electrical properties, such as resistivity, work function, crystallinity, etc. of conductive layers 202 and 206. Such properties of conductive layers 202 and 206 may be tuned individually or collectively as part of stack 200, in accordance with at least one embodiment.

[0063] Referring to **Figures 3A** and **3B**, in at least one embodiment, when an in-situ deposition process is carried out when depositing to form stack 200, 200' or 200", targets T_i or T_i' can include materials utilized in depositing all the layers in stack 200, 200' or 200". In at least one embodiment, minimizing iterations is useful to accelerate development and lower costs.

[0064] In at least one embodiment, evaluation of chemical, mechanical, and electrical properties of stack 200, 200', and 200" can be made by a plethora of measurement techniques. In at least one embodiment, it is useful to perform a ferroelectric hysteresis measurement (P-E loop) to analyze how effective a particular ferroelectric dielectric layer is. In at least one embodiment, a simple measurement technique involves applying an electric field applied across a sample. In at least one embodiment, the field is attenuated by a resistor divider. In at least one embodiment, a measured current through the circuit is integrated into charge by a capacitor that is positioned in series with the sample. In at least one embodiment, the applied voltage and measured voltage drop (current measurement) signals are utilized to generate a Polarization vs Electric field loop by an oscilloscope.

[0065] **Figure 4** schematically illustrates a polarization field (P-E) loop 400 of multi-layer stack that includes a ferroelectric material, such as stack 200, illustrated with respect to **Figure 2A**. In at least one embodiment, dielectric 204 comprises a storage layer, e.g., a ferroelectric layer. Referring again to **Figure 4,** in at least one embodiment, P-E loop 400 may represent that of the ferroelectric layer comprising a polydomain ferroelectric material. In at least one embodiment, prior to polarization for the first time, there may initially be a statistical distribution of ferroelectric domains such that the net polarization at zero field is about zero. In at least one embodiment, the initial polarization (P) may be represented by a P-E curve portion 422. In at least one embodiment, when the ferroelectric layer is polarized for the first time by applying a positive electric field, starting with a polarization P=0, the polarization increases with increasing electric field until it reaches saturation at $+P_{max}$. In at least one embodiment, after the saturation is reached at $+P_{max}$, when the electric field is subsequently reduced according to P-E curve portion 424, at E=0, a polarization may remain. In at least one embodiment, the remaining polarization is referred to herein as a remnant polarization ($+P_r$). In at least one embodiment, to bring the polarization back to zero, a negative electric field may be applied. In at least one embodiment, a sufficient electric field for reducing the polarization back to zero is referred to herein as a coercive field ($+E_c$ or $-E_c$). In at least one embodiment, according to P-E curve portion 424, a negative coercive field ($-E_C$) may be applied to reduce the polarization to zero from the $+P_r$. In at least one embodiment, if the negative voltage or field is further increased in magnitude, then the hysteresis loop may behave similarly to that under a positive but in a reverse sense.

[0066] In at least one embodiment, the negative P increases in magnitude with increasing negative electric field until it reaches saturation at $-P_{max}$. In at least one embodiment, when the electric field is subsequently reduced in magnitude along a P-E curve portion 426, at E=0, a remnant polarization $-P_r$ may remain. In at least one embodiment, the ferroelectric layer exhibits a characteristic of a remnant polarization $+P_r$ or $-P_r$, which can be reversed by an applied electric field in the reverse direction. In at least one embodiment, this gives rise to a hysteretic P-E loop in ferroelectric memory devices. In at least one embodiment, by using thin film technologies, operation fields or voltages may be reduced to a level below standard chip data in a non-volatile state and allows data to be rewritten fast and frequently. In at least one embodiment, a ferroelectric memory device has the advantageous features of both volatile and nonvolatile memory technologies. In at least one embodiment, voltage pulses are used to write and read the digital information. In at least one embodiment, if an electric field pulse is applied in the same direction as the remnant polarization, no switching may occur. In

at least one embodiment, a change in polarization delta P_{NS} or ΔP_{NS} between P_{max} and P_r may be present due to the dielectric response of the ferroelectric material. In at least one embodiment, if an electric field pulse is applied in the opposite direction as the remnant polarization, switching may occur. In at least one embodiment, if the initial polarization is in the opposite direction as the applied electric field, the polarization of the ferroelectric layer reverses giving rise to an increased switching polarization change delta P_s or ΔP_s.

[0067] In at least one embodiment, P-E loop 400 can be measured in blanket stacks. Other measurements described in Table 1 below, can also be performed during the iterative development method described in association with **Figures 1** and **3A-3B**. In at least one embodiment, measurements described provide mechanical/chemical composition and electrical characteristics of one or more layers of a multi-layer stack such as stacks 200, 200' and 200" (**Figures 1, 3A-3B**). Measurement technique and the associated measurement are listed in Table 1, in accordance with at least one embodiment.

Table 1

Measurement Technique	Parameter
Transmission Electron Microscopy	Crystallinity, structure, morphology (e.g., grain size)
X-ray diffraction (Bragg diffraction)	Crystallinity, lattice constants, grain size, concentration gradient, strain
Positive Up Negative Down method	Measurement of switchable polarization vs. electric field
Atomic Force Microscopy (AFM), and Conductive-AFM (c-AFM)	surface roughness (AFM); current-voltage characteristics (c-AFM)
Picoammeter	Current-Voltage, cycling, endurance
Piezoelectric force microscopy	Ferroelectricity of switching layer
Kelvin probe force microscopy	Electrode work function

[0068] In at least one embodiment, measurement techniques such as transmission electron microscopy may be utilized to obtain high resolution images of layers, interfaces between layers, arrangements of atoms, atomic planes, and dislocations among other things. In at least one embodiment, Xray diffraction may be utilized to measure phase identification of crystalline material in electrodes as well as in a ferroelectric dielectric layer. In at least one embodiment, Positive-up and Negative-down method may be utilized to measure switchable polarization versus electric field in a multi-layer stack. In at least one embodiment, Atomic

Force Microscopy (AFM) may be utilized to measure surface roughness and microstructure of an uppermost layer in a stack. In at least one embodiment, conductive AFM may be utilized to measure current-voltage characteristics of the multi-layer stack. In at least one embodiment, piezoelectric force microscopy may be utilized to measure ferroelectricity of the ferroelectric dielectric layer. In at least one embodiment, Kelvin probe force microscopy may be utilized to measure electrode work function of electrodes in the multi-layer stack.

[0069] In at least one embodiment, at least some of the measurements described above may be made after device fabrication. In at least one embodiment, surface roughness, especially of a lower conductive layer, may be measured after depositing a single layer at a time.

[0070] **Figure 5** is a flow diagram of method 500 of iteratively developing a multilayer stack for application to memory devices, in accordance with at least one embodiment of the present disclosure. In at least one embodiment, method 500 includes features of method 100 (**Figure 1**) with an addition of an anneal operation 510 between formation of a multi-layer stack at operation 140 and measuring material composition and performing measurements of material composition and electrical test characterization at operation 150.

[0071] In at least one embodiment, achieving a grain size that is conducive for increasing effective polarization in the dielectric layer is useful for high performance memory devices. In at least one embodiment, modulation of grain size may be accomplished by performing an anneal process at high temperatures. In at least one embodiment, the anneal process includes rapid thermal treatment processes (herein PD-RTA). In at least one embodiment, PD-RTA may utilize temperatures greater than or equal to 400 degrees Celsius. In at least one embodiment, blanket unpatterned stacks may be heated to high temperatures, such as temperatures above 800 degrees Celsius to determine optimal properties of a particular multi-layer stack. In at least one embodiment, anneal durations may be 10-30 minutes to test limits of the multi-layer stack.

[0072] In at least one embodiment, anneal temperatures can be higher than 800 degrees Celsius, the duration of most processes may be limited to approximately 1 minute or less for patterned memory devices, for example, when such memory devices are integrated with a transistor. In at least one embodiment, a process at high temperature but with a short time duration may be compatible with transistors that are embedded within the substrate on which the perovskite material is formed. In at least one embodiment, such a method is particularly advantageous when transistors are fabricated using a gate last process to prevent threshold

voltage shifts arising from high temperature operations lasting substantially greater than 1 minute.

[0073] In at least one embodiment, a post deposition anneal (PDA) may be characterized by a thermal anneal of a layer or a stack after the deposition process has been performed. In at least one embodiment, this contrasts with an in-situ anneal which takes place during deposition. In at least one embodiment, PDA may be performed after all layers in a multi-layer stack, for example, are deposited. In at least one embodiment, the anneal process can be performed following a patterning process utilized to fabricate memory devices. In at least one embodiment, following the deposition of a first conductive layer and a dielectric layer, the anneal process can be performed prior to deposition of a second conductive layer on the dielectric layer. In at least one embodiment, PDA is performed after deposition of the multi-layer stack. In at least one embodiment, where anneal operation 510 is inserted prior to performing measurements of the multi-layer stack, such measurements may be compared to measurements obtained from an identical unannealed multi-layer stack.

[0074] In at least one embodiment, anneal temperatures can be as high as 1300 degrees Celsius, where anneal time durations are limited to less than or equal to 60 seconds. In at least one embodiment, the specific temperature and time duration is dependent on the annealing technique utilized and a maximum thermal budget that is compatible with, for example, a transistor for integrated device applications. In at least one embodiment, for temperatures less than 700 degrees Celsius, a time duration of 60 seconds or less, for example, may be relatively short.

[0075] In at least one embodiment, post deposition rapid thermal annealing may be used to describe all thermal annealing treatments where a wafer is heated and cooled at rates faster than is typical in furnace annealing tools. In at least one embodiment, heating/cooling rates can be more than 10 degrees Celsius/second. In at least one embodiment, such rapid heating and cooling can be achieved using a variety of technologies. The terms "RTP" or "RTA" are sometimes defined to describe the original rapid thermal annealing technique, in which infra-red lamps may be implemented to heat the wafer. In at least one embodiment, Xenon-lamp based heating (also called "Flash" annealing), laser heating (Laser annealing), and microwave energy (Microwave annealing) may be used to heat the wafer. In at least one embodiment, surface temperatures of substrate may be monitored by pyrometer and thermocouples. In at least one embodiment, such techniques can offer extremely fast heating and cooling rates, such as for example 1 million degrees per second. In at least one embodiment, it is useful for the cooling process to be controlled to prevent dislocations in the various layers.

[0076] In at least one embodiment, post deposition anneal can include one or more of the above techniques. In at least one embodiment, RTP/RTA can be performed at temperatures above 1000 degrees Celsius. In at least one embodiment, since the duration is on the order of a minimum of a few seconds, RTP/RTA may be used for annealing to temperatures less than 800 degrees Celsius.

[0077] In at least one embodiment, PDA includes an RTP process which is carried out in O_2, N_2, Argon environment, or in air. In at least one embodiment, processing pressures range from 1 Torr to 760 Torr while flowing in O_2, N_2 or Argon gases. In at least one embodiment, RTP process is carried out in vacuum at pressures less than 1 Torr. In at least one embodiment, processing times range from 1s to 60s. In at least one embodiment, processing temperatures range from 400 to 700 degrees Celsius, where the heating and cooling rate is approximately 40 to 200 degrees Celsius/second.

[0078] In at least one embodiment, PDA includes a flash anneal process. In at least one embodiment, flash and laser annealing offer extremely short durations, and thus can allow high temperatures greater than 1000 degrees Celsius without damaging the underlying structures e.g., transistors on the wafer. In at least one embodiment, flash and laser anneal can include spot heating or beam rastering for increased throughput. In at least one embodiment, processing pressures range from 1 Torr to 760 Torr while flowing in O_2, N_2, Argon gases, or in air. In at least one embodiment, flash anneal process is carried out in vacuum at pressures less than 1 Torr. In at least one embodiment, processing temperatures range from 500 to 1300 degrees Celsius, where the heating and cooling rate is approximately 10^6 degrees Celsius/second. In at least one embodiment, processing times are 1 ms or less. In other embodiments the total anneal time can be 10 ms/ flash. In at least one embodiment, the total number of flashes can be up to 100 flashes per sample (wafer, substrate etc).

[0079] In at least one embodiment, PDA includes a laser anneal process. In at least one embodiment, processing temperatures range from 600 to 1300 degrees Celsius, where the heating and cooling rate is approximately 10^6 degrees Celsius/second. In embodiments, processing times is 100 microseconds or less. In some such embodiment, the anneal time can be 100 ms/ laser anneal process. In at least one embodiment, the total number of laser anneals can be up to 100 per sample (wafer, substrate etc).

[0080] In at least one embodiment, the multi-layer stack may be deposited by a PVD process at 350 degrees Celsius, annealed by PD-RTA process in an RTP tool with a 50 degree Celsius/second heating/cooling rates, in O_2 atmosphere at 760 Torr pressure and at 600 degrees Celsius for 60 seconds. In at least one embodiment, the multi-layer stack may be

deposited by a PVD process at 350 degrees Celsius, annealed by PD-RTA process in a laser annealing tool with a 10^6 degrees Celsius/second heating/cooling rates, in vacuum and at 1200 degrees Celsius for 10 microseconds. In at least one embodiment, other forms of annealing include microwave annealing or hybrid microwave annealing.

[0081] In at least one embodiment, the microwave anneal process comprises heating for a fourth time duration of less than 3600s at a microwave power of less than 1000W.

[0082] Point defects such as oxygen vacancies may lead to increased electrical leakage in capacitor layers which may be detrimental to ferroelectric polarization and switching voltage. Oxygen vacancies and other point defects can also lead to ferroelectric domain-wall pinning. Pining can manifest in detrimental effects such as increased switching voltage and lead to early endurance failure of FE capacitor devices.

[0083] In at least one embodiment, dashed box 500A defines operations that are conducted by a first entity and fabrication of target at operation 132 may be carried out by a second entity such as external suppliers, where the second entity is different from the first entity.

[0084] In at least one embodiment, method 500 iterates (denoted by arrow 190) by implementing a model driven selection, modifying stoichiometric composition of the one or more targets in the successive one or more targets, procuring the successive one or more targets, and depositing a successive multi-layer stack, performing anneal, performing compositional and electrical measurements, matching measurements with target values, and determining whether measurement results are within the tolerance level of target values, until target results are obtained.

[0085] In at least one embodiment, in addition to making changes to composition of one or more layers in the multi-layered stack, additional layers may be added to the multi-layer stack at operation 140. In at least one embodiment, such layers may be formed in accordance with multi-layer stack 600 in **Figure 6**.

[0086] **Figure 6** is a cross-sectional illustration of a multi-layer stack 600 including a ferroelectric material, deposited in accordance with the flow diagram in **Figure 5**, in accordance with at least one embodiment of the present disclosure. In at least one embodiment, layers in multi-layer stack 600 are deposited by a co-sputtering or a reactive sputtering method.

[0087] In at least one embodiment, additional conductive layers 602 and 604 may implemented for different purposes. In at least one embodiment, while conductive layer 202 was previously illustrated to be deposited on substrate 208 for test purposes, for device

fabrication, conductive layer 202 may be coupled with interconnect structures. In at least one embodiment, conductive layer 202 may also be in contact with one or more insulator layers. In at least one embodiment, it may be useful for conductive layer 202 to have a crystallographic structure for templating of dielectric 204. In at least one embodiment, for this reason, among others, conductive layer 202 may be deposited on a secondary electrode layer, such as conductive layer 602. In at least one embodiment, conductive layer 602 includes Pt. In at least one embodiment, conductive layer 604 includes TaN. In at least one embodiment, conductive layers 602 and 604 can be deposited in-situ with the ferroelectric material to prevent interfacial layers I_1 and I_2 from forming between conductive layer 602 and conductive layer 202, and between conductive layer 206 and conductive layer 604, respectively.

[0088] In at least one embodiment, additional layers can aid some structural properties that can be overall detrimental to electrical resistance of the stack. In at least one embodiment, an increase in electrical resistance can detrimentally impose a need for higher operating voltages. In at least one embodiment, higher operating voltages may demand more powerful transistors. In at least one embodiment, the choice of materials may add little electrical resistance while providing crystallographic templating advantages. In at least one embodiment, determining a requisite minimum thickness that can provide compositional benefits should also be balanced with other parameters such as total stack thickness, ease of patterning, and development of interfacial layers during device fabrication process. Iterative device development must be carefully balanced with end goals of electrical requirements.

[0089] In at least one embodiment, patterning of multi-layer stack to fabricate devices further introduces other complexities and iterative methods described above are essential to rapid development.

[0090] **Figure 7** is a flow diagram of method 700 of iteratively developing memory devices, in accordance with at least one embodiment of the present disclosure. In at least one embodiment, method 700 begins at operation 710 by receiving a multi-layer stack from operation 170 (**Figure 5**). In at least one embodiment, method 700 continues at operation 720 with annealing the multi-layer stack. In at least one embodiment, method 700 continues at operation 730 by etching the multi-layer stack to form a memory device. In at least one embodiment, method 700 continues at operation 740 forming an encapsulation layer at least around the memory device. In at least one embodiment, method 700 continues at operation 750 by performing measurements of chemical composition and electrical properties of the memory device.

[0091] In at least one embodiment, method 700 continues at operation 760 by matching measurements of chemical composition and electrical properties of the memory device against target results and determining whether the measurements are within a tolerance level of the target results. In at least one embodiment, method 700 may end at operation 770 if measurements are within a tolerance level of the target results. In at least one embodiment, method 700 can continue at operation 780 by making modifications in response to determining that the measurements are not within the tolerance level. In at least one embodiment, modifications include changing composition of one or more layers in the initial multi-layer stack to form a successive multi-layer stack by implementing a model driven selection, modifying the single elements or the combination of elements in a successive one or more targets to comprise a respective second stoichiometric composition and procuring the successive one or more targets. In at least one embodiment, method 700 continues at operation 790 with forming a multi-layer stack. In at least one embodiment, method 700 iterates at operation 720 with annealing the multi-layer stack, etching the multi-layer stack, etching and forming a memory device, encapsulating the memory device, performing measurements, matching measurements, and determining whether the measurement results are within the tolerance level, until target results are obtained.

[0092] In at least one embodiment, after annealing the multi-layer stack that has been deposited after a first round of iterations, measurements can be made at operation 792 after operation 720 to assess if material composition and electrical characteristics are within tolerance of a desired target. In at least one embodiment, measurements made immediately after annealing at operation 720 can save time that would otherwise be spent in continuing with fabrication of device and discovering results at end of line. In at least one embodiment, operation 792 is eliminated and measurements are made at end of line in a fabrication sequence, after devices are fabricated.

[0093] In at least one embodiment, in addition to making changes to composition of one or more layers in the multi-layered stack, additional layers may be added to the multi-layer stack. In at least one embodiment, such layers may be formed in accordance with the multi-layer stack 600 in **Figure 6**.

[0094] **Figure 8A** is a cross-sectional illustration of a planar capacitor (herein memory device 801) obtained by patterning the multi-layer stack obtained from operation 780 in **Figure 7.** In at least one embodiment, multilayer stack may have properties of stack 200' or 200" in **Figures 3A-3B**, for example, conductive layer 202, dielectric 204 and conductive layer 206.

[0095] Referring again to **Figure 8A,** in at least one embodiment, memory device 801 includes electrode 802, dielectric layer 804 on electrode 802, and electrode 806 on dielectric layer 804.

[0096] In at least one embodiment, electrode 802 comprises a first conductive nonlinear polar material where the first conductive nonlinear polar material has a first grain size. In at least one embodiment, dielectric layer 804 comprises a perovskite material comprising a second grain size. In at least one embodiment, electrode 806 comprises a second conductive nonlinear polar material, where the second conductive nonlinear polar material has a third grain size that is substantially the same as the first grain size or the second grain size. All grain sizes are defined by an "average grain length."

[0097] In at least one embodiment, perovskite film properties needed for high performance devices further necessitate achieving a grain size that is conducive for increasing effective polarization in the dielectric layer. In at least one embodiment, modulation of grain size may be accomplished by performing an anneal process at high temperatures.

[0098] In at least one embodiment, electrode 802 includes a perovskite material. In at least one embodiment, the perovskite material includes one of a non-Pb perovskite metaloxide, such as but not limited to, La-Sr-CoO_3, $SrRuO_3$, La-Sr-MnO_3, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCu_2O_8$, $LaNiO_3$, or $DyScO_3$. In at least one embodiment, electrode 802 has a nanocrystalline to polycrystalline grain structure. In at least one embodiment, grains 802A may be irregular as illustrated. In at least one embodiment, grains 802A have a size defined by average length L_1. In at least one embodiment, L_1 ranges between 15 nm and 50 nm.

[0099] In at least one embodiment, grains 806A have a size defined by average length L_2. In at least one embodiment, L_1 and L_2 are substantially equal. In at least one embodiment, electrode 806 includes grains 806A that are of comparable magnitude to grains 802A of electrode 802. In at least one embodiment, L_2 ranges between 15 nm and 50 nm. In at least one embodiment, ratio L_1:L_2, between grain size of electrodes 802 and 806, is substantially 1:1, but can vary by less than 10% percent.

[00100] In at least one embodiment, electrode 806 can further include a same material as the material of electrode 802. In at least one embodiment, substantially identical materials can provide symmetry and can offer additional advantages, such as reliability, as devices are cycled billions of times over a lifetime of operation. In at least one embodiment, different electrode materials having substantially the same grain size can be implemented in memory device 801. In at least one embodiment, this can be advantageous in some operational

regimes where at least one of the electrodes 802 or 806 is coupled with an external circuit element such as a transistor.

[00101] In at least one embodiment, the dielectric layer 804 has a polycrystalline grain structure. In at least one embodiment, grains 804A may be irregular as illustrated. In at least one embodiment, grains 804A have a size defined by an average length L_3. In at least one embodiment, L_3 ranges between 15 nm and 50 nm. In at least one embodiment, multiple polarization domains may exist within grains 804A. In at least one embodiment, the ratio between L_1 and L_3 can range between 1:3 and 3:1. In at least one embodiment, the ratio between L_1 and L_3 is substantially equal to 1:1, when dielectric layer 804 includes one or more of the elements of electrode 802.

[00102] In at least one embodiment, while grain size is one attribute of the layers within memory device 801, there are others, such as point defects. In at least one embodiment, point defects are sites with missing atoms such as oxygen, or missing cations such as Ba, Bi, Fe, and/or Ti, etc. In at least one embodiment, point defects 803, 805, and 807 are illustrated by points within electrode 802, dielectric layer 804, and electrode 806, respectively. In at least one embodiment, point defects 803, 805, and 807 can correlate with grain size, where a layer comprising a large grain size may have lower point defect.

[00103] In at least one embodiment, electrode 802 has point defects 803 that number less than 1e20 atoms/cm^3. In at least one embodiment, electrode 802 has a grain size between 15 nm and 50 nm and point defects that number less than 1e20 atoms/cm^3. In at least one embodiment, dielectric layer 804 has point defects 805 that number less than 1e20 atoms/cm^3. In at least one embodiment, dielectric layer 804 has a grain size between 15 nm and 50 nm and point defects 805 that number less than 1e20 atoms/cm^3. In at least one embodiment, electrode 806 has a grain size between 15 nm and 50 nm and point defects 807 that number less than 1e20 atoms/cm^3.

[00104] In at least one embodiment, memory device 801 may be coupled with external circuit elements such as transistors through interconnect structures. In at least one embodiment, transition electrode 810 is below electrode 802. In at least one embodiment, transition electrode 810 may include a material such as TiN, W, Ru, TaN, or Ta. In at least one embodiment, transition electrode 810 can provide a surface for crystal templating of material of electrode 802.

[00105] In at least one embodiment, controlling grain sizes of electrodes and dielectric layers can modulate intrinsic behavior, which is equally useful for long term device performance to mitigate damage from extrinsic processes. In at least one embodiment,

FeRAM devices including lead-free perovskite materials may be prone to damage from reaction with hydrogen during processing. The damage may be a result of hydrogen traveling along grain boundaries between or along electrodes coupled with two terminals of a FeRAM device. Hydrogen can cause reduction when it reacts with the one or more materials of the FeRAM device, such as the electrodes or the ferroelectric material itself. During fabrication anneal operations carried to tie up dangling bonds can be sources of hydrogen. FeRAM devices can lose their polarization hysteresis characteristics because of hydrogen reduction.

[00106] In at least one embodiment, where memory device 801 has a planar structure where the individual layers are sequentially layered one on top of another, it is useful to protect capacitor sidewalls, top and bottom surfaces from reacting with hydrogen. In at least one embodiment, solutions against hydrogen diffusion include forming an insulating barrier layer, for example, silicon nitride, to protect sidewalls and top surfaces. In at least one embodiment, a contact electrode may be formed on a top of the memory device 801 by etching through the insulating barrier layer and exposing electrode 806.

[00107] **Figure 8B** is a cross-sectional illustration of plurality of memory devices 820, where individual memory devices 801 are encapsulated by encapsulation layer 812, in accordance with at least one embodiment. In at least one embodiment, to prevent hydrogen from reaching dielectric layer 804, memory device 801 may be at least laterally covered by encapsulation layer 812. In at least one embodiment, sidewall 813 of the memory device 801 is laterally surrounded by encapsulation layer 812. In at least one embodiment, encapsulation layer 812 also extends partially on an uppermost surface of memory device 801(X and Z being respectively the x-axis and the z-axis of the plurality of memory devices 820).

[00108] In at least one embodiment, the process utilized to deposit encapsulation layer 812 can depend on materials utilized, and on a height of memory device 801. In at least one embodiment, which includes a plurality of memory devices, the deposition process can be dependent on relative spacing S_D, between adjacent memory devices. In at least one embodiment, the deposition process utilized to deposit encapsulation layer 812 does not include hydrogen or ammonia containing chemicals to prevent hydrogen exposure to layers within memory device 801. In at least one embodiment, encapsulation layer 812 is blanket deposited.

[00109] In at least one embodiment, encapsulation layer 812 includes an insulator material. In at least one embodiment, the insulator material can include a metal and oxygen, such as, but not limited to Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x. In at least one embodiment, materials such as Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x can be deposited without a hydrogen or

an ammonia containing chemical precursor in an ALD deposition process. In at least one embodiment, encapsulation layer 812 may be deposited to a thickness in the range of 0.5 nm to 10 nm. In at least one embodiment, encapsulation layer 812 may be deposited to a thickness of less than 5 nm. In at least one embodiment, an ALD process can provide a substantially conformal thickness on sidewalls of memory device 801. In at least one embodiment, a PVD deposition process may not conformally deposit encapsulation layer 812 with a uniform thickness.

[00110] In at least one embodiment, a PVD process may be utilized. In at least one embodiment, encapsulation layer 812 can include materials such as compounds of nitrogen, and a transition metal such as, but not limited to AlN, ZrN, HfN, or compounds of Si and O, and one or more of Al, Hf, or Ta, such as, but not limited to, $AlSiO_X$, $HfSiO_X$, and $TaSiO_X$. In at least one embodiment, a PVD process may not provide a substantially conformal deposition on sidewalls of memory device 801. In at least one embodiment, a thickness of approximately 2 nm may be sufficient to prevent hydrogen transport through encapsulation layer 812 that is deposited with a material density of at least 90%.

[00111] In at least one embodiment, the material of encapsulation layer 812 can be chosen based on the material of dielectric layer 804. In at least one embodiment, pairing encapsulation layer 812 with dielectric layer 804 can minimize lattice dislocations that can cause voids and potential pathways for hydrogen diffusion.

[00112] In at least one embodiment, hydrogen may diffuse to electrodes 806 and 802 through one or more materials of a contact electrode and transition electrode 810 respectively. In at least one embodiment, to protect against hydrogen diffusion through a top surface of electrode 806, noble metals can be implemented on electrode 806.

[00113] In at least some embodiments, hydrogen can also diffuse from layers below electrode 802. In at least one embodiment, electrode 802 may be physically isolated from a conductive interconnect by transition electrode 810. In at least one embodiment, transition electrode 810 may be laterally surrounded by insulator layer 808 that can act as a barrier against hydrogen diffusion as well as provide etch stop capability while patterning to form memory device 801.

[00114] In at least one embodiment, to prevent hydrogen from diffusing directly into sidewalls of transition electrode 810, an insulator including an amorphous material may be directly in contact with the sidewalls of transition electrode. In at least one embodiment, an amorphous material may have a high film density (for example, a film density above 90% of theoretical material density or film density).

[00115] In at least one embodiment, an iterative method described above may be useful for choosing a type of material for encapsulation layer 812 as well as for understanding which deposition technique to adopt.

[00116] In at least one embodiment, dielectric 204 can dictate the choice of encapsulation layer 812. In at least one embodiment, encapsulation layer 812 may be chosen to have a Young's modulus similar to the Young's modulus of dielectric 204. In at least one embodiment, encapsulation layer 812 may be chosen to have a low probability of presence of defects at the interface between encapsulation layer 812 and dielectric 204. In at least one embodiment, encapsulation layer 812 can have a lower dielectric constant than the dielectric constant of dielectric 204 to enable field lines to be concentrated between conductive layer 202 and conductive layer 206.

[00117] In at least one embodiment, where dielectric 204 includes a $Pb_xZr_{1-x}Ti_yO_3$ group of families, encapsulation layer 812 can include Al_xO_y, HfO_x, ZrO_x, TaO_x, or TiO_x. In some embodiments, where dielectric 204 includes a $La_xBi_{1-x}Fe_yO_3$ group of families, encapsulation layer 812 can include Al_xO_y, HfO_x, ZrO_x, TaO_x, or TiO_x. In at least one embodiment, where dielectric 204 includes a $BaTiO_3$ group of families, encapsulation layer 812 can include Al_xO_y, HfO_x, ZrO_x, TaO_x, or TiO_x. In at least one embodiment, where dielectric 204 includes a $BiFeO_3$ group of families, encapsulation layer 812 can include Al_xO_y, HfO_x, ZrO_x, TaO_x, or TiO_x.

[00118] **Figure 9** is a flow diagram of method 900 of iteratively developing a 1-Transistor-1-Memory cell, in accordance with at least one embodiment of the present disclosure. In at least one embodiment, method 900 begins at operation 910 by fabricating a transistor or receiving a workpiece that includes a transistor (for example purchased from a third party). In at least one embodiment, method 900 continues at operation 920 by fabricating a multi-layer stack using method 900 described in association with **Figure 7**. Referring again to **Figure 9,** the multi-layer stack is coupled with a first terminal of the transistor. In at least one embodiment, method 900 continues at operation 930 by annealing the multi-layer stack. In at least one embodiment, method 900 continues at operation 940 by etching the multi-layer stack to form a memory device, where a first terminal of the memory device is coupled with the first terminal of the transistor. In at least one embodiment, method 900 continues at operation 950 by forming an encapsulation at least around the memory device and forming a contact on a second end of the memory device. In at least one embodiment, the second terminal is above the first terminal. In at least one embodiment, method 900 continues at operation 960 by performing measurements of chemical

composition and electrical properties of the memory device coupled with the transistor. In at least one embodiment, method 900 continues at operation 970 by matching measurements of compositional and electrical characterization of the memory device coupled with the transistor against target results for a reference memory device coupled with a reference transistor.

[00119] In at least one embodiment, method 900 may end at operation 975 if, after matching measurements against target results, the measurements are within a tolerance level of the target results. In at least one embodiment, if after matching measurements against target results the measurements are not within a tolerance level of the target results, method 900 continues at operation 980 by making modifications in response to determining that the measurements are not within the tolerance level. In at least one embodiment, modifications include changing composition of one or more layers in the initial multi-layer stack to form a successive multi-layer stack by implementing a model driven selection, modifying the single elements or the combination of elements in a successive one or more targets to comprise a respective second stoichiometric composition, and procuring the successive one or more targets. In at least one embodiment, or one or more additional layers can be added or removed.

[00120] In at least one embodiment, method 900 iterates at operation 920 with fabricating a successive multi-layer stack, annealing the successive multi-layer stack, etching the successive multi-layer stack, etching and forming a memory device, encapsulating the memory device, performing measurements, matching measurements, determining whether the measurement results are within the tolerance level, and repeating until target results are obtained.

[00121] In at least one embodiment, method 900 continues at operation 990 by changing the size of transistor to achieve a desired performance. In at least one embodiment, transistor characteristics to be changed include saturation current, operational voltage, gate voltage and physical dimensions. In at least one embodiment, the transistor may be fabricated or purchased from a third party.

[00122] In at least one embodiment, after annealing the multi-layer stack that has been deposited after a first round of iterations, measurements can be made at operation 992 to assess if material composition and electrical characteristics are within tolerance of a desired target. In at least one embodiment, measurements made after annealing can save time that would be spent in continuing with fabrication of device. In at least one embodiment, operation 992 can be eliminated and measurements are made after devices are fabricated.

[00123] **Figure 10** is a cross-sectional illustration of system 1000 that includes a memory device 801 coupled with transistor 1002, in accordance with at least one embodiment. In at least one embodiment, memory device 801 is coupled to transistor 1002 through drain contact 1003. In at least one embodiment, memory device 801 includes one or more features of memory device 801 (**Figure 8A**). In at least one embodiment, memory device 801 is on a transition electrode 810. In at least one embodiment, transition electrode 810 is coupled with drain contact 1003 of transistor 1002.

[00124] In at least one embodiment, memory device 801 can be a planar capacitor (**Figure 8A**) or a trench capacitor In at least one embodiment, memory device 801 have a cylindrical profile. In at least one embodiment, memory device 801 can have a rectangular profile. In at least one embodiment, while memory device 801 is electrically coupled with drain contact 1003, there may be intervening layers of via electrodes between drain contact 1003 and transition electrode 810.

[00125] In at least one embodiment, transistor 1002 is an example of a transistor that is non-planar. In at least one embodiment, transistor 1002 may be, for example, an NMOS or a PMOS transistor. In at least one embodiment, transistor 1002 includes gate structure 1004, between source region 1006 and drain region 1008. In at least one embodiment, source region 1006 includes epitaxial source structure 1010 (herein source structure 1010) and drain region 1008 includes epitaxial drain structure 1012 (herein drain structure 1012). In at least one embodiment, source structure 1010 and drain structure 1012 are separated from gate structure 1004 by spacer 1011 and have faceted sidewall surfaces 1010A and 1012A. Not all faceted surfaces of source structure 1010 and drain structure 1012 are shown. In at least one embodiment, a portion of gate structure 1004 is on dielectric 1022 that separates gate structure 1004 from substrate 1018. In at least one embodiment, drain contact 1003 is coupled to drain structure 1012.

[00126] In at least one embodiment, gate structure 1004 further includes gate dielectric layer 1005 and gate electrode 1007. In at least one embodiment, gate dielectric layer 1005 has a base portion on channel 1018A and sidewall portions that are adjacent to spacer 1011. In at least one embodiment, gate electrode 1007 is confined within gate dielectric layer 1005.

[00127] In at least one embodiment, gate dielectric layer 1005 includes a suitable gate dielectric material such as but not limited to an oxide of one or more of: Si, Hf, Zr, La, Ti, Ta, or Ga; or Al, such as SiO_2, HfO_2, ZrO_2, $HfSiO_x$, $HfZrO_2$, Ta_2O_5, Al_2O_3, La_2O_3, or $TaSiO_x$; or Ga_2O_5. In at least one embodiment, gate electrode 1007 may include one or more of: Ti, Al, W, Pt, Co, Ni, or Pd; nitrogen; one or more of: Ti, Ta, Al, Hf or Zr; or carbon and one or

more of: Ti, Al, Ta, Hf, or Zr. In at least one embodiment, source structure 1010 and drain structure 1012 may include amorphous Si, SiC, SiGe, or Ge and may be doped with As, P, or B, depending on the mobile charge carrier implemented. In at least one embodiment, spacer 1011 includes silicon nitride or silicon nitride doped with carbon. In at least one embodiment, drain contact 1003 includes a conductive material such as Ru, Ti, Co, Mo, Co, Ni, W, or Ta; or nitrides of Ti, W, or Ta. In at least one embodiment, drain contact 1003 includes a liner layer including TiN, TaN, or WN; and a fill metal including one or more of: Ru, Ti, Co, Mo, Co, Ni, W, or Ta.

[00128] In at least one embodiment, memory device 801 may be further coupled with a contact structure 1014. In at least one embodiment, contact structure 1014 is coupled with electrode 806. In at least one embodiment, contact structure 1014 may include conductive hydrogen barrier 1016 that surrounds a fill material 1020. In at least one embodiment, conductive hydrogen barrier 1016 is in contact with encapsulation layer 812. In at least one embodiment, encapsulation layer 812 and conductive hydrogen barrier 1016 together provide a barrier to memory device 801.

[00129] In at least one embodiment, conductive hydrogen barrier 1016 includes a material that is amorphous. In at least one embodiment, amorphous materials lack defined grain boundaries that can facilitate hydrogen diffusion and are thus desirable. In at least one embodiment, conductive hydrogen barrier 1016 includes materials such as, but not limited to: TiAlN, with >30 atomic percent AlN; TaN, with >30 atomic percent N_2; TiSiN, with >20 atomic percent SiN; Ta carbide, TaC, Ti carbide, TiC; tungsten carbide,WC; tungsten nitride, WN; carbonitrides of Ta, Ti, or W, i.e., TaCN, TiCN, or WCN; titanium monoxide, TiO; Ti_2O; Tungsten oxide, WO_3;Tin oxide, SnO_2; indium tin oxide, ITO; Iridium Oxide; Indium Gallium Zinc Oxide, IGZO; Zinc Oxide, or METGLAS series of alloys, e.g., $Fe_{40}Ni_{40}P_{14}B_6$. In at least one embodiment, conductive hydrogen barrier 1016 has a thickness that is less than 5nm.

[00130] In at least one embodiment, transition electrode 810 includes a material that provides a barrier against hydrogen and oxygen diffusion. In at least one embodiment, transition electrode 810 does not include a material that provides a barrier against hydrogen and oxygen diffusion. In at least one embodiment, the transition electrode can be laterally surrounded by a conductive hydrogen barrier layer such as conductive hydrogen barrier 1016.

[00131] In other embodiments, encapsulation layer 812 can include materials that are oxygen diffusion barriers. Examples of oxygen diffusion barrier material includes silicon nitride and silicon carbide.

[00132] In at least one embodiment, the iterative method described in **Figure 9**, may be utilized to determine the choice of materials for encapsulation layer 812, conductive hydrogen barrier 1016, optimization of drive current, threshold voltage, and/or on-off characteristics (among other parameters) of transistor 1002.

[00133] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments," and “at least one embodiment,” generally means that a particular feature, structure, or characteristic described in connection with the embodiments may include at least one embodiment, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," “at least one embodiment,” or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure or characteristic "may," "might," or "could" be included, that component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional elements.

[00134] Furthermore, the features, structures, functions, or characteristics may be combined in any suitable manner in at least one embodiment. In at least one embodiment, a first embodiment may be combined with a second embodiment anywhere the features, structures, functions or characteristics associated with the two embodiments are not mutually exclusive.

[00135] The structures of at least one embodiment described herein can also be described as method(s) of forming those structure(s), apparatus(es), and method(s) of operation of these structure(s) or apparatus(es). In at least one embodiment, the method may be an iterative method. The following examples are provided that illustrate at least one embodiment. The examples can be combined with other examples. As such, at least one embodiment can be combined with another embodiment without changing the scope of the disclosure.

[00136] Example 1: A method comprising: determining a target multi-layer stack, wherein the target multi-layer stack comprises a polar material; implementing a model driven target selection based on a charge:mass ratio and a magnetic moment:mass ratio of target materials; procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition; depositing, using the initial one or more targets, an initial multi-layer stack; performing measurements of chemical composition and electrical properties of the initial multi-layer stack; modifying, in response to determining that measurement results

are not within tolerance levels of target results, composition of one or more layers in the initial multi-layer stack; and iterating depositing of a successive multi-layer stack and determining whether the measurement results of the successive multi-layer stack are within the tolerance levels, until target results are obtained.

[00137] Example 2: The method of example 1, wherein modifying composition of one or more layers in the initial multi-layer stack further comprises: implementing the model driven target selection based on the charge:mass ratio and the magnetic moment:mass ratio of the target materials; modifying stoichiometric composition of one or more targets in a successive one or more targets; and procuring the successive one or more targets.

[00138] Example 3: The method of example 1, wherein after depositing the successive multi-layer stack, the method further comprises: performing measurements of chemical composition and electrical properties of the successive multi-layer stack; and matching measurements of chemical composition and electrical properties of the successive multi-layer stack against target results.

[00139] Example 4: The method of example 1, wherein depositing the initial multi-layer stack comprises: depositing a first conductive layer comprising a first conductive material, wherein the first conductive material comprises one of $(La,Sr)FeO_3$, $(La,Sr)CoO_3$, $(La,Ca)MnO_3$, $(La,Sr)MnO_3$, $SrRuO_3$, Sr_2RuO_4, $(Ba,Sr)RuO_3$, $SrMoO_3$, $(La,Sr)MnO_3$, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, Ir_2O_x, Ru, RuO_x, Mo, MoO_x, W, or WO_x; depositing a dielectric layer on the first conductive layer the dielectric layer comprising one of: a perovskite material which includes one of: $BaTiO_3$, $PbTiO_3$, $KNbO_3$, or $NaTaO_3$; lead zirconium titanate (PZT), or PZT with a doping material, wherein the doping material is one of La or Nb; bismuth ferrite (BFO) with a doping material, wherein the doping material is one of lanthanum, elements from lanthanide series of a periodic table, or elements of a 3d, 4d, 5d, 6d, 4f, and 5f series of the periodic table; a relaxor ferroelectric material which includes one of lead magnesium niobate (PMN), lead magnesium niobate-lead titanate (PMN-PT), lead lanthanum zirconate titanate (PLZT), lead scandium niobate (PSN), barium titanium-bismuth zinc niobium tantalum (BT-BZNT), or Barium titanium-barium strontium titanium (BT-BST); a hexagonal ferroelectric which includes one of: $YMnO_3$ or $LuFeO_3$; hexagonal ferroelectrics of a type h-$RMnO_3$, wherein R is a rare earth element which includes one of: cerium (Ce), dysprosium (Dy), erbium (Er), europium (Eu), gadolinium (Gd), holmium (Ho), lanthanum (La), lutetium (Lu), neodymium (Nd), praseodymium (Pr), promethium (Pm), samarium (Sm), scandium (Sc), terbium (Tb), thulium (Tm), ytterbium (Yb), or yttrium (Y); hafnium (Hf), zirconium (Zr), aluminum (Al),

silicon (Si), their oxides, or their alloyed oxides; Hafnium oxides as $Hf_{1-x}E_xO_y$, where E can be Al, Ca, Ce, Dy, Er, Gd, Ge, La, Sc, Si, Sr, Sn, Zr, or Y;$Al_{(1-x)}Sc_{(x)}N$, $Ga_{(1-x)}Sc_{(x)}N$, $Al_{(1-x)}Y_{(x)}N$, $Al_{(1-x-y)}Mg_{(x)}Nb_{(y)}N$, or E doped HfO_2, where 'x' or 'y' is a fraction; or niobate type compounds $LiNbO_3$ and $LiTaO_3$, lithium iron tantalum oxyfluoride, barium strontium niobate, sodium barium niobate, or potassium strontium niobate; or an improper ferroelectric material which includes one of: [PTO/STO]n or [LAO/STO]n, wherein 'n' is between 1 and 100, or a paraelectric material that comprises $SrTiO_3$, $Ba_{(x)}Sr_{(y)}TiO_3$, $HfZrO_2$, Hf-Si-O, La-substituted $PbTiO_3$, or PMN-PT based relaxor ferroelectrics; and depositing a second conductive layer comprising a second conductive nonlinear polar material, wherein the second conductive nonlinear polar material comprises one of $(La,Sr)FeO_3$, $(La,Sr)CoO_3$, $(La,Ca)MnO_3$, $(La,Sr)MnO_3$, $SrRuO_3$, Sr_2RuO_4, $(Ba,Sr)RuO_3$, $SrMoO_3$, $(La,Sr)MnO_3$, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, Ir_2Ox, Ru, RuO_x, Mo, MoO_x, W, or WO_x.

[00140] Example 5: The method of example 1, wherein the initial one or more targets comprise one or more of: Bi, Fe, O, La, Mn, and Sc.

[00141] Example 6: The method of example 2, wherein compounds in the successive one or more targets comprise Bi, Fe, and O, wherein individual stoichiometry within compounds comprising two or more of Bi, Fe and O, can be different by between 5% and 10% from compounds comprising two or more of Bi, Fe, and O, in the initial one or more targets, and wherein individual ones of the one or more targets comprise between 85% and 95% theoretical material density.

[00142] Example 7: The method of example 1, wherein the initial one or more targets includes elemental targets of Bi and Fe, wherein the elemental targets include a purity of at least 99.5%, and wherein the depositing further comprises depositing in a gas comprising one or more of: Ar, O_2, N_2, H_2, Kr, and Ne.

[00143] Example 8: The method of example 1, wherein depositing comprises depositing using a physical vapor deposition tool.

[00144] Example 9: The method of example 1, wherein prior to performing measurements, the method further comprises performing a post deposition anneal (PDA).

[00145] Example 10: The method of example 9, wherein performing the PDA comprises: utilizing a rapid thermal annealing process, wherein: the rapid thermal annealing process comprises heating to a first temperature of less than 700 degrees Celsius, for a time duration between 1s and 60s, at a first pressure between vacuum and 760 Torr; the rapid thermal annealing process further comprises flowing O_2, N_2, or Argon gas while operating at the first

pressure between 1 Torr and 760 Torr; or utilizing a flash anneal process; the flash anneal process comprises heating to a second temperature between 500 and 1300 degrees Celsius, for a second time duration of less than 10 milliseconds, and at a second pressure between vacuum and 760 Torr; the flash anneal process further comprises flowing O_2, N_2, or Argon gas while operating at the second pressure between 1 Torr and 760 Torr; or utilizing a laser anneal process; the laser anneal process comprises heating to a third temperature of up to 1300 degrees Celsius, for a third time duration of less than 100 microseconds, and at a third pressure between vacuum and 760 Torr; the laser anneal process further comprises flowing O_2, N_2, or Argon gas while operating at the third pressure between 1 Torr and 760 Torr; or utilizing a microwave anneal process, wherein the microwave anneal process comprises heating for a fourth time duration of less than 3600s at a microwave power of less than 1000W.

[00146] Example 11: A method comprising: receiving a multi-layer stack comprising a ferroelectric material obtained by utilizing an iterative stack development process; etching the multi-layer stack to form a memory device; performing measurements of compositional and electrical characterization of the memory device; modifying, in response to determining that measurement results are not within tolerance level of target results, composition of one or more layers in the multi-layer stack by utilizing the iterative stack development process; and iterating receiving of the multi-layer stack, etching the multi-layer stack to form a successive memory device, performing measurements of compositional and electrical characterization of the successive memory device, matching measurement of the successive memory device against target results for a memory device, until measurements are within a tolerance level of the target results for the memory device.

[00147] Example 12: The method of example 11, wherein the iterative stack development process comprises: determining a target multi-layer stack, wherein the target multi-layer stack comprises a polar material; implementing a model driven target selection based on a charge:mass ratio and a magnetic moment:mass ratio of target materials; procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition; depositing an initial multi-layer stack using the initial one or more targets; performing measurements of chemical composition and electrical properties of the initial multi-layer stack; determining whether measurement results are within a tolerance level of the target results; modifying, in response to determining that the measurement results are not within the tolerance level, stoichiometric composition of one or more targets in a successive

one or more targets; and iterating depositing a successive multi-layer stack, determining whether measurement results of the successive multi-layer stack are within the tolerance level, until target results are obtained.

[00148] Example 13: The method of example 12, wherein depositing the initial multi-layer stack comprises: depositing a first conductive layer comprising a first conductive material, wherein the first conductive material comprises one of (La,Sr)FeO_3, (La,Sr)CoO_3, (La,Ca)MnO_3, (La,Sr)MnO_3, $SrRuO_3$, Sr_2RuO_4, (Ba,Sr)RuO_3, $SrMoO_3$, (La,Sr)MnO_3, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, Ir_2O_x, Ru, RuO_x, Mo, MoO_x, W, or WO_x; depositing a dielectric layer on the first conductive layer of the dielectric layer comprising one of: a perovskite material which includes one of: $BaTiO_3$, $PbTiO_3$, $KNbO_3$, or $NaTaO_3$; lead zirconium titanate (PZT) or PZT with a doping material, wherein the doping material is one of La or Nb; bismuth ferrite (BFO) with a doping material, wherein the doping material is one of lanthanum, elements from lanthanide series of a periodic table, or elements of a 3d, 4d, 5d, 6d, 4f, and 5f series of the periodic table; a relaxor ferroelectric material which includes one of lead magnesium niobate (PMN), lead magnesium niobate-lead titanate (PMN-PT), lead lanthanum zirconate titanate (PLZT), lead scandium niobate (PSN), barium titanium-bismuth zinc niobium tantalum (BT-BZNT), or Barium titanium-barium strontium titanium (BT-BST); a hexagonal ferroelectric which includes one of: $YMnO_3$ or $LuFeO_3$; hexagonal ferroelectrics of a type h-$RMnO_3$, wherein R is a rare earth element which includes one of: cerium (Ce), dysprosium (Dy), erbium (Er), europium (Eu), gadolinium (Gd), holmium (Ho), lanthanum (La), lutetium (Lu), neodymium (Nd), praseodymium (Pr), promethium (Pm), samarium (Sm), scandium (Sc), terbium (Tb), thulium (Tm), ytterbium (Yb), or yttrium (Y); hafnium (Hf), zirconium (Zr), aluminum (Al), silicon (Si), their oxides, or their alloyed oxides; Hafnium oxides as$Hf_{1-x}E_xO_y$, where E can be Al, Ca, Ce, Dy, Er, Gd, Ge, La, Sc, Si, Sr, Sn, Zr, or Y; $Al_{(1-x)}$Sc(x)N, $Al_{(1-x)}Y_{(x)}N$, $Ga_{(1-x)}Sc_{(x)}N$, $Al_{(1-x-y)}Mg_{(x)}Nb_{(y)}N$, or E doped HfO_2, where 'x' is a fraction; or niobate type compounds $LiNbO_3$, and $LiTaO_3$, lithium iron tantalum oxyfluoride, barium strontium niobate, sodium barium niobate, or potassium strontium niobate; or an improper ferroelectric material which includes one of: [PTO/STO]n or [LAO/STO]n, wherein 'n' is between 1 and 100, or a paraelectric material that comprises $SrTiO_3$, $Ba_{(x)}Sr_{(y)}TiO_3$, $HfZrO_2$, Hf-Si-O, La-substituted $PbTiO_3$, or a PMN-PT based relaxor ferroelectrics; and depositing a second conductive layer comprising a second conductive nonlinear polar material, wherein the second conductive nonlinear polar material comprises one of (La,Sr)FeO_3, (La,Sr)CoO_3, (La,Ca)MnO_3, (La,Sr)MnO_3, $SrRuO_3$, Sr_2RuO_4, (Ba,Sr)RuO_3, $SrMoO_3$, (La,Sr)MnO_3,

$SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, Ir_2O_x, Ru, RuO_x, Mo, MoO_x, W, or WO_x.

[00149] Example 14: The method of example 12, wherein compounds in the initial one or more targets comprise Bi, Fe, and O, wherein individual stoichiometry within compounds comprising two or more of Bi, Fe, and O can be different by at least 5% from compounds comprising two or more of Bi, Fe, and O in the initial one or more targets.

[00150] Example 15: The method of example 12, wherein the initial one or more targets includes elemental targets of Bi and Fe, wherein the elemental targets include a purity of at least 99.5%, and wherein depositing the initial multi-layer stack further comprises depositing in a gas comprising one or more of: Ar, O_2, N_2, H_2, Kr, and Ne.

[00151] Example 16: The method of example 11, wherein prior to etching the method further comprises annealing the multi-layer stack, wherein annealing comprises utilizing a rapid thermal annealing process, wherein the rapid thermal annealing process comprises heating to a first temperature of less than 700 degrees Celsius, for a time duration between 1s and 60s, at a first pressure between vacuum and 760 Torr, and wherein the rapid thermal annealing process further comprises flowing O_2, N_2, or Argon gas while operating at the first pressure between 1 Torr and 760 Torr.

[00152] Example 17: The method of example 11, wherein the method further comprises forming an encapsulation layer directly surrounding the memory device, wherein the encapsulation layer comprises metal and oxygen, including one of Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x, wherein Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x are deposited without a hydrogen or ammonia containing chemical precursor in an ALD deposition process.

[00153] Example 18: A method comprising: fabricating a transistor or receiving a workpiece comprising a transistor; forming a memory device comprising a multi-layer stack, wherein the memory device is coupled with a gate or a drain of the transistor; performing measurements of compositional and electrical characterization of the memory device coupled with the transistor, and matching measurements against target results for a reference memory device coupled to a reference transistor; modifying, in response to determining that the measurements are not within a tolerance level of the target results for the reference memory device coupled to the reference transistor, composition of one or more layers in the multi-layer stack by utilizing an iterative stack development process; and iterating fabricating of the transistor or receiving the workpiece comprising the transistor, forming a successive memory device, performing measurements of compositional and electrical characterization of the successive memory device coupled with the transistor, matching measurement of the

successive memory device coupled with the transistor against target results for the reference memory device coupled with the reference transistor, until measurements are within a tolerance level of the target results.

[00154] Example 19: The method of example 18, wherein the iterative stack development process comprises: determining a target multi-layer stack, wherein the target multi-layer stack comprises a ferroelectric material; implementing a model driven target selection based on a charge:mass ratio and a magnetic moment:mass ratio of target materials; procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition; depositing, using the initial one or more targets, an initial multi-layer stack; performing measurements of chemical composition and electrical properties of the initial multi-layer stack; matching measurements of chemical composition and electrical properties of the initial multi-layer stack against target results; determining whether measurement results are within a tolerance level of the target results; modifying, in response to determining that the measurement results are not within the tolerance level, stoichiometric composition of one or more targets in a successive one or more targets; and iterating depositing a successive multi-layer stack, determining whether measurement results of the successive multi-layer stack are within the tolerance level, until target results are obtained.

[00155] Example 20: The method of example 18, wherein forming the memory device comprises etching the multi-layer stack, and wherein the method further comprises forming an encapsulation around the memory device, prior to performing measurements of compositional and electrical characterization of the memory device coupled with the transistor.

[00156] Example 21: The method of example 19, wherein compounds in the successive one or more targets comprise Bi, Fe, and O, wherein individual stoichiometry within compounds comprising two or more of Bi, Fe, and O can be different by 5% from compounds comprising two or more of Bi, Fe, and O in the initial one or more targets.

[00157] Example 22: The method of example 18, wherein prior to etching the method further comprises annealing the multi-layer stack, wherein annealing comprises utilizing a rapid thermal annealing process, wherein the rapid thermal annealing process comprises heating to a first temperature of less than 700 degrees Celsius, for a time duration between 1s and 60s, at a first pressure between vacuum and 760 Torr, and wherein the rapid thermal annealing process further comprises flowing O_2, N_2, or Argon gas while operating at the first pressure between 1 Torr and 760 Torr.

[00158] Example 23: The method of example 18, wherein the method further comprises forming an encapsulation layer directly surrounding the memory device, wherein the encapsulation layer comprises metal and oxygen, including one of: Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x, wherein Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x are deposited without a hydrogen or ammonia containing chemical precursor in an ALD deposition process.

[00159] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the examples. The following examples are hereby incorporated into the detailed description, with each example or feature of an example standing on its own as an embodiment.

1. A method comprising:
   determining a target multi-layer stack, wherein the target multi-layer stack comprises a polar material;
   implementing a model driven target selection based on a charge:mass ratio and a magnetic moment:mass ratio of target materials;
   procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition;
   depositing, using the initial one or more targets, an initial multi-layer stack;
   performing measurements of chemical composition and electrical properties of the initial multi-layer stack;
   modifying, in response to determining that measurement results are not within tolerance levels of target results, composition of one or more layers in the initial multi-layer stack; and
   iterating depositing of a successive multi-layer stack and determining whether the measurement results of the successive multi-layer stack are within the tolerance levels, until target results are obtained.

2. The method of claim 1, wherein modifying composition of one or more layers in the initial multi-layer stack further comprises:
   implementing the model driven target selection based on the charge:mass ratio and the magnetic moment:mass ratio of the target materials;
   modifying stoichiometric composition of one or more targets in a successive one or more targets; and
   procuring the successive one or more targets.

3. The method of claim 1, wherein after depositing the successive multi-layer stack, the method further comprises:
   performing measurements of chemical composition and electrical properties of the successive multi-layer stack; and
   matching measurements of chemical composition and electrical properties of the successive multi-layer stack against target results.

4. The method of claim 1, wherein depositing the initial multi-layer stack comprises:

depositing a first conductive layer comprising a first conductive material, wherein the first conductive material comprises one of (La,Sr)FeO_3, (La,Sr)CoO_3, (La,Ca)MnO_3, (La,Sr)MnO_3, $SrRuO_3$, Sr_2RuO_4, (Ba,Sr)RuO_3, $SrMoO_3$, (La,Sr)MnO_3, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, Ir_2O_x, Ru, RuO_x, Mo, MoO_x, W or WO_x;

depositing a dielectric layer on the first conductive layer the dielectric layer comprising one of:

a perovskite material which includes one of: $BaTiO_3$, $PbTiO_3$, $KNbO_3$, or $NaTaO_3$;

lead zirconium titanate (PZT), or PZT with a doping material, wherein the doping material is one of La or Nb;

bismuth ferrite (BFO) with a doping material, wherein the doping material is one of lanthanum, elements from lanthanide series of a periodic table, or elements of a 3d, 4d, 5d, 6d, 4f and 5f series of the periodic table;

a relaxor ferroelectric material which includes one of lead magnesium niobate (PMN), lead magnesium niobate-lead titanate (PMN-PT), lead lanthanum zirconate titanate (PLZT), lead scandium niobate (PSN), barium titanium-bismuth zinc niobium tantalum (BT-BZNT), or Barium titanium-barium strontium titanium (BT-BST);

hexagonal ferroelectric which includes one of: $YMnO_3$ or $LuFeO_3$;

hexagonal ferroelectrics of a type h-$RMnO_3$, wherein R is a rare earth element which includes one of: cerium (Ce), dysprosium (Dy), erbium (Er), europium (Eu), gadolinium (Gd), holmium (Ho), lanthanum (La), lutetium (Lu), neodymium (Nd), praseodymium (Pr), promethium (Pm), samarium (Sm), scandium (Sc), terbium (Tb), thulium (Tm), ytterbium (Yb), or yttrium (Y); hafnium (Hf), zirconium (Zr), aluminum (Al), silicon (Si), their oxides or their alloyed oxides;

Hafnium oxides as Hf1-x Ex Oy, where E can be Al, Ca, Ce, Dy, Er, Gd, Ge, La, Sc, Si, Sr, Sn, Zr, or Y; Al(1-x)Sc(x)N, Ga(1-x)Sc(x)N, Al(1-x)Y(x)N or Al(1-x-y)Mg(x)Nb(y)N, y doped HfO_2, where x includes one of: Al, Ca, Ce, Dy, Er, Gd, Ge, La, Sc, Si, Sr, Sn, or Y, wherein ‘x’ is a fraction; or niobate type compounds $LiNbO_3$, $LiTaO_3$, lithium iron tantalum oxyfluoride, barium strontium niobate, sodium barium niobate, or potassium strontium niobate; or

an improper ferroelectric material which includes one of: [PTO/STO]n or [LAO/STO]n, wherein 'n' is between 1 and 100, or a paraelectric material that comprises $SrTiO_3$, Ba(x)Sr(y)TiO_3, $HfZrO_2$, Hf-Si-O, La-substituted $PbTiO_3$, or a PMN-PT based relaxor ferroelectrics; and

depositing a second conductive layer comprising a second conductive nonlinear polar material, wherein the second conductive nonlinear polar material comprises one of (La,Sr)FeO_3, (La,Sr)CoO_3, (La,Ca)MnO_3, (La,Sr)MnO_3, $SrRuO_3$, Sr_2RuO_4, (Ba,Sr)RuO_3, $SrMoO_3$, (La,Sr)MnO_3, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, Ir2O_x, Ru, RuO_x, Mo, MoO_x, W or WO_x.

5. The method of claim 1, wherein the initial one or more targets comprise one or more of Bi, Fe, O, La, Mn and Sc.

6. The method of claim 2, wherein compounds in the successive one or more targets comprise Bi, Fe, and O, wherein individual stoichiometry within compounds comprising two or more of Bi, Fe and O, can be different by between 5% and 10% from compounds comprising two or more of Bi, Fe and O, in the initial one or more targets, and wherein individual ones of the one or more targets comprise 85% to 95% theoretical material density.

7. The method of claim 1, wherein the initial one or more targets includes elemental targets of Bi and Fe, wherein the elemental targets include a purity of at least 99.5%, and wherein the depositing further comprises depositing in a gas comprising one or more of Ar, O_2, N_2, H_2, Kr, and Ne.

8. The method of claim 1, wherein depositing comprises depositing using a physical vapor deposition tool.

9. The method of claim 1, wherein prior to performing measurements, the method further comprises performing a post deposition anneal (PDA).

10. The method of claim 9, wherein performing the PDA comprises:

utilizing a rapid thermal annealing process, wherein:

the rapid thermal annealing process comprises heating to a first temperature of less than 700 degrees Celsius, for a time duration between 1s and 60s, at a first pressure between vacuum and 760 Torr;

the rapid thermal annealing process further comprises flowing O_2, N_2 or Argon gas while operating at the first pressure between 1 Torr and 760 Torr; or utilizing a flash anneal process;

the flash anneal process comprises heating to a second temperature between 500 and 1300 degrees Celsius, for a second time duration of less than 10 millisecond, and at a second pressure between vacuum and 760 Torr;

the flash anneal process further comprises flowing O_2, N_2 or Argon gas while operating at the second pressure between 1 Torr and 760 Torr; or utilizing a laser anneal process;

the laser anneal process comprises heating to a third temperature of up to 1300 degrees Celsius, for a third time duration of less than 100 microseconds, and at a third pressure between vacuum and 760 Torr;

the laser anneal process further comprises flowing O_2, N_2 or Argon gas while operating at the third pressure between 1 Torr and 760 Torr; or

utilizing a microwave anneal process, wherein the microwave anneal process comprises heating for a fourth time duration of less than 3600s at a microwave power of less than 1000W.

11. A method comprising:

receiving a multi-layer stack comprising a ferroelectric material obtained by utilizing an iterative stack development process;

etching the multi-layer stack to form a memory device;

performing measurements of compositional and electrical characterization of the memory device;

modifying, in response to determining that measurement results are not within tolerance level of target results, composition of one or more layers in the multi-layer stack by utilizing the iterative stack development process; and

iterating receiving of the multi-layer stack, etching the multi-layer stack to form a successive memory device, performing measurements of compositional and electrical characterization of the successive memory device, matching measurement of the

successive memory device against target results for a memory device, until measurements are within a tolerance level of the target results for the memory device.

12. The method of claim 11, wherein the iterative stack development process comprises:
determining a target multi-layer stack, wherein the target multi-layer stack comprises a polar material;
implementing a model driven target selection based on a charge:mass ratio and a magnetic moment:mass ratio of target materials;
procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition;
depositing an initial multi-layer stack using the initial one or more targets;
performing measurements of chemical composition and electrical properties of the initial multi-layer stack;
determining whether measurement results are within a tolerance level of the target results;
modifying, in response to determining that the measurement results are not within the tolerance level, stoichiometric composition of one or more targets in a successive one or more targets; and
iterating depositing a successive multi-layer stack, determining whether measurement results of the successive multi-layer stack are within the tolerance level, until target results are obtained.

13. The method of claim 12, wherein depositing the initial multi-layer stack comprises:
depositing a first conductive layer comprising a first conductive material, wherein the first conductive material comprises one of $(La,Sr)FeO_3$, $(La,Sr)CoO_3$, $(La,Ca)MnO_3$, $(La,Sr)MnO_3$, $SrRuO_3$, Sr_2RuO_4, $(Ba,Sr)RuO_3$, $SrMoO_3$, $(La,Sr)MnO_3$, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, $Ir2O_x$, Ru, RuO_x, Mo, MoO_x, W or WO_x;
depositing a dielectric layer on the first conductive layer the dielectric layer comprising one of:
a perovskite material which includes one of: $BaTiO_3$, $PbTiO_3$, $KNbO_3$, or $NaTaO_3$;

lead zirconium titanate (PZT), or PZT with a doping material, wherein the doping material is one of La or Nb;

bismuth ferrite (BFO) with a doping material, wherein the doping material is one of lanthanum, elements from lanthanide series of a periodic table, or elements of a 3d, 4d, 5d, 6d, 4f and 5f series of the periodic table;

a relaxor ferroelectric material which includes one of lead magnesium niobate (PMN), lead magnesium niobate-lead titanate (PMN-PT), lead lanthanum zirconate titanate (PLZT), lead scandium niobate (PSN), barium titanium-bismuth zinc niobium tantalum (BT-BZNT), or Barium titanium-barium strontium titanium (BT-BST);

hexagonal ferroelectric which includes one of: $YMnO_3$ or $LuFeO_3$;

hexagonal ferroelectrics of a type h-$RMnO_3$, wherein R is a rare earth element which includes one of: cerium (Ce), dysprosium (Dy), erbium (Er), europium (Eu), gadolinium (Gd), holmium (Ho), lanthanum (La), lutetium (Lu), neodymium (Nd), praseodymium (Pr), promethium (Pm), samarium (Sm), scandium (Sc), terbium (Tb), thulium (Tm), ytterbium (Yb), or yttrium (Y); hafnium (Hf), zirconium (Zr), aluminum (Al), silicon (Si), their oxides or their alloyed oxides;

Hafnium oxides as Hf1-x Ex Oy, where E can be Al, Ca, Ce, Dy, Er, Gd, Ge, La, Sc, Si, Sr, Sn, Zr, or Y; Al(1-x)Sc(x)N, Ga(1-x)Sc(x)N, Al(1-x)Y(x)N or Al(1-x-y)Mg(x)Nb(y)N, y doped HfO_2, where x includes one of: Al, Ca, Ce, Dy, Er, Gd, Ge, La, Sc, Si, Sr, Sn, or Y, wherein 'x' is a fraction; or niobate type compounds $LiNbO_3$, $LiTaO_3$, lithium iron tantalum oxyfluoride, barium strontium niobate, sodium barium niobate, or potassium strontium niobate; or

an improper ferroelectric material which includes one of: [PTO/STO]n or [LAO/STO]n, wherein 'n' is between 1 to 100, or a paraelectric material that comprises $SrTiO_3$, $Ba(x)Sr(y)TiO_3$, $HfZrO_2$, Hf-Si-O, La-substituted $PbTiO_3$, or a PMN-PT based relaxor ferroelectrics; and

depositing a second conductive layer comprising a second conductive nonlinear polar material, wherein the second conductive nonlinear polar material comprises one of $(La,Sr)FeO_3$, $(La,Sr)CoO_3$, $(La,Ca)MnO_3$, $(La,Sr)MnO_3$, $SrRuO_3$, Sr_2RuO_4, $(Ba,Sr)RuO_3$, $SrMoO_3$, $(La,Sr)MnO_3$, $SrCoO_3$, $SrCrO_3$, $SrFeO_3$, $SrVO_3$, $CaMoO_3$, $SrNbO_3$, $LaNiO_3$, $YBa_2Cu_3O_7$, $Bi_2Sr_2CaCuO_8$, $CaRuO_3$, Ir, $Ir2O_x$, Ru, RuO_x, Mo, MoO_x, W or WO_x.

14. The method of claim 12, wherein compounds in the initial one or more targets comprise Bi, Fe and O, wherein individual stoichiometry within compounds comprising two or more of Bi, Fe, and O, can be different by at least 5% from compounds comprising two or more of Bi, Fe, and O, in the initial one or more targets.

15. The method of claim 12, wherein the initial one or more targets includes elemental targets of Bi and Fe, wherein the elemental targets include a purity of at least 99.5%, and wherein depositing the initial multi-layer stack further comprises depositing in a gas comprising one or more of Ar, O_2, N_2, H_2, Kr, and Ne.

16. The method of claim 11, wherein prior to etching the method further comprises annealing the multi-layer stack, wherein annealing comprises utilizing a rapid thermal annealing process, wherein the rapid thermal annealing process comprises heating to a first temperature of less than 700 degrees Celsius, for a time duration between 1s and 60s, at a first pressure between vacuum and 760 Torr, and wherein the rapid thermal annealing process further comprises flowing O_2, N_2 or Argon gas while operating at the first pressure between 1 Torr and 760 Torr.

17. The method of claim 11, wherein the method further comprises forming an encapsulation layer directly surrounding the memory device, wherein the encapsulation layer comprises metal and oxygen, including one of Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x, wherein Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x are deposited without a hydrogen or ammonia containing chemical precursor in an ALD deposition process.

18. A method comprising:
    fabricating a transistor or receiving a workpiece comprising a transistor;
    forming a memory device comprising a multi-layer stack, wherein the memory device is coupled with a gate or a drain of the transistor;
    performing measurements of compositional and electrical characterization of the memory device coupled with the transistor, and matching measurements against target results for a reference memory device coupled to a reference transistor;
    modifying, in response to determining that the measurements are not within a tolerance level of the target results for the reference memory device coupled to the reference

transistor, composition of one or more layers in the multi-layer stack by utilizing an iterative stack development process; and

iterating fabricating of the transistor or receiving the workpiece comprising the transistor, forming a successive memory device, performing measurements of compositional and electrical characterization of the successive memory device coupled with the transistor, matching measurement of the successive memory device coupled with the transistor against target results for the reference memory device coupled with the reference transistor, until measurements are within a tolerance level of the target results.

19. The method of claim 18, wherein the iterative stack development process comprises:

determining a target multi-layer stack, wherein the target multi-layer stack comprises a ferroelectric material;

implementing a model driven target selection based on a charge:mass ratio and a magnetic moment:mass ratio of target materials;

procuring an initial one or more targets, wherein individual targets in the initial one or more targets comprise single elements or a combination of elements with a respective initial stoichiometric composition;

depositing, using the initial one or more targets, an initial multi-layer stack;

performing measurements of chemical composition and electrical properties of the initial multi-layer stack;

matching measurements of chemical composition and electrical properties of the initial multi-layer stack against target results;

determining whether measurement results are within a tolerance level of the target results;

modifying, in response to determining that the measurement results are not within the tolerance level, stoichiometric composition of one or more targets in a successive one or more targets; and

iterating depositing a successive multi-layer stack, determining whether measurement results of the successive multi-layer stack are within the tolerance level, until target results are obtained.

20. The method of claim 18, wherein forming the memory device comprises etching the multi-layer stack, and wherein the method further comprises forming an encapsulation

around the memory device, prior to performing measurements of compositional and electrical characterization of the memory device coupled with the transistor.

21. The method of claim 19, wherein compounds in the successive one or more targets comprise Bi, Fe and O, wherein individual stoichiometry within compounds comprising two or more of Bi, Fe and O, can be different by 5% from compounds comprising two or more of Bi, Fe and O, in the initial one or more targets.

22. The method of claim 18, wherein prior to etching the method further comprises annealing the multi-layer stack, wherein annealing comprises utilizing a rapid thermal annealing process, wherein the rapid thermal annealing process comprises heating to a first temperature of less than 700 degrees Celsius, for a time duration between 1s and 60s, at a first pressure between vacuum and 760 Torr, and wherein the rapid thermal annealing process further comprises flowing O_2, N_2 or Argon gas while operating at the first pressure between 1 Torr and 760 Torr.

23. The method of claim 18, wherein the method further comprises forming an encapsulation layer directly surrounding the memory device, wherein the encapsulation layer comprises metal and oxygen, including one of: Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x, wherein Al_xO_y, HfO_x, $AlSiO_x$, ZrO_x, or TiO_x are deposited without a hydrogen or ammonia containing chemical precursor in an ALD deposition process.

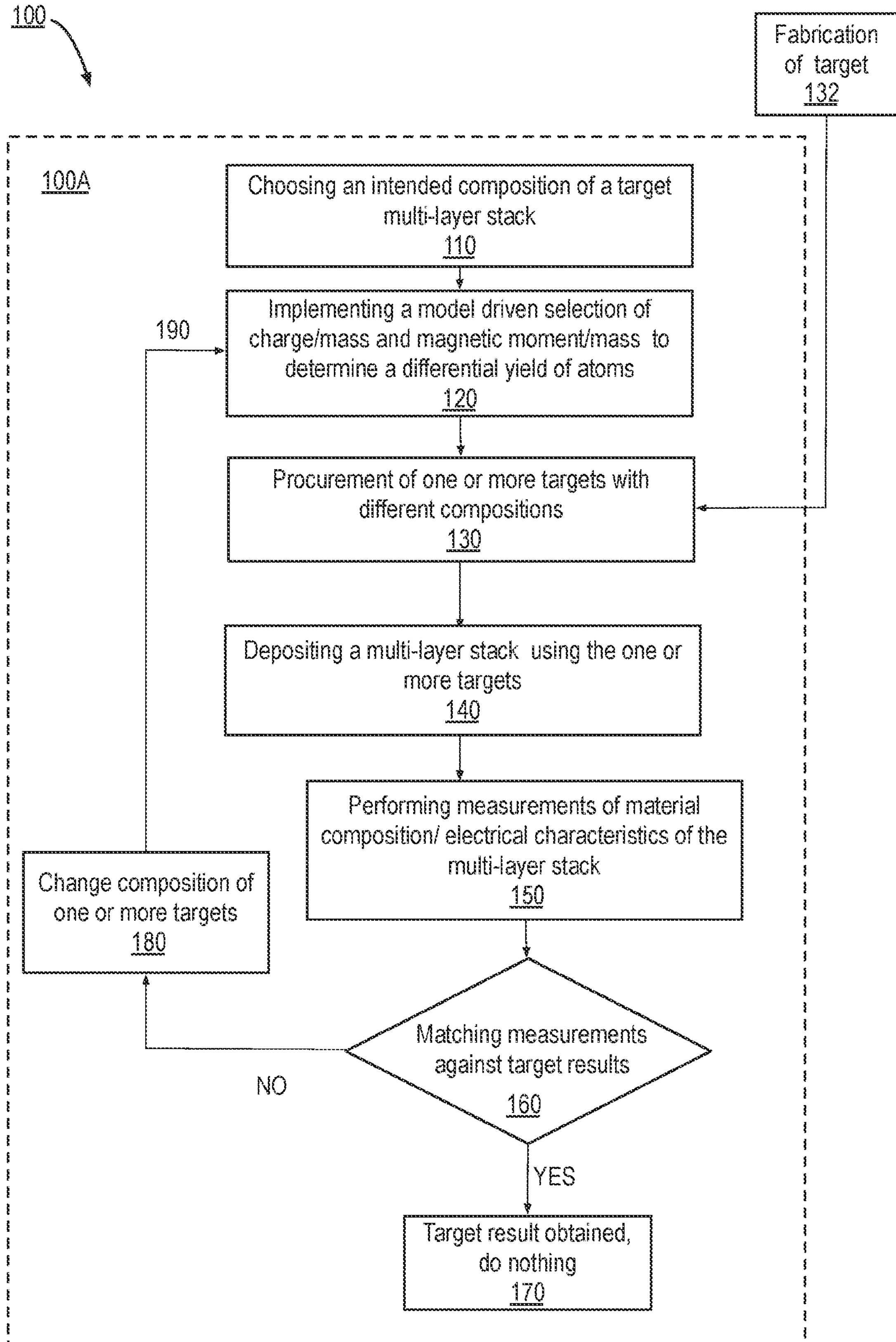


FIG. 1

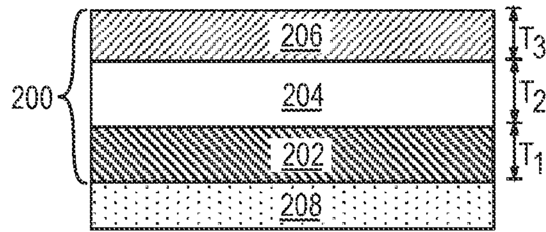


FIG. 2A

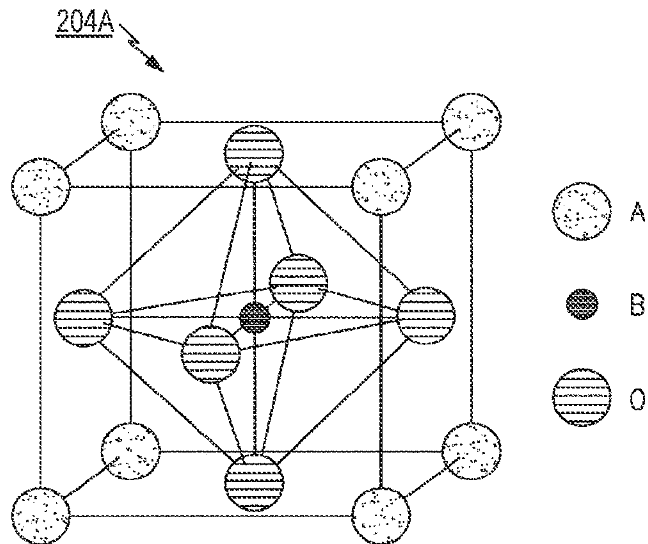


FIG. 2B

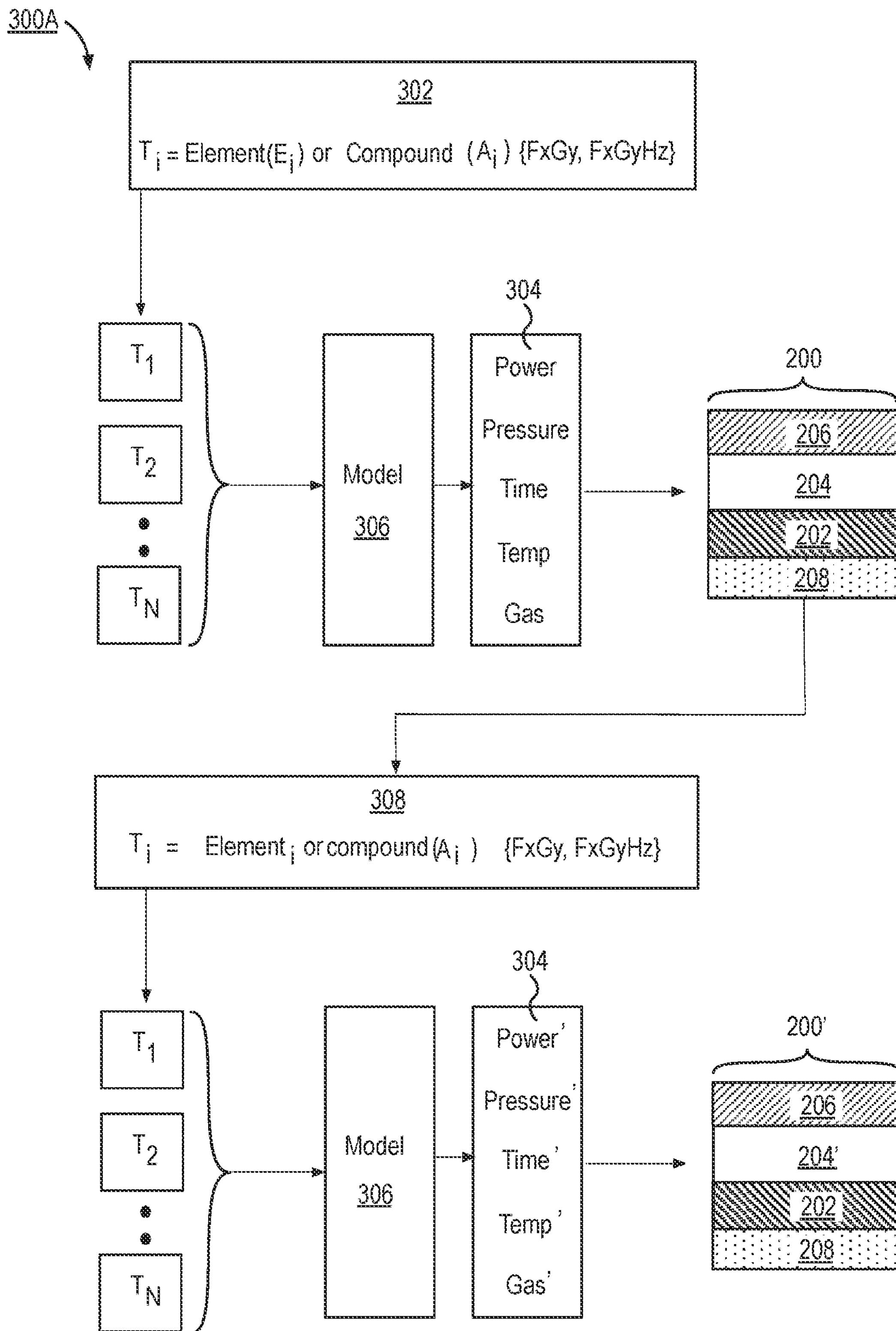


FIG. 3A

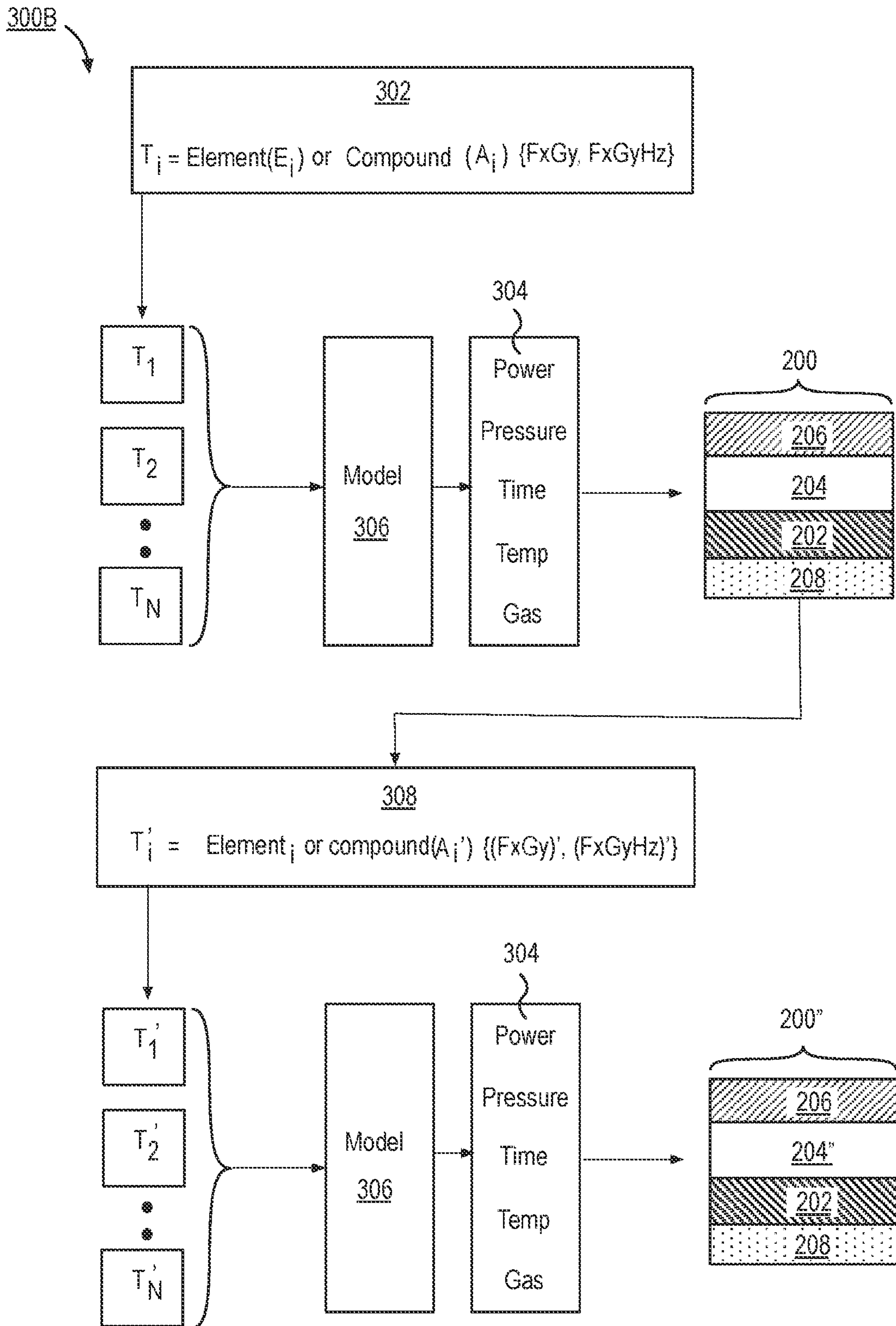


FIG. 3B

FIG. 4

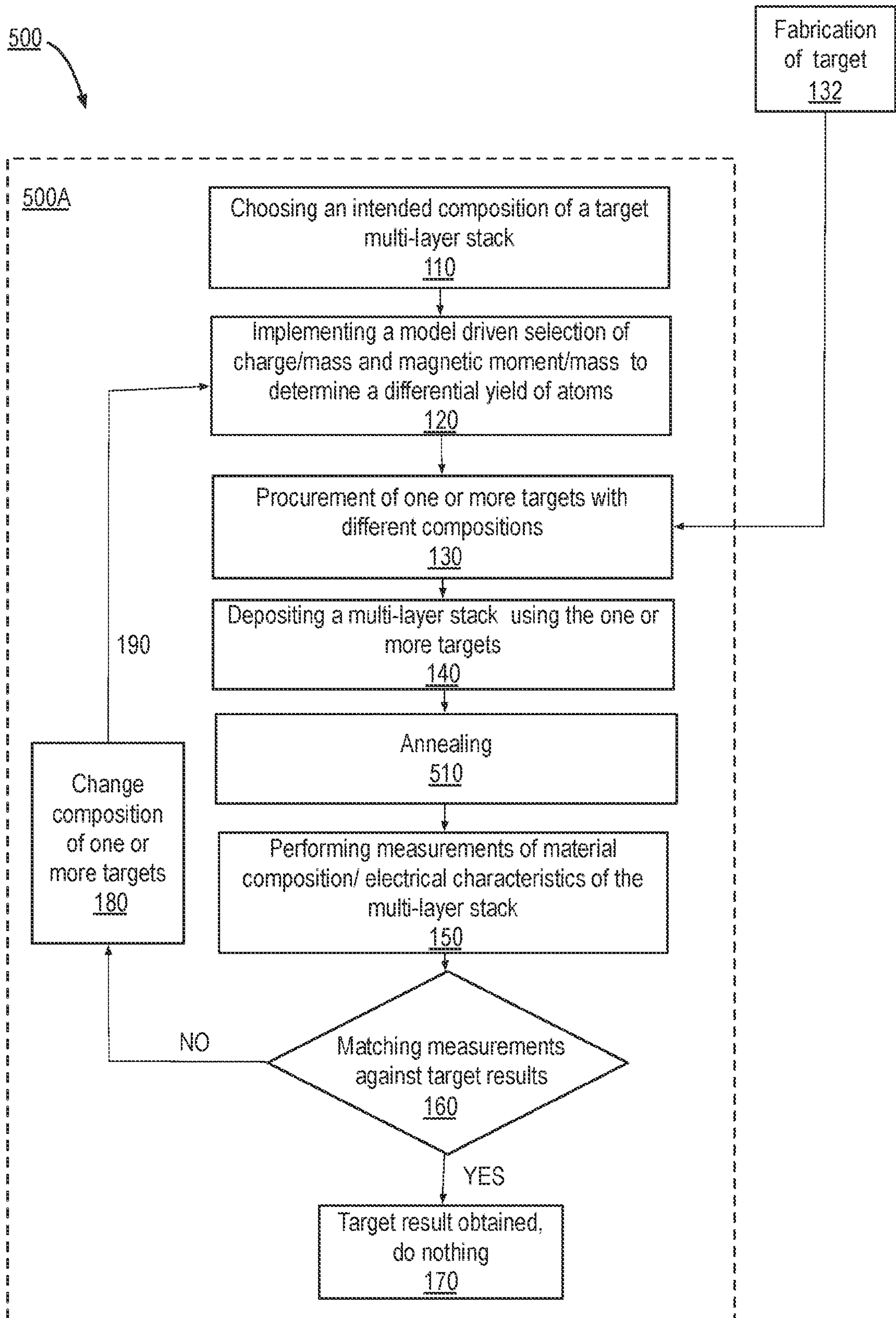


FIG. 5

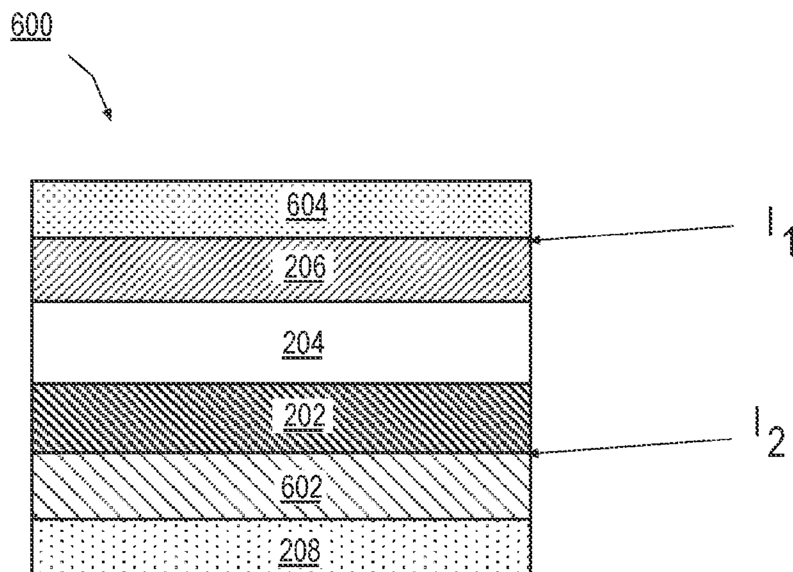


FIG. 6

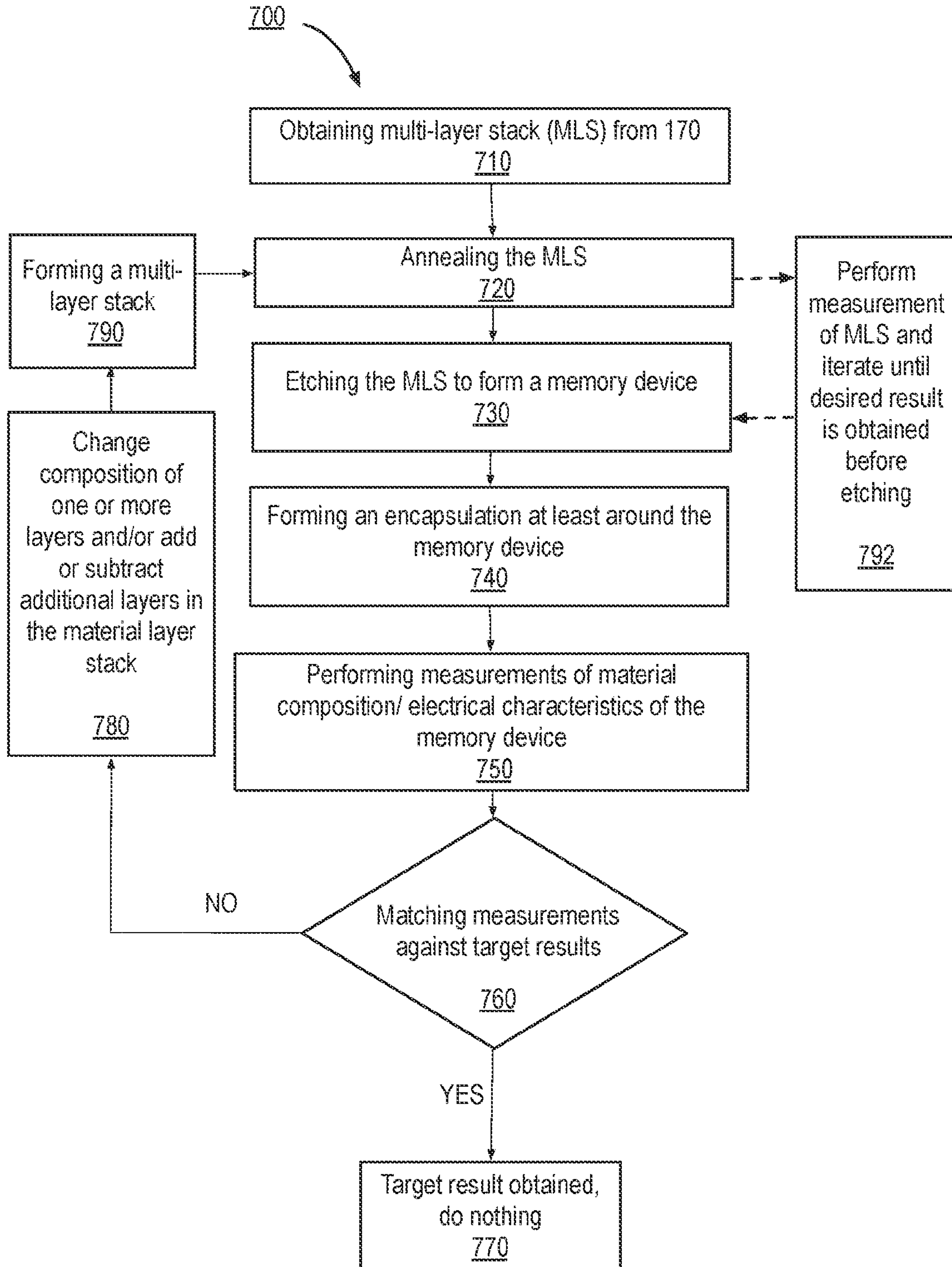


FIG. 7

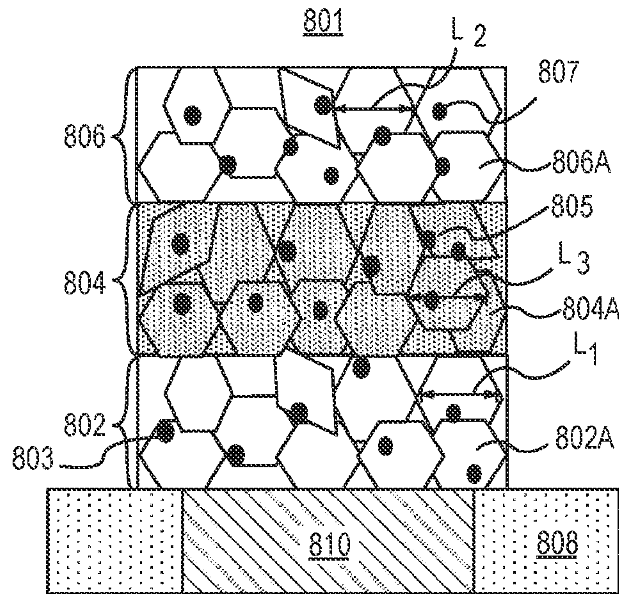


FIG. 8A

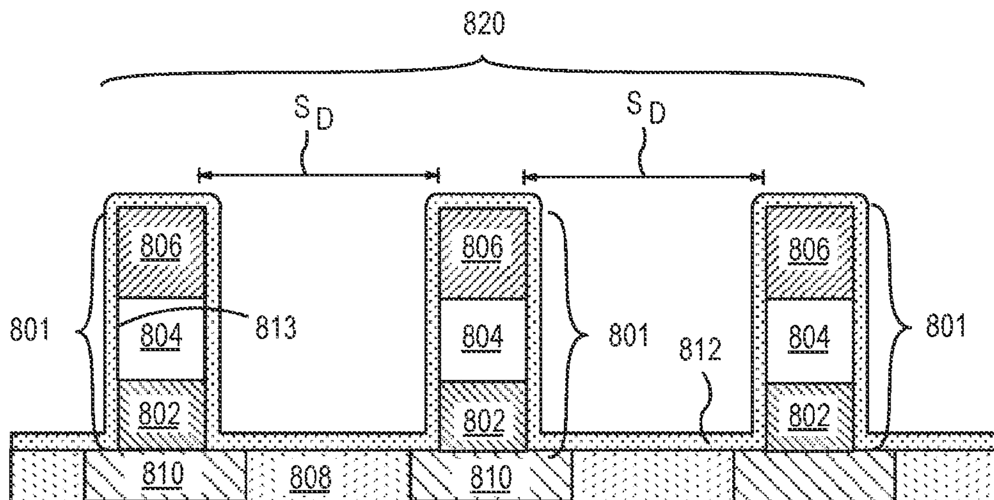
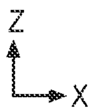


FIG. 8B



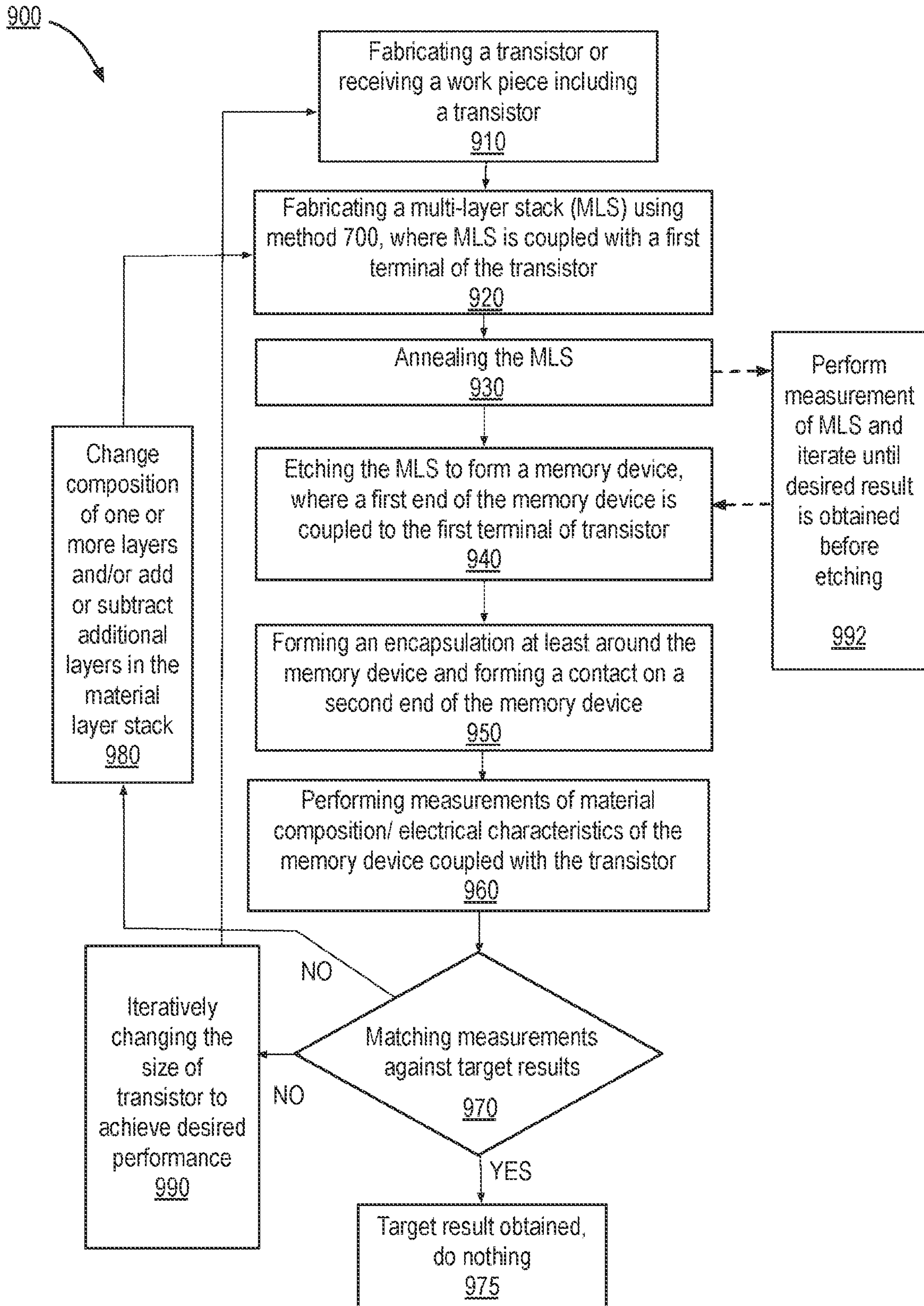


FIG. 9

1000

1020

1016

1014

806

801

804

812

802

808

810

1022

1004

1003

1005

1007

1011

1002

1010

1018A

1012

1010A

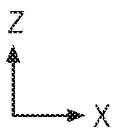
1012A

1018

1006

1008

FIG. 10



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2023/077120

A. CLASSIFICATION OF SUBJECT MATTER

H10N 97/00(2023.01)i; **H10B 53/30**(2023.01)i; **H01L 21/02**(2006.01)i; **H01L 21/285**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H10N 97/00(2023.01); C04B 35/49(2006.01); G01N 23/2204(2018.01); G01N 23/2206(2018.01); G06F 30/20(2020.01); G06F 30/3308(2020.01); H01B 3/12(2006.01); H01L 27/105(2006.01); H01L 49/02(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: memory, material, ratio, measurement, modify, iterate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004-0043522 A1 (YUKINOBU HIKOSAKA) 04 March 2004 (2004-03-04) paragraphs [0007]-[0104]; claims 1-15; and figures 2A-2D	11,16,18,20,22
Y		17,23
A		1-10,12-15,19,21
Y	US 2015-0004718 A1 (CYPRESS SEMICONDUCTOR CORPORATION) 01 January 2015 (2015-01-01) paragraph [0032]; and claim 1	17,23
A	US 2021-0240896 A1 (APPLIED MATERIALS, INC.) 05 August 2021 (2021-08-05) claims 1, 9; and figures 1-3	1-23
A	US 2021-0063329 A1 (KLA CORPORATION) 04 March 2021 (2021-03-04) claims 1-16; and figure 1	1-23

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 February 2024	**06 February 2024**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**KIM, Sung Hoon**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-8710**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/077120

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 11-292626 A (MITSUBISHI MATERIALS CORP. et al.) 26 October 1999 (1999-10-26) paragraphs [0012]-[0058]	1-23

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2023/077120

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2004-0043522 A1	04 March 2004	CN 1479366 A	03 March 2004
		JP 2004-095678 A	25 March 2004
		JP 4267275 B2	27 May 2009
		KR 10-0863117 B1	14 October 2008
		KR 10-2004-0019846 A	06 March 2004
		TW 200403813 A	01 March 2004
		US 6743647 B2	01 June 2004
US 2015-0004718 A1	01 January 2015	CN 105308737 A	03 February 2016
		CN 111785722 A	16 October 2020
		JP 2016-526798 A	05 September 2016
		JP 6563390 B2	21 August 2019
		TW 201523795 A	16 June 2015
		US 9548348 B2	17 January 2017
		WO 2014-209559 A1	31 December 2014
US 2021-0240896 A1	05 August 2021	CN 115151909 A	04 October 2022
		EP 4100861 A1	14 December 2022
		JP 2023-514984 A	12 April 2023
		KR 10-2022-0131334 A	27 September 2022
		TW 202143080 A	16 November 2021
		TW 202247022 A	01 December 2022
		US 11126769 B2	21 September 2021
		US 11763052 B2	19 September 2023
		US 2022-0004689 A1	06 January 2022
		WO 2021-158296 A1	12 August 2021
US 2021-0063329 A1	04 March 2021	CN 114207419 A	18 March 2022
		JP 2022-545724 A	28 October 2022
		KR 10-2022-0050976 A	25 April 2022
		KR 10-2557179 B1	18 July 2023
		TW 202111319 A	16 March 2021
		US 11460418 B2	04 October 2022
		WO 2021-040936 A1	04 March 2021
JP 11-292626 A	26 October 1999	EP 0950727 A1	20 October 1999
		KR 10-0453416 B1	13 June 2005
		KR 10-1999-0081803 A	15 November 1999
		US 2001-0016229 A1	23 August 2001
		US 6203608 B1	20 March 2001