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(54) **CLOSELY PACKED VERTICAL TRANSISTORS WITH REDUCED CONTACT RESISTANCE**

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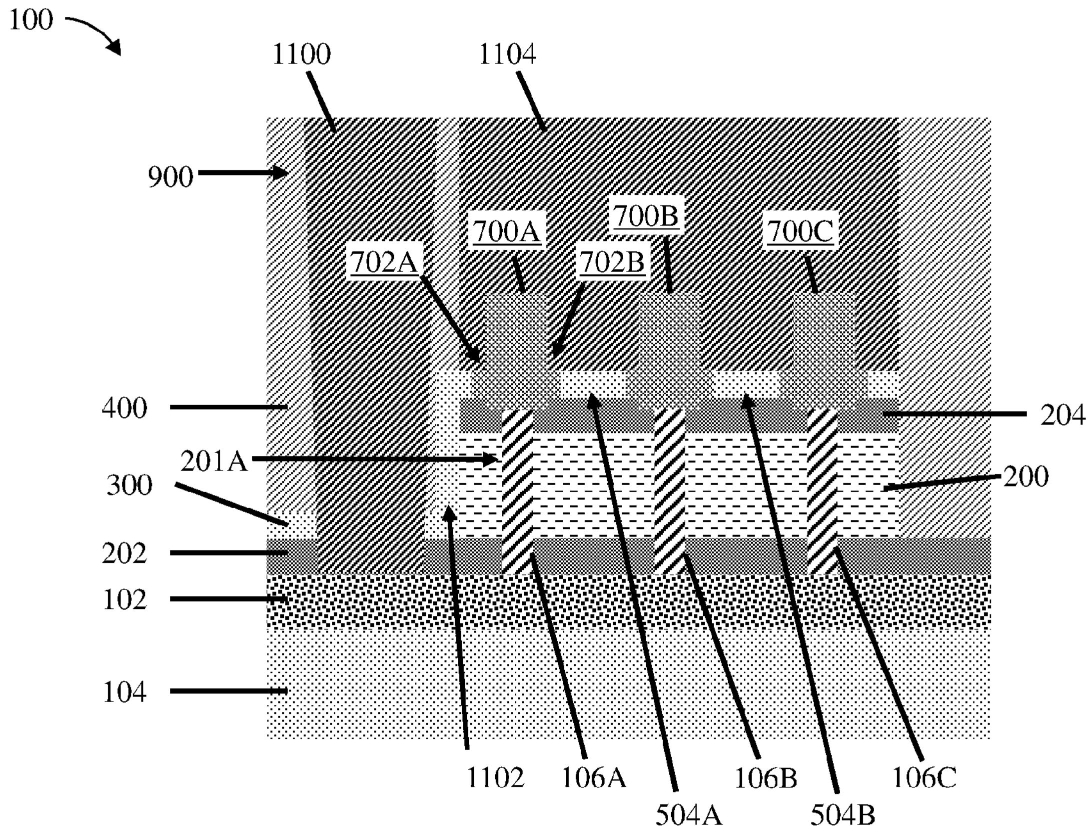
(57) **ABSTRACT**

A method of forming a semiconductor device and resulting structures having closely packed vertical transistors with reduced contact resistance by forming a semiconductor structure on a doped region of a substrate, the semiconductor structure including a gate formed over a channel region of a semiconductor fin. A liner is formed on the gate and the semiconductor fin, and a dielectric layer is formed on the liner. Portions of the liner are removed to expose a top surface and sidewalls of the semiconductor fin and a side-wall of the dielectric layer. A recessed opening is formed by recessing portions of the liner from the exposed sidewall of the dielectric layer. A top epitaxy region is formed on the exposed portions of the semiconductor fin and dielectric layer such that an extension of the top epitaxy region fills the recessed opening. The top epitaxy region is confined between portions of the liner.



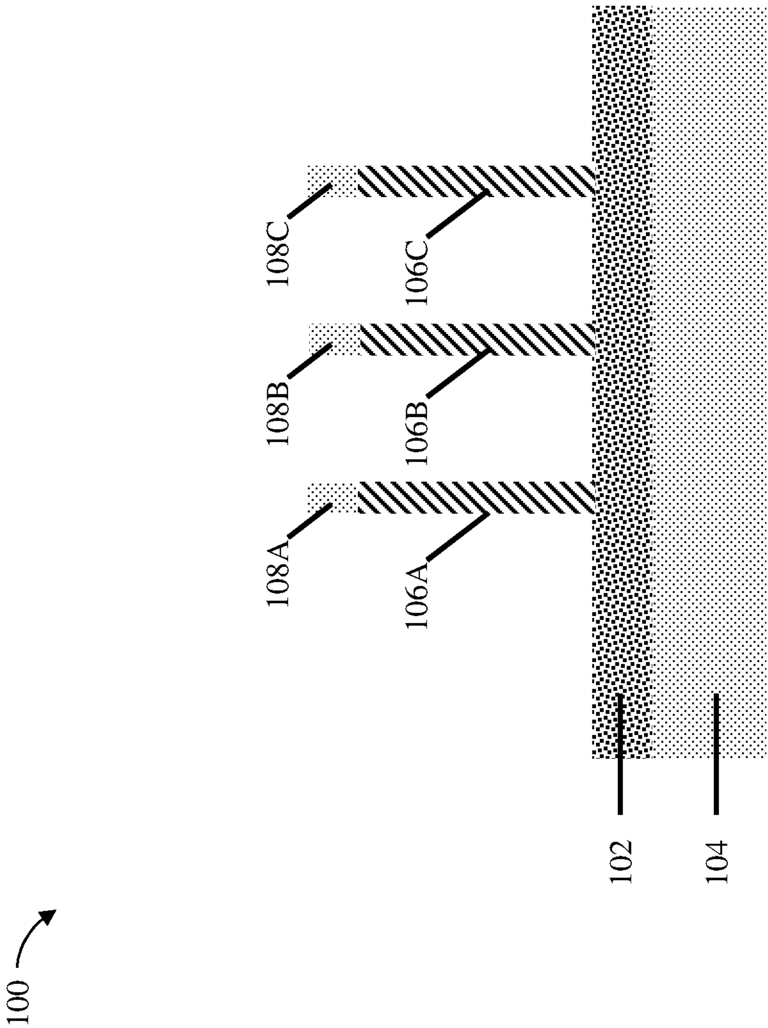


Fig. 1

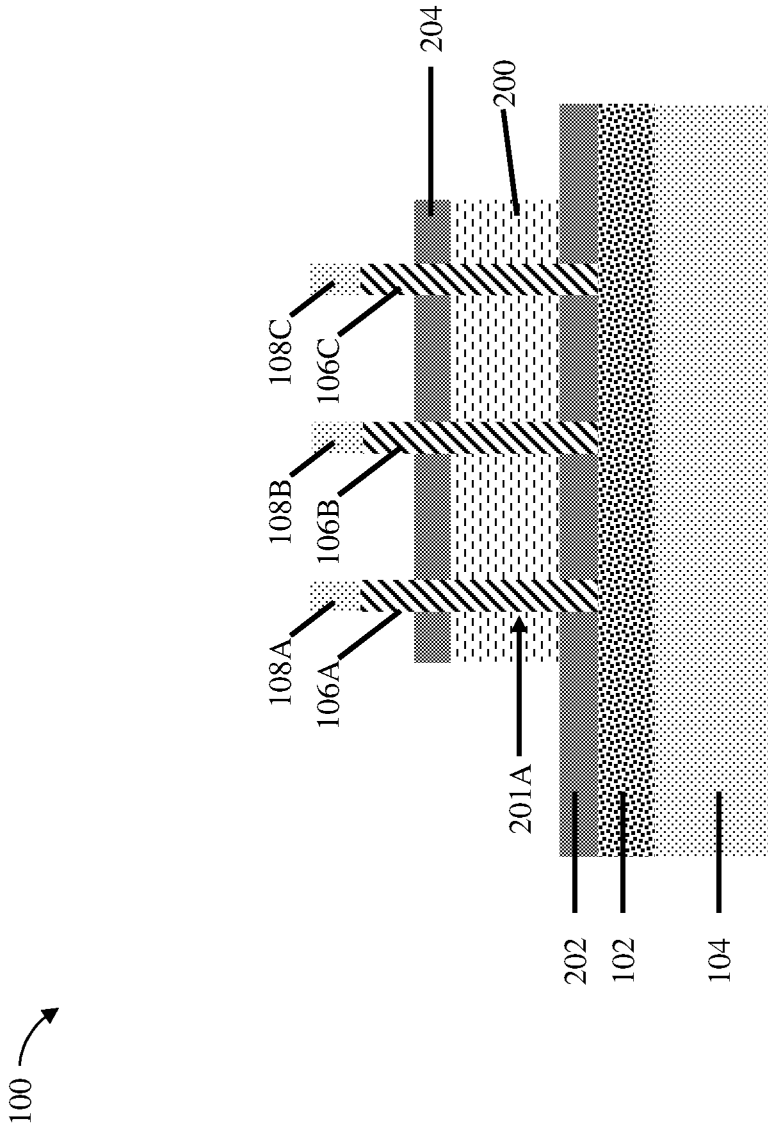


Fig. 2

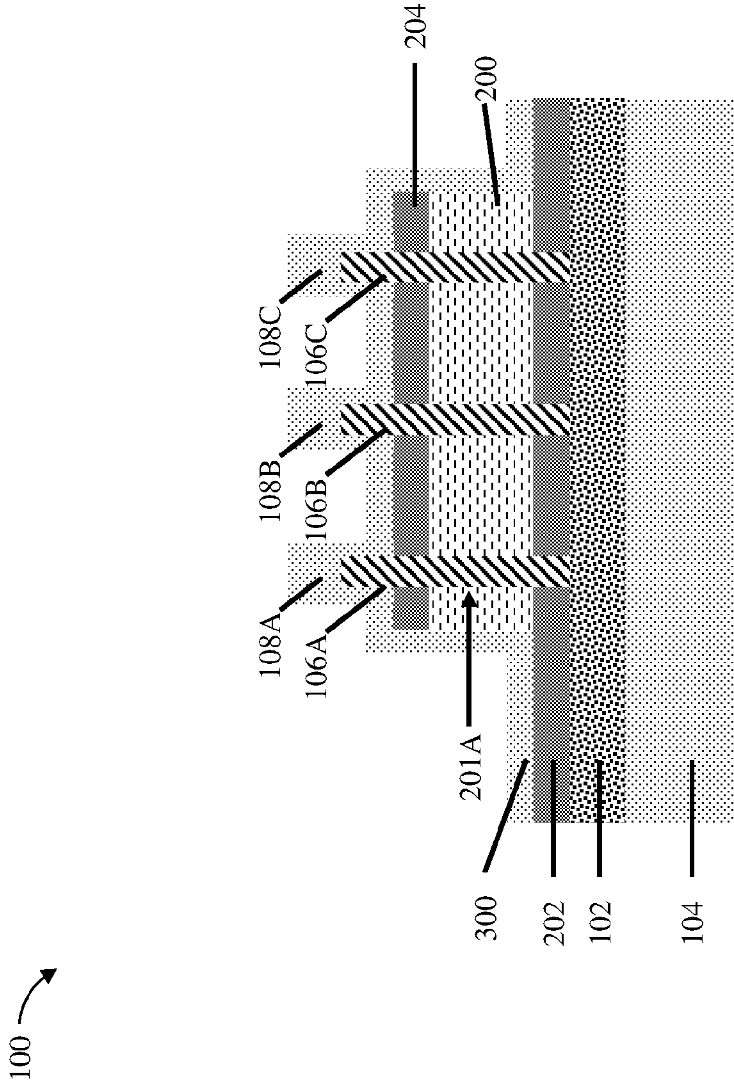


Fig. 3

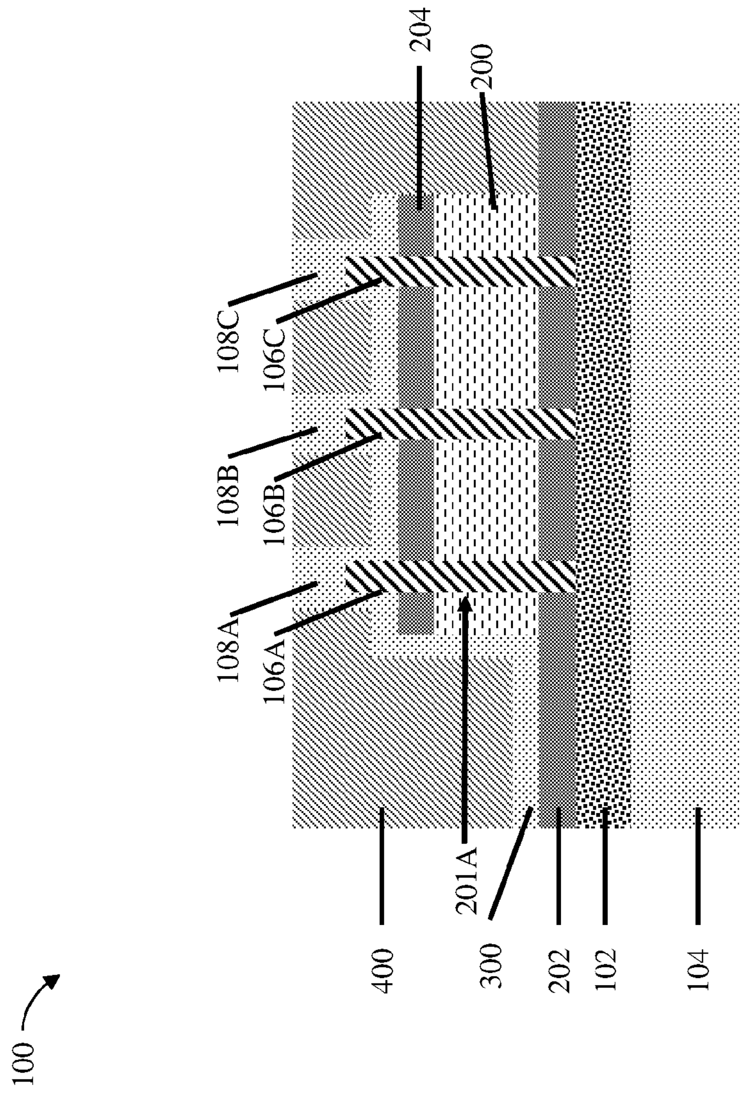


Fig. 4

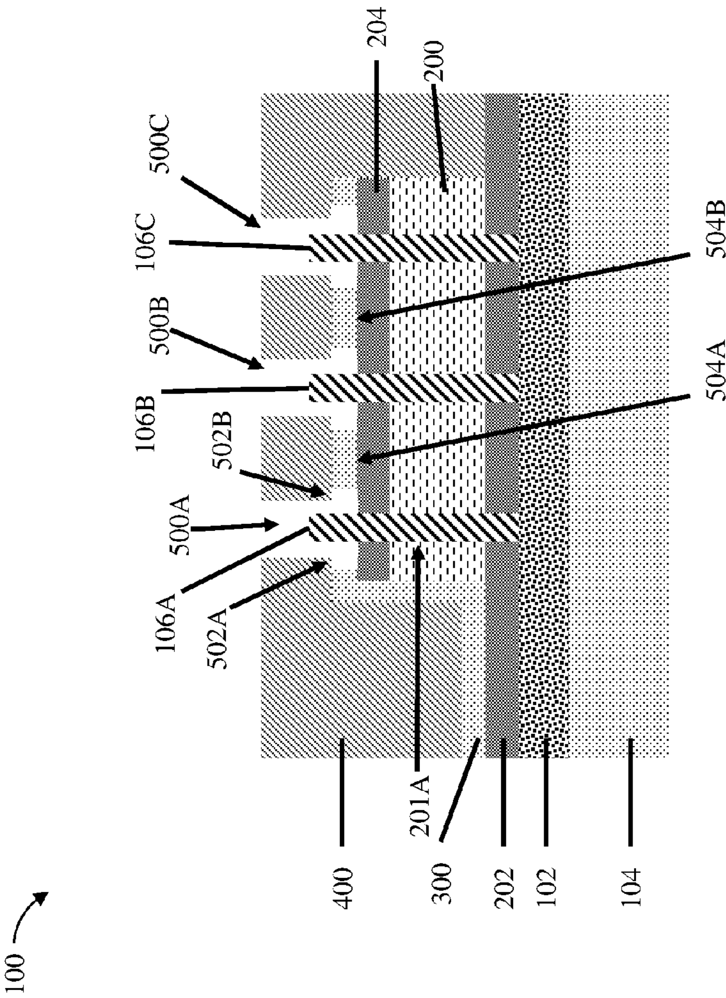


Fig. 5

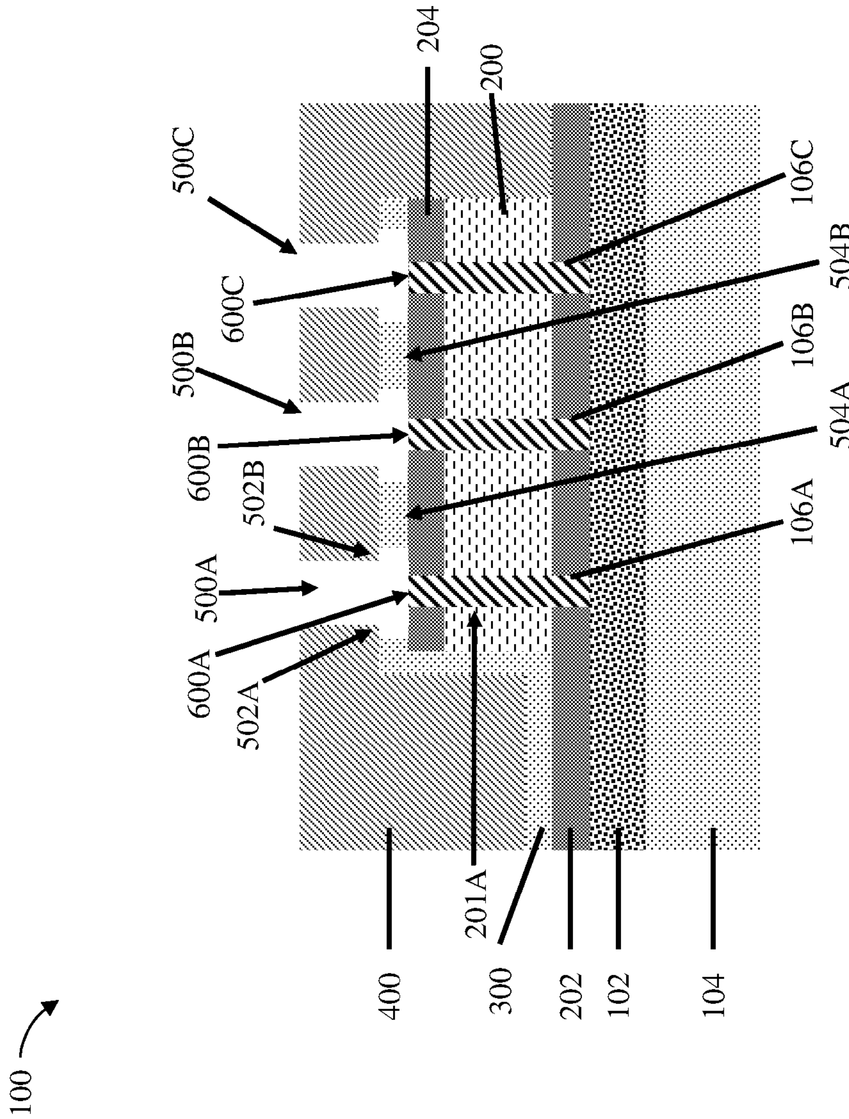


Fig. 6

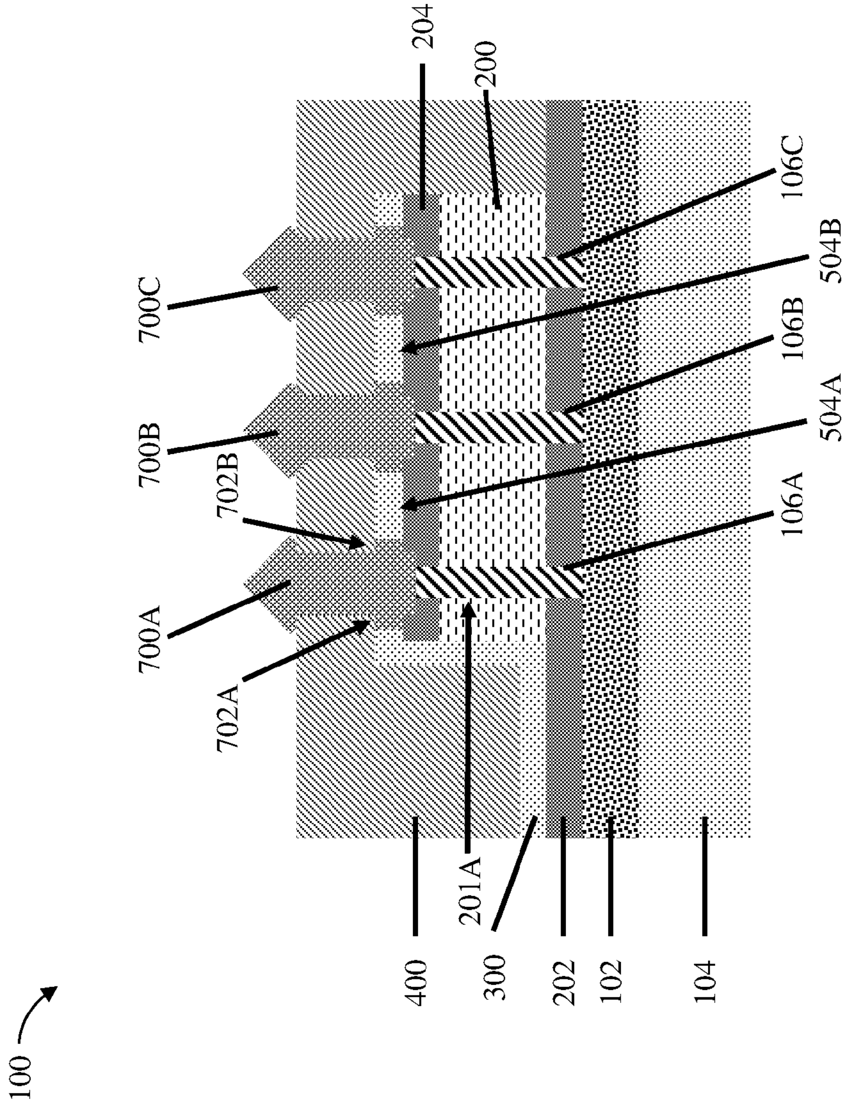


Fig. 7

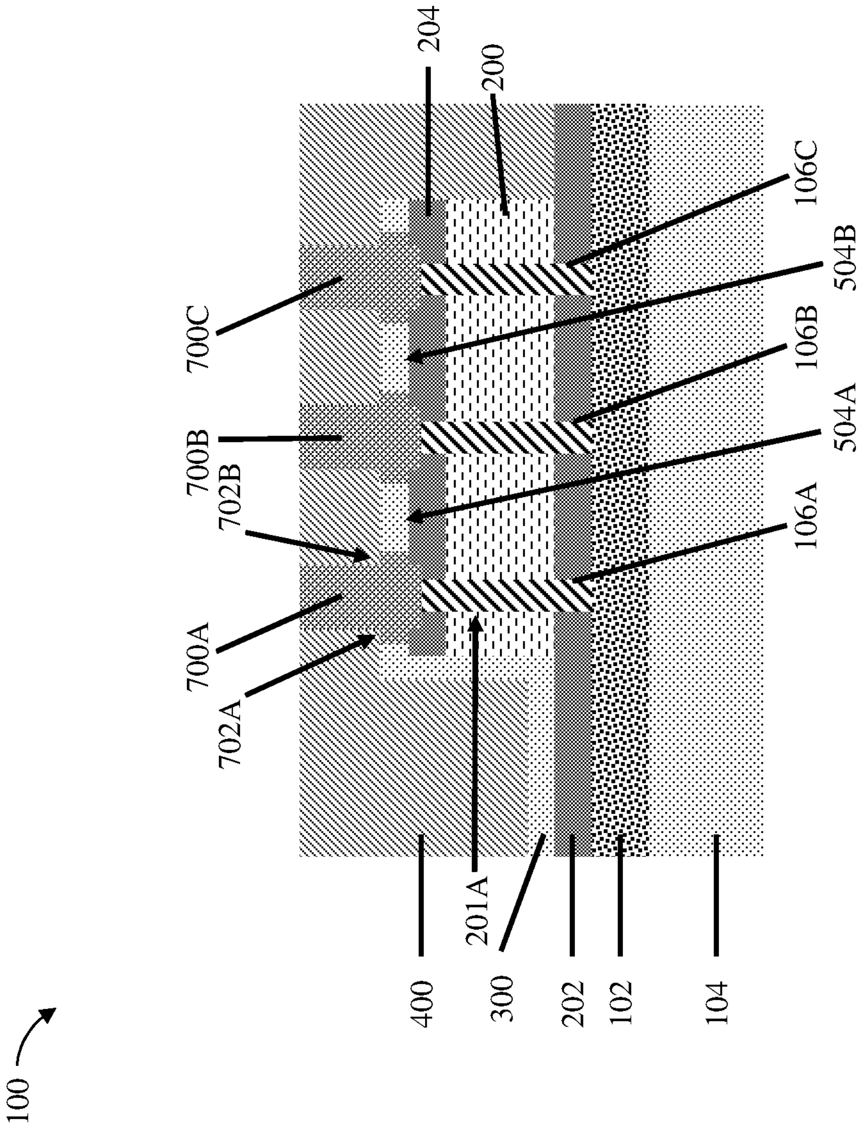


Fig. 8

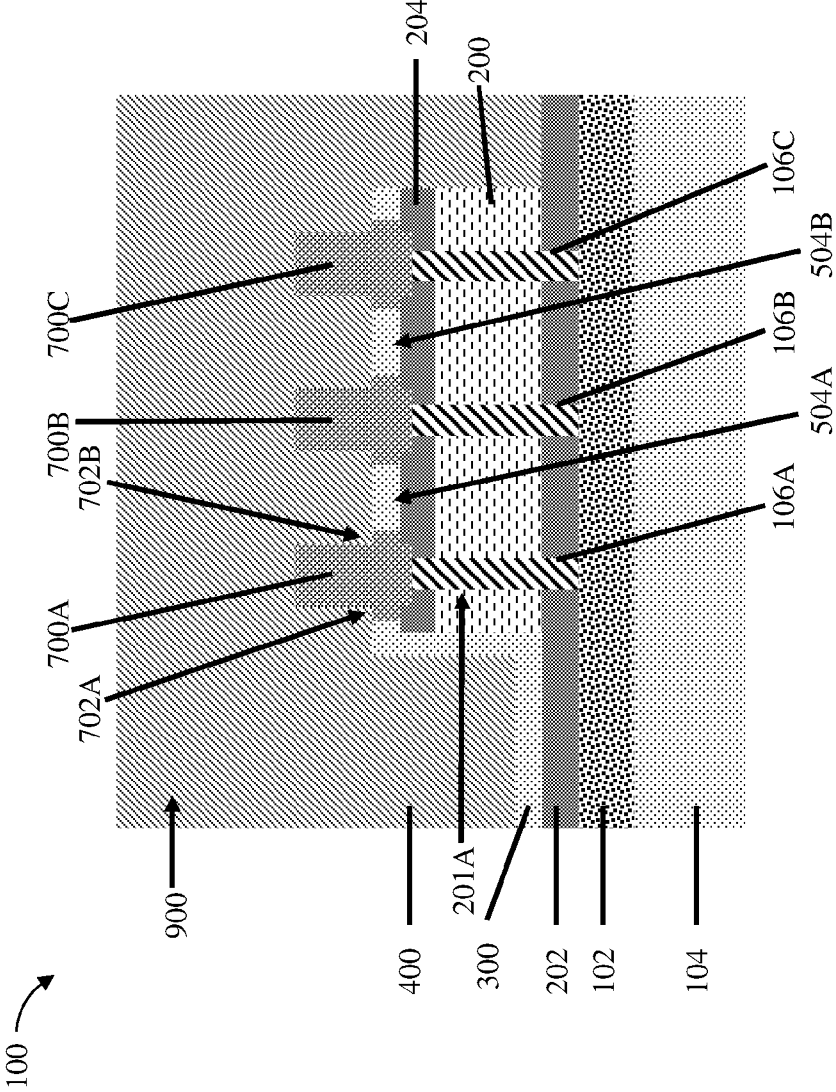


Fig. 9

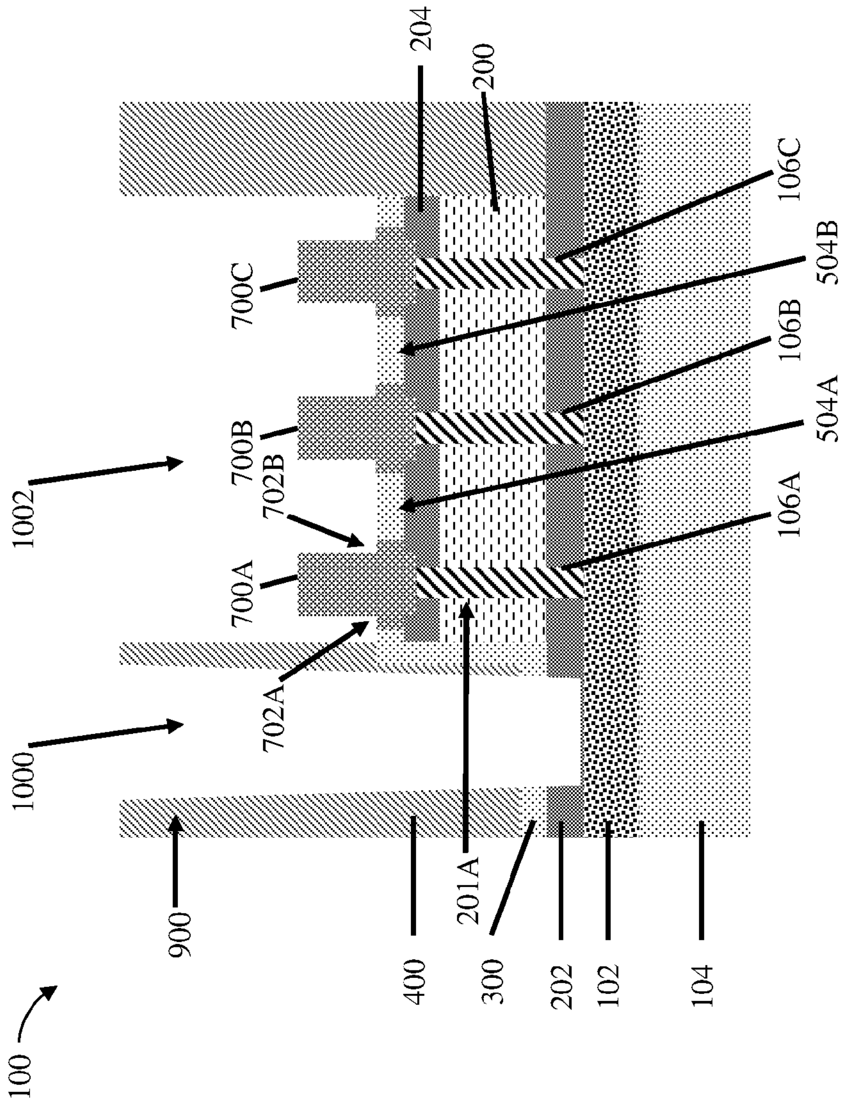


Fig. 10

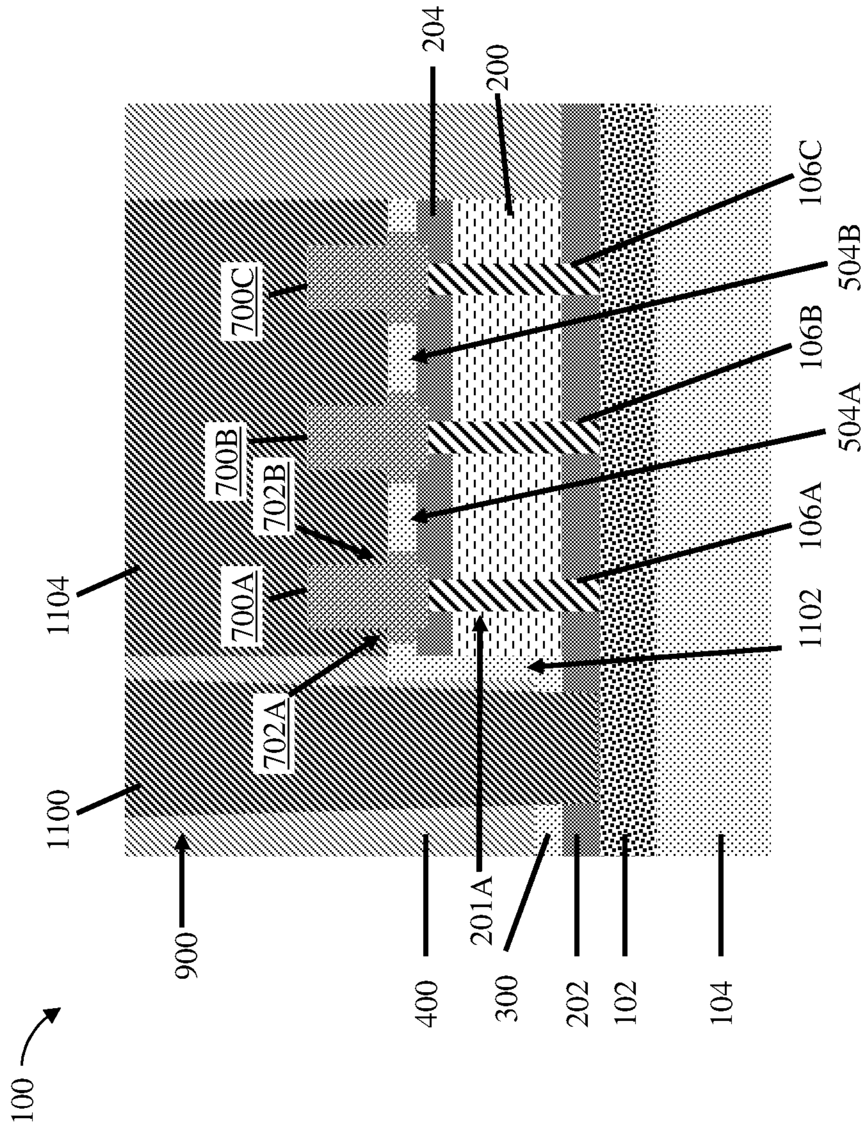


Fig. 11

CLOSELY PACKED VERTICAL TRANSISTORS WITH REDUCED CONTACT RESISTANCE

DOMESTIC AND/OR FOREIGN PRIORITY

[0001] This application is a divisional of U.S. application Ser. No. 15/248,355, titled "CLOSELY PACKED VERTICAL TRANSISTORS WITH REDUCED CONTACT RESISTANCE" filed Aug. 26, 2016, the contents of which are incorporated by reference herein in its entirety.

BACKGROUND

[0002] The present invention relates in general to semiconductor device fabrication methods and resulting structures. More specifically, the present invention relates to fabrication methods and resulting structures for a semiconductor device having closely packed vertical transistors with reduced contact resistance.

[0003] In contemporary semiconductor device fabrication processes, a large number of semiconductor devices, such as field effect transistors (FETs), are fabricated on a single wafer. Some non-planar transistor device architectures, such as vertical field effect transistors (VFETs), employ semiconductor fins and side-gates that can be contacted outside the active region, resulting in increased device density and performance over lateral devices. In contemporary VFET devices, in contrast to conventional FETs, the source to drain current flows through a vertical pillar in a direction that is perpendicular with respect to a horizontal major surface of the wafer or substrate. A VFET can achieve a smaller device footprint because its channel length is decoupled from the contacted gate pitch.

SUMMARY

[0004] According to embodiments of the present invention, a method of fabricating a semiconductor device having closely packed vertical transistors with reduced contact resistance is provided. The method can include forming a semiconductor structure on a bottom doped region of a substrate, the semiconductor structure including a gate formed over a channel region of a semiconductor fin. A liner is formed on the gate and the semiconductor fin and a dielectric layer is formed on the liner. Portions of the liner are removed to expose a top surface and sidewalls of the semiconductor fin and a sidewall of the dielectric layer and a recessed opening is formed by recessing portions of the liner from the exposed sidewall of the dielectric layer. A top epitaxy region is formed on the exposed top surface and sidewalls of the semiconductor fin and the exposed sidewall of the dielectric layer, an extension of the top epitaxy region filling the recessed opening, said top epitaxy region confined between portions of the liner.

[0005] According to embodiments of the present invention, a method of fabricating a semiconductor device having closely packed vertical transistors with reduced contact resistance is provided. The method can include forming a semiconductor structure on a bottom doped region of a substrate, the semiconductor structure including a plurality of gates, each gate formed over a channel region of a semiconductor fin. A liner is formed on the semiconductor structure and a dielectric layer is formed on the liner. Portions of the liner are removed to expose a top surface and sidewalls of each semiconductor fin and a plurality of recessed openings are formed under the dielectric layer by recessing portions of the liner. A top epitaxy region is formed on the exposed top surface and sidewalls of each semiconductor fin, an extension of each top epitaxy region filling one of the plurality of recessed openings, portions of the liner preventing a short between adjacent top epitaxy regions.

[0006] According to embodiments of the present invention, a structure having closely packed vertical transistors with reduced contact resistance is provided. The structure can include a vertical semiconductor structure formed on a bottom doped region of a substrate, the semiconductor structure including a gate formed over a channel region of a semiconductor fin, the gate between a bottom spacer and a top spacer. A top epitaxy region is formed on a surface of the semiconductor fin and a surface of the top spacer. A first contact is formed contacting a surface of the bottom epitaxy region, said first contact prevented from electrically shorting to the gate by portions of a liner formed between the first contact and the semiconductor structure. A second contact is formed wrapping around a top surface and a sidewall of the top epitaxy region, said second contact prevented from electrically shorting to the gate by portions of the liner formed between the second contact and the semiconductor structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The subject matter of the present invention is particularly pointed out and distinctly defined in the claims at the conclusion of the specification. The foregoing and other features and advantages are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0008] FIG. **1** depicts a cross-sectional view of a structure having a bottom doped region formed on a substrate during an intermediate operation of a method of fabricating a semiconductor device according to one or more embodiments of the present invention;

[0009] FIG. **2** depicts the cross-sectional view of the structure after forming a gate over a channel region of a semiconductor fin on the bottom doped region according to one or more embodiments of the present invention;

[0010] FIG. **3** depicts the cross-sectional view of the structure after forming a liner on the gate and the semiconductor fin according to one or more embodiments of the present invention;

[0011] FIG. **4** depicts the cross-sectional view of the structure after forming a dielectric layer on the liner according to one or more embodiments of the present invention;

[0012] FIG. **5** depicts the cross-sectional view of the structure after removing a hard mask and portions of the liner to form an opening around the semiconductor fin according to one or more embodiments of the present invention;

[0013] FIG. **6** depicts the cross-sectional view of the structure after recessing exposed portions of the semiconductor fin such that the recessed surface is flush with a surface of a top spacer according to one or more embodiments of the present invention;

[0014] FIG. **7** depicts the cross-sectional view of the structure after forming a top epitaxy region on the exposed portions of the semiconductor fin and dielectric layer according to one or more embodiments of the present invention;

[0015] FIG. **8** depicts the cross-sectional view of the structure after planarizing the top epitaxy region to a surface of the dielectric layer according to one or more embodiments of the present invention;

[0016] FIG. **9** depicts the cross-sectional view of the structure after forming an interlayer dielectric (ILD) on the dielectric layer and the top epitaxy region according to one or more embodiments of the present invention;

[0017] FIG. **10** depicts the cross-sectional view of the structure after forming a bottom contact trench and a top epitaxy trench according to one or more embodiments of the present invention; and

[0018] FIG. **11** depicts the cross-sectional view of the structure after forming a first contact in the bottom contact trench according to one or more embodiments of the present invention.

DETAILED DESCRIPTION

[0019] Various embodiments of the present invention are described herein with reference to the related drawings. Alternative embodiments can be devised without departing from the scope of this invention. It is noted that various connections and positional relationships (e.g., over, below, adjacent, etc.) are set forth between elements in the following description and in the drawings. These connections and/or positional relationships, unless specified otherwise, can be direct or indirect, and the present invention is not intended to be limiting in this respect. Accordingly, a coupling of entities can refer to either a direct or an indirect coupling, and a positional relationship between entities can be a direct or indirect positional relationship. As an example of an indirect positional relationship, references in the present description to forming layer "A" over layer "B" include situations in which one or more intermediate layers (e.g., layer "C") is between layer "A" and layer "B" as long as the relevant characteristics and functionalities of layer "A" and layer "B" are not substantially changed by the intermediate layer(s).

[0020] The following definitions and abbreviations are to be used for the interpretation of the claims and the specification. As used herein, the terms "comprises," "comprising," "includes," "including," "has," "having," "contains" or "containing," or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a composition, a mixture, process, method, article, or apparatus that comprises a list of elements is not necessarily limited to only those elements but can include other elements not expressly listed or inherent to such composition, mixture, process, method, article, or apparatus.

[0021] Additionally, the term "exemplary" is used herein to mean "serving as an example, instance or illustration." Any embodiment or design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or designs. The terms "at least one" and "one or more" are understood to include any integer number greater than or equal to one, i.e. one, two, three, four, etc. The terms "a plurality" are understood to include any integer number greater than or equal to two, i.e. two, three, four, five, etc. The term "connection" can include an indirect "connection" and a direct "connection."

[0022] References in the specification to "one embodiment," "an embodiment," "an example embodiment," etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment may or may not include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0023] For purposes of the description hereinafter, the terms "upper," "lower," "right," "left," "vertical," "horizontal," "top," "bottom," and derivatives thereof shall relate to the described structures and methods, as oriented in the drawing figures. The terms "overlying," "atop," "on top," "positioned on" or "positioned atop" mean that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements such as an interface structure can be present between the first element and the second element. The term "direct contact" means that a first element, such as a first structure, and a second element, such as a second structure, are connected without any intermediary conducting, insulating or semiconductor layers at the interface of the two elements. It should be noted, the term "selective to," such as, for example, "a first element selective to a second element," means that a first element can be etched and the second element can act as an etch stop.

[0024] For the sake of brevity, conventional techniques related to semiconductor device and integrated circuit (IC) fabrication may or may not be described in detail herein. Moreover, the various tasks and process steps described herein can be incorporated into a more comprehensive procedure or process having additional steps or functionality not described in detail herein. In particular, various steps in the manufacture of semiconductor devices and semiconductor-based ICs are well known and so, in the interest of brevity, many conventional steps will only be mentioned briefly herein or will be omitted entirely without providing the well-known process details.

[0025] By way of background, however, a more general description of the semiconductor device fabrication processes that can be utilized in implementing one or more embodiments of the present invention will now be provided. Although specific fabrication operations used in implementing one or more embodiments of the present invention can be individually known, the described combination of operations and/or resulting structures of the present invention are unique. Thus, the unique combination of the operations described in connection with the fabrication of a semiconductor device having closely packed vertical transistors with reduced contact resistance according to the present invention utilize a variety of individually known physical and chemical processes performed on a semiconductor (e.g., silicon) substrate, some of which are described in the immediately following paragraphs.

[0026] In general, the various processes used to form a micro-chip that will be packaged into an IC fall into four general categories, namely, film deposition, removal/etching, semiconductor doping and patterning/lithography. Deposition is any process that grows, coats, or otherwise transfers a material onto the wafer. Available technologies include physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), electrochemical deposition (ECD),

molecular beam epitaxy (MBE) and more recently, and atomic layer deposition (ALD) among others.

[0027] Removal/etching is any process that removes material from the wafer. Examples include etch processes (either wet or dry), and chemical-mechanical planarization (CMP), and the like. Reactive ion etching (RIE), for example, is a type of dry etching that uses chemically reactive plasma to remove a material, such as a masked pattern of semiconductor material, by exposing the material to a bombardment of ions that dislodge portions of the material from the exposed surface. The plasma is generated under low pressure (vacuum) by an electromagnetic field.

[0028] Semiconductor doping is the modification of electrical properties by doping, for example, transistor sources and drains, generally by diffusion and/or by ion implantation. These doping processes are followed by furnace annealing or by rapid thermal annealing (RTA). Annealing serves to activate the implanted dopants. Films of both conductors (e.g., poly-silicon, aluminum, copper, etc.) and insulators (e.g., various forms of silicon dioxide, silicon nitride, etc.) are used to connect and isolate transistors and their components. Selective doping of various regions of the semiconductor substrate allows the conductivity of the substrate to be changed with the application of voltage. By creating structures of these various components, millions of transistors can be built and wired together to form the complex circuitry of a modern microelectronic device.

[0029] Semiconductor lithography is the formation of three-dimensional relief images or patterns on the semiconductor substrate for subsequent transfer of the pattern to the substrate. In semiconductor lithography, the patterns are formed by a light sensitive polymer called a photo-resist. To build the complex structures that make up a transistor and the many wires that connect the millions of transistors of a circuit, lithography and etch pattern transfer steps are repeated multiple times. Each pattern being printed on the wafer is aligned to the previously formed patterns and slowly the conductors, insulators and selectively doped regions are built up to form the final device.

[0030] Turning now to a more detailed description of technologies relevant to the present invention, as previously noted herein, some non-planar transistor device architectures, such as VFETs, employ semiconductor fins and side-gates that can be contacted outside the active region, resulting in increased device density over lateral devices. However, there are challenges to providing VFETs with equal or superior performance characteristics to lateral devices. For example, reducing contact resistance is can improve the performance of VFETs, particularly for closely packed transistors having a tight fin pitch. Furthermore, as the features of a VFET are reduced in size and increased in aspect ratio, it can be increasingly difficult to prevent an electrical short between the bottom source/drain contact and the VFET gate. Thus, a method and structure is desired for reducing the contact resistance of closely packed VFETs while simultaneously preventing a short between the source/drain epitaxy and the metal gate of each VFET.

[0031] Turning now to an overview of aspects of the present invention, one or more embodiments provide methods of fabricating a semiconductor device having closely packed vertical transistors with reduced contact resistance. The described methods employ a wrap-around contact metal formed on all sides of the top source/drain epitaxy to increase the epitaxy contact area and reduce contact resistance. A dual-purpose nitride liner is used to confine the top epitaxy in a trench and to prevent an electrical short between the bottom source/drain contact and the metal gate. Methods for forming a wrap-around contact metal and a dual-purpose nitride liner and the resulting structures therefrom in accordance with embodiments of the present invention are described in detail below by referring to the accompanying drawings in FIGS. **1**-**11**.

[0032] FIG. **1** illustrates a cross-sectional view of a structure **100** having a bottom doped region **102** formed on a substrate **104** during an intermediate operation of a method of fabricating a semiconductor device according to one or more embodiments. The bottom doped region **102** can be a source or drain region formed on the substrate **104** by a variety of methods, such as, for example, diffusion, ion implantation of a dopant into the substrate, or in-situ doped epitaxy. The substrate **104** can be any suitable substrate material, such as, for example, monocrystalline Si, SiGe, SiC, III-V compound semiconductor, II-VI compound semiconductor, or semiconductor-on-insulator (SOI). For ease of discussion, reference can be made to operations performed on and to a single semiconductor fin of the structure **100**. It is understood that the structure **100** can include a plurality of semiconductor fins.

[0033] A semiconductor fin **106**A having a hard mask **108**A is formed on the bottom doped region **102** using known semiconductor fabrication techniques. For example, in some embodiments, a patterned hard mask (not illustrated) is etched to expose portions of the substrate **104**. The exposed portions of the substrate **104** can be removed to form a plurality of semiconductor fins. The patterned hard mask is then removed using an etch process, which can be a wet etch process, a dry etch process or a combination thereof. The semiconductor fin **106**A can be any suitable material, such as, for example, Si, SiGe, Group III-V channel material, or other suitable channel materials. Group III-V channel materials include materials having at least one group III element and at least one group V element, such as, for example, one or more of aluminum gallium arsenide, aluminum gallium nitride, aluminum arsenide, aluminum indium arsenide, aluminum nitride, gallium antimonide, gallium aluminum antimonide, gallium arsenide, gallium arsenide antimonide, gallium nitride, indium antimonide, indium arsenide, indium gallium arsenide, indium gallium arsenide phosphide, indium gallium nitride, indium nitride, indium phosphide and alloy combinations including at least one of the foregoing materials. The hard mask **108**A can be any suitable material, such as, for example, a nitride or silicon nitride. In some embodiments, a plurality of semiconductor fins (i.e., **106**A, **106**B, and **106**C) is formed on the bottom doped region **102**. In some embodiments, the fin pitch, or spacing, between each semiconductor fin can be about 20 nm to about 100 nm. In other embodiments, the fin pitch is about 30 nm to about 50 nm.

[0034] FIG. **2** illustrates a cross-sectional view of the structure **100** after forming a gate **200** over a channel region **201**A of the semiconductor fin **106**A on the bottom doped region **102**. For clarity, only the channel region **201**A is illustrated. It is understood that each semiconductor fin (e.g., **106**B, **106**C) also includes a channel region. In some embodiments, the gate **200** includes a gate dielectric (e.g., high-k dielectric) region defining a channel interface between the semiconductor fin **106**A and the gate **200**. In some embodiments, the gate dielectric region is formed

between the gate **200** and the semiconductor fin **106**A to modify the work function of the gate. Any known composition and manner of forming the gate **200** having a gate dielectric region can be utilized. The gate **200** (sometimes referred to as a gate conductor) can be made of, for example, polycrystalline or amorphous silicon, germanium, silicon germanium, a metal (e.g., tungsten, titanium, tantalum, ruthenium, zirconium, cobalt, copper, aluminum, lead, platinum, tin, silver, gold), a conducting metallic compound material (e.g., tantalum nitride, titanium nitride, tantalum carbide, titanium carbide, titanium aluminum carbide, tungsten silicide, tungsten nitride, ruthenium oxide, cobalt silicide, nickel silicide), carbon nanotube, conductive carbon, graphene, or any suitable combination of these materials. The conductive material can further include dopants that are incorporated during or after deposition. The gate can further include a work function metal layer next to the gate dielectric region. The work function layer can be a nitride, including but not limited to titanium nitride (TiN), hafnium nitride (HfN), hafnium silicon nitride (HfSiN), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tungsten nitride (WN), molybdenum nitride (MoN), niobium nitride (NbN); a carbide, including but not limited to titanium carbide (TiC) titanium aluminum carbide (TiAlC), tantalum carbide (TaC), hafnium carbide (HfC), and combinations thereof, during an operation for forming a VFET, according to one or more embodiments.

[0035] The gate dielectric region can be made of, for example, silicon oxide, silicon nitride, silicon oxynitride, boron nitride, high-k materials, or any combination of these materials. Examples of high-k materials include but are not limited to metal oxides such as hafnium oxide, hafnium silicon oxide, hafnium silicon oxynitride, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, zirconium silicon oxynitride, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The high-k materials can further include dopants such as lanthanum and aluminum. In some embodiments, the gate dielectric region can have a thickness of about 0.5 nm to about 4 nm. In other embodiments, the gate dielectric region can have a thickness of about 2 nm to about 3 nm.

[0036] In some embodiments, the gate **200** is formed between a bottom spacer **202** and a top spacer **204**, wherein the bottom spacer **202** is formed on the bottom doped region **102**. The bottom spacer **202** and the top spacer **204** can be any suitable material, such as, for example, a low-k dielectric, a nitride, silicon nitride (SiN), silicon oxygen carbonitride (SiOCN), or silicoboron carbonitride (SiBCN). In some embodiments, the bottom spacer **202** and top spacer **204** are different materials.

[0037] FIG. **3** illustrates a cross-sectional view of the structure **100** after forming a liner **300** on the gate **200** and the semiconductor fin **106**A. In one embodiment, the liner **300** is conformal ("conformal" as used herein means that the thickness of the liner **300** is substantially the same on all surfaces, or the thickness variation is less than 15% of the nominal thickness). The liner **300** can be any suitable material, such as, for example, a nitride, a silicon nitride, SiOC, SiOCN, or SiBCN. In some embodiments, the liner **300** is of the same material as the hard mask **108**A. Any known composition and manner of forming the liner **300** can be utilized. In some embodiments, the liner **300** can be conformally formed using CVD, PECVD, atomic layer deposition (ALD), evaporation, physical vapor deposition (PVD), chemical solution deposition, or other like processes. In some embodiments, the liner **300** has a thickness of about 3 nm to about 20 nm. In other embodiments, the liner **300** has a thickness of about 3 nm to about 8 nm. In still other embodiments, the liner **300** has a thickness of about 5 nm.

[0038] FIG. **4** illustrates a cross-sectional view of the structure **100** after forming a dielectric layer **400** on the liner **300**. Any known composition and manner of forming the dielectric layer **400** can be utilized. In some embodiments, the dielectric layer **400** is deposited by a spin-on coating operation. In still other embodiments, a CMP selective to the liner **300** is used to remove any excess portion of the dielectric layer **400** (known as overburden) that extends above a top surface of the liner **300**. The dielectric layer **400** can be any suitable material, such as, for example, an oxide. In some embodiments, the dielectric layer **400** is silicon oxide.

[0039] FIG. **5** illustrates a cross-sectional view of the structure **100** after removing the hard mask **108**A and portions of the liner **300** to form an opening **500**A around the semiconductor fin **106**A. The opening **500**A exposes a top surface and sidewalls of the semiconductor fin **106**A and sidewalls of the dielectric layer **400**. The liner **300** is recessed horizontally from the exposed sidewalls of the dielectric layer **400** to form recessed openings **502**A and **502**B. For clarity, only recessed openings **502**A and **502**B are illustrated. It is understood that recessed openings are formed in like manner for each of the semiconductor fins (e.g., **106**B, **106**C). In some embodiments, portions of the liner **300** are removed to form a plurality of openings (i.e., openings **500**A, **500**B, and **500**C), each opening exposing a top surface and sidewalls of one of a plurality of semiconductor fins (i.e., **106**A, **106**B, and **106**C). After recessing portions of the liner **300**, recessed portions (i.e., **504**A and **504**B) of the liner **300** remain to separate adjacent openings. Any known manner of removing the hard mask **108**A and portions of the liner **300** can be utilized. In some embodiments, a directional etch, such as a RIE, selective to the dielectric layer **400** material is used to form the opening **500**A.

[0040] FIG. **6** illustrates a cross-sectional view of the structure **100** after recessing the exposed portions of the semiconductor fin **106**A such that the recessed surface **600**A is flush with a surface of the top spacer **204**. In some embodiments, the surface **600**A is instead recessed slightly below the surface of the top spacer **204**. In other embodiments, the surface **600**A is instead slightly capped above the surface of the top spacer **204**.

[0041] FIG. **7** illustrates a cross-sectional view of the structure **100** after forming a top epitaxy region **700**A on the exposed portions of the semiconductor fin and dielectric layer to fill the opening **500**A (depicted in FIG. **5**). Extensions **702**A and **702**B of the top epitaxy region **700**A fill the recessed openings **502**A and **502**B (depicted in FIG. **5**). For clarity, only extensions **702**A and **702**B are illustrated. It is understood that extensions are formed for each semiconductor fin (e.g., **106**B, **106**C). In some embodiments, a plurality of top epitaxy regions (i.e., **700**A, **700**B, and **700**C) is formed to fill a plurality of openings (**500**A, **500**B, and **500**C, depicted in FIG. **5**). Recessed portions (i.e., **504**A and

504B) of the liner 300 separate adjacent top epitaxy regions. Any known manner of forming the top epitaxy region 700A can be utilized. In some embodiments, epitaxial growth, CVD, ECD, MBE, or ALD is employed to form the top epitaxy region 700A. In some embodiments, the top epitaxy region 700 extends beyond a top surface of the dielectric layer 400. In some embodiments, the top epitaxy region 700 is in-situ doped. In some embodiments, the top epitaxy region 700 is formed using ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), metalorganic chemical vapor deposition (MOCVD), low-pressure chemical vapor deposition (LPCVD), limited reaction processing CVD (LRPCVD), or molecular beam epitaxy (MBE). Epitaxial materials can be grown from gaseous or liquid precursors. Epitaxial materials can be grown using vapor-phase epitaxy (VPE), molecular-beam epitaxy (MBE), liquid-phase epitaxy (LPE), or other suitable process. Epitaxial silicon, silicon germanium (SiGe), and/or carbon doped silicon (Si:C) silicon can be doped during deposition (in-situ doped) by adding dopants, n-type dopants (e.g., phosphorus or arsenic) or p-type dopants (e.g., boron or gallium), depending on the type of transistor. The dopant concentration in the source/drain can range from 1×10^{19} cm−3 to 2×10^{21} cm^{-3}, or preferably between 2×10^{20} cm^{-3} to 1×10^{21} cm^{-3}.

[0042] FIG. **8** illustrates a cross-sectional view of the structure **100** after planarizing the top epitaxy region **700**A to a surface of the dielectric layer **400**. In some embodiments, a CMP selective to the dielectric layer **400** is used to remove any excess portion of the top epitaxy region **700**A (known as overburden) that extends above the surface of the dielectric layer **400**.

[0043] FIG. **9** illustrates a cross-sectional view of the structure **100** after forming an interlayer dielectric (ILD) **900** on the dielectric layer **400** and the top epitaxy region **700**A. Any known manner of forming the ILD **900** can be utilized. In some embodiments, the ILD **900** is deposited by a spin-on coating operation. The ILD **900** can be any suitable material, such as, for example, an oxide. In some embodiments, the ILD **900** is silicon dioxide (SiO_2). In some embodiments, the ILD **900** is of the same material as the dielectric layer **400**.

[0044] FIG. **10** illustrates a cross-sectional view of the structure **100** after forming a bottom contact trench **1000** and a top epitaxy trench **1002**. Any known manner of forming the bottom contact trench **1000** and top epitaxy trench **1002** can be utilized. In some embodiments, a patterned photomask is formed on the ILD **900**. The patterned photomask exposes portions of the ILD **900** for selective removal. In some embodiments, the bottom contact trench **1000** is formed by a series of directional etches (e.g., RIEs). In some embodiments, a first RIE selective to the liner **300** removes exposed portions of the ILD **900** and dielectric layer **400** to expose a surface of the liner **300**. In some embodiments, a subsequent RIE selective to the bottom doped region **102** material removes portions of the liner **300** and bottom spacer **202** to expose a surface of the bottom doped region **102**. In some embodiments, the top epitaxy trench **1002** is formed by a RIE selective to the top epitaxy region **700**A material and the liner **300** material. The RIE exposes a top surface, a sidewall, and the extensions (**702**A and **702**B, depicted in FIG. **7**) of the top epitaxy region **700**A, as well as a surface of the recessed portions (i.e., **504**A and **504**B) of the liner **300**.

[0045] FIG. **11** illustrates a cross-sectional view of the structure **100** after forming a first contact **1100** in the bottom contact trench **1000** (depicted in FIG. **10**). The first contact **1100** can be of any suitable conducting material, such as, for example, a metal (e.g., tungsten, titanium, tantalum, ruthenium, zirconium, cobalt, copper, aluminum, lead, platinum, tin, silver, gold), a conducting metallic compound material (e.g., tantalum nitride, titanium nitride, tantalum carbide, titanium carbide, titanium aluminum carbide, tungsten silicide, tungsten nitride, ruthenium oxide, cobalt silicide, nickel silicide), carbon nanotube, conductive carbon, graphene, or any suitable combination of these materials. The conductive material can further include dopants that are incorporated during or after deposition. Any known manner of forming the first contact **1100** can be utilized. In some embodiments, the first contact **1100** can be copper and can include a barrier metal liner. In some embodiments, the barrier metal liner is deposited into the bottom contact trench **1000** prior to depositing the first contact **1100**. The barrier metal liner prevents the copper from diffusing into, or doping, the surrounding materials, which can degrade their properties. Silicon, for example, forms deep-level traps when doped with copper. An ideal barrier metal liner must limit copper diffusivity sufficiently to chemically isolate the copper conductor from the surrounding materials and should have a high electrical conductivity, for example, tantalum nitride and tantalum (TaN/Ta), titanium, titanium nitride, cobalt, ruthenium, and manganese. The first contact **1100** is prevented from shorting to the gate **200** by a sidewall portion **1102** of the liner **300**.

[0046] A second contact **1104** is formed in the top epitaxy trench **1002** (depicted in FIG. **10**). Any known manner of forming the second contact **1104** can be utilized. In some embodiments, the second contact **1104** can be copper and can include a barrier metal liner. The second contact **1104** wraps around the top epitaxy region **700**A, contacting the top surface, sidewalls, and the extensions (**702**A and **702**B, depicted in FIG. **7**) of the top epitaxy region **700**A. The second contact **1104** is prevented from shorting to the gate **200** by the liner **300** (including, for example, portions **504**A and **504**B of the liner **300**).

[0047] In some embodiments, the first contact **1100** and the second contact **1104** are deposited into the bottom contact trench **1000** and the top epitaxy trench **1002**, respectfully, each contact forming an overburden above a surface of the ILD **900**. In some embodiments, a CMP selective to the ILD **900** removes the overburden of each contact.

[0048] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments described. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The terminology used herein was chosen to best explain the principles of the embodiment, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments described herein.

What is claimed is:

1. A method for forming a semiconductor device, the method comprising:

forming a semiconductor structure on a bottom doped region on a substrate, the semiconductor structure including a gate formed over a channel region of a semiconductor fin;
forming a top spacer on the gate;
forming a liner on the top spacer, the gate, and the semiconductor fin;
forming a dielectric layer on the liner;
removing portions of the liner to expose a top surface and sidewalls of the semiconductor fin and a sidewall of the dielectric layer;
recessing a portion of the semiconductor fin such that a surface of the recessed semiconductor fin is flush to a surface of the top spacer.
forming a recessed opening by recessing portions of the liner from the exposed sidewall of the dielectric layer; and
forming a top epitaxy region on the exposed top surface of the semiconductor fin and the exposed sidewall of the dielectric layer, an extension of the top epitaxy region filling the recessed opening, said top epitaxy region confined between portions of the liner.

2. The method of claim **1**, further comprising further recessing the surface of the recessed semiconductor fin below the surface of the top spacer prior to forming the top epitaxy region.

3. The method of claim **1**, wherein the bottom spacer comprises a low-k dielectric and the top spacer comprises a low-k dielectric.

4. The method of claim **1**, wherein the liner has a thickness of about 3 nm to about 20 nm.

5. The method of claim **1**, wherein the liner has a thickness of about 3 nm to about 8 nm.

6. The method of claim **1**, wherein the liner comprises a nitride liner having a thickness of about 5 nm.

7. A semiconductor device, the device comprising:
a vertical semiconductor structure formed on a bottom doped region of a substrate, the semiconductor structure including a gate formed over a channel region of a semiconductor fin, the gate between a bottom spacer and a top spacer;
a top epitaxy region formed on a surface of the semiconductor fin and a surface of the top spacer;
a first contact contacting a surface of the bottom doped region, said first contact prevented from electrically shorting to the gate by portions of a liner formed between the first contact and the semiconductor structure; and
a second contact wrapping around a top surface and a sidewall of the top epitaxy region, said second contact prevented from electrically shorting to the gate by portions of the liner formed between the second contact and the semiconductor structure.

8. The semiconductor device of claim **7**, wherein the semiconductor fin is recessed to a surface of the top spacer.

9. The semiconductor device of claim **7**, wherein the semiconductor fin is recessed below a surface of the top spacer.

10. The semiconductor device of claim **7**, wherein the vertical semiconductor structure comprises a plurality of gates, each gate formed over a channel region of a semiconductor fin.

11. The semiconductor device of claim **10**, further comprising a plurality of top epitaxy regions, each top epitaxy region formed on a surface of a semiconductor fin.

12. The semiconductor device of claim **11**, wherein portions of the liner prevent a short between adjacent top epitaxy regions.

13. The semiconductor device of claim **7**, wherein the liner has a thickness of about 3 nm to about 20 nm.

14. The semiconductor device of claim **7**, wherein the liner has a thickness of about 3 nm to about 8 nm.

15. The semiconductor device of claim **7**, wherein the liner comprises a nitride liner having a thickness of about 5 nm.

16. A semiconductor device, the device comprising:
a semiconductor fin on a substrate;
a gate formed over a channel region of the semiconductor fin;
a liner formed over the semiconductor fin and the gate;
a bottom source/drain contact, the bottom source/drain contact prevented from electrically shorting to the gate by a first portion of the liner; and
a top source/drain contact, the top source/drain contact prevented from electrically shorting to the gate by a second portion of the liner.

17. The semiconductor device of claim **16**, further comprising a top epitaxy region formed on a surface of the semiconductor fin.

18. The semiconductor device of claim **17**, wherein the top source/drain contact wraps around a top surface and a sidewall of the top epitaxy region.

19. The semiconductor device of claim **16**, wherein portions of the liner are recessed in a direction orthogonal to the channel region.

20. The semiconductor device of claim **16**, wherein the liner comprises a nitride liner having a thickness of about 3 nm to about 20 nm.

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