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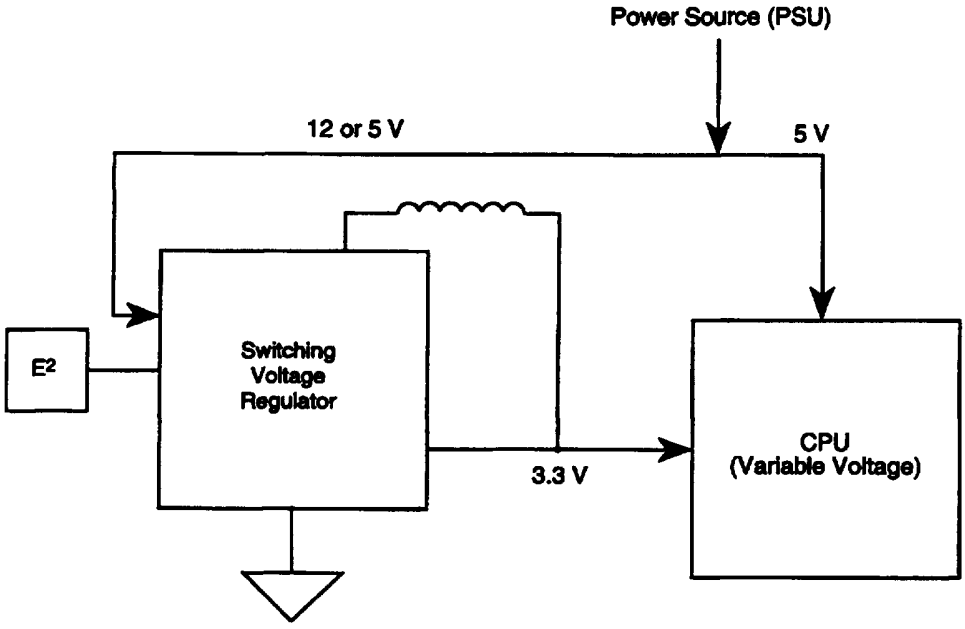
(54) Title: AN IMPROVED VARIABLE-VOLTAGE CPU VOLTAGE REGULATOR



(57) Abstract

An integrated CPU has an on-board switching voltage regulator with an electrically-erasable programmable read-only memory electronically accessible for storing a feedback reference coefficient for control. In further embodiments, output voltage is tuned via a second EEPROM storing an electronically accessible value in concert with a solid-state resistor ladder. In other embodiments, signals on interrupt lines to the CPU are monitored to provide a prewarning of impending activity by the CPU requiring dramatically increased current flow. In yet other embodiments, solid-state circuitry is provided to reduce or eliminate capacitors used for dealing with input current surges to the CPU.

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An Improved Variable-Voltage CPU Voltage Regulator

Field of the Invention

The present invention is in the area of general-purpose computers such as desktop computers and portable computers, and pertains in particular to supplying regulated electrical power to central processing units (CPUs) and other computer elements.

Background of the Invention

In the development of power supplies and power management for computer systems, as in most technologies, new concepts and products bring with them new problems, and sometimes older problems are exacerbated. Supplying power to CPUs on computer motherboards is a case in point.

As CPUs have gotten faster and more powerful, they have also increased in load requirements and in total power consumed. Moreover, efforts have been made to reduce the voltage required for microprocessors used in and for CPUs. AT lower voltage, such as 3.3 volts now required by some microprocessors commercially available, instead of the traditional 5 volts, voltage regulation becomes more important.

Voltage regulation is more important with newer microprocessors also because of the higher power, hence higher current, and the speed with which events transpire in modern computers. A high-power microprocessor suddenly activated, with immediate processing activity as well, generates a relatively high rate of change of current with respect to time, which can (and does) seriously effect the voltage supplied, unless adequate steps are taken to avoid or manage the transient circumstances.

In current art there are three fundamental implementations of variable-voltage CPU voltage regulators:

1. Regulator in power supply. This implementation is not accurate, its cross regulation is not good, and losses on line are too high.
2. Line regulator on motherboard. This method is cost effective, but efficiency is low and reaction speed is poor.
3. Switching regulator on motherboard. Efficiency improves, but the cost is high and reaction speed remains poor.

Fig. 1 shows a voltage regulator and dual-voltage CPU in current technology. A power source (the power supply unit) supplies 12-volt and 5-volt output. A 5-volt CPU uses power directly from the PSU. A 3.3-volt CPU requires conversion through the voltage regulator.

In all current art, the best accuracy without manual adjustment is 3% or worse. Improving accuracy below a 3% tolerance increases the cost unacceptably and needs continual manual adjustment-not acceptable requirements in a personal computer.

Fig. 3 shows the details of the switching voltage regulator chip with a resistor or potentiometer, as used in current art.

What is clearly needed is improved methods and apparatus for regulating voltage to CPUs to improve regulation, control line losses, improve reaction time (speed), and to improve efficiency.

Summary of the Invention

In a preferred embodiment of the present invention, a switching voltage regulator has an electrically erasable programmable read-only memory unit EEPROM or E^2) for storing a coefficient for feedback loop voltage regulation. The coefficient is adjusted by clocking a serial data stream into a register until a desired value for the feedback coefficient is reached, then storing the value in the EEPROM by means of an input line.

In another embodiment, the adjustment potentiometer used in prior art devices is replaced by an external E^2 and a resistor ladder to adjust output voltage.

In various embodiments, regulator apparatus according to the invention is implemented on a motherboard, in a multi-chip CPU package, and integrated in a single chip CPU. There are also several embodiments to deal with current surges, reducing or eliminating capacitors conventionally required. In yet another embodiment, the voltage regulator receives a pre-warning based on a wakeup mechanism according to the invention.

The invention provides vastly improved efficiency and regulation, reaction time, reduced line losses, and reduced probability of failure under rapidly changing circumstances, than may be found in current art.

Brief Description of the Drawings

Fig. 1 is a block diagram of a CPU voltage regulator in current art.

Fig. 2 is a block diagram of a CPU voltage regulator according to an embodiment of the present invention.

Fig. 3 is a schematic of a switching voltage regulator chip with a resistor or potentiometer as used in current art.

Fig. 4 is a partly schematic diagram of a CPU voltage regulator replacing the current art potentiometer of the regulator of Fig. 3 with an external EEPROM and a resistor ladder.

Fig. 5 is a block diagram of an enhanced embodiment of the present invention showing a prewarning system based on a wakup mechanism.

Fig. 6 shows an embodiment using a synchronous digital buck converter.

Fig. 7 shows an embodiment incorporating a series of dummy

capacitors, controlled by a EEPROM for slowing the rise time of the switching regulator and inductor to match the CPU rise time.

Description of the Preferred Embodiments

Fig. 2 shows a switching voltage regulator with an erasable EPROM (E^2) that holds the coefficient for the feedback loop voltage regulation. To adjust the output value of the regulator, a serial data stream can be clocked into the register until the desired value is obtained. At this point, that value can be stored in the E^2 by means of a line not shown. The stored value can be read permanently and is easily changed again, if required, without manual adjustment.

In Fig. 4 the potentiometer is replaced by an external E^2 and an R-ladder to adjust the output voltage. Data and clock values are input upon system initialization. The circuit can be tuned for optional voltage for the CPU, and then the E^2 is programmed.

This circuit may be implemented on a motherboard, in a multi-chip CPU package, or integrated in a single-chip CPU. It has several different enhancements to reduce or eliminate the capacitors required to deal with the current surge that occurs when the CPU goes from idle (typically in the milliamp range) to active (typically in a range of multiple amperes), in approximately 100ns.

Fig. 5 shows the first enhancement. The voltage regulator receives a prewarning based on a wake-up mechanism. The signals on the interrupt lines (NMI. INT, SMI) to the CPU are sensed and combined with some logic (e.g., PAL). The resulting lines send a warning of imminent activity by the CPU, with dramatically increased current requirements. Thus the voltage regulator can take countermeasures in anticipation of CPU activity.

The second and third enhancements may be used when the first enhancement is in place. In Fig. 6 the enhancement uses a

synchronous digital Buck converter running on a divided CPU clock. To allow the prewarning logic to work properly, the divider must be synchronized as well.

The third enhancement (see Fig. 7) uses a series of dummy capacitors, controlled by the E^2, to slow the rise time of the switching regulator and inductor to match the CPU rise time.

It will be apparent to those with skill in the art that there are many alterations that may be made without departing from the spirit and scope of the invention. There are, for example, many equivalent ways the circuitry elements might be arranged to produce essentially the same result, and there are many ways IC elements might be arranged as well.

What is claimed is:

1. A voltage regulated, single chip microprocessor-based CPU for a general-purpose computer, comprising:

a CPU portion;

a switching voltage regulator portion connected to the CPU portion, and having a feedback loop: and

an electrically erasable programmable read-only memory connected to the voltage regulator portion for storing a feedback reference coefficient in a manner allowing adjustment by electronic logic.

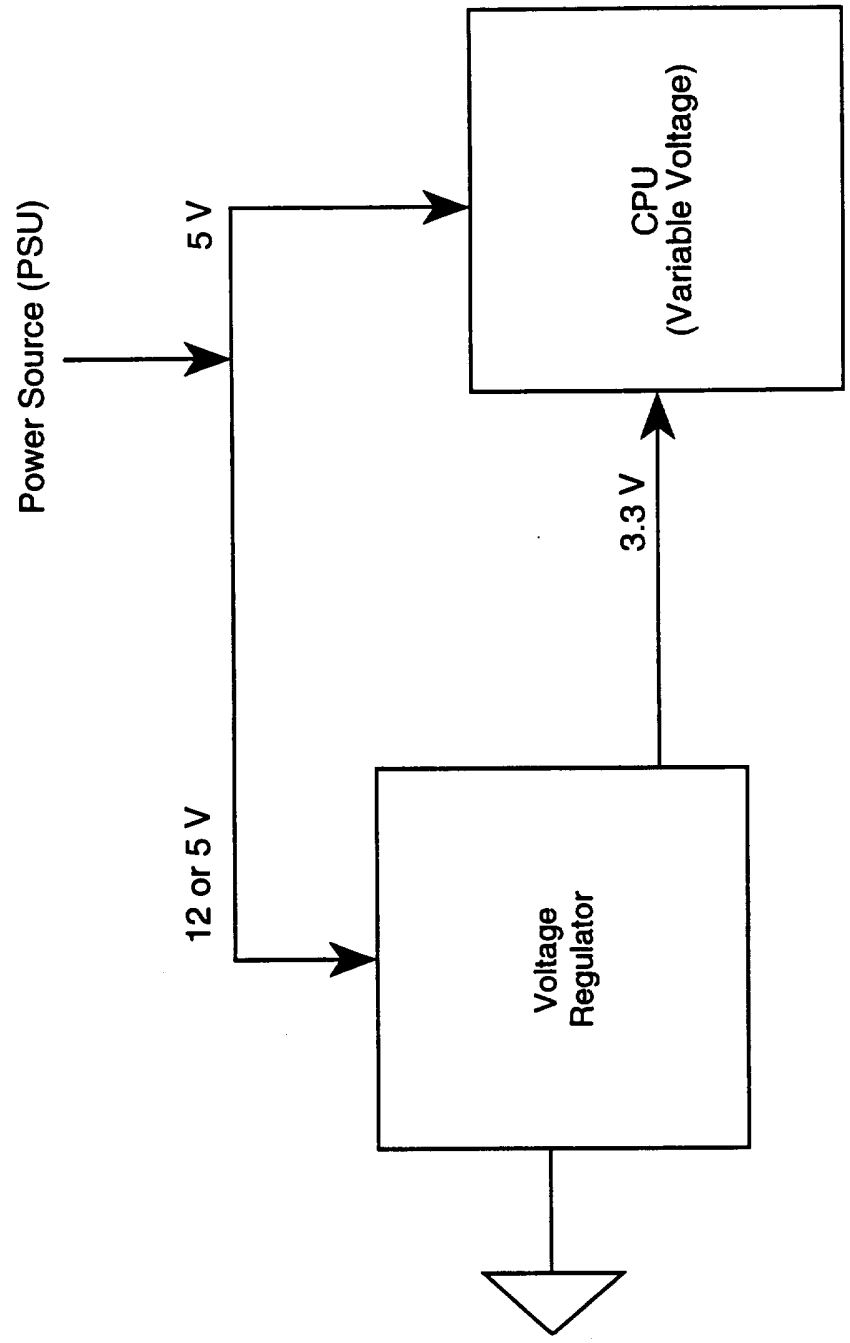

Fig. 1 (Prior Art)

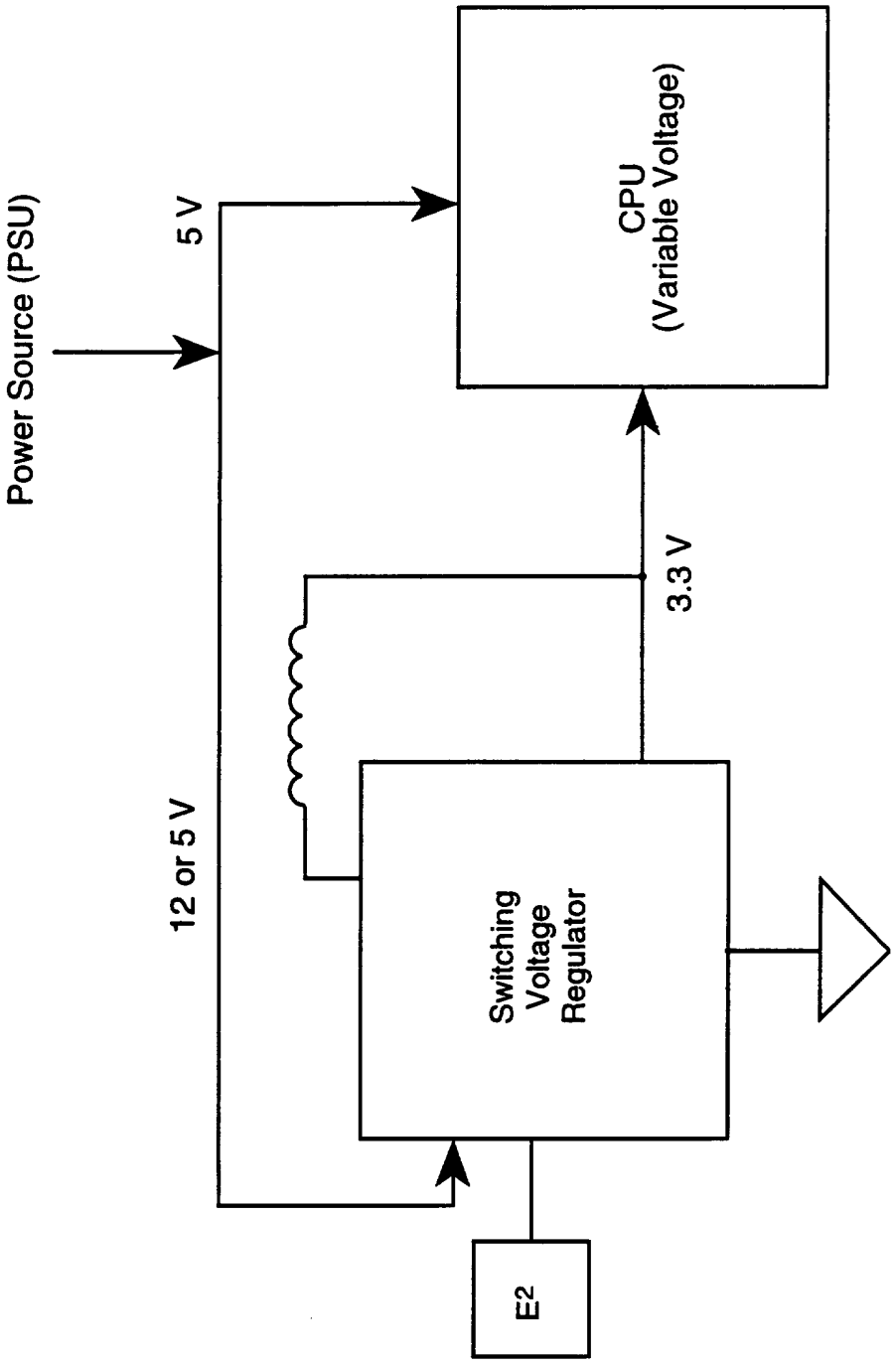
Power Source (PSU)
5 V
CPU
(Variable Voltage)
3.3 V
12 or 5 V
Switching
Voltage
Regulator
E²

Fig. 2

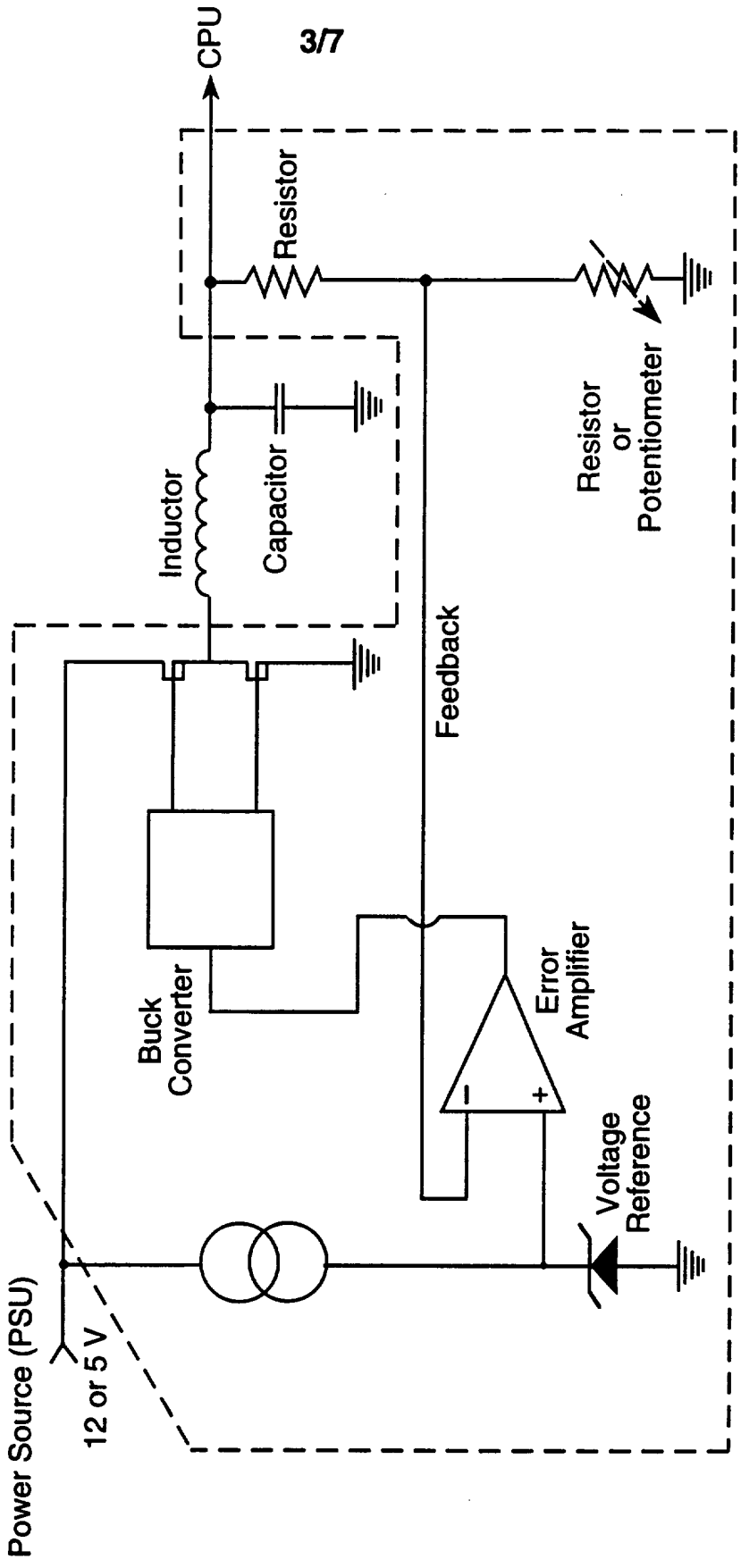

Fig. 3 (Prior Art)

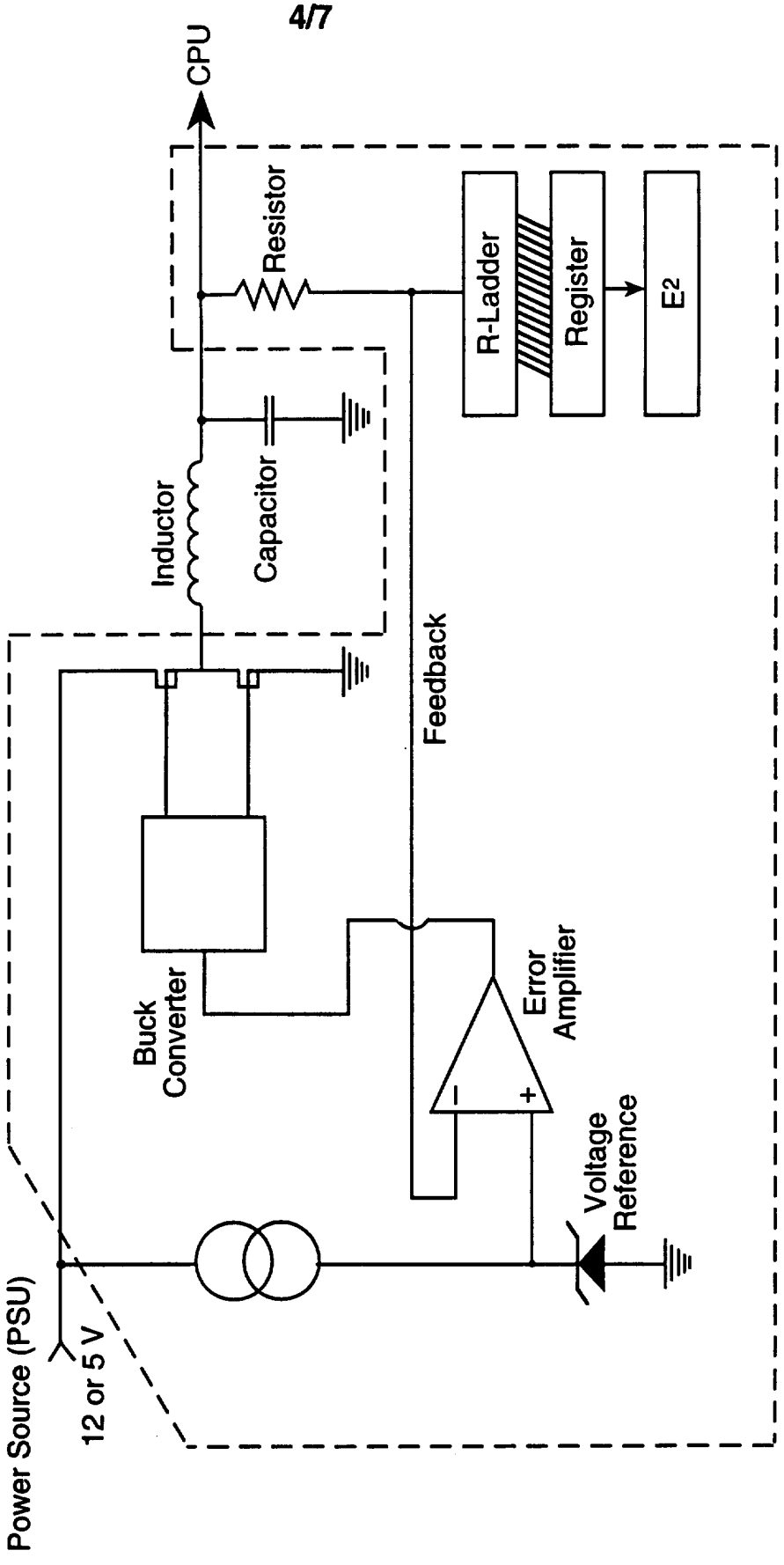
CPU
Resistor
R-Ladder
Register
E2
Inductor
Capacitor
Feedback
Buck Converter
Error Amplifier
Voltage Reference
Power Source (PSU)
12 or 5 V

Fig. 4

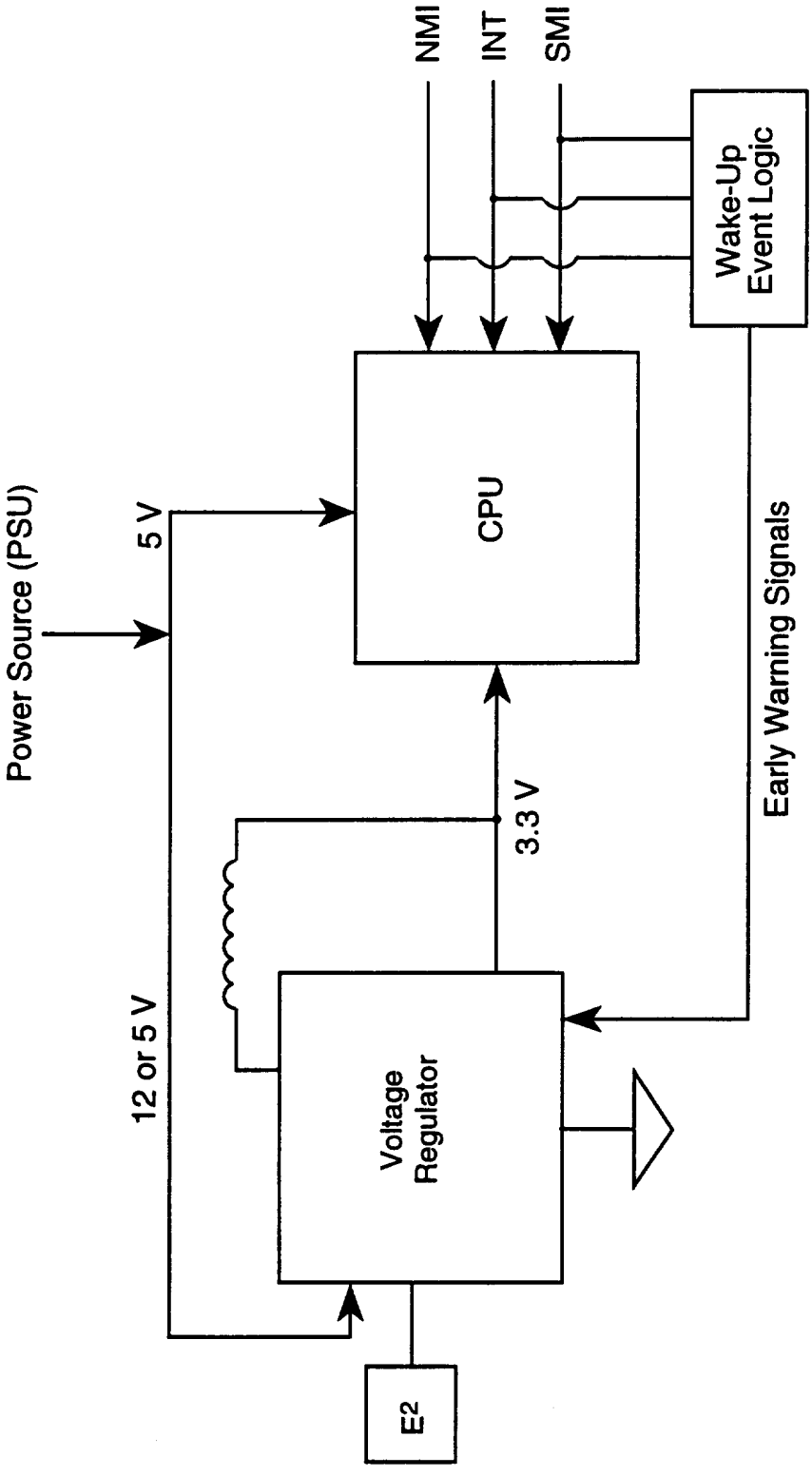
NMI
INT
SMI
Wake-Up Event Logic
CPU
Power Source (PSU)
5 V
3.3 V
Early Warning Signals
12 or 5 V
Voltage Regulator
E²

Fig. 5

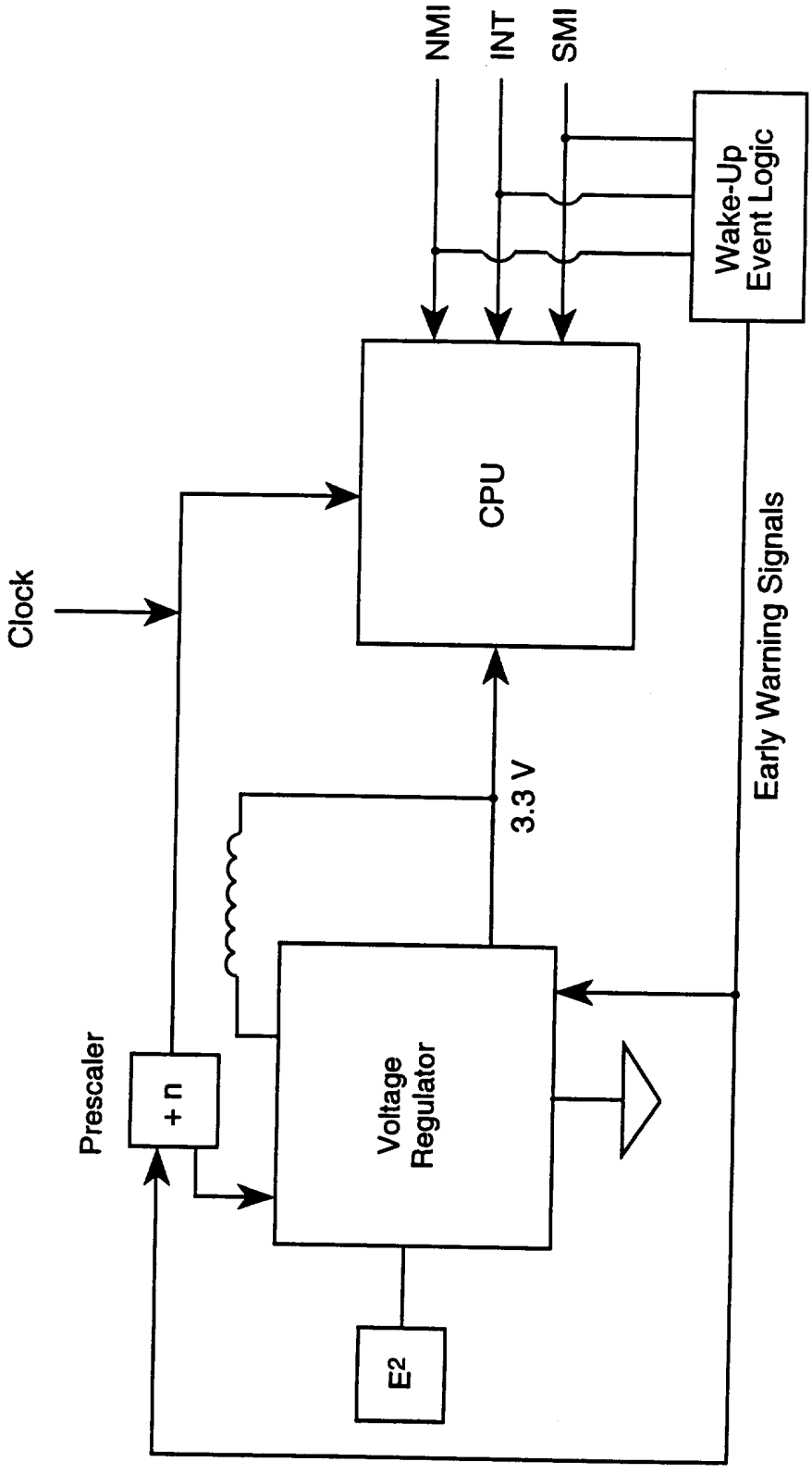
NMI
INT
SMI
Wake-Up Event Logic
CPU
Clock
Early Warning Signals
3.3 V
Prescaler
+ n
Voltage Regulator
E2

Fig. 6

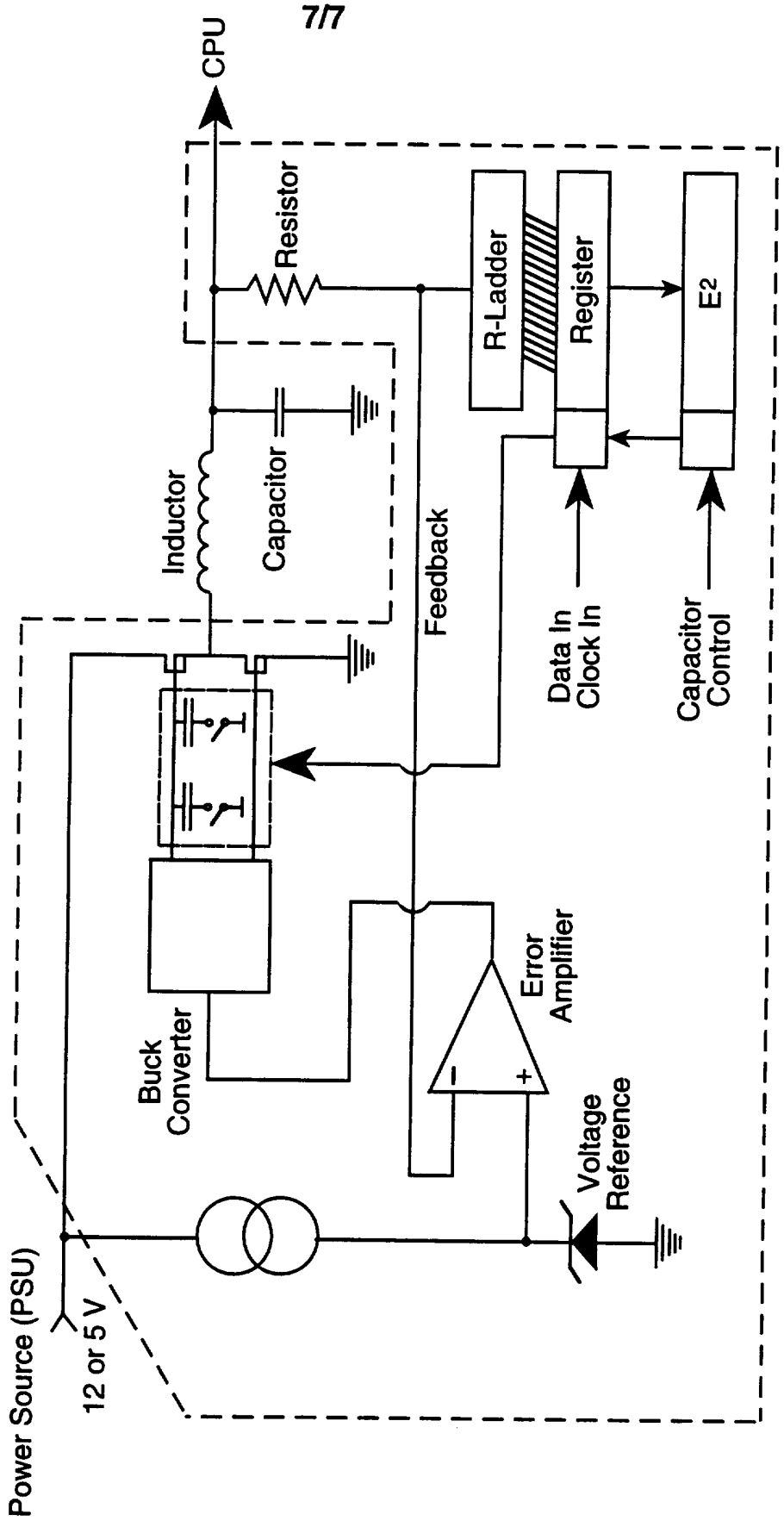
CPU
Resistor
R-Ladder
Register
E2
Inductor
Capacitor
Feedback
Data In
Clock In
Capacitor
Control
Buck
Converter
Error
Amplifier
Voltage
Reference
Power Source (PSU)
12 or 5 V

Fig. 7

INTERNATIONAL SEARCH REPORT

Inte...tional application No.
PCT/US95/13227

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 1/00; G05F 1/40
US CL :395/750; 323/280, 282

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/750; 323/280, 282

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,426,395 (CYGAN) 20 June 1995, see Figure 1 and col. 2, lines 9-46.	1
Y,P	US, A, 5,429,959 (SMAYLING) 04 July 1995, see col. 5, lines 41-63 and col. 6, lines 35-58.	1
A,P	US, A, 5,381,115 (TIMMONS ET AL) 10 January 1995, see abstract.	1
A	US, A, 5,325,071 (WESTMORELAND) 28 June 1994, see Figure 1.	1
A	US, A, 4,810,909 (ASAZAWA) 07 March 1989, see Figures 2 and 3.	1

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of mailing of the international search report

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