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(54) **ARRAY SUBSTRATE AND METHOD OF MANUFACTURING THE SAME, AND DISPLAY PANEL**

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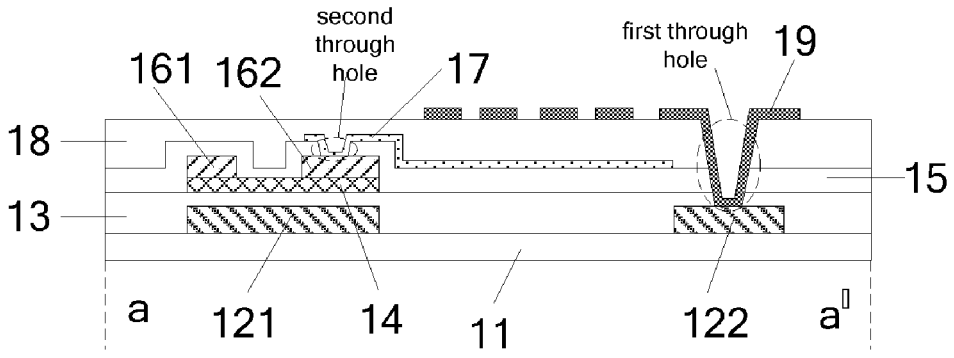
(57) **ABSTRACT**

The present disclosure provide an array substrate and a method of manufacturing the same, and a display panel. The array substrate includes: a base substrate; a first signal transmission layer comprising a common electrode line; a first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line; a first electrode layer located on the first insulating layer, the first electrode layer comprising a connection electrode located at the position of the first through hole; a second insulating layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode; and a second electrode layer comprising a common electrode that covers the second through hole; the connection electrode contacts the common electrode line and the common electrode respectively.



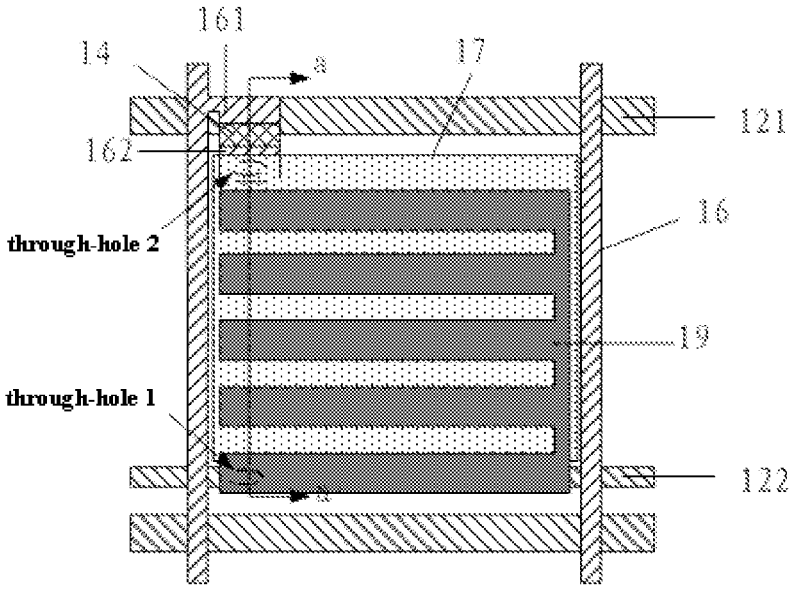


Fig. 1

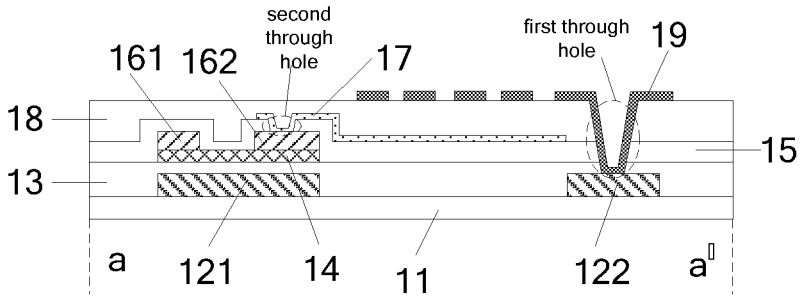


Fig. 2

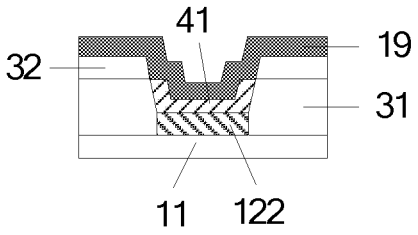


Fig. 3

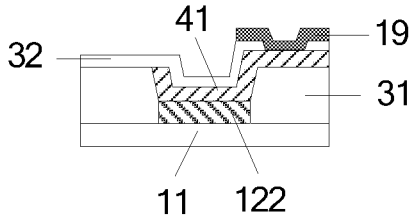


Fig. 4

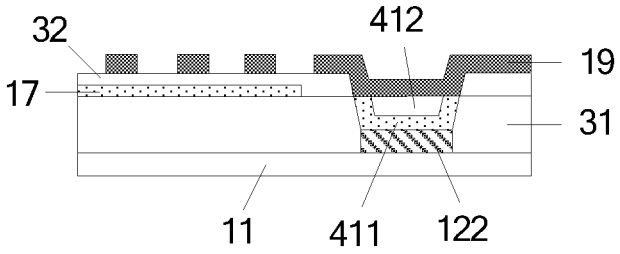


Fig. 5

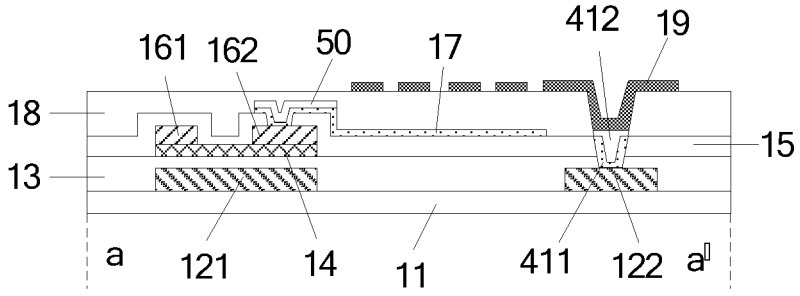


Fig. 6

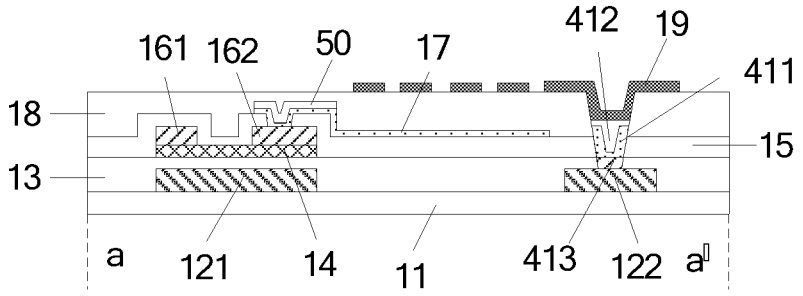


Fig. 7

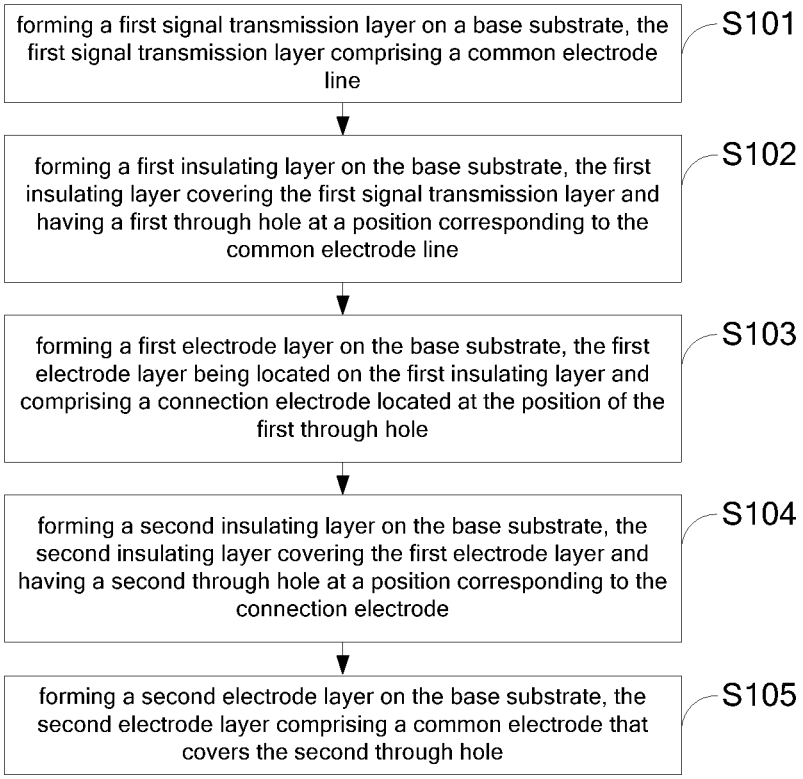

forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a common electrode line
S101
forming a first insulating layer on the base substrate, the first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line
S102
forming a first electrode layer on the base substrate, the first electrode layer being located on the first insulating layer and comprising a connection electrode located at the position of the first through hole
S103
forming a second insulating layer on the base substrate, the second insulating layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode
S104
forming a second electrode layer on the base substrate, the second electrode layer comprising a common electrode that covers the second through hole
S105

Fig. 8

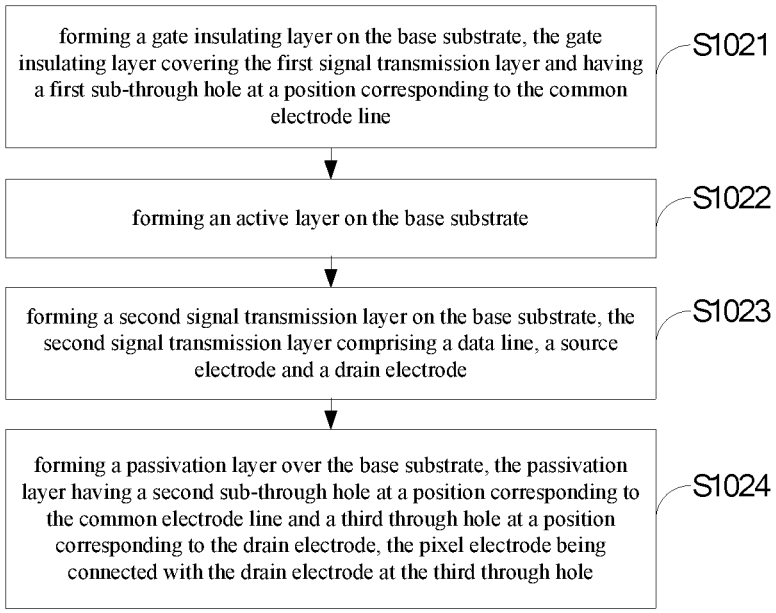

forming a gate insulating layer on the base substrate, the gate insulating layer covering the first signal transmission layer and having a first sub-through hole at a position corresponding to the common electrode line
S1021
forming an active layer on the base substrate
S1022
forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode and a drain electrode
S1023
forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode, the pixel electrode being connected with the drain electrode at the third through hole
S1024

Fig. 9

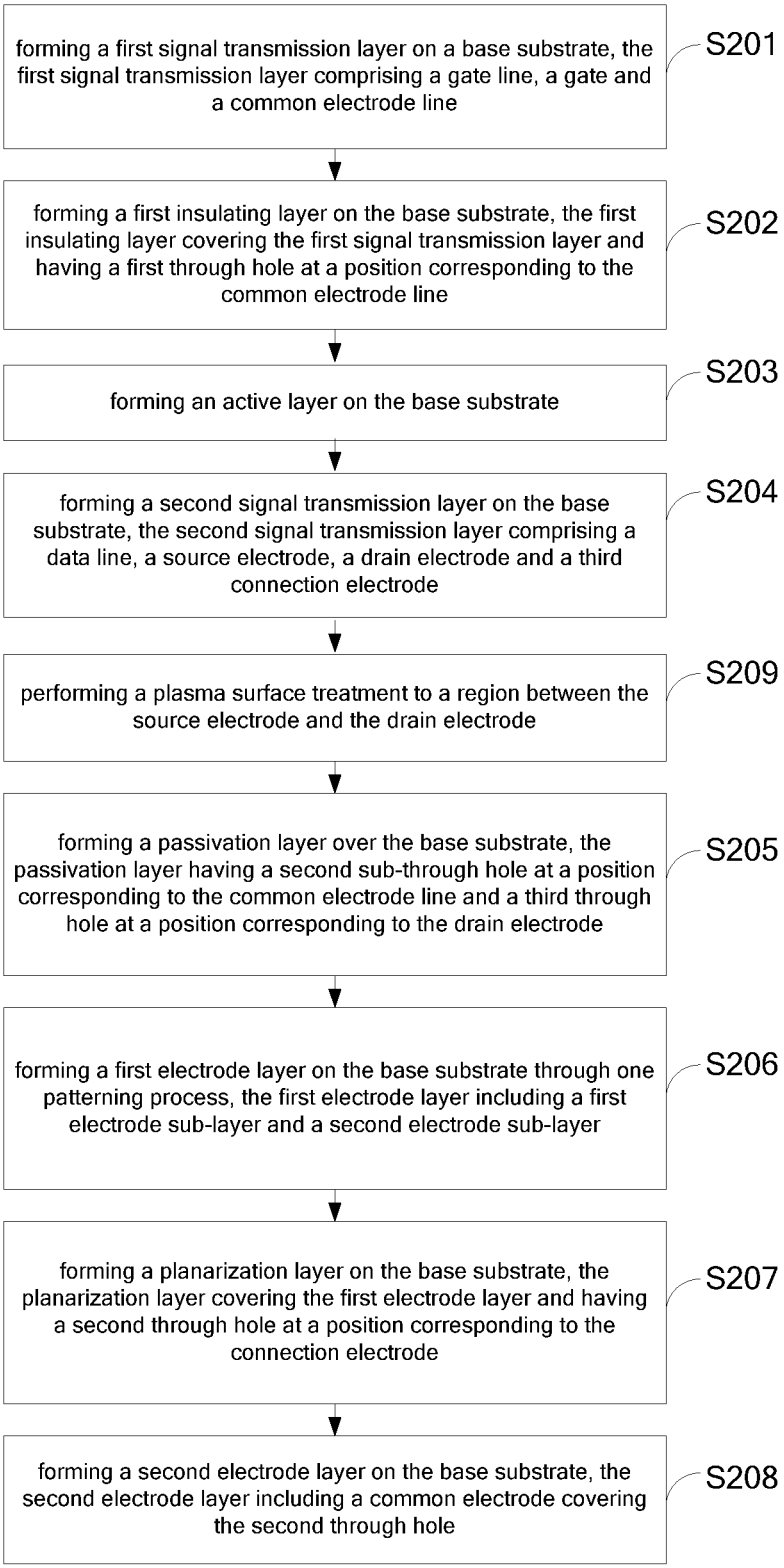

forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a gate line, a gate and a common electrode line
S201
forming a first insulating layer on the base substrate, the first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line
S202
forming an active layer on the base substrate
S203
forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode, a drain electrode and a third connection electrode
S204
performing a plasma surface treatment to a region between the source electrode and the drain electrode
S209
forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode
S205
forming a first electrode layer on the base substrate through one patterning process, the first electrode layer including a first electrode sub-layer and a second electrode sub-layer
S206
forming a planarization layer on the base substrate, the planarization layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode
S207
forming a second electrode layer on the base substrate, the second electrode layer including a common electrode covering the second through hole
S208

Fig. 10

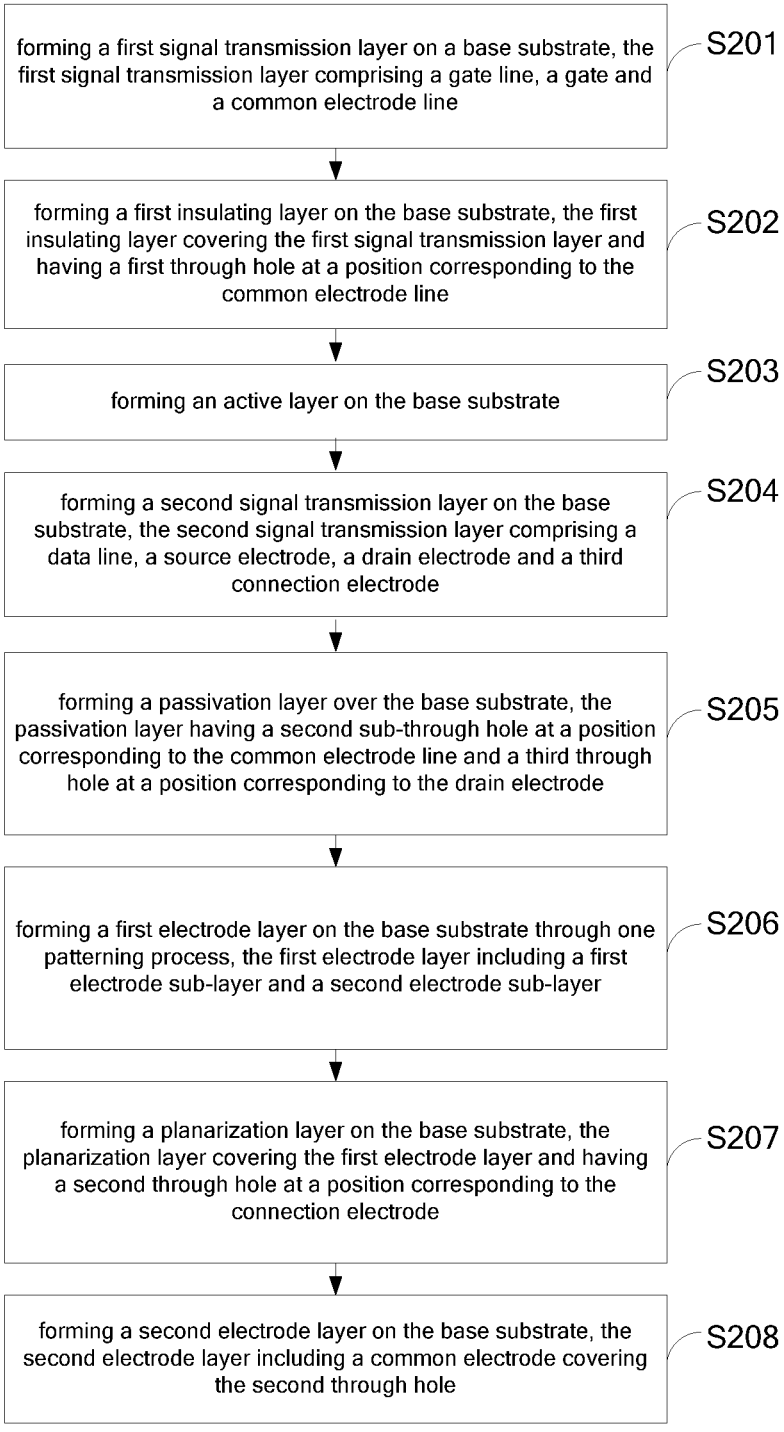

forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a gate line, a gate and a common electrode line
S201
forming a first insulating layer on the base substrate, the first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line
S202
forming an active layer on the base substrate
S203
forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode, a drain electrode and a third connection electrode
S204
forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode
S205
forming a first electrode layer on the base substrate through one patterning process, the first electrode layer including a first electrode sub-layer and a second electrode sub-layer
S206
forming a planarization layer on the base substrate, the planarization layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode
S207
forming a second electrode layer on the base substrate, the second electrode layer including a common electrode covering the second through hole
S208

Fig. 11

ARRAY SUBSTRATE AND METHOD OF MANUFACTURING THE SAME, AND DISPLAY PANEL

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Chinese Patent Application No. 201510629727.0 filed on Sep. 28, 2015 in the State Intellectual Property Office of China, the whole disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] Technical Field

[0003] Embodiments of the present disclosure generally relate to the field of display technologies, and particularly, to an array substrate and a method of manufacturing the same, and a display panel.

[0004] Description of the Related Art

[0005] TFT-LCDs become dominant in current market of flat panel display due to their advantages such as small volume, light weight, low power consumption, no radiation and the like. A TFT-LCD display screen generally includes an array substrate, a color filter base substrate and liquid crystal therebetween. The TFT-LCD display screen is provided with hundreds of thousands to millions of display units arranged in an array, and each display unit displays an image under control of TFT. It is desired to further improve yield of the display unit.

[0006] Exemplarily, as shown in FIG. **1**, there is shown a schematic diagram of a display unit on an array substrate of an existing TFT-LCD display screen, and a plurality of gate lines **121** and data lines **16** are formed on the array substrate, the gate lines **121** and the data lines **16** cross each other to define a display unit. FIG. **2** is a schematic diagram taken along line a-a' shown in FIG. **1**. As shown in FIG. **2**, the array substrate comprises: a base substrate **11**; a gate electrode (a portion of the gate line **121**) and a common electrode line **122** formed on base substrate **11**; a gate insulating layer **13** covering the gate electrode **121** and the common electrode line **122**; an active layer **14**, a source electrode **161** and a drain electrode **162** formed on gate insulating layer **13**; a passivation layer **15** and a pixel electrode **17** formed on the passivation layer **15**; a planarization layer **18** and a common electrode **19** formed on the planarization layer **18**. Generally, the common electrode **19** is connected with the common electrode line **122** through a through hole **1** through the planarization layer **18**, the passivation layer **15** and the gate insulating layer **13**, and the pixel electrode **17** is connected with drain electrode **162** through a through hole **2** in the passivation layer **15**.

[0007] It has been found by inventors that for the existing array substrate, as shown in FIG. **2**, since the through hole **1** penetrates through the planarization layer **18**, the passivation layer **15** and the gate insulating layer **13**, the through hole **1** has a larger depth, so that a connection between the common electrode **19** and the common electrode line **122** will easily be broken, resulting in a poor display effect and reduction in yield of product.

SUMMARY

[0008] Embodiments of the present disclosure provide an array substrate and a method of manufacturing the same, and a display panel, for avoiding a bad connection due to a deeper through hole by connecting a common electrode on the array substrate with a common electrode line through a plurality of conductive layers.

[0009] Embodiments of the present disclosure provide following technique solutions:

[0010] In an aspect, an embodiment of the present disclosure provides an array substrate, comprising:

[0011] a base substrate;

[0012] a first signal transmission layer comprising a common electrode line;

[0013] a first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line;

[0014] a first electrode layer located on the first insulating layer, the first electrode layer comprising a connection electrode located at the position of the first through hole;

[0015] a second insulating layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode; and

[0016] a second electrode layer comprising a common electrode that covers the second through hole;

[0017] the connection electrode is in contact with the common electrode line and the common electrode respectively.

[0018] Optionally, the second through hole is located at a position corresponding to the first through hole; or

[0019] the connection electrode extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer; and the second through hole is formed at a position of the second insulating layer corresponding to a portion, which extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, of the connection electrode.

[0020] Optionally, the first electrode layer comprises:

[0021] a first electrode sub-layer comprising a pixel electrode and a first connection electrode located at the position of the first through hole; and

[0022] a second electrode sub-layer comprising a second connection electrode located at located at the position of the first through hole, the second electrode sub-layer being disposed on the first electrode sub-layer.

[0023] Optionally, a material for forming the first electrode sub-layer comprises a tin indium oxide material and a material for forming the second electrode sub-layer a comprises metal.

[0024] Optionally, the second sub-layer comprises two molybdenum metal layers and an aluminum metal layer located between the two molybdenum metal layers.

[0025] Optionally, the first signal transmission layer further comprises a gate line and a gate electrode; and

[0026] the array substrate further comprises:

[0027] a gate insulating layer covering the first signal transmission layer and having a first sub-through hole at a position corresponding to the common electrode line;

[0028] an active layer located on the gate insulating layer;

[0029] a second signal transmission layer comprising a data line, a source electrode and a drain electrode; and

[0030] a passivation layer having a second sub-through hole at a position corresponding to the first sub-through hole and a third through hole at a position corresponding to the drain electrode, a pixel electrode being connected with the drain electrode at the third sub-through hole;

[0031] wherein, the first electrode layer is disposed on the passivation layer, the first insulating layer comprises the gate insulating layer and the passivation layer, the second electrode sub-layer further comprises an auxiliary electrode connected with the pixel electrode at least at a position corresponding to the third through hole.

[0032] Optionally, the array substrate comprises a transparent region and a non-transparent region, and the auxiliary electrode is connected with the pixel electrode within the non-transparent region.

[0033] Optionally, the second signal transmission layer further comprises a third connection electrode located at the position of the first through hole.

[0034] In another aspect, an embodiment of the present disclosure provides a method of manufacturing an array substrate, comprising steps of:

[0035] forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a common electrode line;

[0036] forming a first insulating layer on the base substrate, the first insulating layer covering the first signal transmission layer and the first insulating layer having a first through hole at a position corresponding to the common electrode line;

[0037] forming a first electrode layer on the base substrate, the first electrode layer being located on the first insulating layer and comprising a connection electrode located at the position of the first through hole;

[0038] forming a second insulating layer on the base substrate, the second insulating layer covering the first electrode layer and the second insulating layer having a second through hole at a position corresponding to the connection electrode; and

[0039] forming a second electrode layer on the base substrate, the second electrode layer comprising a common electrode that covers the second through hole;

[0040] wherein the connection electrode is in contact with the common electrode line and the common electrode respectively.

[0041] Optionally,

[0042] the step of the second insulating layer having the second through hole at the position corresponding to the connection electrode further comprises:

[0043] the connection electrode layer has the second through hole at a position corresponding to the first through hole; or

[0044] the connection electrode extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, and the second through hole is formed at a position of the second insulating layer corresponding to a portion, which extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, of the connection electrode.

[0045] Optionally,

[0046] the step of forming the first electrode layer on the base substrate further comprises:

[0047] forming a first conductive film, a second conductive film and photoresist on the base substrate to cover the first electrode layer, the first conductive film and the second conductive film covering the first through hole;

[0048] performing exposure and development processes to the photoresist by using a half gray-scale mask, which includes a transparent region, a semitransparent region corresponding to a pixel electrode and a non-transparent region corresponding to the first through hole;

[0049] fully removing a portion of the developed photoresist corresponding to the transparent region so as to expose the second conductive film, and partially removing a portion of the developed photoresist corresponding to the semitransparent region;

[0050] etching portions of the second conductive film and the first conductive film corresponding to the transparent region;

[0051] performing an ashing treatment to the photoresist such that a portion of the photoresist corresponding to semitransparent region is fully removed to expose the second conductive film and a portion of the photoresist corresponding to the non-transparent region is remained;

[0052] etching a portion of the second conductive film corresponding to the semitransparent region; and

[0053] peeling off the photoresist.

[0054] Optionally, the first conductive film is formed from a tin indium oxide material and the second conductive film is formed from a metal material.

[0055] Optionally, the step of forming the first conductive film, the second conductive film and photoresist on the base substrate to cover the first electrode layer further comprises:

[0056] forming the first conductive film on the first insulating layer;

[0057] forming the second conductive film on the first conductive film, including forming a molybdenum metal film, an aluminum metal film and a molybdenum metal film sequentially; and

[0058] forming the photoresist over the second conductive film.

[0059] Optionally, the first signal transmission layer further comprises a gate line and a gate electrode; and the step of forming the first insulating layer on the base substrate to cover the first signal transmission layer further comprises:

[0060] forming a gate insulating layer on the base substrate, the gate insulating layer covering the first signal transmission layer and the gate insulating layer having a first sub-through hole at a position corresponding to the common electrode line;

[0061] forming an active layer on the base substrate;

[0062] forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode and a drain electrode;

[0063] forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode, a pixel electrode being connected with the drain electrode at the third through hole;

[0064] the first insulating layer comprises the gate insulating layer and the passivation layer, the second electrode sub-layer further comprises an auxiliary electrode connected with the pixel electrode at least at a position corresponding to the third through hole.

[0065] Optionally, after forming the second signal transmission layer on the gate insulating layer and before forming the passivation layer over the second signal transmission layer, the method further comprises:

[0066] performing a plasma surface treatment to a region between the source electrode and the drain electrode.

[0067] In a further aspect, an embodiment of the present disclosure provides a display panel, comprising the array substrate of any of embodiments of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0068] In order to explain technical solutions in embodiments of the present disclosure or in prior arts more clearly, the drawings that are used to illustrate the embodiments or prior art will be described briefly below. Apparently, the drawings described below only show some of the embodiments of the present disclosure. One skilled in the art can obtain other drawings according to these drawings without paying any inventive efforts.

[0069] FIG. **1** is a schematic diagram of an existing array substrate;

[0070] FIG. **2** is a schematic diagram taken along line a-a' shown in FIG. **1**;

[0071] FIG. **3** is a schematic diagram of an array substrate provided according to an embodiment of the present disclosure;

[0072] FIG. **4** is a schematic diagram of another array substrate provided according to an embodiment of the present disclosure;

[0073] FIG. **5** is a schematic diagram of a further array substrate provided according to an embodiment of the present disclosure;

[0074] FIG. **6** is a schematic diagram of a still further array substrate provided according to an embodiment of the present disclosure;

[0075] FIG. **7** is a schematic diagram of a yet still further array substrate provided according to an embodiment of the present disclosure;

[0076] FIG. **8** is a schematic diagram showing a method of manufacturing an array substrate provided according to an embodiment of the present disclosure;

[0077] FIG. **9** is a schematic diagram showing a method of manufacturing a first insulating layer provided according to an embodiment of the present disclosure;

[0078] FIG. **10** is a schematic diagram showing another method of manufacturing a first insulating layer provided according to an embodiment of the present disclosure; and

[0079] FIG. **11** is a schematic diagram showing another method of manufacturing an array substrate provided according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0080] Technique solutions in exemplary embodiments of the present disclosure will be described hereinafter in detail with reference to the attached drawings in the embodiments. Obviously, the described embodiments are only some of embodiments of the present disclosure, instead of all of the embodiments of the present disclosure. For those skilled in the art, other embodiments achieved by referring to the following embodiments without involving any inventive steps also fall into the scope of the present disclosure.

[0081] It is noted that orientation terms used herein, such as "upper", "lower" or the like, are used to define an position orientation with relative to the array substrate shown in the drawings, and it should be understood that these orientation terms are relative terms used for relative description and clarification and may be correspondingly changed as the orientation at which the array substrate shown in the drawings is placed varies.

[0082] In all embodiments of the present disclosure, definitions of phrases "film", "layer" and "pattern" and relationships thereamong will be expounded. Particularly, a "film" is a layer of film manufactured from a certain material on a base substrate by using a deposition process or other process. If no patterning process is performed to the "film" during the whole manufacturing, the "film" may be also called as a "layer"; if a patterning process needs be performed to the "film" during the whole manufacturing, the "film" may be called as a "film" before the patterning process and as a "layer" after the patterning process. The "layer" which has been subject to the patterning process includes at least one film "pattern".

[0083] Exemplarily, a gate insulating layer may be manufactured by depositing SiNx (silicon nitride) on a transparent base substrate. The gate insulating layer is generally not subject to any patterning process. Further exemplarily, an active layer is formed by performing a patterning process to an oxide semiconductor film. A gate electrode metal layer comprises a gate electrode and a gate line, so the gate electrode and the gate line are together called as a pattern.

[0084] The called "patterning process" is a process for forming a film into a layer including at least one pattern; the patterning process generally includes: coating photoresist over a film, exposing the photoresist to light by using a mask, then eroding and washing off a portion of the photoresist to be removed by using a developer, etching off a portion of the film which is not covered with the photoresist, and finally peeling off remained photoresist. In all embodiment of the present disclosure, phrase "one patterning process" is directed to processes of forming a desired layer structure through one exposure process.

[0085] Exemplarily, as shown in FIG. **1**, there is shown a schematic diagram of a display unit on an array substrate of an existing TFT-LCD display screen, and a plurality of gate lines **121** and data lines **16** are formed on the array substrate, the gate lines **121** and the data lines **16** cross each other to define a display unit. FIG. **2** is a schematic diagram taken along line a-a'shown in FIG. **1**. As shown in FIG. **2**, the array substrate comprises: a base substrate **11**; a gate electrode (a portion of the gate line **121**) and a common electrode line **122** formed on base substrate **11**; a gate insulating layer **13** covering the gate electrode **121** and the common electrode line **122**; an active layer **14**, a source electrode **161** and a drain electrode **162** formed on gate insulating layer **13**; a passivation layer **15** and a pixel electrode **17** formed on the passivation layer **15**; a planarization layer **18** and a common electrode **19** formed on the planarization layer **18**. Generally, the common electrode **19** is connected with the common electrode line **122** through a through hole **1** through the planarization layer **18**, the passivation layer **15** and the gate insulating layer **13**, and the pixel electrode **17** is connected with drain electrode **162** through a through hole **2** in the passivation layer **15**.

[0086] It has been found by inventors that for the existing array substrate, as shown in FIG. **2**, since the through hole **1** penetrates through the planarization layer **18**, the passivation layer **15** and the gate insulating layer **13**, the through hole **1** has a larger depth, so that a connection between the common electrode **19** and the common electrode line **122**

will easily be broken, resulting in a poor display effect and reduction in yield of product.

[0087] An embodiment of the present disclosure provides an array substrate, as shown in FIG. **3**, comprising:

[0088] a base substrate **11**;

[0089] a first signal transmission layer comprising a common electrode line **122**;

[0090] a first insulating layer **31** covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line **122**; the first through hole being formed by removing a portion of the first insulating layer **31** at a position corresponding to the common electrode line **122**, and by forming the first through hole, an upper surface of a portion of the common electrode line **122** located below the first insulating layer **31** being exposed;

[0091] a first electrode layer located on the first insulating layer **31**, the first electrode layer comprising a connection electrode **41** located at the position of the first through hole; in other words, the connection electrode **41** being in direct contact with the upper surface of the common electrode line **122** exposed from the first through hole;

[0092] a second insulating layer **32** covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode **41**; and the second through hole being formed by removing a portion of the second insulating layer **32** at a position corresponding to the common electrode line **122**, and by forming the second through hole, an upper surface of a portion of the connection electrode **41** located below the second insulating layer **32** being exposed

[0093] a second electrode layer comprising a common electrode **19** that covers the second through hole; in other words, the common electrode **19** is in direct contact with an upper surface of the connection electrode **41** that is exposed from the second through hole and thus the connection electrode **41** contacts the common electrode line **122** and the common electrode **19** respectively, in other words, the common electrode **19** is connected with the common electrode line **122** through the connection electrode **41**.

[0094] It is noted that the array substrate may be further provided with other film or layer structures, and the array substrate has been described above by taking a region of the array substrate corresponding to a connection between the common electrode and the common electrode line as an example. Other film or layer structures may be not provided at a position corresponding to the common electrode, or the above described layer structure may include other film or layer structures. For example, in one embodiment, the array substrate comprises a thin film transistor, and if an active layer of the thin film transistor is only located at a position corresponding to a gate electrode, the pattern of the active layer is not included at a position corresponding to the common electrode line; and the thin film transistor may further comprise a source-drain metal layer, which may include the above connection electrode.

[0095] Embodiments of the present disclosure provide an array substrate, where the common electrode is connected with the common electrode line through the first through hole in the first insulating layer and the second through hole in second insulating layer, and the connection electrode is further formed at the first through hole so that the common electrode is connected with a common electrode line through the connection electrode. Compared with the configuration in which the common electrode is directly connected with the common electrode line, with the array substrate and the method of manufacturing the same, and the display panel provided according to the embodiments of the present disclosure, a depth for a connection between the common electrode and the common electrode line may be reduced, thereby preventing easy breakage between the connection between the common electrode and the common electrode line due to larger depths of the first through hole and the second through hole.

[0096] Optionally, the second through hole is located at a position corresponding to the first through hole. For example, as shown in FIG. **3**, the common electrode **19** is connected with the common electrode line **122** at a depth which is a sum of depths of the first through hole and the second through hole. Compared to an existing common electrode being directly connected with a common electrode line at the first through hole and a second through hole, the array substrate according to embodiments of the present disclosure, as shown in FIG. **3**, is configured such that the connection electrode **41** is located at the first through hole so that the depth at which the common electrode **19** is connected with the common electrode line **122** is reduced, thereby preventing easy breakage between the common electrode and the common electrode line due to larger depths of the first through hole and the second through hole.

[0097] In one embodiment of the present disclosure, as shown in FIG. **4**, the connection electrode **41** extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer **31**; and the second through hole is formed at a position of the second insulating layer **32** corresponding to a portion, which extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer **31**, of the connection electrode **41**. In other words, the first through hole may be located at a position offset from the second through hole, and the common electrode **19** is connected with the common electrode line **122** through the connection electrode **41**, thereby preventing easy breakage between the common electrode and the common electrode line due to larger depths of the first through hole and the second through hole.

[0098] In one embodiment of the present disclosure, as shown in FIG. **5**, the first electrode layer comprises:

[0099] a first electrode sub-layer comprising a pixel electrode **17** and a first connection electrode **411** located at the position of the first through hole; and

[0100] a second electrode sub-layer comprising a second connection electrode **412** located at the position of the first through hole, the second electrode sub-layer being disposed on the first electrode sub-layer **411**.

[0101] It is noted that the first electrode layer may include a plurality of conductive layers, which are not limited to the first electrode sub-layer and the second electrode sub-layer described above. In an embodiment of the present disclosure, the first electrode layer may further comprise a third electrode sub-layer and the like. Since the array substrate is formed with a pixel electrode, the first electrode sub-layer includes the pixel electrode and the first connection electrode, in other words, the pixel electrode and the first connection electrode are formed through one patterning process, thereby an additional exposure process for separately forming the first electrode sub-layer may be avoided.

[0102] In one embodiment of the present disclosure, a material for forming the first electrode sub-layer comprises a tin indium oxide material and a material for forming the second electrode sub-layer comprises metal. The pixel electrode is generally a transparent electrode, so the material for forming the first electrode sub-layer may be tin indium oxide. Metal has a better conductivity compared to a metal oxide. In order to improve the conductivity of the connection electrode, it is preferable that the material of the second electrode sub-layer is metal. An exemplary material of the second electrode sub-layer may be molybdenum metal, aluminum metal or the like.

[0103] In one embodiment of the present disclosure, the second sub-layer may comprise two molybdenum metal layers and an aluminum metal layer between the two molybdenum metal layers. In prior arts, the material of the second electrode sub-layer is aluminum, which has a more active metallicity. Thus, when forming other film or layer structures after the second electrode sub-layer, for example, when forming the second electrode layer, the aluminum metal will easily regrow under a high temperature environment, that is, there will be formed a smaller protrusion, which will contact the second electrode layer, thereby resulting in a short circuit. Thus, in one embodiment of the present disclosure, molybdenum metal layers are formed on either side of the aluminum metal layer respectively. Since the molybdenum metal layer is more stable than the aluminum metal layer, the second electrode sub-layer may be prevented from contacting other electrode layer at high temperature.

[0104] In one embodiment, as shown in FIG. **6**, the first signal transmission layer further comprises a gate line and a gate electrode **121**; the array substrate further comprises:

[0105] a gate insulating layer **13** covering the first signal transmission layer and having a first sub-through hole at a position corresponding to the common electrode line **122**;

[0106] an active layer **14** located on the gate insulating layer **13**;

[0107] a second signal transmission layer comprising a data line, a source electrode **161** and a drain electrode **162**; and

[0108] a passivation layer **15** having a second sub-through hole at a position corresponding to the first sub-through hole and a third through hole at a position corresponding to the drain electrode, the pixel electrode **17** being connected with the drain electrode **162** at the third sub-through hole;

[0109] the first electrode layer is disposed on the passivation layer **15**, the first insulating layer comprises the gate insulating layer **14** and the passivation layer **15**, the second electrode sub-layer further comprises an auxiliary electrode **50** connected with the pixel electrode **17** at least at a position corresponding to the third through hole.

[0110] That is, the first insulating layer includes the gate insulating layer **13** and the passivation layer **15**, and the first through hole includes the first sub-through hole in the gate insulating layer **13** and the second sub-through hole in the passivation layer **15**.

[0111] The array substrate further comprises a thin film transistor, which comprises the gate electrode, the source electrode and the drain electrode; wherein, the passivation layer has the third through hole at a position corresponding to the drain electrode and the pixel electrode is connected with drain electrode at the third through hole, and, as the second electrode sub-layer is located above the first electrode sub-layer, the auxiliary electrode, which is connected with the pixel electrode, is formed at a position of the second electrode sub-layer corresponding to the third through hole. In one embodiment, the second electrode sub-layer includes two molybdenum metal layers having a better stability, with an aluminum metal layer located between the two molybdenum metal layers; and the second electrode sub-layer is located above the pixel electrode at a position where the pixel electrode is connected with the drain electrode, such that the pixel electrode may be further prevented from contacting air at the position, thereby further protecting a normal connection between the pixel electrode and the drain electrode.

[0112] In one embodiment, the array substrate comprises a transparent region and a non-transparent region, and the auxiliary electrode is connected with the pixel electrode within the non-transparent region. Since the pixel electrode is formed within the transparent region mainly for light transmission display, the auxiliary electrode is provided within the non-transparent region and connected with the pixel electrode, thereby further protecting a normal connection between the pixel electrode and the drain electrode.

[0113] In one embodiment, as shown in FIG. **7**, the second signal transmission layer further comprises a third connection electrode **413** located at the position of the first through hole; that is, the second signal transmission layer further comprises the third connection electrode **413** between the common electrode **19** and the common electrode line **122**, thereby further reducing the depth at which the common electrode **19** is connected with the common electrode line **122**. Further, the third connection electrode, the source electrode and the drain electrode are formed simultaneously, reducing the number of patterning processes by one.

[0114] An embodiment of the present disclosure provides a method of manufacturing an array substrate. As shown in FIG. **8**, the method comprises a step **101**: forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a common electrode line.

[0115] Exemplarily, the step **101** comprises: forming a metal film on the base substrate, exposing the metal film, and etching the metal film to form the first signal transmission layer including the common electrode line. Particularly, the exposure and etching may be performed in a mask patterning process.

[0116] The method further comprises a step **102**: forming a first insulating layer on the base substrate, the first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line.

[0117] Exemplarily, the step **102** includes: forming the first insulating film on the base substrate to cover the first signal transmission layer, performing exposure and etching processes to the first insulating film so as to form a through hole in the first insulating film at a position corresponding to the common electrode line, such that an upper surface of the common electrode line is exposed from the through hole of the first insulating film.

[0118] The method further comprises a step **103**: forming a first electrode layer on the base substrate, the first electrode layer being located on the first insulating layer and comprising a connection electrode located at the position of the first through hole.

[0119] In an embodiment, the step **103** includes: forming a first conductive film, a second conductive film and photoresist on the base substrate to cover the first electrode

layer, the first conductive film and the second conductive film covering the first through hole.

[0120] In an embodiment of the present disclosure, the exposure and development processes are performed to a photoresist by using a half gray-scale mask, in which the half gray-scale mask includes a transparent region, a semi-transparent region corresponding to a pixel electrode and a non-transparent region corresponding to the first through hole; a portion of the developed photoresist corresponding to the transparent region is fully removed so as to expose the second conductive film, and a portion of the developed photoresist corresponding to the semitransparent region is partially removed; portions of the second conductive film and the first conductive film corresponding to the transparent region are etched off; an ashing treatment is performed to the photoresist such that a portion of the photoresist corresponding to semitransparent region is fully removed to expose the second conductive film and a portion of the photoresist corresponding to the non-transparent region is remained; a portion of the second conductive film corresponding to the semitransparent region is etched off; and the photoresist is peeled off.

[0121] In one embodiment of the present disclosure, the conductive film is made of metal, i.e., the second electrode sub-layer is formed from a metal. Compared to metal oxide, the metal has a better conductivity. In one embodiment, in order to improve the conductivity of the connection electrode, the material of the second electrode sub-layer is metal. For example, the material of the second electrode sub-layer may be molybdenum metal, aluminum metal or the like.

[0122] It is noted that the second electrode sub-layer is generally made of metal, and thus, the second electrode sub-layer is generally dry-etched, while the first electrode sub-layer is wet-etched. If the material of the second electrode sub-layer is molybdenum metal, both the second electrode sub-layer and the first electrode sub-layer may be wet-etched, thereby simplifying process steps.

[0123] In one embodiment, the step of forming a first conductive film, a second conductive film and photoresist on the base substrate to cover the first electrode layer further comprises:

[0124] forming the first conductive film on the first insulating layer;

[0125] forming the second conductive film on the first conductive film, including forming a molybdenum metal film, an aluminum metal film and a molybdenum metal film sequentially; and

[0126] forming the photoresist over the second conductive film.

[0127] That is, the second electrode sub-layer may comprise two molybdenum metal layers and an aluminum metal layer between the two molybdenum metal layers. In as an exemplary embodiment where the material of the second electrode sub-layer is aluminum, as the aluminum has a more active metallicity, when forming other film or layer structures after the second electrode sub-layer, for example, when forming the second electrode layer, the aluminum metal will easily regrow under a high temperature environment, that is, there will be formed smaller protrusions, which will contact the second electrode layer, thereby resulting in a short circuit. Thus, in an embodiment of the present disclosure, molybdenum metal layers are formed on either side of the aluminum metal layer respectively. Since the molybdenum metal layer is more stable than the aluminum metal layer, the second electrode sub-layer may be prevented from contacting other electrode layers.

[0128] It is noted that when the second electrode includes three material layers of molybdenum, aluminum and molybdenum, the second electrode sub-layer is dry-etched, while the first electrode is wet-etched.

[0129] In one embodiment, the first conductive film is formed from a tin indium oxide material. The pixel electrode is generally a transparent electrode, and thus the first electrode sub-layer is formed from a tin indium oxide material.

[0130] The method further comprises a step **104**: forming a second insulating layer on the base substrate, the second insulating layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode.

[0131] Exemplarily, the step **104** includes: forming the second insulating film on the first electrode layer to cover first electrode layer, and performing exposure and etching processes to the second insulating film so as to remove a portion of the second insulating film corresponding to the through hole of the first insulating layer, such that an upper surface of the connection electrode is exposed.

[0132] In one embodiment, the step of the second insulating layer having a second through hole at a position corresponding to the connection electrode particularly comprises:

[0133] the connection electrode layer has the second through hole at a position corresponding to the first through hole. That is, the second through hole is located at a position corresponding to the first through hole, as shown in FIG. **3**, The common electrode **19** is connected with the common electrode line **122** at a depth which is a sum of depths the first through hole and the second through hole.

[0134] Or, the connection electrode extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, and the second insulating layer having a second through hole at a position corresponding to the connection electrode particularly comprises: the second insulating layer having the second through hole at a position corresponding to a portion of the connection electrode extending out of the first through hole.

[0135] Particularly, by referring to FIG. **4**, the connection electrode **19** extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer **31**; and the second insulating layer **31** has a second through hole at a position corresponding to a portion of the connection electrode **41** extending out of the first through hole. That is, the first through hole may be also located at a position offset from the second through hole, and the common electrode is connected with the common electrode line through the connection electrode, thereby preventing easy breakage between the common electrode and the common electrode line due to larger depths of the first through hole and the second through hole.

[0136] The method may further comprise a step **105**: forming a second electrode layer on the base substrate, the second electrode layer comprising a common electrode that covers the second through hole. In an example, the connection electrode contacts the common electrode line and the common electrode respectively.

[0137] Optionally, the first signal transmission layer further comprises a gate line and a gate electrode. As shown in

FIG. **9**, the step of forming a first insulating layer on the base substrate to cover the first signal transmission layer further comprises:

[0138] a step **1021**: forming a gate insulating layer on the base substrate, the gate insulating layer covering the first signal transmission layer and having a first sub-through hole at a position corresponding to the common electrode line.

[0139] Exemplarily, the step **201** includes: forming an insulating film on the base substrate, and performing exposure and etching processes to the insulating film so as to form a gate insulating layer, which has a first sub-through hole at a position corresponding to the common electrode line.

[0140] The step of forming a first insulating layer on the base substrate to cover the first signal transmission layer may further comprise a step **1022**: forming an active layer on the base substrate. Particularly it comprises: forming a semiconductor film on the base substrate, and performing exposure and etching processes to the semiconductor film to form an active layer.

[0141] The step of forming a first insulating layer on the base substrate to cover the first signal transmission layer may further comprise a step **1023**: forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode and a drain electrode.

[0142] Particularly, the step **1023** includes: forming a metal film and photoresist on the active layer; performing exposure and development processes to the photoresist by using a mask, which includes a transparent region and a non-transparent region corresponding to the data line, the source electrode and the drain electrode, fully removing a portion of the developed photoresist corresponding to the transparent region so as to expose the metal film, and etching a portion of the metal film corresponding to the transparent region; and peeling off the photoresist.

[0143] The step of forming a first insulating layer on the base substrate to cover the first signal transmission layer may further comprise a step **1024**: forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode, and the pixel electrode being connected with the drain electrode at the third through hole.

[0144] Particularly, the step **1024** includes: forming an insulating film on the second signal transmission layer, performing exposure and etching processes to the insulating film so as to form through holes at positions corresponding to the drain electrode and the common electrode line, such that an upper surface of the drain electrode and an upper surface of the common electrode line are exposed.

[0145] The first insulating layer comprises the gate insulating layer and the passivation layer, and the second electrode sub-layer further comprises an auxiliary electrode connected with the pixel electrode at least at a position corresponding to the third through hole.

[0146] The formed array substrate is shown in FIG. **6**, the array substrate further comprises a thin film transistor, which comprises the gate electrode, the source electrode and the drain electrode. In an example, the passivation layer has the third through hole at a position corresponding to the drain electrode and is connected with drain electrode at the third through hole, and, as the second electrode sub-layer is located above the first electrode sub-layer, the auxiliary electrode, which is connected with the pixel electrode, is formed at a position of the second electrode sub-layer corresponding to the third through hole. In an example where the second electrode sub-layer includes two molybdenum metal layers and an aluminum metal layer located between the two molybdenum metal layers, the molybdenum metal layer has a better stability, and the second electrode sub-layer is located above the pixel electrode at a position where the pixel electrode is connected with the drain electrode, such that the pixel electrode may be further prevented from contact air at the position, thereby further protecting a normal connection between the pixel electrode and the drain electrode.

[0147] In the array substrate shown in FIG. **6**, the first insulating layer includes the gate insulating layer **13** and the passivation layer **15**, and the first through hole includes the first sub-through hole in the gate insulating layer **13** and the second sub-through hole in the passivation layer **15**.

[0148] In one embodiment, the second signal transmission layer further comprises a third connection electrode located at the position of the first through hole. As shown in FIG. **7**, the second signal transmission layer further comprises the third connection electrode **413** between the common electrode **19** and the common electrode line **122**, thereby the depth at which the common electrode **19** is connected with the common electrode line **122** may be further reduced. Further, the third connection electrode, the source electrode and the drain electrode are formed simultaneously, reducing the number of patterning processes by one.

[0149] In one embodiment, as shown in FIG. **10**, after the step **1023** and before the step **1024**, the method further comprises:

[0150] a step **1025**: performing a plasma surface treatment to a region between the source electrode and the drain electrode.

[0151] In an example, the plasma surface treatment may be performed by using gases such as SF_6+O_2, H_2 or the like, for purpose of clearing impurity ions in a conductive channel and reducing defects in a layer of the conductive channel. Of course, the plasma surface treatment may be performed to the region between the source electrode and the drain electrode by using other gases, and embodiments of the present disclosure are only described by taking the above as an example.

[0152] In the method of manufacturing an array substrate provided according to the embodiments of the present disclosure, the channel region is subject to the plasma treatment before forming the passivation layer such that impact damages of the channel generated during etching the channel may be corrected and alleviated, and a gas treatment may be performed to the channel to clear impurity ions in the conductive channel such that defects in the layer of the conductive channel may be reduced, thereby performances of the thin film transistor may be improved.

[0153] Hereinafter, an exemplary embodiment is provided to describe the method of manufacturing an array substrate shown in FIG. **7**; as shown in FIG. **11**, the method includes:

[0154] step **201**: forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a gate line, a gate electrode and a common electrode line;

[0155] step **202**: forming a first insulating layer on the base substrate, the first insulating layer covering the first

signal transmission layer and having a first through hole at a position corresponding to the common electrode line;

[0156] step **203**: forming an active layer on the base substrate;

[0157] step **204**: forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode, a drain electrode and a third connection electrode;

[0158] step **205**: performing a plasma surface treatment to a region between the source electrode and the drain electrode;

[0159] step **206**: forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode;

[0160] step **207**: forming a first electrode layer on the base substrate through a single patterning process, the first electrode layer including a first electrode sub-layer and a second electrode sub-layer, the first electrode sub-layer including a pixel electrode and a first connection electrode, the second electrode sub-layer including a second connection electrode; and details may be obtained by referring to the above step **103**;

[0161] step **208**: forming a planarization layer on the base substrate, the planarization layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode; and

[0162] step **209**: forming a second electrode layer on the base substrate, the second electrode layer including a common electrode covering the second through hole, and the connection electrode contacting the common electrode line and the common electrode respectively.

[0163] Of course, the method of manufacturing an array substrate shown in FIG. **7** is not limited to the above steps. For example, the first electrode sub-layer and the second electrode sub-layer may be formed through two patterning processes. The embodiments of the present disclosure are only described by taking the above as an example.

[0164] The embodiments of the present disclosure provide an array substrate and a method of manufacturing the same, and a display panel, where the common electrode on the array substrate is connected with the common electrode line through the first through hole in the first insulating layer and the second through hole in second insulating layer, and the connection electrode is further formed at the first through hole so that the common electrode is connected with the connection electrode. With the array substrate and the method of manufacturing the same, and the display panel provided according to the embodiments of the present disclosure, compared to a direct connection between a common electrode and a common electrode line, a depth for a connection between the common electrode and the common electrode line may be reduced, thereby preventing easy breakage between the connection between the common electrode and the common electrode line due to larger depths of the first through hole and the second through hole.

[0165] The above described contents are only exemplary embodiments of the present disclosure, and the scope of the present invention is not limited to those. Various changes or modifications, which may be easily envisaged by those skilled in the art in these embodiments without departing from the principles and spirit of the present disclosure, are intended to be covered within the scope of the present invention. Therefore, the scope of the present invention is defined in the claims and their equivalents.

1. An array substrate, comprising:

a base substrate;

a first signal transmission layer comprising a common electrode line;

a first insulating layer covering the first signal transmission layer and having a first through hole at a position corresponding to the common electrode line;

a first electrode layer located on the first insulating layer, the first electrode layer comprising a connection electrode located at the position of the first through hole;

a second insulating layer covering the first electrode layer and having a second through hole at a position corresponding to the connection electrode; and

a second electrode layer comprising a common electrode that covers the second through hole;

wherein the connection electrode is in contact with the common electrode line and the common electrode respectively; and

wherein the first electrode layer comprises:

a first electrode sub-layer, comprising a pixel electrode and a first connection electrode located at the position of the first through hole; and

a second electrode sub-layer comprising a second connection electrode located at the position of the first through hole, the second sub-layer being disposed on the first electrode sub-layer.

2. The array substrate according to claim **1**, wherein

the second through hole is located at a position corresponding to the first through hole; or

the connection electrode extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer; and the second through hole is formed at a position of the second insulating layer corresponding to a portion, which extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, of the connection electrode.

3. (canceled)

4. The array substrate according to claim **1**, wherein a material for forming the first electrode sub-layer comprises a tin indium oxide material and a material for forming the second electrode sub-layer comprises a metal.

5. The array substrate according to claim **4**, wherein the second sub-layer comprises two molybdenum metal layers and an aluminum metal layer located between the two molybdenum metal layers.

6. The array substrate according to claim **1**, wherein the first signal transmission layer further comprises a gate line and a gate electrode;

the array substrate further comprises:

a gate insulating layer covering the first signal transmission layer and having a first sub-through hole at a position corresponding to the common electrode line;

an active layer located on the gate insulating layer;

a second signal transmission layer comprising a data line, a source electrode and a drain electrode; and

a passivation layer having a second sub-through hole at a position corresponding to the first sub-through hole and a third through hole at a position corresponding

to the drain electrode, a pixel electrode being connected with the drain electrode at the third sub-through hole;

wherein, the first electrode layer is disposed on the passivation layer, the first insulating layer comprises the gate insulating layer and the passivation layer, the second electrode sub-layer further comprises an auxiliary electrode connected with the pixel electrode at least at a position corresponding to the third through hole.

7. The array substrate according to claim **6**, wherein the array substrate comprises a transparent region and a non-transparent region, and the auxiliary electrode is connected with the pixel electrode within the non-transparent region.

8. The array substrate according to claim **6**, wherein the second signal transmission layer further comprises a third connection electrode located at the position of the first through hole.

9. A method of manufacturing an array substrate, comprising steps of:

forming a first signal transmission layer on a base substrate, the first signal transmission layer comprising a common electrode line;

forming a first insulating layer on the base substrate, the first insulating layer covering the first signal transmission layer and the first insulating layer having a first through hole at a position corresponding to the common electrode line;

forming a first electrode layer on the base substrate, the first electrode layer being located on the first insulating layer and comprising a connection electrode located at the position of the first through hole;

forming a second insulating layer on the base substrate, the second insulating layer covering the first electrode layer and the second insulating layer having a second through hole at a position corresponding to the connection electrode; and

forming a second electrode layer on the base substrate, the second electrode layer comprising a common electrode that covers the second through hole;

wherein the connection electrode is in contact with the common electrode line and the common electrode respectively; and

wherein the step of forming the first electrode layer on the base substrate further comprises:

forming a first conductive film, a second conductive film and photoresist on the base substrate to cover the first electrode layer, the first conductive film and the second conductive film covering the first through hole;

performing exposure and development processes to the photoresist by using a half gray-scale mask, which includes a transparent region, a semitransparent region corresponding to a pixel electrode and a non-transparent region corresponding to the first through hole;

full removing a portion of the developed photoresist corresponding to the transparent region so as to expose the second conductive film, and partially removing a portion of the developed photoresist corresponding to the semitransparent region;

etching portions of the second conductive film and the first conductive film corresponding to the transparent region;

performing an ashing treatment to the photoresist such that a portion of the photoresist corresponding to semitransparent region is fully removed to expose the second conductive film and a portion of the photoresist corresponding to the non-transparent region is remained;

etching a portion of the second conductive film corresponding to the semitransparent region; and

peeling off the photoresist.

10. The method according to claim **9**, wherein in the step of forming a second insulating layer on the base substrate,

the connection electrode layer has the second through hole at a position corresponding to the first through hole; or

the connection electrode extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, and the second through hole is formed at a position of the second insulating layer corresponding to a portion, which extends out of the first through hole and extends over at least a portion of an upper surface of the first insulating layer, of the connection electrode.

11. (canceled)

12. The method according to claim **9**, wherein the first conductive film is formed from a tin indium oxide material and the second conductive film is formed from a metal material.

13. The method according to claim **9**, wherein the step of forming the first conductive film, the second conductive film and photoresist on the base substrate to cover the first electrode layer further comprises:

forming the first conductive film on the first insulating layer;

forming the second conductive film on the first conductive film, including forming a molybdenum metal film, an aluminum metal film and a molybdenum metal film sequentially; and

forming the photoresist over the second conductive film.

14. The method according to claim **9**, wherein the first signal transmission layer further comprises a gate line and a gate electrode; and the step of forming the first insulating layer on the base substrate to cover the first signal transmission layer further comprises:

forming a gate insulating layer on the base substrate, the gate insulating layer covering the first signal transmission layer and the gate insulating layer having a first sub-through hole at a position corresponding to the common electrode line;

forming an active layer on the base substrate;

forming a second signal transmission layer on the base substrate, the second signal transmission layer comprising a data line, a source electrode and a drain electrode; and

forming a passivation layer over the base substrate, the passivation layer having a second sub-through hole at a position corresponding to the common electrode line and a third through hole at a position corresponding to the drain electrode, a pixel electrode being connected with the drain electrode at the third through hole;

wherein the first insulating layer comprises the gate insulating layer and the passivation layer, and the second electrode sub-layer further comprises an auxil-

iary electrode connected with the pixel electrode at least at a position corresponding to the third through hole.

15. The method according to claim **12**, wherein after forming the second signal transmission layer on the gate insulating layer and before forming the passivation layer over the second signal transmission layer, the method further comprises:

performing a plasma surface treatment to a region between the source electrode and the drain electrode.

16. A display panel, comprising the array substrate according to claim **1**.

17. The method according to claim **13**, wherein after forming the second signal transmission layer on the gate insulating layer and before forming the passivation layer over the second signal transmission layer, the method further comprises:

performing a plasma surface treatment to a region between the source electrode and the drain electrode.

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