(19) **United States**
(12) **Patent Application Publication**
Kuo et al.
(10) **Pub. No.: US 2018/0269112 A1**
(43) **Pub. Date: Sep. 20, 2018**

(54) **MULTI-GATE DEVICES WITH REPLACED-CHANNELS AND METHODS FOR FORMING THE SAME**

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

(72) Inventors: **Chih-Wei Kuo**, Tainan (TW); **Yuan-Shun Chao**, Zhubei City (TW); **Hou-Yu Chen**, Zhubei City (TW); **Shyh-Horng Yang**, Hsinchu (TW)

(21) Appl. No.: **15/985,830**

(22) Filed: **May 22, 2018**

Related U.S. Application Data

(60) Continuation of application No. 14/887,102, filed on Oct. 19, 2015, now Pat. No. 10,014,223, which is a division of application No. 13/457,258, filed on Apr. 26, 2012, now Pat. No. 9,171,925.

Publication Classification

(51) **Int. Cl.**

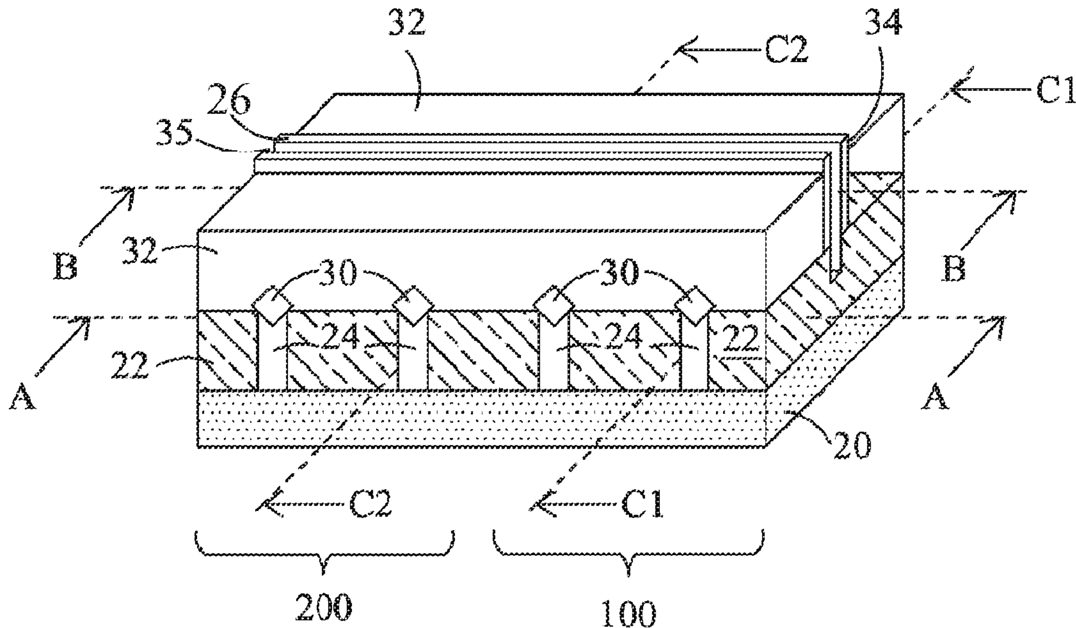
H01L 21/8238	(2006.01)
H01L 27/092	(2006.01)
H01L 29/66	(2006.01)
H01L 29/78	(2006.01)
H01L 21/8234	(2006.01)

(52) **U.S. Cl.**

CPC .. ***H01L 21/823821*** (2013.01); ***H01L 27/0924*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/7849*** (2013.01); ***H01L 29/7848*** (2013.01); *H01L 21/31055* (2013.01); *H01L 29/6656* (2013.01); ***H01L 21/823481*** (2013.01); ***H01L 21/823437*** (2013.01); ***H01L 21/823431*** (2013.01)

(57) **ABSTRACT**

A device includes a semiconductor substrate, isolation regions in the semiconductor substrate, and a Fin Field-Effect Transistor (FinFET). The FinFET includes a channel region over the semiconductor substrate, a gate dielectric on a top surface and sidewalls of the channel region, a gate electrode over the gate dielectric, a source/drain region, and an additional semiconductor region between the source/drain region and the channel region. The channel region and the additional semiconductor region are formed of different semiconductor materials, and are at substantially level with each other.



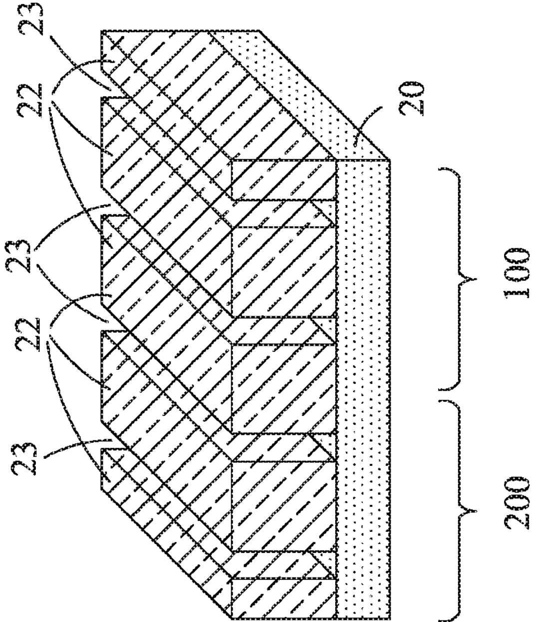


Fig. 2

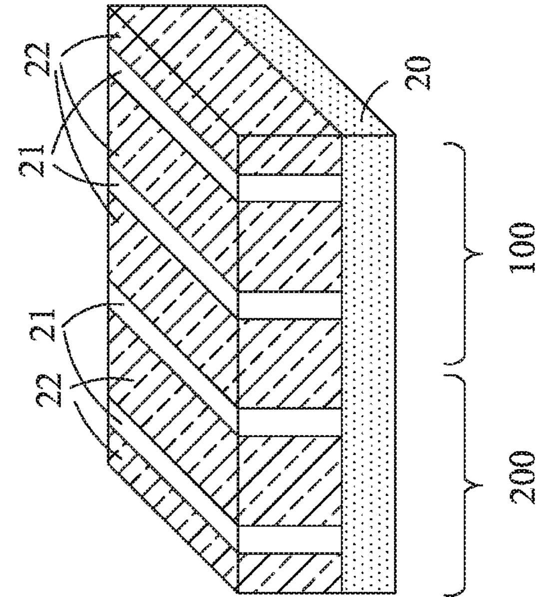


Fig. 1

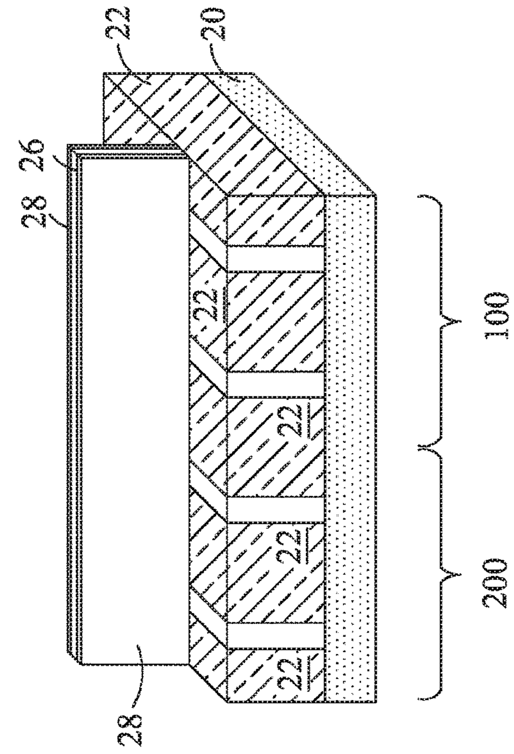


Fig. 4

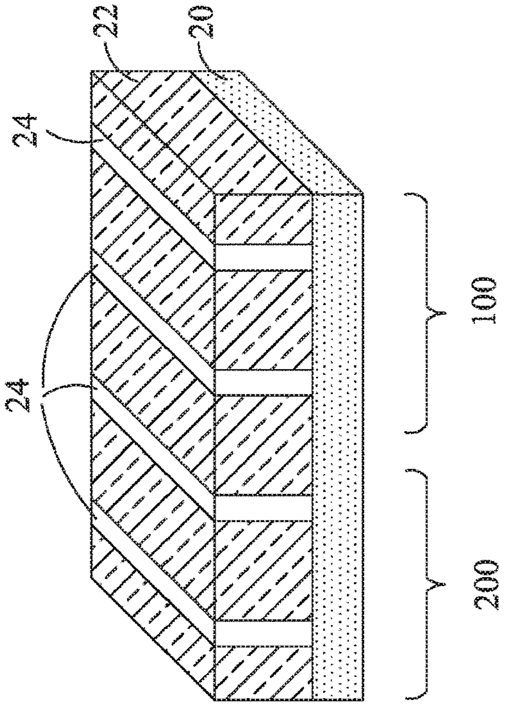


Fig. 3

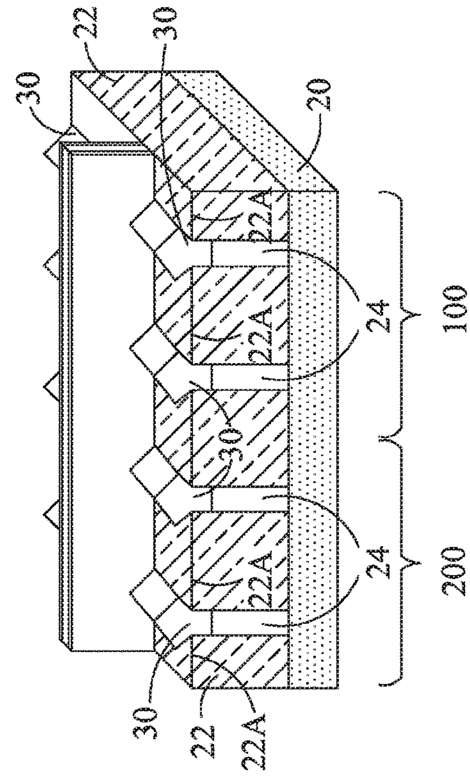


Fig. 6

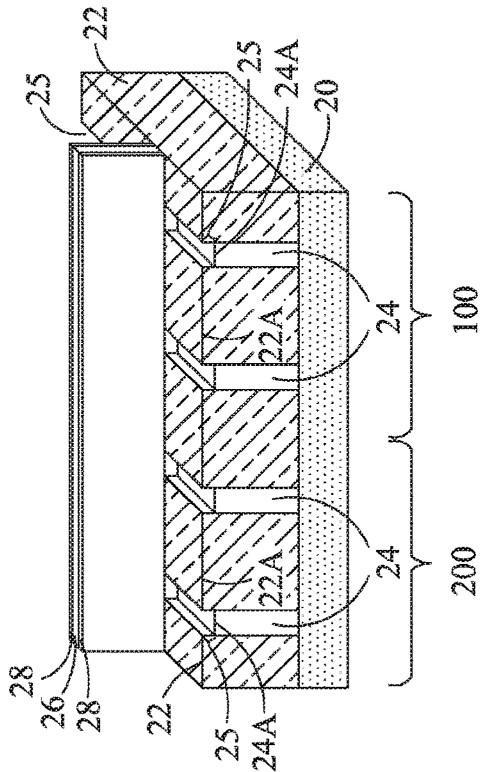


Fig. 5

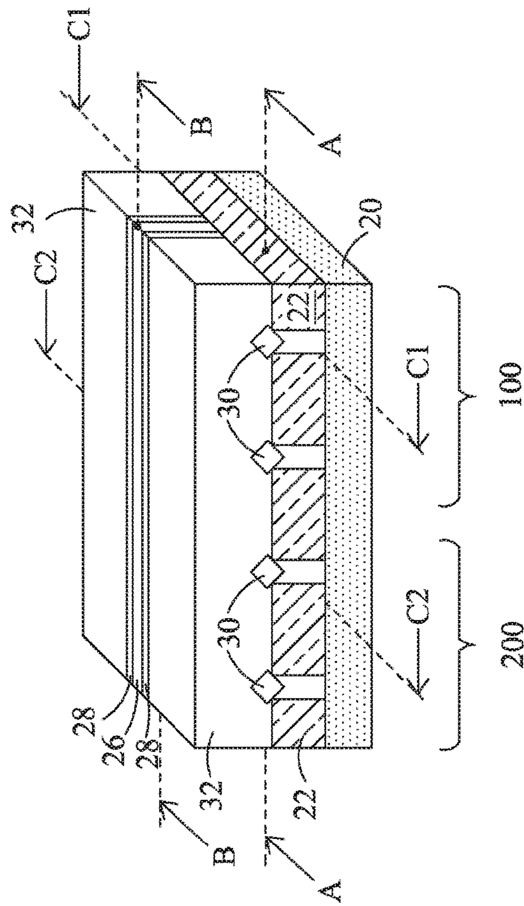


Fig. 7A

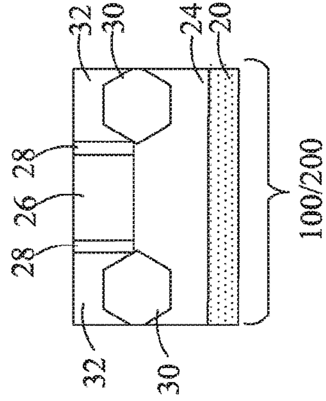


Fig. 7D

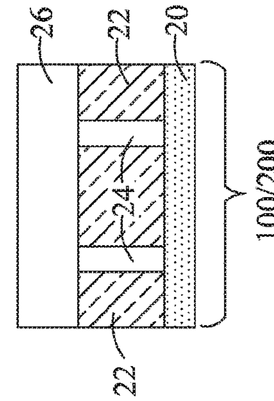


Fig. 7C

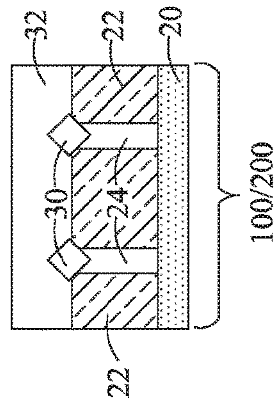


Fig. 7B

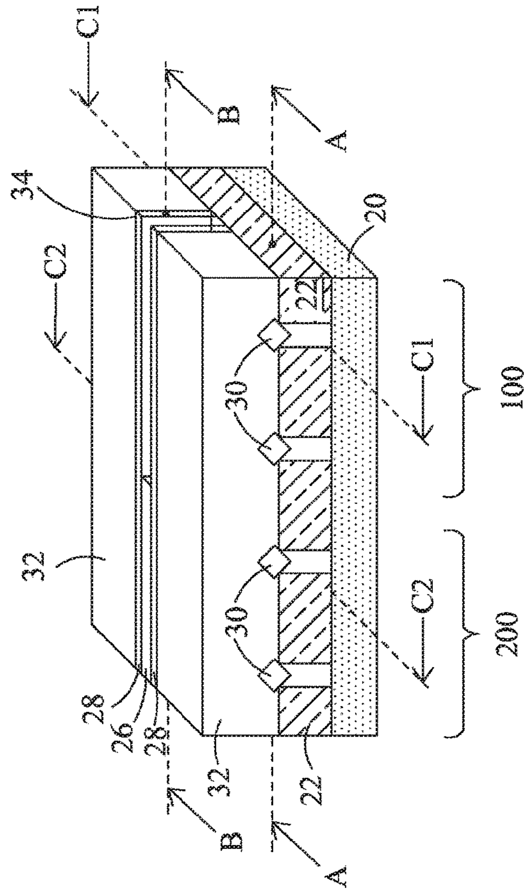


Fig. 8A

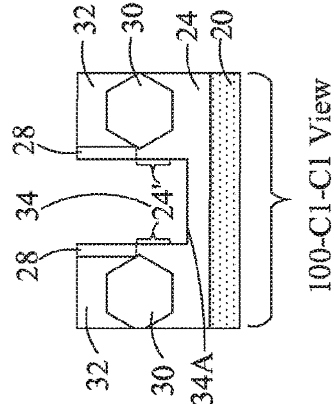


Fig. 8D

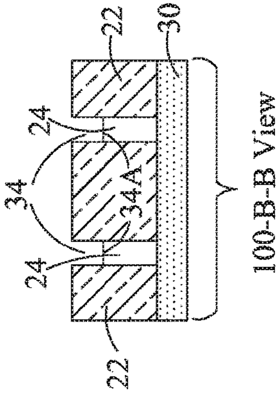


Fig. 8C

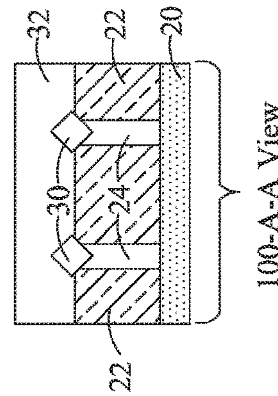


Fig. 8B

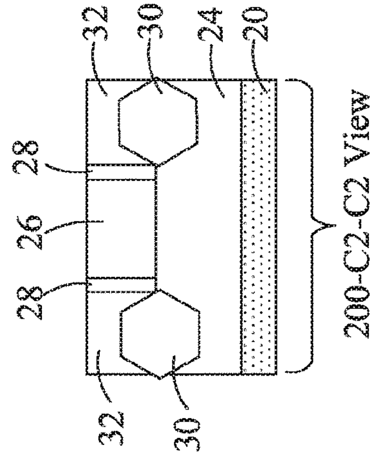


Fig. 8G

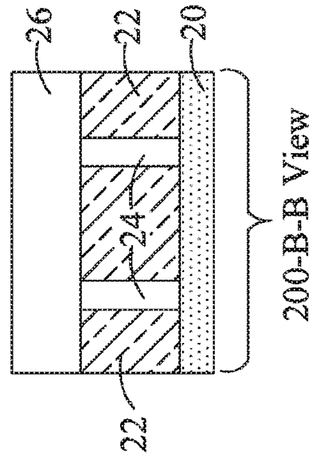


Fig. 8F

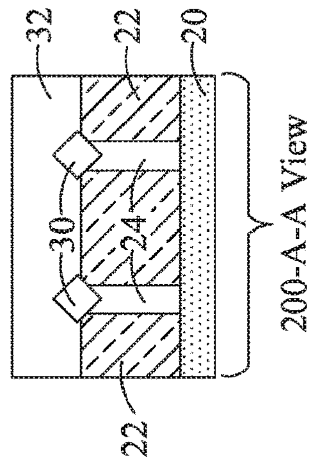


Fig. 8E

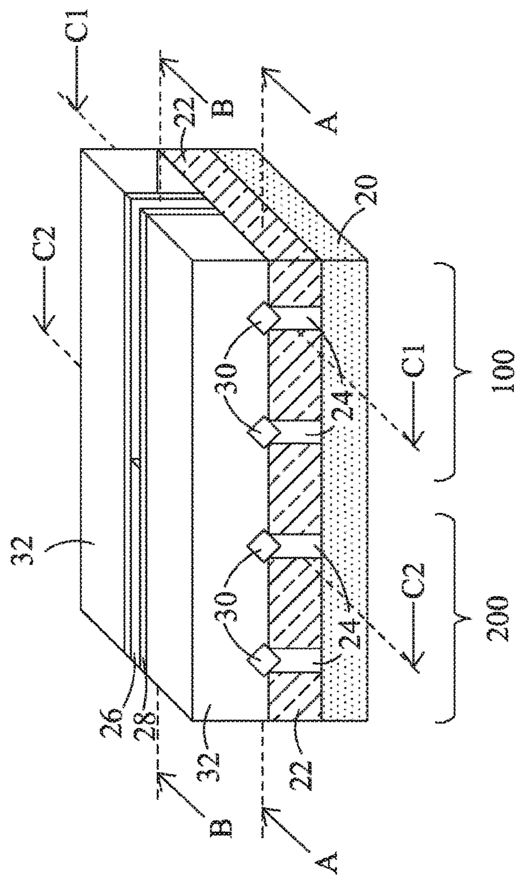


Fig. 9A

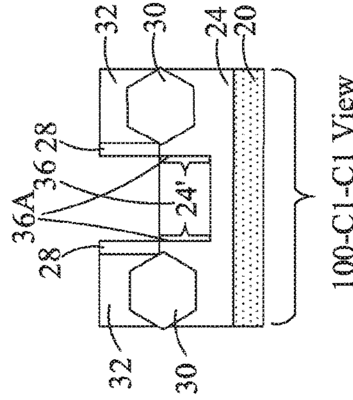


Fig. 9D

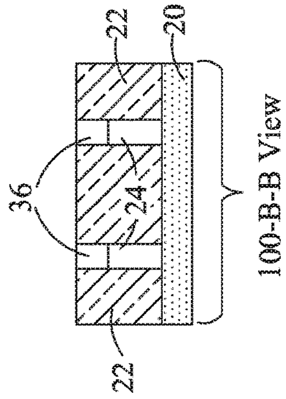


Fig. 9C

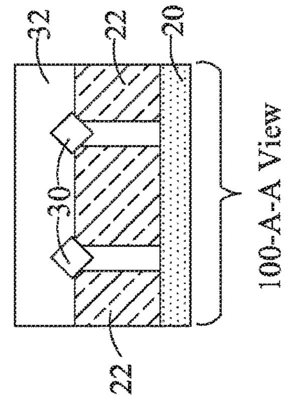


Fig. 9B

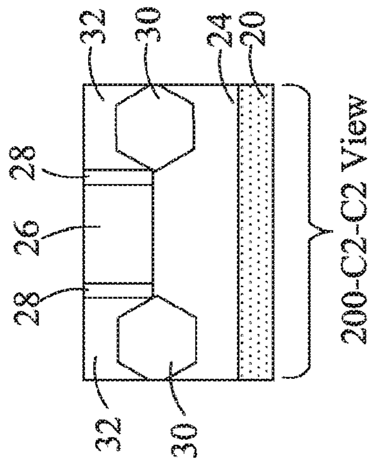


Fig. 9G

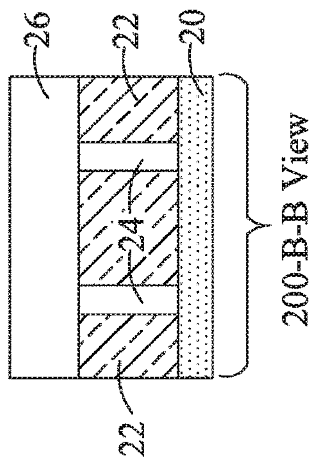


Fig. 9F

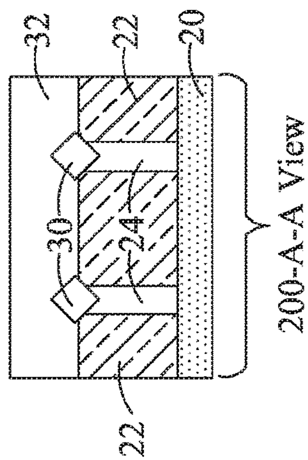


Fig. 9E

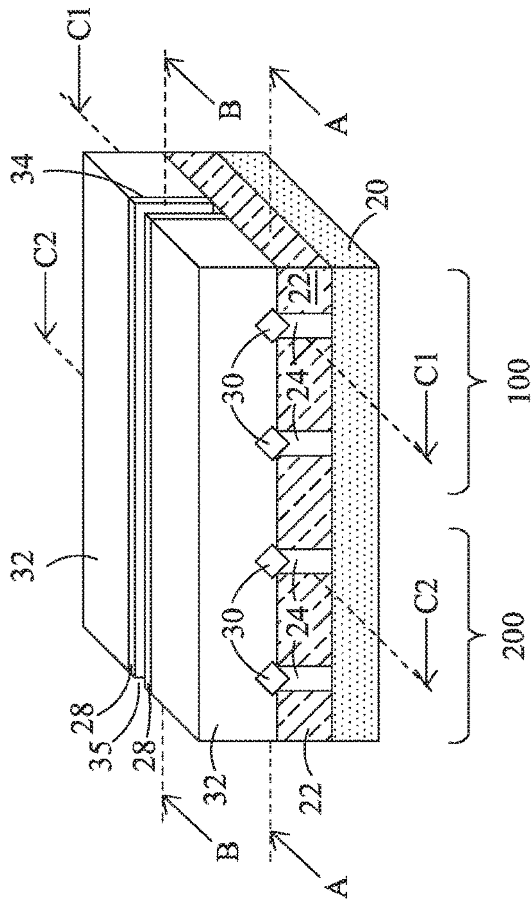


Fig. 10A

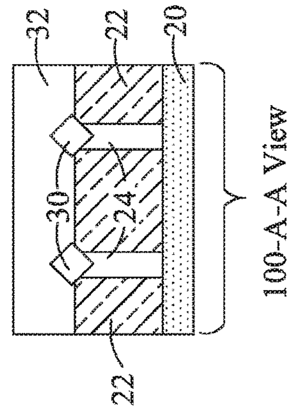


Fig. 10B

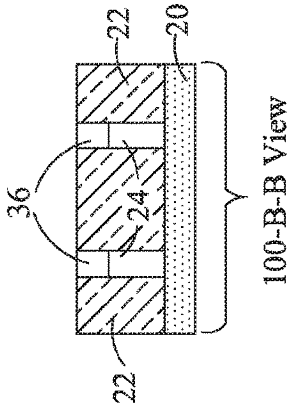


Fig. 10C

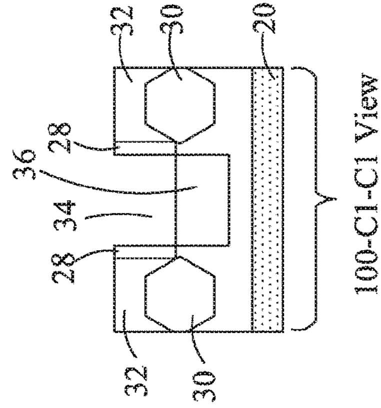


Fig. 10D

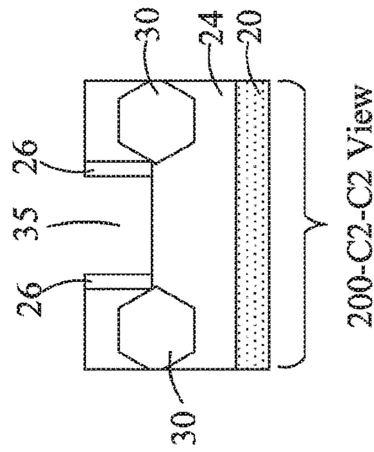


Fig. 10G

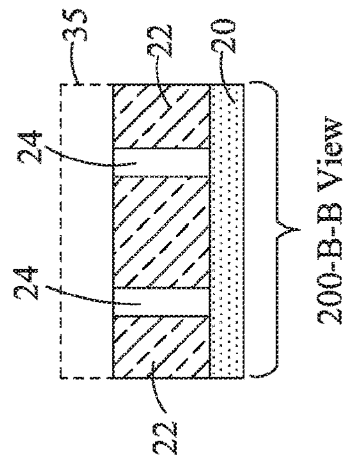


Fig. 10F

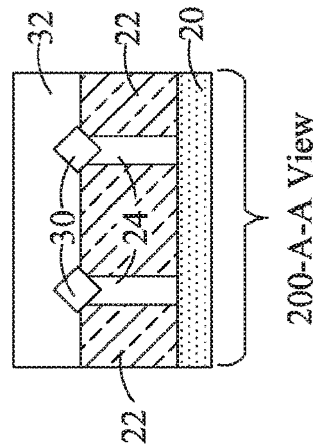


Fig. 10E

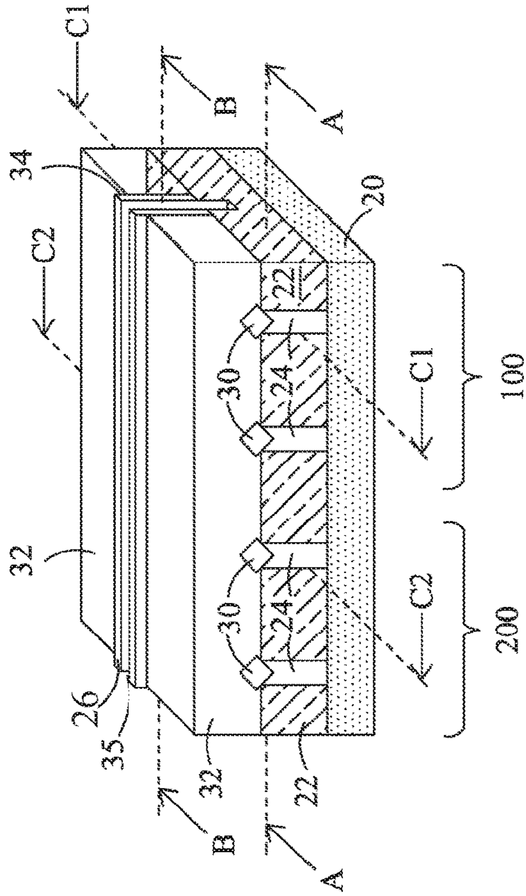


Fig. 11A

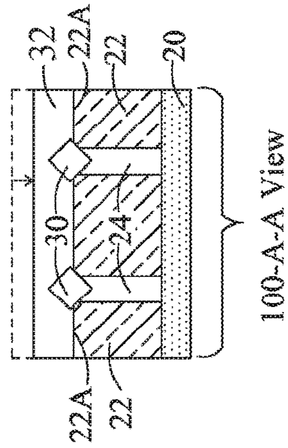


Fig. 11B

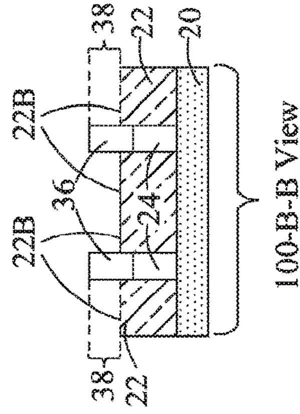


Fig. 11C

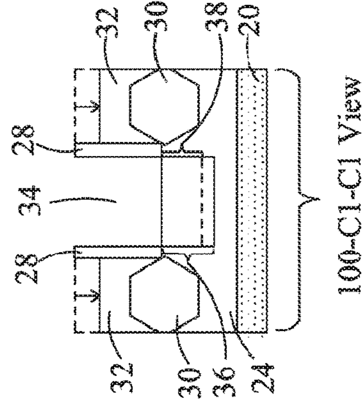


Fig. 11D

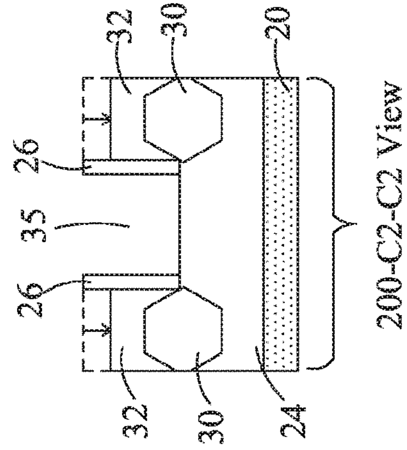


Fig. 11G

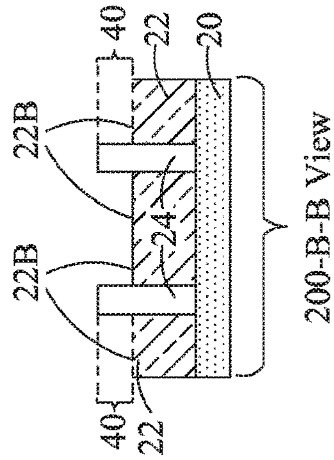


Fig. 11F

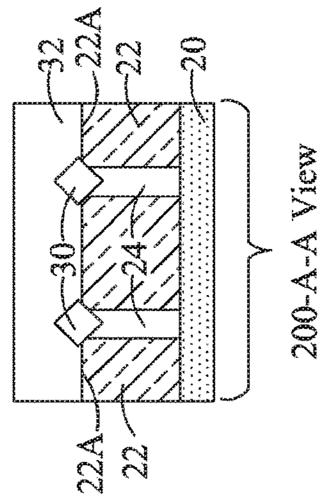


Fig. 11E

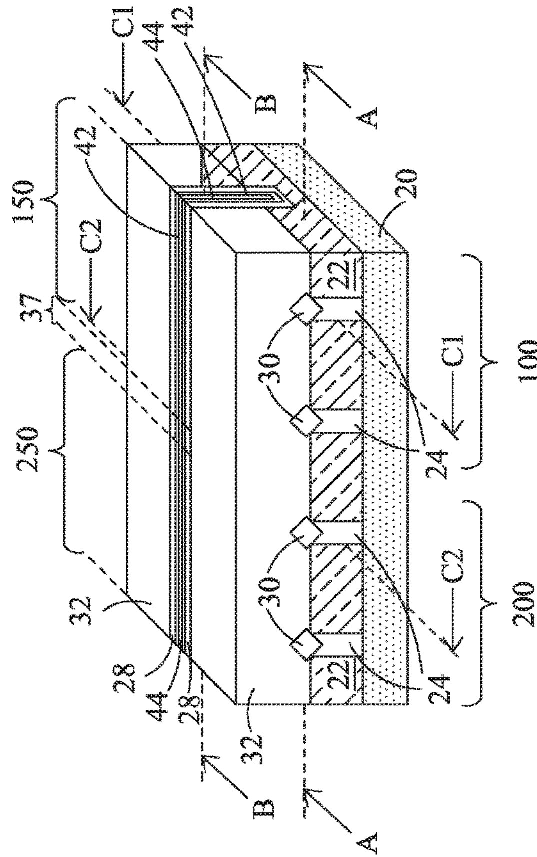


Fig. 12A

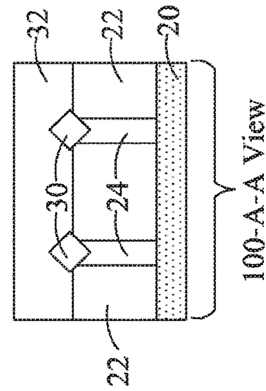


Fig. 12B

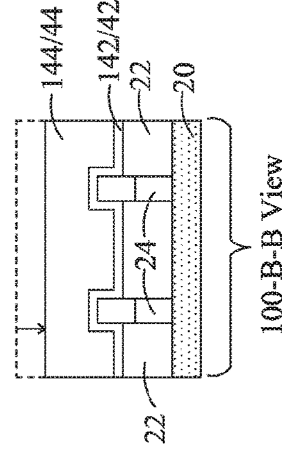


Fig. 12C

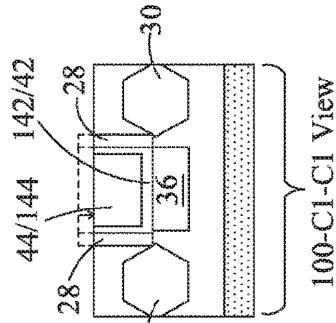
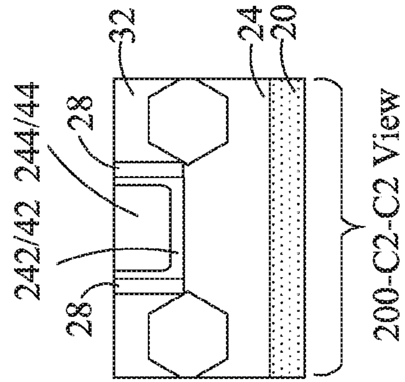


Fig. 12D



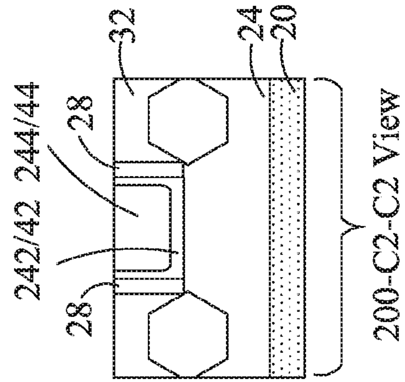


Fig. 12G

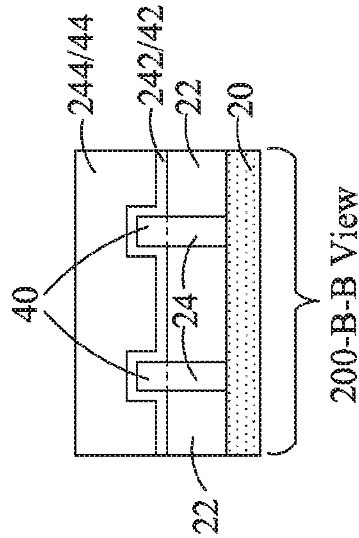


Fig. 12F

Fig. 12E

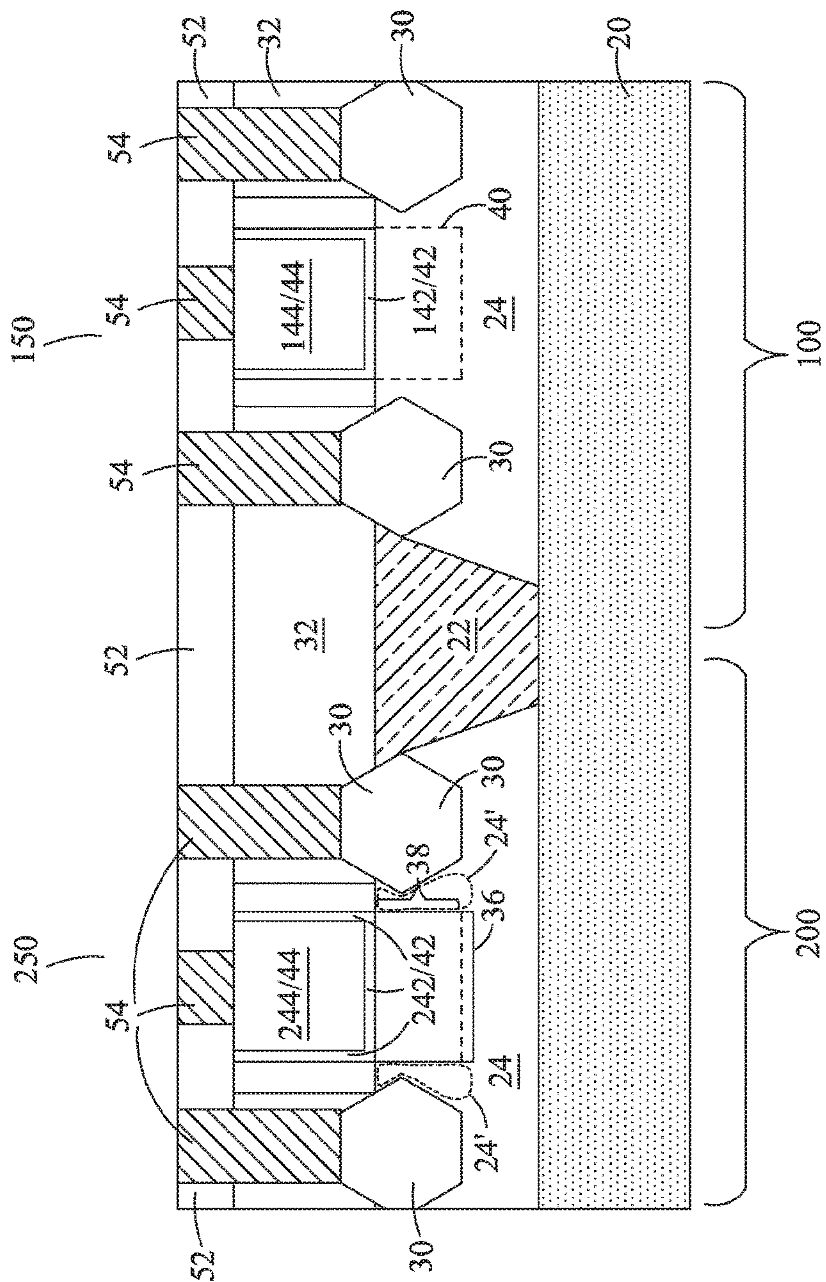


Fig. 13

MULTI-GATE DEVICES WITH REPLACED-CHANNELS AND METHODS FOR FORMING THE SAME

[0001] This application is a continuation application of patent application Ser. No. 14/887,102, entitled "Multi-Gate Devices with Replaced-Channels and Methods for Forming the Same," filed on Oct. 19, 2015, which is a divisional application of patent application Ser. No. 13/457,258, entitled "Multi-Gate Devices with Replaced-Channels and Methods for Forming the Same," filed on Apr. 26, 2012, now U.S. Pat. No. 9,171,925, each application is incorporated herein by reference.

CROSS-REFERENCE TO RELATED APPLICATION

[0002] This application relates to the following commonly-assigned co-pending U.S. patent application: application Ser. No. 13/356,769, filed Jan. 24, 2012, and entitled "FinFETs and Methods for Forming the Same;" which application is hereby incorporated herein by reference.

BACKGROUND

[0003] With the increasing down-scaling of integrated circuits and increasingly demanding requirements to the speed of integrated circuits, transistors need to have higher drive currents with smaller dimensions. Fin Field-Effect Transistors (FinFETs) were thus developed. FinFETs have increased channel widths. The increase in the channel widths is achieved by forming channels that include portions on the sidewalls of semiconductor fins and portions on the top surfaces of the semiconductor fins. Since the drive currents of transistors are proportional to the channel widths, the drive currents of the FinFETs are increased.

[0004] In an existing FinFET formation process, Shallow Trench Isolation (STI) regions are first formed in a silicon substrate. The STI regions are then recessed to form silicon fins, which comprise portions of the silicon substrate that are over the recessed STI regions. Next, a gate dielectric and a gate electrode are formed. A source and a drain region are then formed, for example, by recessing the silicon fin, and then performing an epitaxy. The epitaxy source and drain regions may have a lattice constant different from that of the respective silicon fin, and hence may provide a beneficial strain to the respective channel region of the FinFET. However, during the subsequent thermal processes, the strain may be relaxed. Furthermore, the impurities in the epitaxy source and drain regions may be adversely diffused into the channel in the subsequent thermal processes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0006] FIGS. **1** through **13** are perspective views and cross-sectional views of intermediate stages in the manufacturing of Fin Field-Effect Transistors (FinFETs) in accordance with various exemplary embodiments.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0007] The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are illustrative, and do not limit the scope of the disclosure.

[0008] Fin Field-Effect Transistors (FinFETs) and the methods of forming the same are provided in accordance with various embodiments. The intermediate stages of forming the FinFETs are illustrated. The variations of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0009] FIGS. **1** through **13** are cross-sectional views and perspective views of intermediate stages in the manufacturing of Fin Field-Effect Transistors (FinFETs) in accordance with some exemplary embodiments. FIG. **1** illustrates a perspective view of an initial structure. The initial structure includes substrate **20**. Substrate **20** may be semiconductor substrate, which may further be a silicon substrate, a silicon germanium substrate, or a substrate formed of other semiconductor materials. Substrate **20** may be doped with a p-type or an n-type impurity. Isolation regions such as Shallow Trench Isolation (STI) regions **22** may be formed to extend from a top surface of substrate **20** into substrate **20**. Substrate **20** includes a first portion in device region **100** and a second portion in device region **200**. In some embodiments, one of the device regions **100** and **200** is a p-type FinFET region, and the other device region is an n-type FinFET region. The portions of substrate **20** between neighboring STI regions **22** form semiconductor strips **21**. The top surfaces of semiconductor strips **21** and the top surfaces of STI regions **22** may be substantially level with each other.

[0010] Referring to FIG. **2**, at least upper portions, or substantially entireties, of semiconductor strips **21** are removed. Accordingly, recesses **23** are formed in STI regions **22**. Next, as shown in FIG. **3**, an epitaxy is performed to epitaxially grow semiconductor strips **24** in recesses **23**. Semiconductor strips **24** may have a lattice constant greater than, substantially equal to, or smaller than, the lattice constant of substrate **20**. In some embodiments, Semiconductor strips **24** comprise silicon germanium, silicon carbon, a III-V compound semiconductor, or the like. The top surface of the resulting semiconductor strips **24** may be higher than, level with, or lower than the top surface of STI regions **22**.

[0011] In some embodiments, the process steps in FIGS. **2** and **3** are omitted, and semiconductor strips **21** remain. Accordingly, semiconductor strips **24** that are illustrated in subsequent drawings are actually semiconductor strips **21**, which may be formed of a same semiconductor material as substrate **20**.

[0012] Referring to FIG. **4**, dummy gate **26** is formed. Dummy gate **26** may be formed of, for example, polysilicon, although other materials that have a high etching selectivity from STI regions **22** may also be used. Dummy gate **26** is over portions of semiconductor strips **24**, and may crossover a plurality of semiconductor strips **24** and/or STI regions **22**. Dummy gate **26** may also have a lengthwise direction substantially perpendicular to the lengthwise direction of semiconductor strips **24**. Dummy gate **26** may include a portion in device region **100** and a portion in device region **200**.

[0013] Next, as also shown in FIG. **4**, gate spacers **28** are formed on the sidewalls of dummy gate **26**. In some embodi-

ments, gate spacers **28** comprise silicon oxide, silicon nitride, and the like, and may have a multi-layer structure.

[0014] Referring to FIG. **5**, an etching step is performed to etch portions of semiconductor strips **24** that are not covered by dummy gate **26** and gate spacers **28**. The resulting top surfaces **24**A of the recessed semiconductor strips **24** is thus lower than the top surfaces **22**A of STI regions **22**. Recesses **25** are accordingly formed between STI regions **22**. Recesses **25** are located on opposite sides of dummy gate **26**. Next, as shown in FIG. **6**, epitaxy regions **30** are formed by selectively growing a semiconductor material in recesses **25**. In some exemplary embodiments, epitaxy regions **30** comprise silicon germanium or silicon carbon. Alternatively, epitaxy regions **30** are formed of silicon, III-V semiconductor materials, or the like. After recesses **25** are filled with epitaxy regions **30**, the further epitaxial growth of epitaxy regions **30** causes epitaxy regions **30** to expand horizontally, and facets start to form. Furthermore, some of top surfaces **22**A of STI regions **22** are underlying and aligned to portions of epitaxy regions **30** due to the lateral growth of epitaxy regions **30**. Alternatively, no recess of semiconductor strips **24** is performed, and epitaxy regions **30** are formed on the un-recessed semiconductor strips **24**.

[0015] After the epitaxy step, epitaxy regions **30** may be implanted to form source and drain regions, which are also denoted using reference numeral **30**. Source and drain regions **30** are on opposite sides of dummy gate **26**, and may be overlying and overlapping portions of surfaces **22**A of STI regions **22**. When device regions **100** and **200** include an n-type FinFET region and a p-type FinFET region, the source/drain regions **30** in device regions **100** and **200** have opposite conductivity types. Following the formation of source and drain regions **30**, source and drain silicide regions (not shown) may be formed by siliciding the top portions of source and drain regions **30**. Alternatively, the source and drain silicide regions may be formed in the step shown in FIG. **13**.

[0016] FIG. **7**A illustrates a perspective view of the structure after Inter-Layer Dielectric (ILD) **32** is formed. A Chemical Mechanical Polish (CMP) may be performed to level the top surfaces of ILD **32**, dummy gate **26**, and gate spacers **28**. FIG. **7**B illustrates a cross-sectional view obtained from the plane crossing line A-A in FIG. **7**A. FIG. **7**C illustrates a cross-sectional view obtained from the plane crossing line B-B in FIG. **7**A. FIG. **7**D illustrates a cross-sectional view obtained from the plane crossing line C**1**-C**1** or C**2**-C**2** in FIG. **7**A. The exemplary locations of regions **22**, **24**, **30**, and **32** are also illustrated in the cross-sectional views.

[0017] FIGS. **8**A through **12**G illustrate the perspective views and the respective cross-sectional views in the further manufacturing steps of the FinFETs. Throughout FIGS. **8**A through **12**G, each of the Figures is marked with a number followed by a letter. The Figures with the same number are different views of a same process step and a same structure. In each of the cross-sectional views, the respective device region and the plane, from which the respective cross-sectional view is retrieved, are marked. For example, in FIG. **8**B, "**100**—A-A View" is marked, indicating that the cross-sectional view is obtained from device region **100**, and from the plane crossing line A-A in FIG. **8**A.

[0018] Referring to FIG. **8**A, the portion of dummy gate **26** in device region **100** is removed, for example, through etching. The portion of dummy gate **26** in device region **200**, however, remains not removed. FIGS. **8**B through **8**G are different views of the structure shown in FIG. **8**A, wherein the removal of dummy gate **26** is illustrated in FIGS. **8**C and **8**D, and may be observed by comparing to FIGS. **7**C and **7**D, respectively. As shown in FIG. **8**D, the removed portion of dummy gate **26** is at substantially a same level as gate spacers **28**.

[0019] Referring to FIG. **8**A, the removal of dummy gate **26** may be performed by forming a photo resist (not shown) to protect device region **200**, and then etching dummy gate **26**. Next, as shown in FIGS. **8**C and **8**D, the exposed semiconductor strips **24** are recessed, forming recesses **34** in STI regions **22**. The recessing may comprise an anisotropic etching using gate spacers **28** as an etching mask, so that the sidewalls of recesses **34** are substantially vertical, and are substantially aligned to the edges of gate spacers **28**. Bottoms **34**A of recesses **34** may be higher than the bottom surfaces of semiconductor strips **24**, and may be substantially level with, or slightly higher than, the bottoms of source/drain regions **30** (FIG. **8**D). In some embodiments, as shown in FIG. **8**D, semiconductor strips **24** may have portions **24'** left unetched, with portions **24'** having side edges exposed to recess **34**. In FIGS. **8**E, **8**F, and **8**G, which are the views of device region **200**, however, dummy gate **26** and semiconductor strips **24** are not recessed.

[0020] FIGS. **9**A through **9**D illustrate a perspective view and cross-sectional views in the formation of epitaxy semiconductor regions **36** (FIGS. **9**C and **9**D), which is formed by selective epitaxial growth. Epitaxy semiconductor regions **36** are grown from semiconductor strips **24**, and are not grown on STI regions **22**. As shown in FIG. **9**D, epitaxy semiconductor regions **36** may have edges **36**A (which are also the edges of portions **24'**) substantially aligned to the edges of gate spacers **28**. It is appreciated that since epitaxy regions **36** and semiconductor strips **24** are formed in different process steps, there are visible and distinguishable interfaces (also shown as **36**A) between epitaxy regions **36** and semiconductor strips **24**. FIGS. **9**E, **9**F, and **9**D illustrate the same process step. It is observed that when epitaxy semiconductor regions **36** are grown in device region **100**, epitaxy semiconductor regions **36** are not grown in device region **200**.

[0021] In some embodiments, epitaxy semiconductor regions **36** have a lattice constant greater than, substantially equal to, or smaller than, the lattice constant of semiconductor strips **24**. For example, epitaxy semiconductor regions **36** may comprise silicon germanium, silicon carbon, III-V compound semiconductors, or the like. Furthermore, epitaxy semiconductor regions **36** and semiconductor strips **24** may include same elements that have different percentages. In some exemplary embodiments, epitaxy semiconductor regions **36** and semiconductor substrate **24** both comprise silicon germanium, and have different germanium percentages. The desirable material of epitaxy regions **36** are selected according to the desirable stress in the channel region of the FinFET in device region **100**.

[0022] FIG. **10**A and FIGS. **10**B through **10**G illustrate a perspective view and cross-sectional views in the removal of dummy gate **26** from device region **200**. As shown in FIGS. **10**F and **10**G, dummy gate **26** is removed to form recess **35** in device region **200** and between gate spacers **28**, and the underlying semiconductor strips **24** are exposed. The cross-sectional view shown in FIGS. **10**B, **10**C, and **10**D remain the same as in FIGS. **9**B, **9**C, and **9**D, respectively.

[0023] Next, referring to FIGS. **11**A through **11**G, in both device regions **100** and **200**, an etching is performed to etch the portions of STI regions **22** underlying the removed dummy gate **26**, so that epitaxy regions **36** (FIG. **11**C) in device region **100** and semiconductor strips **24** (FIG. **11**F) in device region **200** protrude over the respective adjoining STI regions **22**. Throughout the description, the protruding portions of epitaxy regions **36** are referred to as semiconductor fins **38**, and the protruding portions of semiconductor strips **24** are referred to as semiconductor fins **40**. As a result of the etching, as shown in FIGS. **11**B and **11**E, some portions of STI regions **22** are not etched, and have top surfaces **22**A, while portions of STI regions **22** that were previously underlying dummy gate **26** are recessed to have top surfaces **22**B (FIGS. **11**C and **11**F). Top surfaces **22**B are lower than top surfaces **22**A by the height of semiconductor fins **38** and **40**. Furthermore, top surfaces **22**A may be substantially level with the top surfaces of semiconductor fins **38** and **40**.

[0024] As shown in FIGS. **11**D and **11**G, at the time STI regions **22** are recessed, ILD **32** may also be recessed as a side effect. The recess of ILD **32** is shown by arrows. As a result of the etching of ILD **32**, the top surface of ILD **32** may be lower than the top surface of gate spacers **28**.

[0025] FIGS. **12**A through **12**G illustrate the formation of gate dielectrics **42** (including **142** and **242**) and gate electrodes **44** (including **144** and **244**). To form gate dielectrics **42** and gate electrodes **44**, first, a gate dielectric layer is formed in recess **34** and **35** (FIG. **11**A) and on the top surfaces and the sidewalls of semiconductor fins **38** and **40** (FIGS. **12**C, **12**D, **12**F, and **12**G). In accordance with some embodiments, the gate dielectric layer comprises silicon oxide, silicon nitride, or multilayers thereof. In alternative embodiments, the gate dielectric layer comprises a high-k dielectric material, and hence are high-k gate dielectrics. The high-k gate dielectric layer may have a k value greater than about 7.0, and may include a metal oxide or a silicate of Hf, Al, Zr, La, Mg, Ba, Ti, Pb, and combinations thereof. The formation methods of the gate dielectric layer may include Molecular-Beam Deposition (MBD), Atomic Layer Deposition (ALD), Physical Vapor Deposition (PVD), and the like.

[0026] Next, a conductive material, which is used to form gate electrodes **44**, is formed over the gate dielectric layer, and fills the remaining recesses **34** and **35** (FIG. **11**A). After the filling of the conductive material, a CMP may be performed to remove the excess portions of the gate dielectric layer and the conductive material over the top surface of ILD **32**. In the CMP, portions of gate spacers **28** are also polished, as illustrated by the arrow in FIG. **12**D, and the top surfaces of gate spacers **28**, ILD **32**, gate dielectrics **42**, and gate electrodes **44** are level with each other. Gate electrodes **44** may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof, and multilayers thereof.

[0027] A patterning step may further be performed to remove the portions of the gate dielectric layer and the conductive material in region **37** (FIG. **12**A). As a result, gate dielectrics **142** and **242** are separated from each other, and gate electrodes **144** and **244** are separated from each other. Accordingly, FinFETs **150** and **250** are formed in device regions **100** and **200**, respectively. FinFET **150** includes gate dielectric **142** and gate electrode **144** (FIGS. **12**C and **12**D). FinFET **250** includes gate dielectric **242** and gate electrode **244** (FIGS. **12**F and **12**G). Gate electrodes **144** and **244** are referred to replacement gates hereinafter since they are formed by replacing dummy gate **26**. Due to the replacement gate formation, gate dielectrics **142** and **242** have top edges level with the top surfaces of gate electrodes **144** and **244**.

[0028] FIG. **13** schematically illustrates cross-sectional views of FinFETs **150** and **250**. It is appreciated that the cross-sectional views of FinFETs **150** and **250** are shown as being in a same plane in FIG. **13**, although they are actually in different planes crossing lines C**1**-C**1** and C**2**-C**2**, respectively, in FIG. **12**A. In subsequent process steps, an additional ILD **52** is formed over ILD **32**, and contact plugs **54** may be formed to penetrate through ILDs **32** and **52** to electrically couple to gate electrode **44** and source/drain silicide regions (not shown). ILD **52** and ILD **32** may be formed of a same dielectric material or different dielectric materials. A visible interface may be generated between ILD **52** and ILD **32** regardless of whether they are formed of a same material or different materials.

[0029] It is observed that in the resulting FinFETs **150**, the STI regions **22** that are on opposite sides of a same gate electrode **144** (FIGS. **11**B and **11**E) have top surfaces **22**A that are higher than top surface **22**B (FIGS. **11**C and **11**F), which are underlying (and aligned to) gate electrodes **44**. This is different from the conventional FinFETs. In the conventional FinFETs, the STI regions **22** that are on the opposite sides of a gate electrodes have top surfaces that are level with the top surface of the portion of the STI region that is underlying (and aligned to) the respective gate electrode. In addition, in FIGS. **11**C and **11**F, top surfaces **22**A of STI regions **22** that are on the opposite sides of a same epitaxy source/drain region **30** are substantially level with the top surfaces of semiconductor fins **38**, as shown in FIGS. **11**C and **11**F. This is also different from the conventional FinFETs, in which the top surfaces of the STI regions that are on the opposite sides of a same epitaxy source/drain region are lower than the respective semiconductor fin of the respective FinFET.

[0030] In addition, referring to FIG. **13**, due to the formation of replacement channel **38**, which is formed by replacing the original semiconductor strips **24**, semiconductor strips **24** may include extending portions **24'** extending between semiconductor fin **38** (which also forms the channel region) and source/drain regions **30**, wherein portions **24'** are formed of a material different from the materials of both semiconductor fin **38** and source/drain region **30**.

[0031] Further referring to FIG. **13**, each of FinFETs **150** and **250** may be a p-type FinFET or an n-type FinFET. The respective materials of semiconductor strips **24** and semiconductor regions **36** are selected to generate desirable strains for the respective FinFETs **150** and **250**. For example, for a p-type FinFET, a compressive stress is generated in the respective channel region (the fins **38** or **40** in FIGS. **11**C and **11**F, respectively). For an n-type FinFET, a tensile strain is generated in the respective channel regions **38** or **40**. In some exemplary embodiments, FinFET **150** is a p-type FinFET, and semiconductor strips **24** may comprise silicon, germanium, silicon germanium, III-V compound semiconductor materials, or the like. FinFET **250** is an n-type FinFET, and semiconductor region **36** may comprise silicon, silicon germanium, germanium, III-V compound semiconductor, or the like.

[0032] In accordance with embodiments, a device includes a semiconductor substrate, isolation regions in the semicon-

ductor substrate, and a FinFET. The FinFET includes a channel region over the semiconductor substrate, a gate dielectric on a top surface and sidewalls of the channel region, a gate electrode over the gate dielectric, a source/drain region, and an additional semiconductor region between the source/drain region and the channel region. The channel region and the additional semiconductor region are formed of different semiconductor materials, and are at substantially level with each other.

[0033] In accordance with other embodiments, a device includes a semiconductor substrate, isolation regions in the semiconductor substrate, and a FinFET. The FinFET includes a semiconductor strip, wherein opposite edges of the semiconductor strip are in contact with opposite sidewalls of the isolation strips, and a semiconductor channel over top surfaces of the isolation regions and overlapping a first portion of the semiconductor strip. The semiconductor channel and the semiconductor strip include different materials. A source/drain region is disposed adjacent the semiconductor channel. The semiconductor strip further includes a second portion extending between the semiconductor channel and the source/drain region, and wherein the second portion has an edge contacting an edge of the semiconductor channel.

[0034] In accordance with yet other embodiments, a method includes forming isolation regions extending from a top surface of a semiconductor substrate into the semiconductor substrate, wherein the isolation regions have a first top surface, and wherein a portion of the semiconductor substrate between two neighboring ones of the isolation regions forms a semiconductor strip. The method further includes forming a dummy gate over the semiconductor strip and the isolation regions, removing the dummy gate, etching a portion of the semiconductor strip under the dummy gate to form a first recess in the semiconductor strip, and performing an epitaxy to grow an epitaxy semiconductor region in the first recess. A portion of the isolation regions under the dummy gate is recessed to form a second recess, wherein a recessed portion of the isolation regions has a second top surface lower than the first top surface. A portion of the epitaxy semiconductor region exposed through the recess forms a semiconductor fin that is over the second top surface of the isolation regions.

[0035] In accordance with yet other embodiments, a method includes forming a first fin, a second fin, and a first dielectric layer along sidewalls of the first fin and the second fin, and forming a dummy gate over the first fin, the second fin, and the first dielectric layer. A first semiconductor material is epitaxially grown over the first fin and the second fin on opposing sides of the dummy gate, and a second dielectric layer is formed over the first semiconductor material. A first portion of the dummy gate is removed to expose a first channel region of the first fin and a first portion of the first dielectric layer, and a second semiconductor material is epitaxially grown over the first fin in the first channel region. The first portion of the first dielectric layer is recessed, and a gate electrode is formed over the first fin.

[0036] In accordance with yet other embodiments, a method includes forming isolation regions extending from a top surface of a semiconductor substrate into the semiconductor substrate, wherein the isolation regions have a first top surface, and wherein a portion of the semiconductor substrate between two neighboring ones of the isolation regions forms a semiconductor strip, and forming a dummy gate over the semiconductor strip and the isolation regions. A dielectric layer is formed over the semiconductor strip and along sidewalls of the dummy gate, and the dummy gate is removed, thereby exposing an exposed portion of the semiconductor strip and an exposed portion of the isolation regions. Etching is performed on the exposed portion of the semiconductor strip to form a first recess in the semiconductor strip, and an epitaxy process is used to grow an epitaxy semiconductor region in the first recess. The exposed portion of the isolation regions is recessed to form a second recess, wherein a recessed portion of the isolation regions has a second top surface lower than the first top surface, and wherein a portion of the epitaxy semiconductor region exposed through the second recess forms a semiconductor fin extending above the second top surface of the isolation regions.

[0037] In accordance with yet other embodiments, a method includes forming trenches in a first dielectric layer over a substrate, forming a first semiconductor layer in the trenches to form a plurality of fins, and forming a dummy gate extending over the fins. The fins are recessed on opposing sides of the dummy gate, and a second semiconductor layer is formed over the fins on opposing sides of the dummy gate. A second dielectric layer is formed over the second semiconductor layer on opposing sides of the dummy gate, and a first portion of the dummy gate is removed over one or more first fins of the plurality of fins to expose one or more first channel regions and a first portion of the first dielectric layer, and the first channel regions are recessed. A third semiconductor layer is formed in the first channel regions, and a gate electrode is formed over the one or more first fins.

[0038] Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A device comprising:

a semiconductor substrate, the semiconductor substrate comprising a first semiconductor material;

a first epitaxial region and a second epitaxial region in semiconductor substrate, the first epitaxial region and the second epitaxial region comprising a second semiconductor material different than the first semiconductor material;

a third epitaxial region interposed between the first epitaxial region and the second epitaxial region, the third epitaxial region comprising a third semiconductor material different than the first semiconductor material and the second semiconductor material; and

a gate electrode over the third epitaxial region.

2. The device of claim **1**, wherein the first semiconductor material is interposed between the second semiconductor material and the third semiconductor material.

3. The device of claim **2**, wherein the first semiconductor material completely separates the second semiconductor material and the third semiconductor material.

4. The device of claim **1**, further comprising a gate dielectric interposed between the gate electrode and the third epitaxial region, wherein the third semiconductor material in the third epitaxial region is completely contained within lateral boundaries of the gate dielectric.

5. The device of claim **4**, wherein the gate dielectric completely covers the third epitaxial region in a direction orthogonal to a direction of current flow between the first epitaxial region and the second epitaxial region.

6. The device of claim **1**, wherein the first epitaxial region and the second epitaxial region extend higher than the third epitaxial region.

7. The device of claim **1**, further comprising a first spacer and a second spacer on opposing sides of the gate electrode, wherein the first epitaxial region extends under the first spacer and the second epitaxial region extends under the second spacer.

8. A device comprising:

a first semiconductor material;

a second semiconductor material extending into the first semiconductor material, the second semiconductor material having a different lattice structure than the first semiconductor material;

a first source/drain region in the second semiconductor material;

a third semiconductor material extending into the first semiconductor material, the third semiconductor material having a different lattice structure than the first semiconductor material; and

a gate electrode over the third semiconductor material.

9. The device of claim **8**, wherein the second semiconductor material does not share an interface with the third semiconductor material.

10. The device of claim **8**, further comprising an inter-layer dielectric along opposing sides of the first semiconductor material.

11. The device of claim **10**, wherein the third semiconductor material extends lower than an uppermost surface of the inter-layer dielectric.

12. The device of claim **10**, wherein an upper surface of the inter-layer dielectric adjacent the gate electrode is higher than an upper surface of the inter-layer dielectric directly below the gate electrode.

13. The device of claim **8**, wherein the first semiconductor material extends to an uppermost surface of the third semiconductor material.

14. The device of claim **8**, further comprising an inter-layer dielectric on opposing sides of the gate electrode, wherein an upper surface of the inter-layer dielectric is level with an upper surface of the gate electrode.

15. A device comprising:

a first semiconductor material;

a second semiconductor material adjacent the first semiconductor material, the second semiconductor material having a different lattice structure than the first semiconductor material;

a first source/drain region in the second semiconductor material;

a third semiconductor material adjacent the first semiconductor material, the third semiconductor material having a different lattice structure than the first semiconductor material, wherein the first semiconductor material extends between the second semiconductor material and the third semiconductor material; and

a gate electrode over the third semiconductor material.

16. The device of claim **15**, wherein the third semiconductor material extends to an uppermost surface of the first semiconductor material.

17. The device of claim **15**, wherein the third semiconductor material does not contact the second semiconductor material.

18. The device of claim **15**, further comprising a gate dielectric interposed between the gate electrode and the third semiconductor material, the gate dielectric extending over a first inter-layer dielectric, the gate dielectric extending lower than an uppermost surface of the first inter-layer dielectric.

19. The device of claim **15**, wherein the third semiconductor material comprises a first channel region of a first transistor, further comprising a second transistor having a second channel region, wherein the second channel region comprises the first semiconductor material.

20. The device of claim **19**, wherein the gate electrode extends over the third semiconductor material in the first channel region of the first transistor and extends over the first semiconductor material in the second channel region of the second transistor.

* * * * *