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(54) **SENSOR APPARATUS**

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(57) **ABSTRACT**

The present invention relates to a sensor apparatus having a structure capable of obtaining digital values of signal components with a high accuracy using an A/D conversing circuit with the outputted digital value thereof having a small number of expressive bits. In the sensor apparatus, a voltage value corresponding to the amount of incident light to a photodiode is held by a holding circuit through an integrating circuit and a CDS circuit. Meanwhile, a voltage value corresponding to the amount of incident light to an adjacent photodiode is held by another holding circuit through an integrating circuit and a CDS circuit. The voltage values held by the respective different holding circuits are inputted to a subtracting circuit through different paths. The subtracting circuit outputs a voltage value corresponding to the difference between the two inputted voltage values. In an A/D converting section, the difference voltage outputted from the subtracting circuit is converted into a digital value.

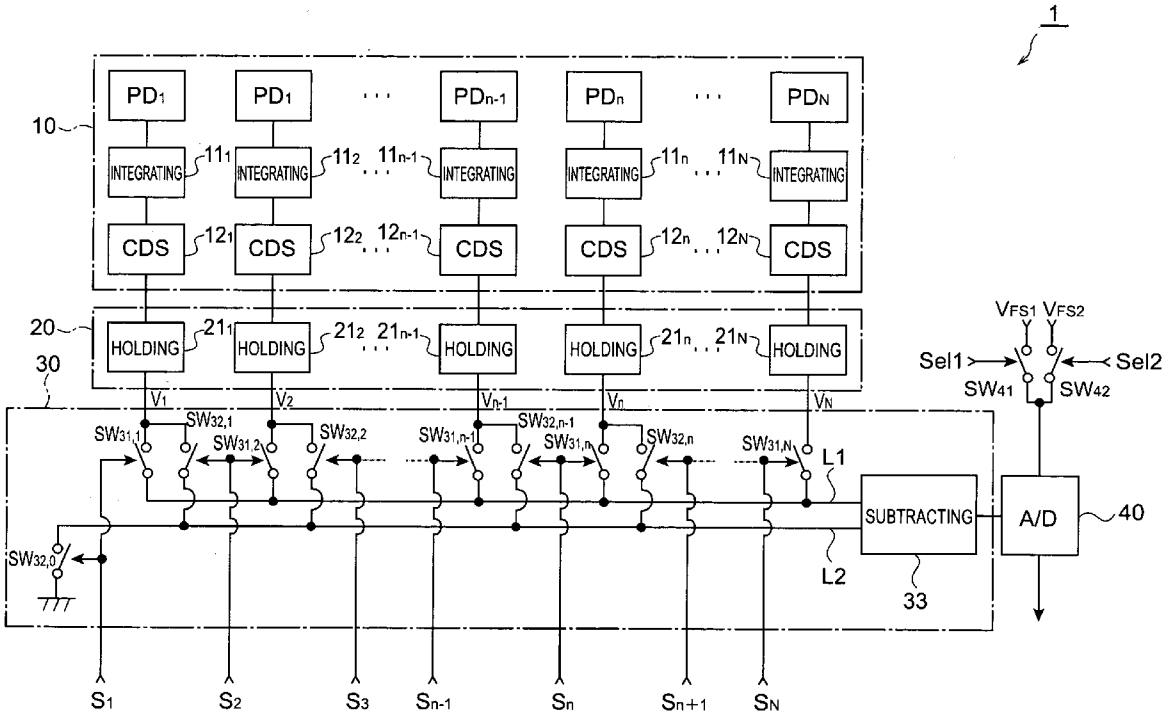
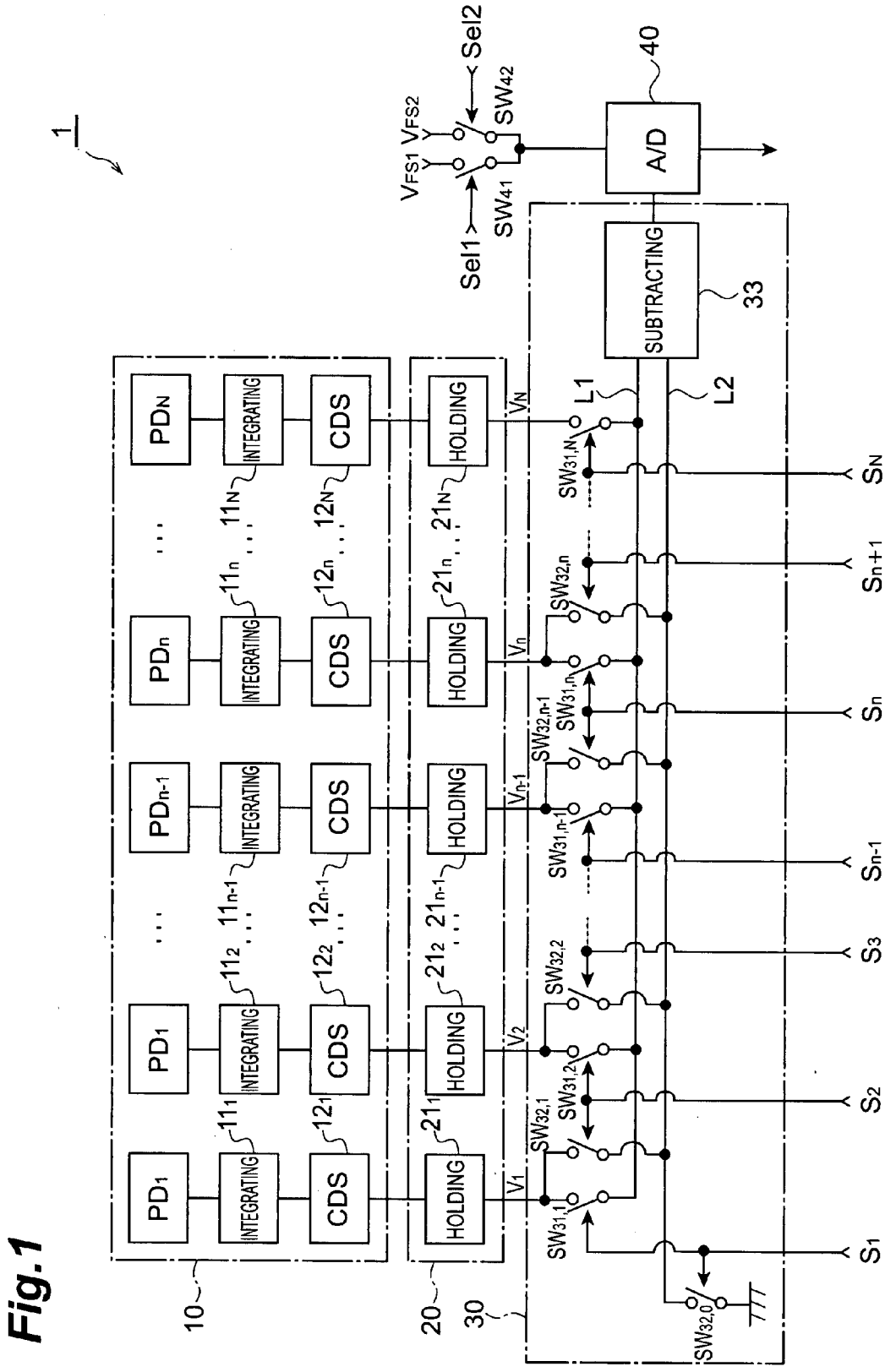


Fig.1


1
10
20
30
PD1
PDn-1
PDn
PDN
INTEGRATING
CDS
HOLDING
A/D
SUBTRACTING
33
40
L1
L2
Sel1
Sel2
VFS1
VFS2
SW41
SW42
V1
V2
Vn-1
Vn
VN
S1
S2
S3
Sn-1
Sn
Sn+1
SN

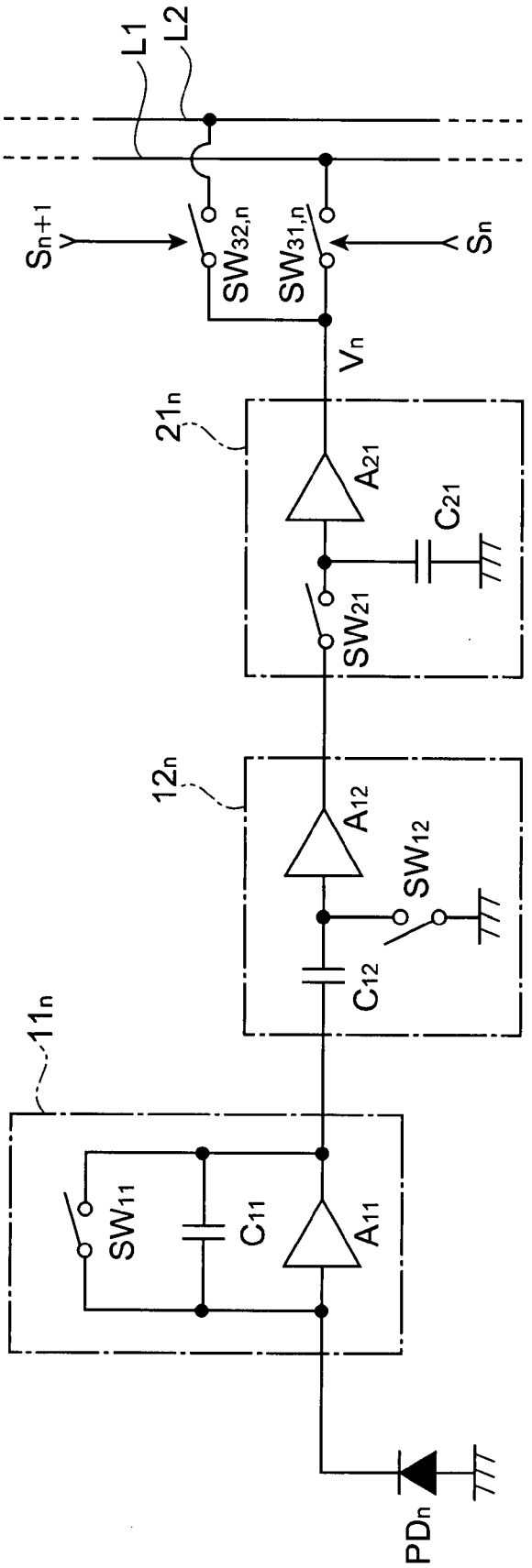

L1
L2
Sn+1
SW32,n
SW31,n
Sn
Vn
21n
A21
C21
SW21
12n
A12
SW12
C12
11n
SW11
C11
A11
PDn

Fig.2

Fig.3

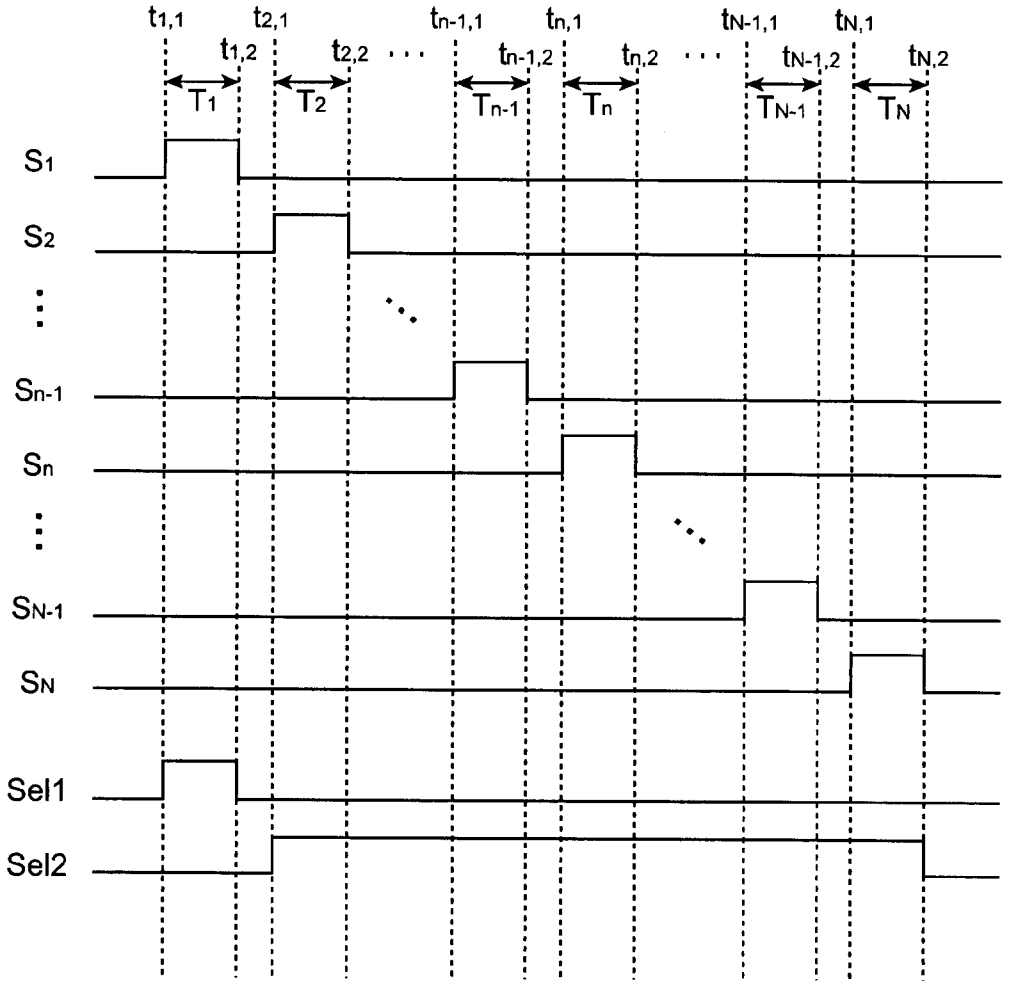
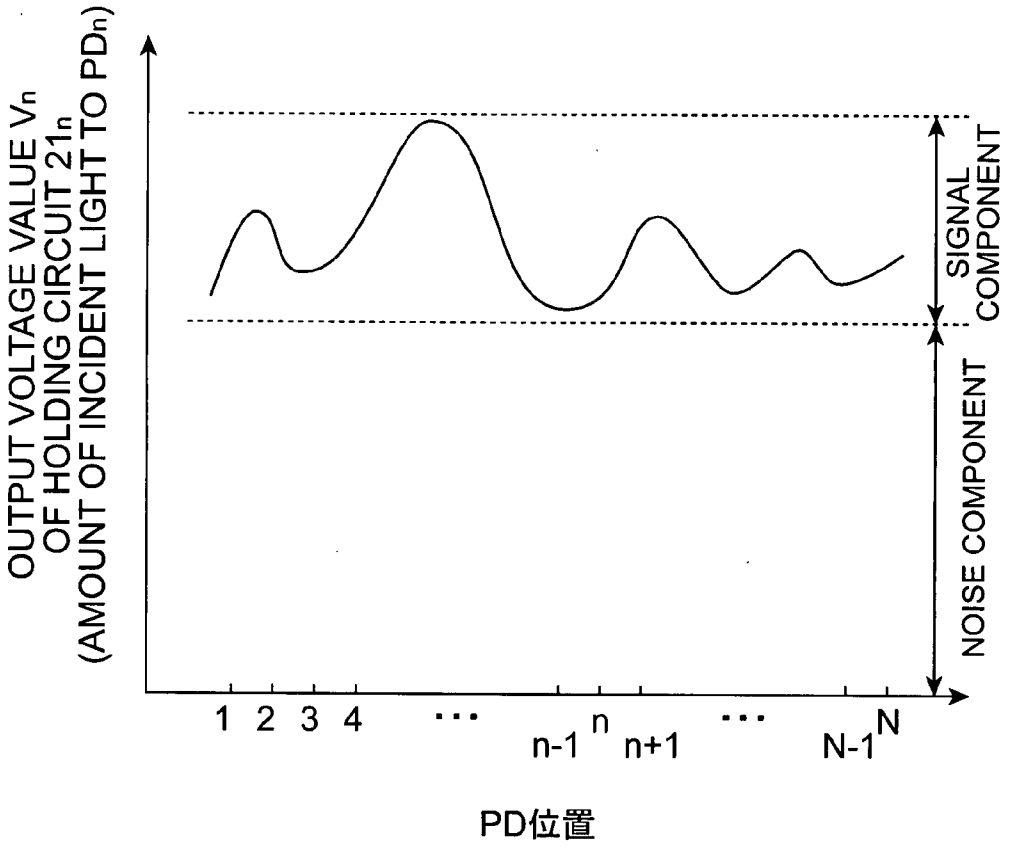

t1,1
t2,1
tn-1,1
tn,1
tN-1,1
tN,1
t1,2
t2,2
tn-1,2
tn,2
tN-1,2
tN,2
T1
T2
Tn-1
Tn
TN-1
TN
S1
S2
Sn-1
Sn
SN-1
SN
Sel1
Sel2

Fig.4


OUTPUT VOLTAGE VALUE Vn
OF HOLDING CIRCUIT 21n
(AMOUNT OF INCIDENT LIGHT TO PDn)
SIGNAL COMPONENT
NOISE COMPONENT
1 2 3 4 ... n-1 n n+1 ... N-1 N
PD位置

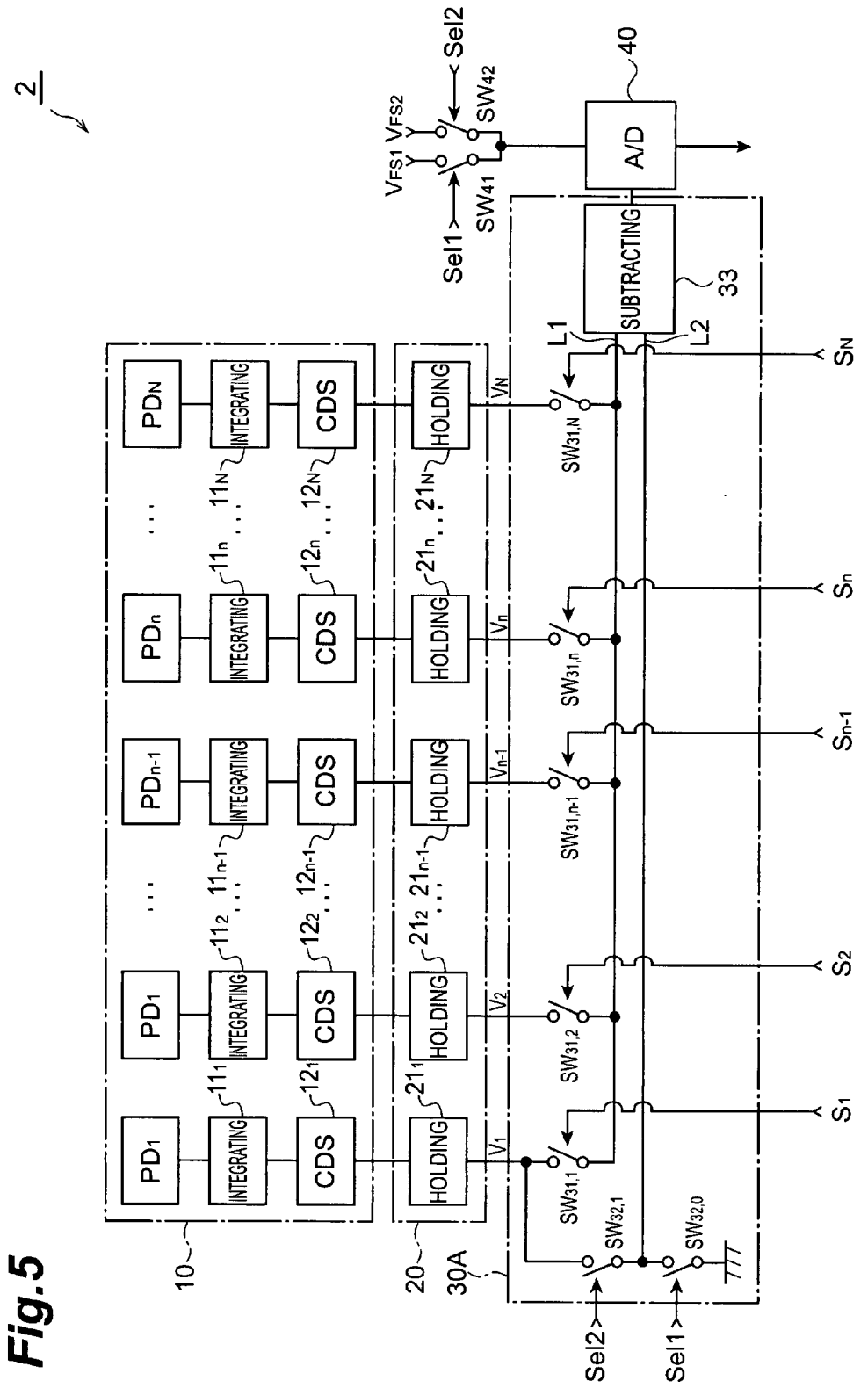
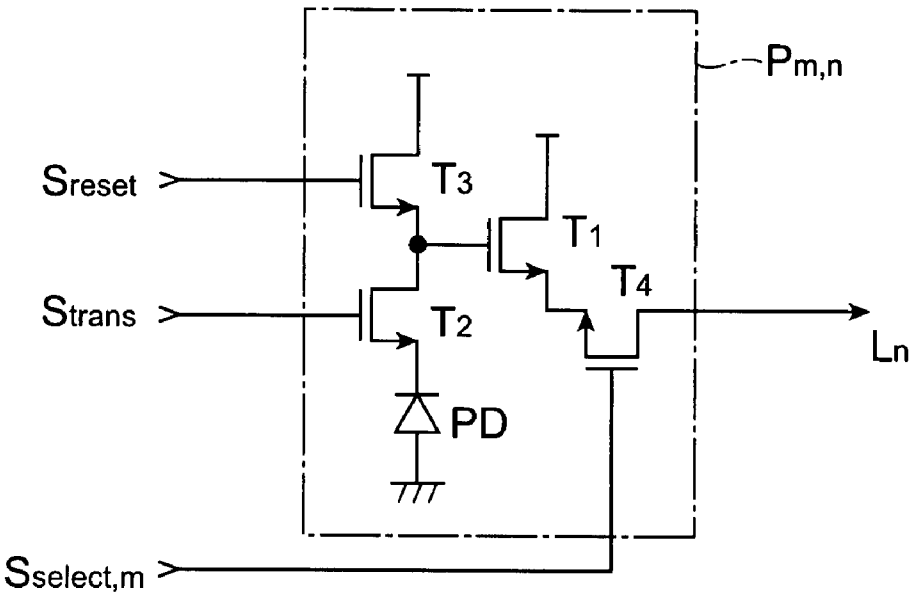

2
10
20
30A
PD1
PDn-1
PDn
PDN
INTEGRATING
CDS
HOLDING
A/D
SUBTRACTING
33
40
L1
L2
Sel1
Sel2
VFS1
VFS2
SW41
SW42
SW31,1
SW31,2
SW31,n-1
SW31,n
SW31,N
SW32,1
SW32,0
V1
V2
Vn-1
Vn
VN
S1
S2
Sn-1
Sn
SN

Fig.5

Fig.6



SENSOR APPARATUS

TECHNICAL FIELD

[0001] The present invention relates to a sensor apparatus including a plurality of sensor elements.

BACKGROUND ART

[0002] In sensor apparatuses including a plurality of sensor elements, voltage values corresponding to the detection result of the amount of sensing by the respective sensor elements are outputted from a signal processing circuit, and further digital values corresponding to the voltage values are outputted from an A/D conversing circuit. Then, one- or two-dimensional distribution of the amount of sensing (e.g. light intensity, temperature, displacement) is obtained based on the digital values corresponding to the amount of sensing for the respective sensor elements. As an example of such a sensor apparatus, there can be cited an image pickup apparatus including a plurality of photodiodes that are arranged one- or two-dimensionally (refer to Patent Document 1).

[0003] Patent Document 1: Japanese Patent Application Laid-Open No. H9-51476

DISCLOSURE OF THE INVENTION

Problem to be Solved by the Invention

[0004] The inventors have studied conventional sensor apparatuses in detail, and as a result, have found problems as follows. That is, the amount of sensing detected by such a sensor apparatus as described above may include not only a signal component that is supposed to be detected but also a noise component (disturbing light component, background light component) that is superimposed on the signal component. When the noise component (disturbing light component, background light component) is significantly indefinite, the A/D conversing circuit requires 10-bit outputted digital values for inputted voltage values with noise components (disturbing light components, background light components) superimposed on signal components, though 8-bit outputted digital values would suffice for, for example, inputted voltage values including signal components only, to A/D-convert the signal components with an accuracy equivalent to the 8-bit case.

[0005] When the outputted digital value of the A/D conversing circuit has a large number of bits, the A/D conversing circuit results in a long conversion time, large power consumption, and large circuit scale. It is generally necessary to A/D-convert the detection result of the amount of sensing by all sensor elements within a certain time period, which may require parallel processing using a plurality of A/D conversing circuits, resulting in a larger power consumption and larger circuit scale.

[0006] In order to overcome the above-mentioned problems, it is an object of the present invention to provide a sensor apparatus capable of obtaining digital values of signal components with a high accuracy, even in the case of the amount of sensing with noise components (disturbing light components, background light components) superimposed on the signal components, using an A/D conversing circuit with the outputted digital value thereof having a small number of bits.

Means for Solving Problem

[0007] A sensor apparatus according to the present invention comprises a sensor array section, a difference operating section, and an A/D converting section. In a first aspect of the sensor apparatus, the sensor array section includes N sensor elements (N represents an integer of 2 or more) and outputs a voltage value V_n in response to the result of sensing by the n-th sensor element ("n" represents any integer of 1 or more but N or less) among the N sensor elements. The difference operating section receives N voltage values V_1 to V_N outputted from the sensor array section and outputs a voltage value U_n ($n \neq 1$) corresponding to the difference ($V_n - V_{n-1}$) between voltage values V_n and V_{n-1}. The A/D converting section receives the voltage value U_n outputted from the difference operating section, converts the voltage value U_n into a digital value, and then outputs the converted digital value.

[0008] In the sensor apparatus according to the above-described first aspect, the A/D converting section may converts at least one voltage value among the N voltage values V_1 to V_N into a digital value, and then outputs the converted digital value.

[0009] Also, in a second aspect of the sensor apparatus, the difference operating section may receives N voltage values V_1 to V_N outputted from the sensor array section and outputs a voltage value W_n corresponding to the difference ($V_n - V_{n0}$) between a specific voltage value V_{n0} and the voltage value V_n among the N voltage values V_1 to V_N. In this case, the A/D converting section receives the voltage value W_n outputted from the difference operating section, converts the voltage value W_n into a digital value, and then outputs the converted digital value.

[0010] In the sensor apparatus according to the above-described second aspect, the A/D converting section may converts the specific voltage value V_{n0} into a digital value, and then outputs the converted digital value.

[0011] The sensor apparatus according to the present invention preferably further includes a holding section that receives the N voltage values V_1 to V_N outputted from the sensor array section and once holds the N voltage values V_1 to V_N. In this case, the difference operating section outputs the voltage value U_n or W_n based on the N voltage values V_1 to V_N held by the holding section.

[0012] In the sensor apparatus according to the present invention, each of the N sensor elements preferably includes a photodiode. In this case, the one- or two-dimensional intensity distribution of incident light can be detected. Also, even when the intensity of incident light may include signal components and noise components (disturbing light components, background light components) and the noise components (disturbing light components, background light components) may be significantly indefinite, it is possible to obtain digital values of the signal components with a high accuracy using an A/D conversing circuit with the outputted digital value thereof having a small number of bits.

[0013] The present invention will be more fully understood from the detailed description given hereinbelow and the accompanying drawings, which are given by way of illustration only and are not to be considered as limiting the present invention.

[0014] Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will be apparent to those skilled in the art from this detailed description.

EFFECT OF THE INVENTION

[0015] In accordance with the sensor apparatus according to the present invention, it is possible to obtain digital values of signal components with a high accuracy, even in the case of the amount of sensing with noise components (disturbing light components, background light components) superimposed on the signal components, using an A/D conversing circuit with the outputted digital value thereof having a small number of bits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. **1** is a view showing the overall configuration of a sensor apparatus according to a first embodiment of the present invention;

[0017] FIG. **2** is a circuit diagram including a photodiode PD_n, an integrating circuit $\mathbf{11}_n$, a CDS circuit $\mathbf{12}_n$, and a holding circuit $\mathbf{21}_n$ in the sensor apparatus according to the first embodiment;

[0018] FIG. **3** is a timing chart for explaining the operation of a difference operating section and an A/D converting section in the sensor apparatus according to the first embodiment;

[0019] FIG. **4** is a view showing the intensity distribution of light to be detected by the sensor apparatus according to the first embodiment;

[0020] FIG. **5** is a view showing the overall configuration of a sensor apparatus according to a second embodiment of the present invention; and

[0021] FIG. **6** is a circuit diagram of an APS circuit included in each pixel, showing the partial configuration of a sensor apparatus according to a modified example of the present invention.

DESCRIPTION OF THE REFERENCE NUMERALS

[0022] **1**, **2** . . . sensor apparatuses; **10** . . . sensor array section; **11** . . . integrating circuit; **12** . . . CDS circuit; **20** . . . holding section; **30**, **30**A . . . difference operating sections; **33** . . . subtracting circuit; and **40** . . . A/D converting section.

BEST MODES FOR CARRYING OUT THE INVENTION

[0023] In the following, embodiments of a sensor apparatus according to the present invention will be explained in detail with reference to FIGS. **1** to **6**. In the explanation of the drawings, constituents identical to each other will be referred to with numerals identical to each other without repeating their overlapping descriptions.

First Embodiment

[0024] First, a sensor apparatus according to a first embodiment of the present invention will be explained. FIG. **1** is a view showing the overall configuration of the sensor apparatus according to the first embodiment of the present invention. The sensor apparatus **1** shown in FIG. **1** comprises a sensor array section **10**, a holding section **20**, a difference operating section **30**, and an A/D converting section **40**.

[0025] The sensor array section **10** includes N photodiodes PD_1 to PD_N, N integrating circuits $\mathbf{11}_1$ to $\mathbf{11}_N$, and N CDS circuits $\mathbf{12}_1$ to $\mathbf{12}_N$. Also, the holding section **20** includes N holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$. Each of the photodiodes PD_1 to PD_N has a common composition, each of the integrating circuits $\mathbf{11}_1$ to $\mathbf{11}_N$ also has a common composition, each of the CDS circuits $\mathbf{12}_1$ to $\mathbf{12}_N$ also has a common composition, and each of the holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$ also has a common composition. The N photodiodes PD_1 to PD_N are arranged one-dimensionally. The n-th integrating circuit $\mathbf{11}_n$, n-th CDS circuit $\mathbf{12}_n$, and n-th holding circuit $\mathbf{21}_n$ are provided correspondingly to the n-th photodiode PD_n. Here, N represents an integer of 2 or more. Also, "n" represents any integer of 1 or more but N or less, unless otherwise specified.

[0026] The photodiode PD_n generates electric charges corresponding to the amount of incident light and outputs the electric charges to the integrating circuit $\mathbf{11}_n$. Each integrating circuit $\mathbf{11}_n$ accumulates the electric charges outputted from the photodiode PD_n into a capacitive element and outputs a voltage value corresponding to the amount of accumulated charge to the CDS circuit $\mathbf{12}_n$. The CDS circuit $\mathbf{12}_n$ receives the voltage value outputted from the integrating circuit $\mathbf{11}_n$ and outputs a voltage value corresponding to the change of the inputted voltage value after a reference time based on the inputted voltage value at the reference time to the holding circuit $\mathbf{21}_n$. That is, the sensor array section **10** includes the N photodiodes PD_1 to PD_N as sensor elements and outputs a voltage value corresponding to the detection result of light by the photodiode PD_n. The holding circuit $\mathbf{21}_n$ receives the voltage value outputted from the CDS circuit $\mathbf{12}_n$ and outputs the voltage value V_n held therein.

[0027] The difference operating section **30** includes switches $SW_{31,1}$ to $SW_{31,N}$, switches $SW_{32,0}$ to $SW_{32,N-1}$, and a subtracting circuit **33**. The output terminal of the holding circuit $\mathbf{21}_n$ is connected to a wiring L**1** via the switch $SW_{31,n}$ and to a wiring L**2** via the switch $SW_{32,n}$. However, the output terminal of the N-th holding circuit $\mathbf{21}_N$ is connected to the wiring L**1** via the switch $SW_{31,N}$ but may not be connected to the wiring L**2** via a switch. Also, the wiring L**2** is connected with the ground potential via the switch $SW_{32,0}$. The switches $SW_{31,n}$ and $SW_{32,n-1}$ open and close based on the level of a control signal S_n. The subtracting circuit **33** outputs a voltage value corresponding to the difference between voltage values to be inputted through the respective wirings L**1** and L**2**.

[0028] The A/D converting section **40** is used together with switches SW_{41} and SW_{42}. The A/D converting section **40** receives one of a voltage value V_{FS1} to be inputted via the switch SW_{41} and a voltage value V_{FS2} to be inputted via the switch SW_{42} as a full scale in A/D conversion. Then, the A/D converting section **40** converts the voltage value outputted from the subtracting circuit **33** into a digital value at a

resolution of one 2M-th of the full scale (voltage value V_{FS1} or V_{FS2}), and then outputs the converted digital value. It is noted that M represents the number of bits of the outputted digital value. It is preferable that the voltage value V_{FS1} is greater than V_{FS2} and the ratio therebetween be a power of two. The switch SW_{41} opens and closes based on the level of a control signal Sel**1**, while the switch SW_{42} opens and closes based on the level of a control signal Sel**2**.

[**0029**] FIG. **2** is a circuit diagram including a photodiode PD_n, an integrating circuit $\mathbf{11}_n$, a CDS circuit $\mathbf{12}_n$, and a holding circuit $\mathbf{21}_n$ in the sensor apparatus **1** according to the first embodiment. The anode terminal of the photodiode PD_n is grounded, while the cathode terminal thereof is connected to the input terminal of the integrating circuit $\mathbf{11}_n$, and the photodiode PD_n generates electric charges corresponding to the amount of incident light and outputs the electric charges to the integrating circuit $\mathbf{11}_n$.

[**0030**] The integrating circuit $\mathbf{11}_n$ includes an amplifier A_{11}, a capacitive element C_{11}, and a switch SW_{11}. The input terminal of the amplifier A_{11} is connected to the cathode terminal of the photodiode PD_n. The capacitive element C_{11} and switch SW_{11} are provided between the input and output terminals of the amplifier A_{11} by being connected parallel with each other. The outputted voltage value of the integrating circuit $\mathbf{11}_n$ is initialized by closing the switch SW_{11} so that the capacitive element C_{11} is discharged. The integrating circuit $\mathbf{11}_n$ also accumulates electric charges outputted from the photodiode PD_n into the capacitive element C_{11} when the switch SW_{11} is opened, and then outputs a voltage value corresponding to the amount of accumulated charge to the CDS circuit $\mathbf{12}_n$.

[**0031**] The CDS circuit $\mathbf{12}_n$ includes an amplifier A_{12}, a capacitive element C_{12}, and a switch SW_{12}. The input terminal of the amplifier A_{12} is connected to the amplifier A_{11} in the integrating circuit $\mathbf{11}_n$ via the capacitive element C_{12} and is grounded via the switch SW_{12}. The CDS circuit $\mathbf{12}_n$ receives the voltage value outputted from the integrating circuit $\mathbf{11}_n$ and outputs a voltage value corresponding to the change of the inputted voltage value after a reference time (when the switch SW_{12} is opened) based on the inputted voltage value at the reference time from the amplifier A_{12} to the holding circuit $\mathbf{21}_n$.

[**0032**] The holding circuit $\mathbf{21}_n$ includes an amplifier A_{21}, a capacitive element C_{21}, and a switch SW_{21}. The input terminal of the amplifier A_{21} is connected to the amplifier A_{12} in the CDS circuit $\mathbf{12}_n$ via the switch SW_{21} and is grounded via the capacitive element C_{21}. The output terminal of the amplifier A_{21} is connected to the wiring L**1** via the switch $SW_{31,n}$ and to the wiring L**2** via the switch $SW_{32,n}$. The holding circuit $\mathbf{21}_n$ holds the voltage value, which is outputted from the CDS circuit $\mathbf{12}_n$ at a time when the switch SW_{21} is opened, in the capacitive element C_{21} also after the time of the state variation, and then outputs a voltage value V_n corresponding to the held voltage value from the amplifier A_{21}.

[**0033**] The operation of the photodiode PD_n, integrating circuit $\mathbf{11}_n$, CDS circuit $\mathbf{12}_n$, and holding circuit $\mathbf{21}_n$ is as follows.

[**0034**] That is, when the switch SW_{11} in the integrating circuit $\mathbf{11}_n$ is opened, electric charges outputted from the photodiode PD_n are accumulated into the capacitive element C_{11}, and then a voltage value corresponding to the amount of accumulated charge is outputted from the integrating circuit $\mathbf{11}_n$. As the amount of charge accumulated in the capacitive element C_{11} increases gradually, the voltage value outputted from the integrating circuit $\mathbf{11}_n$ varies. While the switch SW_{11} in the integrating circuit $\mathbf{11}_n$ is opened, the switch SW_{12} in the CDS circuit $\mathbf{12}_n$ is opened at a first time, and then the switch SW_{21} in the holding circuit $\mathbf{21}_n$ is opened at a second time. The voltage value outputted from the CDS circuit $\mathbf{12}_n$ after the first time corresponds to the change of the voltage value outputted from the integrating circuit $\mathbf{11}_n$ based on the voltage value outputted from the integrating circuit $\mathbf{11}_n$ at the first time. Then, the voltage value V_n held by the holding circuit $\mathbf{21}_n$ after the second time corresponds to the voltage value outputted from the CDS circuit $\mathbf{12}_n$ at the second time.

[**0035**] That is, the voltage value V_n held by the holding circuit $\mathbf{21}_n$ after the second time corresponds to the difference between the voltage values outputted from the integrating circuit $\mathbf{11}_n$ at the first and second time, and when the time difference between the first and second time is constant, corresponds to the intensity of light incident to the photodiode PD_n. It is noted that the N integrating circuits $\mathbf{11}_1$ to $\mathbf{11}_N$ operate at the same timing; the N CDS circuits $\mathbf{12}_1$ to $\mathbf{12}_N$ also operate at the same timing; and the N holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$ also operate at the same timing. Therefore, a voltage value V_n corresponding to the amount of incident light to the photodiode PD_n during a common period of time is to be held by the holding section **20**.

[**0036**] Next, the operation of the difference operating section **30** and the A/D converting section **40** in the sensor apparatus **1** according to the first embodiment will be explained. FIG. **3** is a timing chart for explaining the operation of the difference operating section **30** and the A/D converting section **40** in the sensor apparatus **1** according to the first embodiment. FIG. **3** shows a timing chart when the difference operating section **30** and A/D converting section **40** process voltage values V_1 to V_N are held by the holding section **20** as described above. It is noted that not only the above-described operation of the sensor array section **10** and holding section **20** but also the operation of the difference operating section **30** and A/D converting section **40** to be explained hereinafter is performed based on various control signals outputted from a control section (not shown in the figures). FIG. **3** shows the level of each control signal S_n to be inputted to the difference operating section **30**, the level of a control signal Sel**1** for instructing the switch SW_{41} to open and close, and the level of a control signal Sel**2** for instructing the switch SW_{42} to open and close in this order from the top.

[**0037**] As shown in FIG. **3**, the control signals S_1 to S_N are made high sequentially. During the time period T_n from time $t_{n,1}$ to time $t_{n,2}$, only the control signal S_n is made high among the control signals S_1 to S_N. During the time period T_1, the control signal Sel**1** is made high, while the control signal Sel**2** is made low. Also, from the time period T_2 through the time period T_N, the control signal Sel**1** is made low, while the control signal Sel**2** is made high.

[**0038**] During the time period T_1 from time $t_{1,1}$ to time $t_{1,2}$, only the control signal S_1 is made high among the control signals S_1 to S_N, so that the switches $SW_{31,1}$ and $SW_{32,0}$ in the difference operating section **30** are closed. Also, the

control signal Sel**1** is made high, so that the switch SW_{41} is closed. When the switch $SW_{31,1}$ is closed, the voltage value V_1 held by the holding circuit $\mathbf{21}_1$ is inputted to the subtracting circuit **33** through the switch $SW_{31,1}$ and the wiring L**1**. Also, when the switch $SW_{32,0}$ is closed, the ground potential is inputted to the subtracting circuit **33** through the switch $SW_{32,0}$ and the wiring L**2**. In the subtracting circuit **33**, the ground potential is subtracted from the voltage value V_1, and the subtracted voltage value V_1 is outputted. Then, in the A/D converting section **40**, the voltage value V_1 outputted from the subtracting circuit **33** is converted into an M-bit digital value using the voltage value V_{FS1} inputted through the switch SW_{41} as a full scale.

[**0039**] During the time period T_n from time $t_{n,1}$ to time $t_{n,2}$ ($n \neq 1$), only the control signal S_n is made high among the control signals S_1 to S_N, so that the switches $SW_{31,n}$ and $SW_{32,n-1}$ in the difference operating section **30** are closed. Also, the control signal Sel**2** is made high, so that the switch SW_{42} is closed. When the switch $SW_{31,n}$ is closed, the voltage value V_n held by the holding circuit $\mathbf{21}_n$ is inputted to the subtracting circuit **33** through the switch $SW_{31,n}$ and the wiring L**1**. Also, when the switch $SW_{32,n-1}$ is closed, the voltage value V_{n-1} held by the holding circuit $\mathbf{21}_{n-1}$ is inputted to the subtracting circuit **33** through the switch $SW_{32,n-1}$ and the wiring L**2**. In the subtracting circuit **33**, the voltage value V_{n-1} is subtracted from the voltage value V_n, and a voltage value U_n corresponding to the subtraction result is outputted. Then, in the A/D converting section **40**, the voltage value U_n outputted from the subtracting circuit **33** is converted into an M-bit digital value using the voltage value V_{FS2} inputted through the switch SW_{42} as a full scale.

[**0040**] That is, during the time period T_1, the A/D converting section **40** converts the voltage value V_1 corresponding to the amount of incident light to the first photodiode PD_1 into an M-bit digital value using the voltage value V_{FS1} as a full scale. Also, during each time period T_n ($n \neq 1$), the difference operating section **30** calculates a voltage value U_n according to the difference ($V_n - V_{n-1}$) between voltage values V_n and V_{n-1} that correspond to the amount of incident light to the respective photodiodes PD_n and PD_{n-1}, and then the A/D converting section **40** converts the voltage value U_n into an M-bit digital value using the voltage value V_{FS2} as a full scale.

[**0041**] Therefore, as shown in FIG. **4**, even when significant noise components (disturbing light components, background light components) may be superimposed on signal components that are supposed to be detected in the intensity distribution of light to be detected by the sensor apparatus **1**, the sensor apparatus **1** can obtain digital values of the signal components with a high accuracy using an A/D conversing circuit with the outputted digital value thereof having a small number of bits of M as the A/D converting section **40**.

[**0042**] That is, the maximum value of the difference ($V_n - V_{n-1}$) between two adjacent voltage values V_n and V_{n-1} among the voltage values V_1 to V_N outputted from the respective holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$ is smaller than the maximum value of the voltage values V_1 to V_N. Hence, the voltage value V_{FS2} to be used by the A/D converting section **40** as a full scale during the time period T_n ($n \neq 1$) is set to the maximum value of the difference ($V_n - V_{n-1}$) (or a value somewhat greater than the maximum value) or to the difference between the maximum and minimum values of signal components included in the voltage values V_1 to V_N (or a value somewhat greater than the difference). Thus, in the A/D converting section **40**, the voltage value V_{FS2} to be used as a full scale is set appropriately and a voltage value U_n corresponding to the difference ($V_n - V_{n-1}$) is converted into a digital value. Therefore, the digital value to be outputted from the A/D converting section **40** represents signal components with a high accuracy, though having a small number of bits of M.

[**0043**] Meanwhile, the maximum value of the voltage values V_1 to V_N outputted from the respective holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$ is larger. Hence, the voltage value V_{FS1} to be used by the A/D converting section **40** as a full scale during the time period T_1 is set to the maximum value of the voltage values V_1 to V_N (or a value somewhat greater than the maximum value) that is greater than the voltage value V_{FS2}. Thus, in the A/D converting section **40**, the voltage value V_{FS1} to be used as a full scale is set appropriately and the voltage value V_1 is converted into a digital value. Therefore, the digital value to be outputted from the A/D converting section **40** represents the sum of signal components and noise components (disturbing light components, background light components), though having a small number of bits of M.

[**0044**] As described heretofore, the sensor apparatus **1** according to the first embodiment can obtain digital values of signal components with a high accuracy using an A/D conversing circuit with the outputted digital value thereof having a small number of bits of M as the A/D converting section **40**. Therefore, the A/D converting section **40** results in a short conversion time, small power consumption, and small circuit scale. Also, even in the case of performing A/D conversion processing in parallel due to the requirement of performing the A/D conversion processing within a certain time period, the number of A/D converting sections for the parallel processing may be small, which also results in a small power consumption and small circuit scale.

Second Embodiment

[**0045**] Next, a sensor apparatus according to a second embodiment of the present invention will be explained. FIG. **5** is a view showing the overall configuration of the sensor apparatus according to the second embodiment of the present invention. The sensor apparatus **2** shown in FIG. **5** comprises a sensor array section **10**, a holding section **20**, a difference operating section **30**A, and an A/D converting section **40**. As compared with the configuration of the sensor apparatus **1** according to the above-described first embodiment (FIGS. **1** and **2**), the sensor apparatus **2** according to the second embodiment is different from the first embodiment in that the difference operating section **30**A is provided instead of the difference operating section **30**.

[**0046**] The difference operating section **30**A includes switches $SW_{31,1}$ to $SW_{31,N}$, switches $SW_{32,0}$ and $SW_{32,1}$, and a subtracting circuit **33**. The output terminal of the holding circuit $\mathbf{21}_n$ is connected to a wiring L**1** via the switch $SW_{31,n}$. The output terminal of the first holding circuit $\mathbf{21}_1$ is connected to a wiring L**2** via the switch $SW_{32,1}$. Also, the wiring L**2** is connected with the ground potential via the switch $SW_{32,0}$. The switch $SW_{31,n}$ opens and closes based on the level of a control signal S_n, and the switch $SW_{32,0}$ opens and closes based on the level of a control signal Sel**1**, while

the switch $SW_{32,1}$ opens and closes based on the level of a control signal Sel**2**. The subtracting circuit **33** outputs a voltage value corresponding to the difference between voltage values to be inputted through the respective wirings L**1** and L**2**.

[**0047**] Next, the operation of the difference operating section **30**A and the A/D converting section **40** in the sensor apparatus **2** according to the second embodiment will be explained. The timing chart for explaining the operation of the difference operating section **30**A and the A/D converting section **40** in the sensor apparatus **2** according to the second embodiment is the same as in FIG. **3**.

[**0048**] During the time period T_1 from time $t_{1,1}$ to time $t_{1,2}$, only the control signal S_1 is made high among the control signals S_1 to S_N, so that the switch $SW_{31,1}$ in the difference operating section **30**A is closed. Also, the control signal Sel**1** is made high, so that the switches $SW_{32,0}$ and SW_{41} are closed. When the switch $SW_{31,1}$ is closed, the voltage value V_1 held by the holding circuit $\mathbf{21}_1$ is inputted to the subtracting circuit **33** through the switch $SW_{31,1}$ and the wiring L**1**. Also, when the switch $SW_{32,0}$ is closed, the ground potential is inputted to the subtracting circuit **33** through the switch $SW_{32,0}$ and the wiring L**2**. In the subtracting circuit **33**, the ground potential is subtracted from the voltage value V_1, and the subtracted voltage value V_1 is outputted. Then, in the A/D converting section **40**, the voltage value V_1 outputted from the subtracting circuit **33** is converted into an M-bit digital value using the voltage value V_{FS1} inputted through the switch SW_{41} as a full scale.

[**0049**] During the time period T_n from time $t_{n,1}$ to time $t_{n,2}$ ($n \neq 1$), only the control signal S_n is made high among the control signals S_1 to S_N, so that the switch $SW_{31,n}$ in the difference operating section **30**A is closed. Also, the control signal Sel**2** is made high, so that the switch SW_{42} is closed. When the switch $SW_{31,n}$ is closed, the voltage value V_n held by the holding circuit $\mathbf{21}_n$ is inputted to the subtracting circuit **33** through the switch $SW_{31,n}$ and the wiring L**1**. Also, when the switch $SW_{32,1}$ is closed, the voltage value V_1 held by the holding circuit $\mathbf{21}_1$ is inputted to the subtracting circuit **33** through the switch $SW_{32,1}$ and the wiring L**2**. In the subtracting circuit **33**, the voltage value V_1 is subtracted from the voltage value V_n, and a voltage value W_n corresponding to the subtraction result is outputted. Then, in the A/D converting section **40**, the voltage value W_n outputted from the subtracting circuit **33** is converted into an M-bit digital value using the voltage value V_{FS2} inputted through the switch SW_{42} as a full scale.

[**0050**] That is, during the time period T_1, the A/D converting section **40** converts the voltage value V_1 corresponding to the amount of incident light to the first photodiode PD_1 into an M-bit digital value using the voltage value V_{FS1} as a full scale. Also, during the time period T_n ($n \neq 1$), the difference operating section **30**A calculates a voltage value W_n corresponding to the difference ($V_n - V_1$) between voltage values V_n and V_1 that correspond to the amount of incident light to the respective photodiodes PD_n and PD_1, and then the A/D converting section **40** converts the voltage value W_n into an M-bit digital value using the voltage value V_{FS2} as a full scale.

[**0051**] Therefore, as shown in FIG. **4**, even when significant noise components (disturbing light components, background light components) may be superimposed on signal components that are supposed to be detected in the intensity distribution of light to be detected by the sensor apparatus **2**, the sensor apparatus **2** can obtain digital values of the signal components with a high accuracy using an A/D conversing circuit with the outputted digital value thereof having a small number of bits of M as the A/D converting section **40**.

[**0052**] That is, the maximum value of the voltage value W_n to be obtained by a difference operation from the voltage values V_1 to V_N outputted from the respective holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$ is smaller than the maximum value of the voltage values V_1 to V_N. Hence, the voltage value V_{FS2} to be used by the A/D converting section **40** as a full scale during the time period T_n ($n \neq 1$) is set to the maximum value of the voltage value W_n (or a value somewhat greater than the maximum value) or to the difference between the maximum and minimum values of signal components included in the voltage values V_1 to V_N (or a value somewhat greater than the difference). Thus, in the A/D converting section **40**, the voltage value V_{FS2} to be used as a full scale is set appropriately and a voltage value W_n corresponding to the difference ($V_n - V_1$) is converted into a digital value. Therefore, the digital value to be outputted from the A/D converting section **40** represents signal components with a high accuracy, though having a small number of bits of M.

[**0053**] Meanwhile, the maximum value of the voltage values V_1 to V_N outputted from the respective holding circuits $\mathbf{21}_1$ to $\mathbf{21}_N$ is larger. Hence, the voltage value V_{FS1} to be used by the A/D converting section **40** as a full scale during the time period T_1 is set to the maximum value of the voltage values V_1 to V_N (or a value somewhat greater than the maximum value) that is greater than the voltage value V_{FS2}. Thus, in the A/D converting section **40**, the voltage value V_{FS1} to be used as a full scale is set appropriately and the voltage value V_1 is converted into a digital value. Therefore, the digital value to be outputted from the A/D converting section **40** represents the sum of signal components and noise components (disturbing light components, background light components), though having a small number of bits of M.

[**0054**] As described above, the sensor apparatus **2** according to the second embodiment can obtain digital values of signal components with a high accuracy using an A/D conversing circuit with the outputted digital value thereof having a small number of bits of M as the A/D converting section **40**. Therefore, the A/D converting section **40** results in a short conversion time, small power consumption, and small circuit scale. Also, even in the case of performing A/D conversion processing in parallel due to the requirement of performing the A/D conversion processing within a certain time period, the number of A/D converting sections for the parallel processing may be small, which also results in a small power consumption and small circuit scale.

[**0055**] (Exemplary Variation)

[**0056**] The present invention is not restricted to the above-described first and second embodiments, and various modifications may be made. For example, although the sensor apparatuses according to the above-described first and second embodiments are image pickup apparatuses including a plurality of photodiodes that are arranged one-dimensionally, the sensor apparatus according to the present invention may be an image pickup apparatus including a plurality of photodiodes that are arranged two-dimensionally. Further,

the sensor apparatus according to the present invention may be an imaging apparatus in which each pixel includes an APS (Active Pixel Sensor) circuit shown in FIG. **6** as well as a plurality of photodiodes and the pixels are arranged one- or two-dimensionally. Also, the sensor apparatus according to the present invention is not restricted to an image pickup apparatus, but may include a plurality of sensor elements for detecting the amount of another sensing parameter (e.g. temperature, displacement).

[0057] From the invention thus described, it will be obvious that the embodiments of the invention may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended for inclusion within the scope of the following claims.

INDUSTRIAL APPLICABILITY

[0058] The sensor apparatus according to the present invention is applicable to, for example, an image pickup apparatus including a plurality of photodiodes that are arranged one- or two-dimensionally.

1. A sensor apparatus comprising:

a sensor array section including N sensor elements (N represents an integer of 2 or more) and outputting a voltage value V_n in response to the result of sensing by the n-th sensor element ("n" represents any integer of 1 or more but N or less) among said N sensor elements;

a difference operating section outputting a voltage value U_n ($n \neq 1$) corresponding to the difference ($V_n - V_{n-1}$) between the voltage values V_n and V_{n-1} among N voltage values V_1 to V_N outputted from said sensor array section; and

an A/D converting section converting the voltage value U_n outputted from said difference operating section into a digital value.

2. A sensor apparatus according to claim 1, wherein said A/D converting section converts at least one voltage value of the N voltage values V_1 to V_N into a digital value.

3. A sensor apparatus according to claim 1, further comprising a holding section once holding the N voltage values V_1 to V_N outputted from said sensor array section, and

wherein said difference operating section outputs the voltage value U_n based on the N voltage values V_1 to V_N held by said holding section.

4. A sensor apparatus according to claim 1, wherein each of said N sensor elements includes a photodiode.

5. A sensor apparatus comprising:

a sensor array section including N sensor elements (N represents an integer of 2 or more) and adapted to output a voltage value V_n in response to the result of sensing by the n-th sensor element ("n" represents any integer of 1 or more but N or less) among said N sensor elements;

a difference operating section outputting a voltage value W_n corresponding to the difference ($V_n - V_{n0}$) between a specific voltage value V_{n0} and the voltage value V_n among N voltage values V_1 to V_N outputted from said sensor array section; and

an A/D converting section converting the voltage value W_n outputted from said difference operating section into a digital value.

6. A sensor apparatus according to claim 5, wherein said A/D converting section converts the specific voltage value V_{n0} into a digital value.

7. A sensor apparatus according to claim 5, further comprising a holding section once holding the N voltage values V_1 to V_N outputted from said sensor array section, and

wherein said difference operating section outputs the voltage value W_n based on the N voltage values V_1 to V_N held by said holding section.

8. A sensor apparatus according to claim 5, wherein each of said N sensor elements includes a photodiode.

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