

CORRECTED VERSION

(19) World Intellectual Property Organization International Bureau



(10) International Publication Number WO 2014/189983 A8

(43) International Publication Date 27 November 2014 (27.11.2014)

(51) International Patent Classification:

H01L 23/60 (2006.01) H01L 25/07 (2006.01)
H01L 25/065 (2006.01) H01L 25/18 (2006.01)

(21) International Application Number:

PCT/US2014/038862

(22) International Filing Date:

20 May 2014 (20.05.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

13/899,129 21 May 2013 (21.05.2013) US

(71) Applicant: XILINX, INC. [US/US]; Attn: Legal Dept., 2100 Logic Drive, San Jose, CA 95124 (US).

(72) Inventors: XIANG, Qi; 2100 Logic Drive, San Jose, CA 95124 (US). LI, Xiao-Yu; 2100 Logic Drive, San Jose, CA 95124 (US). CHEN, Cinti, X; 2100 Logic Drive, San Jose, CA 95124 (US). O'ROURKE, Glenn; 2100 Logic Drive, San Jose, CA 95124 (US).

(74) Agents: PARANDOOSH, David, A et al.; Xilinx, Inc., Attn: Legal Dept., 2100 Logic Drive, San Jose, CA 95124 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(48) Date of publication of this corrected version:

17 March 2016

(15) Information about Correction:

see Notice of 17 March 2016

(54) Title: CHARGE DAMAGE PROTECTION ON AN INTERPOSER FOR A STACKED DIE ASSEMBLY

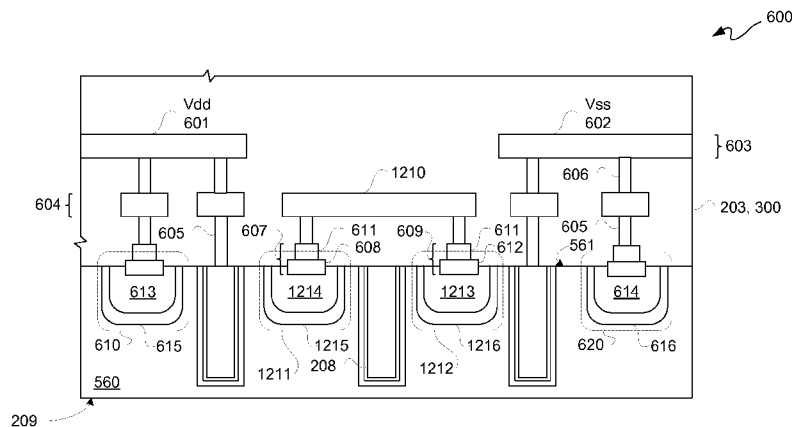
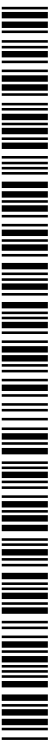


FIG. 12

(57) Abstract: An apparatus relating generally to an interposer (600, 700, 800) is disclosed. In such an apparatus, the interposer (600, 700, 800) has a plurality of conductors (208, 451-459, 603-606) and a plurality of charge attracting structures (610, 620, 710, 720, 810, 820). The plurality of charge attracting structures (610, 620, 710, 720, 810, 820) are to protect at least one integrated circuit die (202) to be coupled to the interposer (600, 700, 800) to provide a stacked die (200). The plurality of conductors (208, 451-459, 603-606) include a plurality of through-substrate vias (208).



WO 2014/189983 A8