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(54) **ARRAY SUBSTRATE, TOUCH DISPLAY SCREEN AND MANUFACTURING METHOD OF ARRAY SUBSTRATE**

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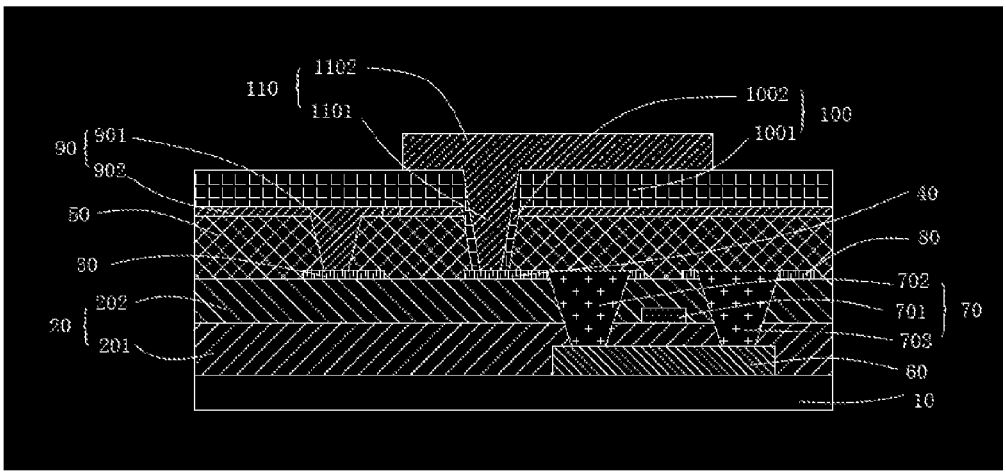
(57) **ABSTRACT**

An array substrate used for a touch display screen is provided. The array substrate comprises a substrate; a polysilicon layer disposed on the substrate; a dielectric layer disposed on the polysilicon layer and the substrate; a touch line, a connecting line and data line arranged sequentially at intervals on the dielectric layer; a planarization layer covering the connecting line and data line; wherein a first through-hole and second through-hole arranged sequentially at intervals are formed on planarization layer, the touch line is facing and exposed from first through-hole; a portion of the connecting line is facing and exposed from second through-hole; a source and drain in contact with a portion of the surface of polysilicon layer are formed in dielectric layer arranged at intervals, the drain and source are respectively connected with the connecting line and data line, and the first through-hole is completely misplaced with the second through-hole,



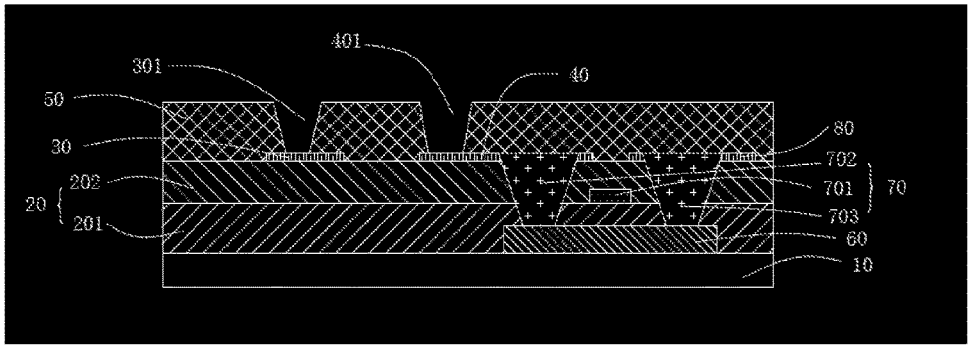


Fig. 1

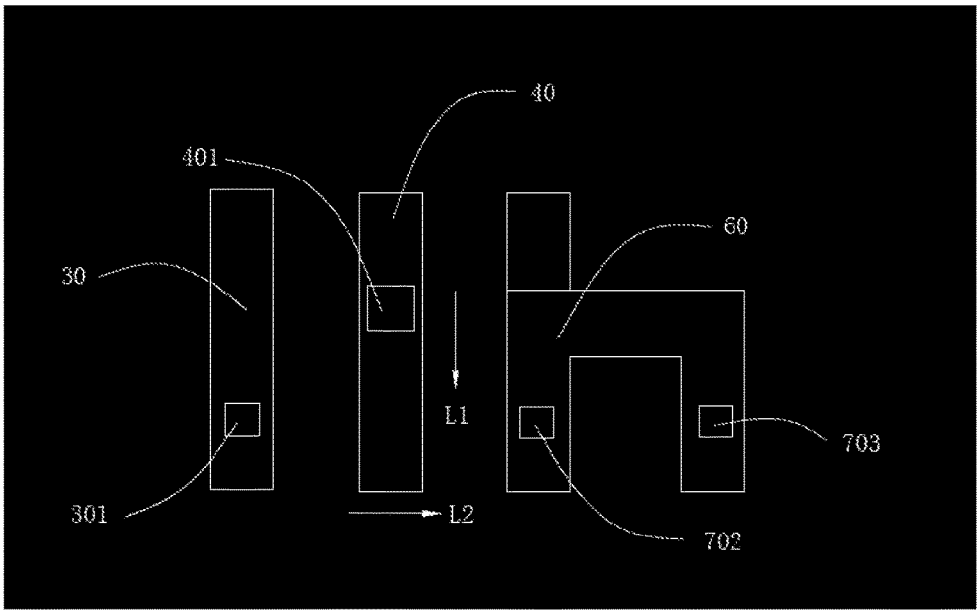

40
401
60
30
L1
703
301
L2
702

Fig. 2

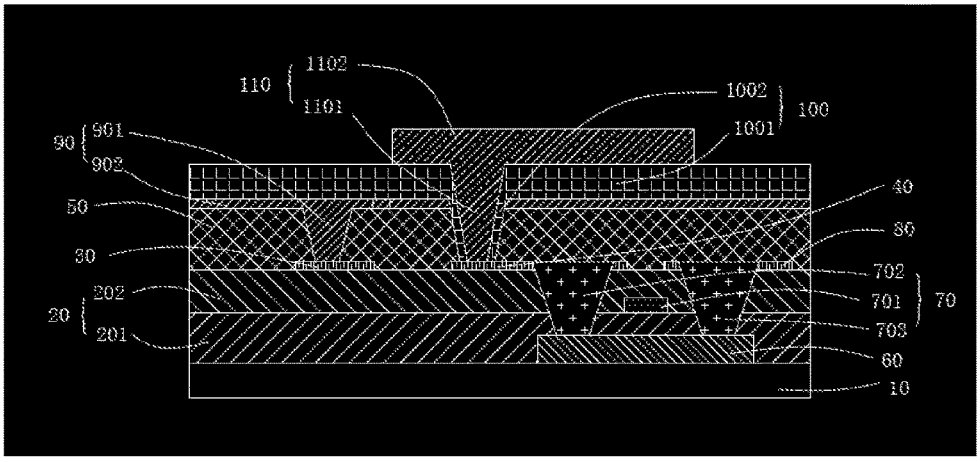

110
1102
1101
1002
100
1001
90
901
902
40
50
80
30
702
202
701
70
20
703
201
60
10

Fig. 3

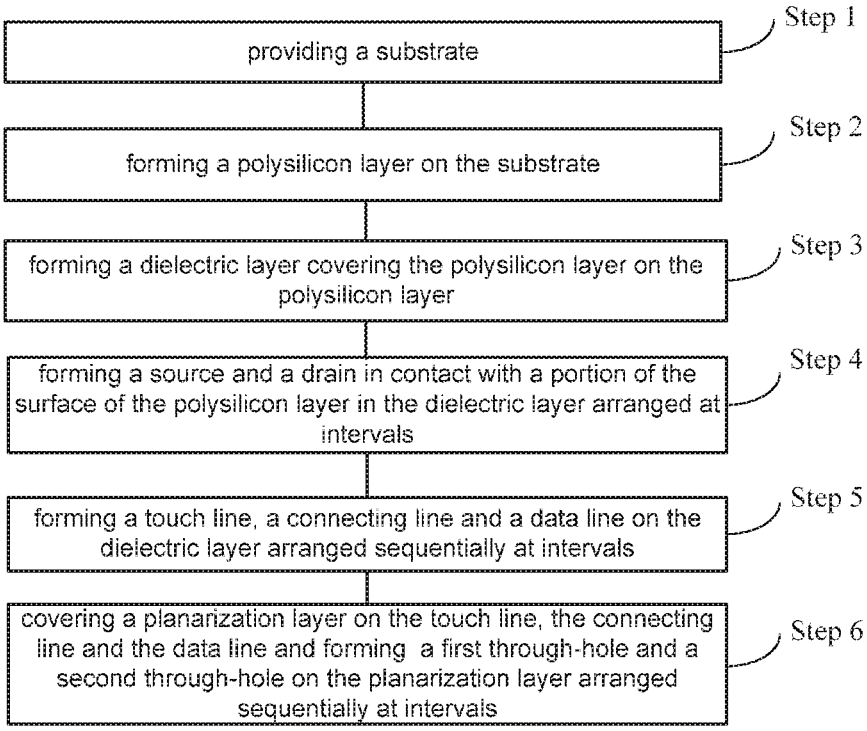

providing a substrate
Step 1
forming a polysilicon layer on the substrate
Step 2
forming a dielectric layer covering the polysilicon layer on the polysilicon layer
Step 3
forming a source and a drain in contact with a portion of the surface of the polysilicon layer in the dielectric layer arranged at intervals
Step 4
forming a touch line, a connecting line and a data line on the dielectric layer arranged sequentially at intervals
Step 5
covering a planarization layer on the touch line, the connecting line and the data line and forming a first through-hole and a second through-hole on the planarization layer arranged sequentially at intervals
Step 6

Fig. 4

ARRAY SUBSTRATE, TOUCH DISPLAY SCREEN AND MANUFACTURING METHOD OF ARRAY SUBSTRATE

RELATED APPLICATION

[0001] The present application is a continuation application of POT Patent Application No. PCT/CN2018/082799 filed on Apr. 12, 2018, which claims the priority benefit of Chinese Patent Application No. 201810160028.X, entitled "array substrate, touch display screen and manufacturing method of array substrate", filed on Feb. 26, 2018, which is herein incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present disclosure relates to a display field, in particular to an array substrate, a touch display screen and a manufacturing method of an array substrate.

BACKGROUND OF THE INVENTION

[0003] Touch functions are usually achieved by touch lines in the touch display field, but the touch lines need to pass through via-holes of a planarization layer to ensure the connection with electrodes, and the purpose of signal transmission through touch lines is mainly achieved by forming holes in the planarization layer under the existing design. However, in the case of a product of smaller size, the simultaneous presence of via-holes of a planarization layer probably leads that the distance between two via-holes of the planarization layer is too small and two adjacent via-holes of the planarization layer merge into a large via-hole, thereby causing uneven display and reducing the yield of the product

SUMMARY OF THE INVENTION

[0004] The object of the present disclosure is to provide an array substrate, a touch display screen and a manufacturing method of an array substrate, thereby reducing the probability of uneven display of a touch display screen and improving the yield of a product.

[0005] The present disclosure provides an array substrate used for a touch display screen, wherein the array substrate comprises

[0006] a substrate,

[0007] a polysilicon layer disposed on the substrate,

[0008] a dielectric layer disposed on the polysilicon layer and the substrate,

[0009] a touch line, a connecting line and a data line arranged sequentially at intervals on the dielectric layer, the touch line,

[0010] a planarization layer covering the connecting line and the data line;

[0011] wherein a first through-hole and a second through-hole arranged sequentially at intervals are formed on the planarization layer; the touch line is facing and exposed from the first through-hole; a portion of the connecting line is facing and exposed from the second through-hole;

[0012] a source and a drain, which are in contact with a portion of the surface of the polysilicon layer, are formed in the dielectric layer arranged at intervals; the drain is connected with the connecting line; the source is connected with the data line, and the first through-hole is completely misplaced with the second through-hole

[0013] The array substrate disclosed herein may further comprise a gate; the dielectric layer comprises a first dielectric layer and a second dielectric layer stacked on the first dielectric layer; the polysilicon layer is formed on the substrate and covered by the first dielectric layer, and the gate is formed on the first dielectric layer and covered by the second dielectric layer.

[0014] The array substrate disclosed herein may further comprise a common electrode layer disposed on the planarization layer, and the common electrode layer is connected with the touch line through the first through-hole.

[0015] The array substrate disclosed herein may further comprise a passivation layer, and the common electrode layer and the side wall of the second through-hole are covered by the passivation layer.

[0016] The array substrate disclosed herein may further comprise a pixel electrode layer, and the pixel electrode layer is disposed on the passivation layer and connected with the connecting line through the second through-hole.

[0017] The present disclosure further provides a touch display screen, and the touch display screen comprises the array substrates as described above.

[0018] The present disclosure further provides a manufacturing method of an array substrate comprising:

[0019] providing a substrate;

[0020] forming a polysilicon layer on the substrate;

[0021] forming a dielectric layer covering the polysilicon layer on the polysilicon layer, wherein the dielectric layer comprises a first dielectric layer and a second dielectric layer stacked on the first dielectric layer;

[0022] forming a source and a drain in contact with a portion of the surface of the polysilicon layer in the dielectric layer arranged at intervals;

[0023] forming a touch line, a connecting line and a data line on the dielectric layer arranged sequentially at intervals, wherein the drain is connected with the connecting line and the source is connected with the data line;

[0024] covering a planarization layer on the touch line, the connecting line and the data line and forming a first through-hole and a second through-hole on the planarization layer arranged sequentially at intervals; wherein the touch line is facing and exposed from the first through-hole; a portion of the connecting line is facing and exposed from the second through-hole; and the first through-hole is completely misplaced with the second through-hole.

[0025] The step of forming a dielectric layer covering the polysilicon layer on the polysilicon layer disclosed herein may further comprise:

[0026] forming the polysilicon layer on the substrate;

[0027] forming the first dielectric layer covering the polysilicon layer on the polysilicon layer;

[0028] forming a gate on the first dielectric layer;

[0029] forming the second dielectric layer covering the gate on the gate.

[0030] The step of forming a source and a drain in contact with a portion of the surface of the polysilicon layer in the dielectric layer arranged at intervals disclosed herein may further comprise: forming two spaced third through-holes in the dielectric layer, and the source and the drain are formed in the third through-holes,

[0031] After covering a planarization layer on the touch line, the connecting line and the data line and forming a first through-hole and a second through-hole on the planarization layer arranged sequentially at intervals, the manufacturing method disclosed herein may further comprise:

[0032] forming a common electrode layer on the planarization layer, wherein the common electrode layer is connected with the touch line through the first through-hole;

[0033] forming a passivation layer covering the common electrode layer and the side wall of the second through-hole on the common electrode layer;

[0034] forming a pixel electrode layer on the passivation layer, wherein the pixel electrode layer is connected with the connecting line through the second through-hole.

[0035] In summary, the first through-hole is completely misplaced with the second through-hole in the present disclosure, which realizes that the distance between the first through-hole and the second through-hole is increased and the probability of merging the first through-hole with the second through-hole is reduced, thereby effectively avoiding the risk of uneven display caused by small distance between the first through-hole and the second through-hole, and improving the performance of the touch display screen and the yield of the product. According to the present disclosure, the ouch line, the connecting line and the data line are arranged at intervals on the dielectric layer, which requires only one photomask for photolithography to obtain the touch line, the connecting line and the data line, and avoids the use of the traditional photoetching method that requires at least two masks to obtain the touch line, thereby simplifying the preparation of an array substrate, reducing production costs, improving the production efficiency, and improving the yield of the product.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] In order to illustrate implementations of present disclosure or the technical solutions of other implementations more clearly, the drawings according to the implementations of present disclosure or the drawings according to the other implementations will be introduced briefly. Apparently, hereinafter described drawings are merely a portion of implementations of present disclosure. For those skilled in the art, they can obtain other drawings on the base of these drawings without creative work.

[0037] FIG. **1** is a schematic sectional view of certain components of an array substrate provided by implementations of the present disclosure.

[0038] FIG. **2** is a plan view perspective diagram of a touch line, a connecting line, a data line and a polysilicon layer in the array substrate shown in FIG. **1**.

[0039] FIG. **3** is a schematic sectional view illustrating the array substrate shown in FIG. **1** having a planarization layer, a common electrode layer, a passivation layer and a pixel electrode layer.

[0040] FIG. **4** is a schematic diagram illustrating the process of manufacturing an array substrate provided by the present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

[0041] See FIG. **1** and FIG. **2**. The present disclosure provides an array substrate used for a touch display screen, wherein the array substrate comprises a substrate **10**; a polysilicon layer **60** disposed on the substrate **10**; a dielectric layer **20** disposed on the polysilicon layer **60** and the substrate **10**; a touch line **30**, a connecting line **40** and a data line **80** arranged sequentially at intervals on the dielectric layer **20**; a planarization layer **50** covering the touch line **30**, the connecting line **40** and the data line **80**, wherein a first through-hole **301** and a second through-hole **401** arranged sequentially at intervals are formed on the planarization layer **50**; the touch line **30** is facing and exposed from the first through-hole **301**; a portion of the connecting line **40** is facing and exposed from the second through-hole **401**; a source **703** and a drain **702**, which are in contact with a portion of the surface of the polysilicon layer **60**, are formed in the dielectric layer **20** arranged at intervals; the drain **702** is connected with the connecting line **40**; the source **703** is connected with the data line **80**, and the first through-hole **301** is completely misplaced with the second through-hole **401**.

[0042] The first through-hole **301** is completely misplaced with the second through-hole **401** in the present disclosure, which realizes that the distance between the first through-hole **301** and the second through-hole **401** is increased and the probability of merging the first through-hole **301** with the second through-hole **401** is reduced, thereby effectively avoiding the risk of uneven display caused by small distance between the first through-hole **301** and the second through-hole **401**, and improving the performance of the touch display screen and the yield of the product.

[0043] According to the present disclosure, the ouch line, the touch line **30**, the connecting line **40** and the data line **80** are arranged at intervals on the dielectric layer **20**, which requires only one photomask for photolithography to obtain the touch line **30**, the connecting line **40** and the data line **80**, and avoids the use of the traditional photoetching method that requires at least two masks to obtain the touch line **3**, thereby simplifying the preparation of an array substrate, reducing production costs, improving the production efficiency, and improving the yield of a product.

[0044] For the convenience of description, the extension direction of the touch line **30** is defined as a first direction L**1**, and the direction perpendicular to the first direction L**1** is defined as a second direction L**2**. Specifically, the first through-hole **301** is formed on the planarization layer **50** and extends to the surface of the touch line **30**, the second through-hole **401** is formed on the planarization layer **50** and extends to the surface of the connecting line **40**, the center of the first through-hole **301** and the center of the second hole **401** are not on the straight line of the second direction L**2** at the same time, and the first through-hole **301** is completely misplaced with the second through-hole **401**. The specific location of the first through-hole **301** on the touch line **30** and the specific location of the second through-hole **401** on the connecting line **40** are not limited in the present disclosure so long as the first through-hole **301** is completely misplaced with the second through-hole **401**. In the implementation, the array substrate comprises a thin film transistor **70**, the thin film transistor **70** comprises the source **703** and the drain **702**, the drain **702** is near the second through-hole **401**, and the two ends of the drain **702** are connected with the polysilicon layer **60** and the connecting line **40** respectively, the drain **703** is far away from the second through-hole **401** and the two ends of the source **703** are connected with the polysilicon layer **60** and the data line **80**, respectively.

[0045] Thin film transistor **70** further comprises a gate **701**, the dielectric layer **20** comprises a first dielectric layer **201** and a second dielectric layer **202** stacked on the first dielectric layer **201**, the polysilicon layer **60** is formed on the substrate **10** and covered by the first dielectric layer **201**, and

the gate **701** is formed on the first dielectric layer **201** and covered by the second dielectric layer **202**. In the implementation, the gate **701** is formed between the source **703** and the drain **702**.

[0046] See FIG. **3**. The array substrate further comprises a common electrode layer **90** disposed on the planarization layer **50**, and the common electrode layer **90** is connected with the touch line **30** through the first through-hole **301**. Specifically, the common electrode layer **90** comprises a first common electrode **901** and a second common electrode **902** connected with the first common electrode **901**, and the first common electrode **901** is filled in the first through-hole **301** and connected with the touch line **30**, and the planarization layer is covered by the second common electrode **902**.

[0047] The array substrate further comprises a passivation layer **100**, and the common electrode layer **90** and the side wall of the second through-hole **401** are covered by the passivation layer **100**. Specifically, the passivation layer **100** is an organic film. The passivation layer **100** comprises a first passivation sublayer **1001** and a second passivation sublayer **1002** connected with the first passivation sublayer **1001**, the second common electrode **902** is covered by the first passivation sublayer **1001**, and the second passivation sublayer **1002** is fitted to the sides of the common electrode layer **90** and the flat layer **50** and extends into the second through-hole **401**. That is to say, the second passivation sublayer **1002** is fitted to the side wall of the second through-hole **401** and is connected with part of bottom wall of the second through-hole **401**.

[0048] The array substrate further comprises a pixel electrode layer **110**, and the pixel electrode layer **110** is disposed on the passivation layer **100** and connected with the connecting line **40** through the second through-hole **401**. Specifically, the pixel electrode layer **110** comprises a first sub-pixel electrode **1101** and a second sub-pixel electrode **1102** connected with the first sub-pixel electrode **1101**, the first sub-pixel electrode **1101** extends into the second through-hole **401** and is connected with the connecting line **40**, and the second sub-pixel electrode **1102** is disposed between the first sub-pixel electrode **1101** and the side wall of the second through-hole **401**. In the implementation, a projection of the second through-hole **401** on the substrate **10** is misplaced with those of the source **703** and the drain **702** on the substrate **10**. The drain is connected with the pixel electrode layer **110** through the connecting line **40**. Since a projection of the second through-hole **401** on the substrate **10** is misplaced with those of the source **703** and the drain **702** on the substrate **10**, the drain **702** and the pixel electrode layer **110** need to be connected through the connecting line **40**, and the connection of the connecting line **40** improves the electrical connection between the drain **702** and the pixel electrode layer **110**. Therefore, the stability of the array substrate is improved because of the misplacement between a projection of the second through-hole **401** on the substrate **10** and those of the source **703** and the drain **702** on the substrate **10**. The misplacement between a projection of the second through-hole **401** on the substrate **10** and those of the source **703** and the drain **702** on the substrate **10** can be partial or complete misplacement.

[0049] The present disclosure provides a touch display screen, and the touch display screen comprises the array substrates as described above. The touch display screen of the present disclosure realizes that the distance between the first through-hole **301** and the second through-hole **401** is increased and the probability of merging the first through-hole **301** with the second through-hole **401** is reduced, thereby effectively avoiding the risk of uneven display caused by small distance between the first through-hole **301** and the second through-hole **401**, and improving the performance of the touch display screen and the yield of the product. According to the present disclosure, the ouch line, the touch line **30**, the connecting line **40** and the data line **80** are arranged at intervals on the dielectric layer **20**, which requires only one photomask for photolithography to obtain the touch line **30**, the connecting line **40** and the data line **80**, and avoids the use of the traditional photoetching method that requires at least two masks to obtain the touch line **30**, thereby simplifying the preparation of an array substrate, reducing production costs, improving the production efficiency, and improving the yield of a product.

[0050] See FIG. **4**. The present disclosure provides a manufacturing method of an array substrate, and the manufacturing method comprises following step **1**, step **2**, step **3**, step **4**, step **5** and step **6**.

[0051] At step **1**, a substrate **10** is provided,

[0052] At step **2**, a polysilicon layer **60** is formed on the substrate.

[0053] At step **3**, a dielectric layer **20** covering the polysilicon layer **60** is formed on the polysilicon layer **60**, wherein the dielectric layer **20** comprises a first dielectric layer **201** and a second dielectric layer **202** stacked on the first dielectric layer **201**.

[0054] Further, the step of forming a dielectric layer covering the polysilicon layer on the polysilicon layer further comprises:

[0055] forming the polysilicon layer **60** on the substrate **10**;

[0056] forming the first dielectric layer **201** covering the polysilicon layer **60** on the polysilicon layer **60**;

[0057] forming a gate **701** on the first dielectric layer **201**;

[0058] forming the second dielectric layer **202** covering the gate **701** on the gate **701**.

[0059] At step **4**, a source **703** and a drain **702** in contact with a portion of the surface of the polysilicon layer **60** are formed in the dielectric layer **20** arranged at intervals.

[0060] Further, the step **4** further comprises: forming two spaced third through-holes in the dielectric layer **20**, and the source **703** and the drain **702** are formed in the third through-holes.

[0061] At step **5**, a touch line **30**, a connecting line **40** and a data line **80** are formed on the dielectric layer **20** arranged sequentially at intervals, wherein the drain **702** is connected with the connecting line **40** and the source **703** is connected with the data line **80**,

[0062] At step **6**, a planarization layer **50** is covered on the touch line **30**, the connecting line **40** and the data line **80**; a first through-hole **301** and a second through-hole **401** are formed on the planarization layer **50** arranged sequentially at intervals; wherein the touch line **30** is facing and exposed from the first through-hole **301**; a portion of the connecting line **40** is facing and exposed from the second through-hole **401**, and the first through-hole **301** is completely misplaced with the second through-hole **401**.

[0063] In this step, a projection of the second through-hole **401** on the substrate **10** is misplaced with those of the source **703** and the drain **702** on the substrate **10**. That is to say, a projection of the second through-hole **401** on the substrate **10** is misplaced with those of the third second through-holes.

The connection between the second through-hole **401** and the third through-hole through the connecting line **40** is achieved by the misplacement between the second through-hole **401** and the third through-holes, thus improving the electrical connection between materials in the second hole **401** and materials in the third through-hole and improving the stability of the array substrate.

[0064] Further, after covering a planarization layer **50** on the touch line **30**, the connecting line **40** and the data line **80** and forming a first through-hole **301** and a second through-hole **401** on the planarization layer **50** arranged sequentially at intervals, the manufacturing method further comprises:

[0065] forming a common electrode layer **90** on the planarization layer **50**, wherein the common electrode layer **90** is connected with the touch line **30** through the first through-hole **301**;

[0066] forming a passivation layer **100** covering the common electrode layer **90** and the side wall of the second through-hole **401** on the common electrode layer **90**;

[0067] forming a pixel electrode layer **110** on the passivation layer **100**, wherein the pixel electrode layer **110** is connected with the connecting line **40** through the second through-hole **410**.

[0068] The above disclosure is merely preferred implementations of the present disclosure, but the disclosure is not to be construed as being limited thereto. Those skilled in the art can understand all or part of the process of implementing the above implementations and equivalent changes made to the implementations in accordance with the claim of the present disclosure shall be covered within the scope of the present disclosure.

What is claimed is:

1. An array substrate used for a touch display screen, wherein the array substrate comprises

a substrate;

a polysilicon layer disposed on the substrate;

a dielectric layer disposed on the polysilicon layer and the substrate;

a touch line, a connecting line and a data line arranged sequentially at intervals on the dielectric layer, the touch line;

a planarization layer covering the connecting line and the data line;

wherein a first through-hole and a second through-hole arranged sequentially at intervals are formed on the planarization layer; the touch line is facing and exposed from the first through-hole; a portion of the connecting line is facing and exposed from the second through-hole;

a source and a drain, which are in contact with a portion of the surface of the polysilicon layer, are formed in the dielectric layer arranged at intervals; the drain is connected with the connecting line; the source is connected with the data line, and the first through-hole is completely misplaced with the second through-hole.

2. The array substrate as claimed in claim **1**, wherein the array substrate further comprises a gate; the dielectric layer comprises a first dielectric layer and a second dielectric layer stacked on the first dielectric layer; the polysilicon layer is formed on the substrate and covered by the first dielectric layer, and the gate is formed on the first dielectric layer and covered by the second dielectric layer.

3. The array substrate as claimed in claim **2**, wherein the array substrate further comprises a common electrode layer disposed on the planarization layer, and the common electrode layer is connected with the touch line through the first through-hole.

4. The array substrate as claimed in claim **3**, wherein the array substrate further comprises a passivation layer, and the common electrode layer and the side wall of the second through-hole are covered by the passivation layer.

5. The array substrate as claimed in claim **4**, wherein the array substrate further comprises a pixel electrode layer, and the pixel electrode layer is disposed on the passivation layer and connected with the connecting line through the second through-hole.

6. A touch display screen, wherein the touch display screen comprises the array substrates as claimed in claim **1**.

7. The touch display screen as claimed in claim **6**, wherein the array substrate further comprises a gate; the dielectric layer comprises a first dielectric layer and a second dielectric layer stacked on the first dielectric layer; the polysilicon layer is formed on the substrate and covered by the first dielectric layer, and the gate is formed on the first dielectric layer and covered by the second dielectric layer.

8. The touch display screen as claimed in claim **7**, wherein the array substrate further comprises a common electrode layer disposed on the planarization layer, and the common electrode layer is connected with the touch line through the first through-hole.

9. The touch display screen as claimed in claim **8**, wherein the array substrate further comprises a passivation layer, and the common electrode layer and the side wall of the second through-hole are covered by the passivation layer.

10. The touch display screen as claimed in claim **9**, wherein the array substrate further comprises a pixel electrode layer, and the pixel electrode layer is disposed on the passivation layer and connected with the connecting line through the second through-hole.

11. A manufacturing method of an array substrate, wherein the manufacturing method of an array substrate comprises:

providing a substrate;

forming a polysilicon layer on the substrate;

forming a dielectric layer covering the polysilicon layer on the polysilicon layer, wherein the dielectric layer comprises a first dielectric layer and a second dielectric layer stacked on the first dielectric layer;

forming a source and a drain in contact with a portion of the surface of the polysilicon layer in the dielectric layer arranged at intervals;

forming a touch line, a connecting line and a data line on the dielectric layer arranged sequentially at intervals, wherein the drain is connected with the connecting line and the source is connected with the data line;

covering a planarization layer on the touch line, the connecting line and the data line and forming a first through-hole and a second through-hole on the planarization layer arranged sequentially at intervals; wherein the touch line is facing and exposed from the first through-hole; a portion of the connecting line is facing and exposed from the second through-hole; and the first through-hole is completely misplaced with the second through-hole.

12. The manufacturing method of the array substrate as claimed in claim **11**, wherein the step of forming a dielectric layer covering the polysilicon layer on the polysilicon layer further comprises:

forming the polysilicon layer on the substrate;
forming the first dielectric layer covering the polysilicon layer on the polysilicon layer;
forming a gate on the first dielectric layer;
forming the second dielectric layer covering the gate on the gate.

13. The manufacturing method of the array substrate as claimed in claim **12**, wherein the step of forming a source and a drain in contact with a portion of the surface of the polysilicon layer in the dielectric layer arranged at intervals further comprises: forming two spaced third through-holes in the dielectric layer, and the source and the drain are formed in the third through-holes.

14. The manufacturing method of the array substrate as claimed in claim **13**, after covering a planarization layer on the touch line, the connecting line and the data line and forming a first through-hole and a second through-hole on the planarization layer arranged sequentially at intervals, wherein the manufacturing method further comprises:
forming a common electrode layer on the planarization layer, wherein the common electrode layer is connected with the touch line through the first through-hole;
forming a passivation layer covering the common electrode layer and the side wall of the second through-hole on the common electrode layer;
forming a pixel electrode layer on the passivation layer, wherein the pixel electrode layer is connected with the connecting line through the second through-hole.

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