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HASEGAWA et al.

(54) **DIAGNOSIS METHOD, CHARGED PARTICLE BEAM LITHOGRAPHY APPARATUS, AND RECORDING MEDIUM**

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(57) **ABSTRACT**

Disclosed is a method of diagnosing a conversion process for converting a format of image data including unit data corresponding to charged particle beams into a format suitable for an aperture array, the aperture array having a plurality of controllers provided to match a plurality of the charged particle beams to control the charged particle beams, and a driver configured to drive the controllers. The method includes: extracting the unit data having an identical first rank based on an arrangement of the unit data in the image data from the unit data of each block including a predetermined number of the unit data and calculating a first checksum of each of the first rank; extracting the unit data having an identical second rank after the conversion process from the unit data of each block and calculating a second checksum of each of the second rank; and comparing the first and second checksums.

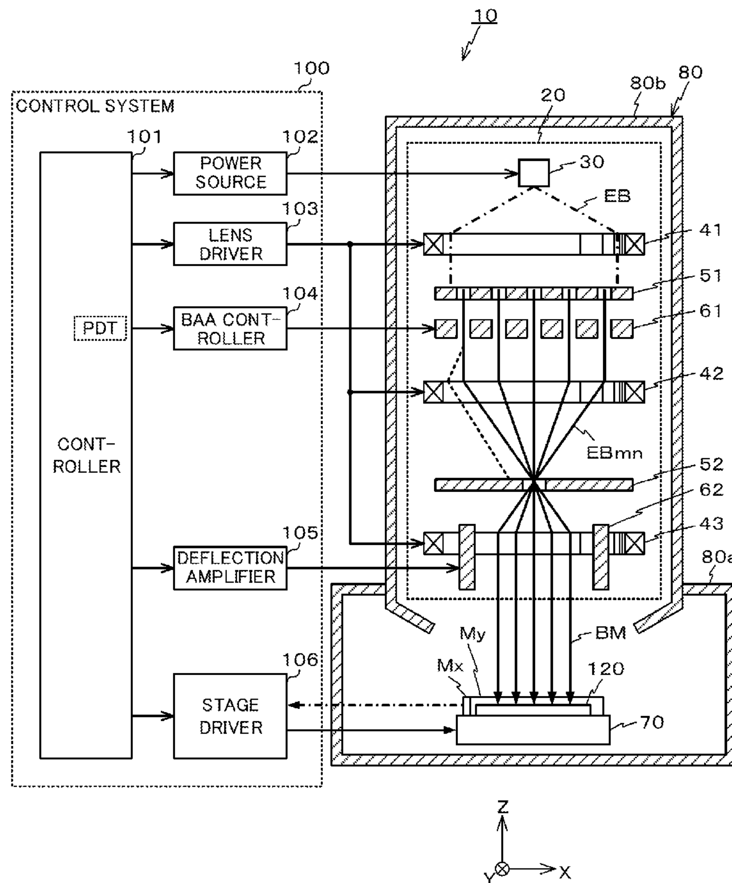


FIG.1

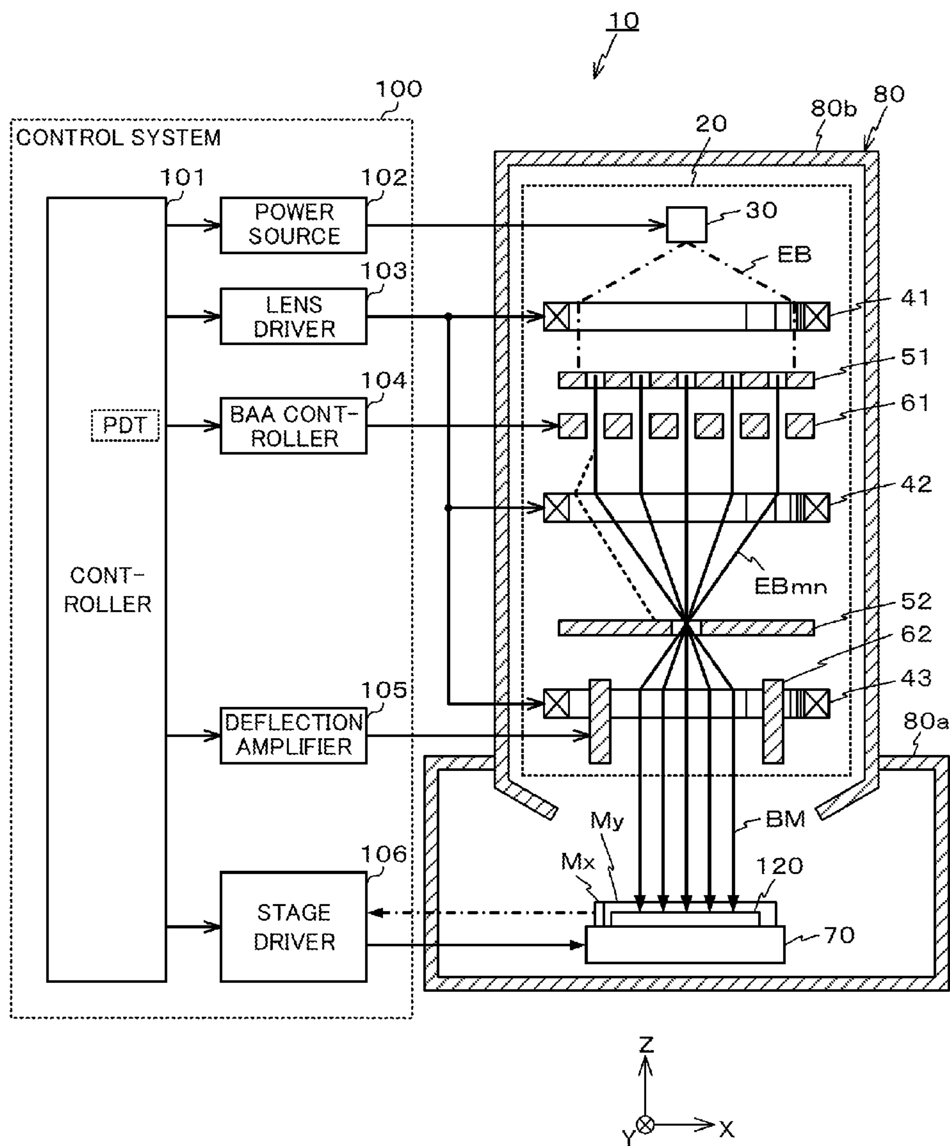


FIG.2

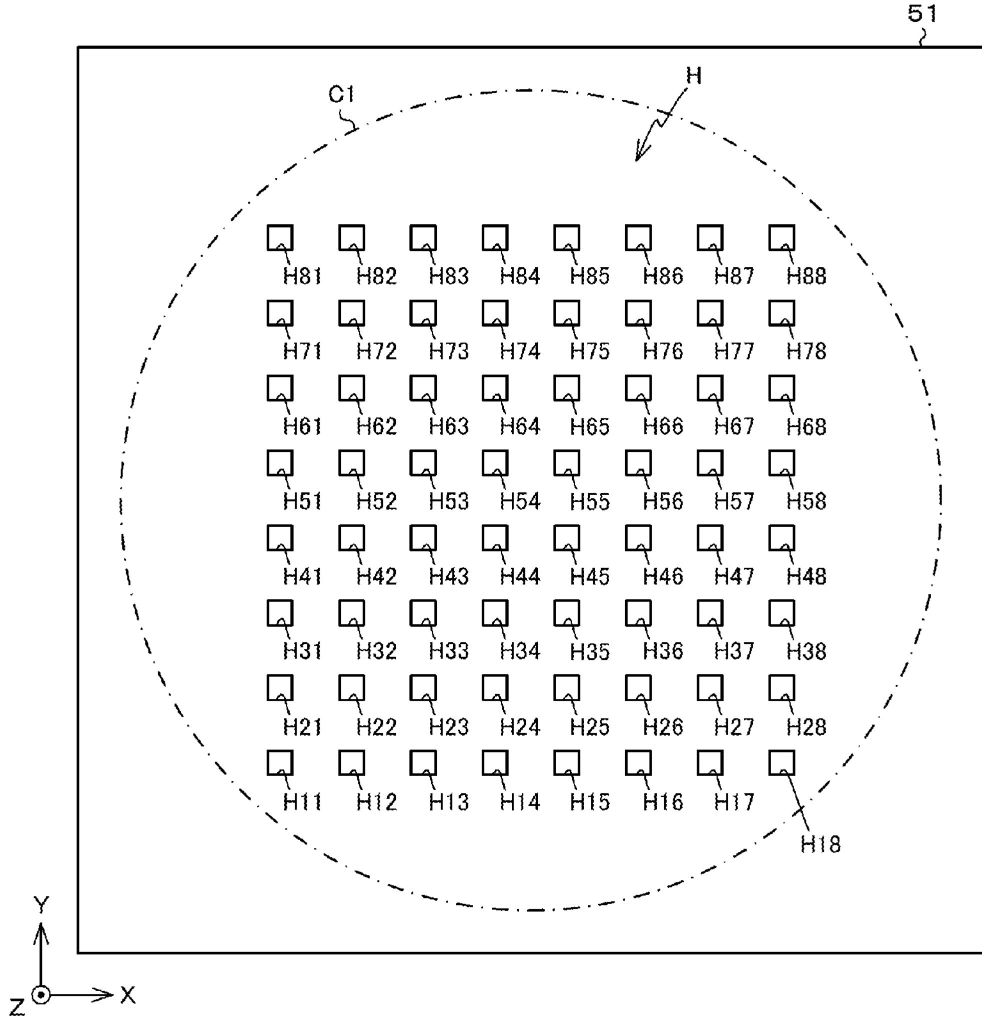


FIG.3

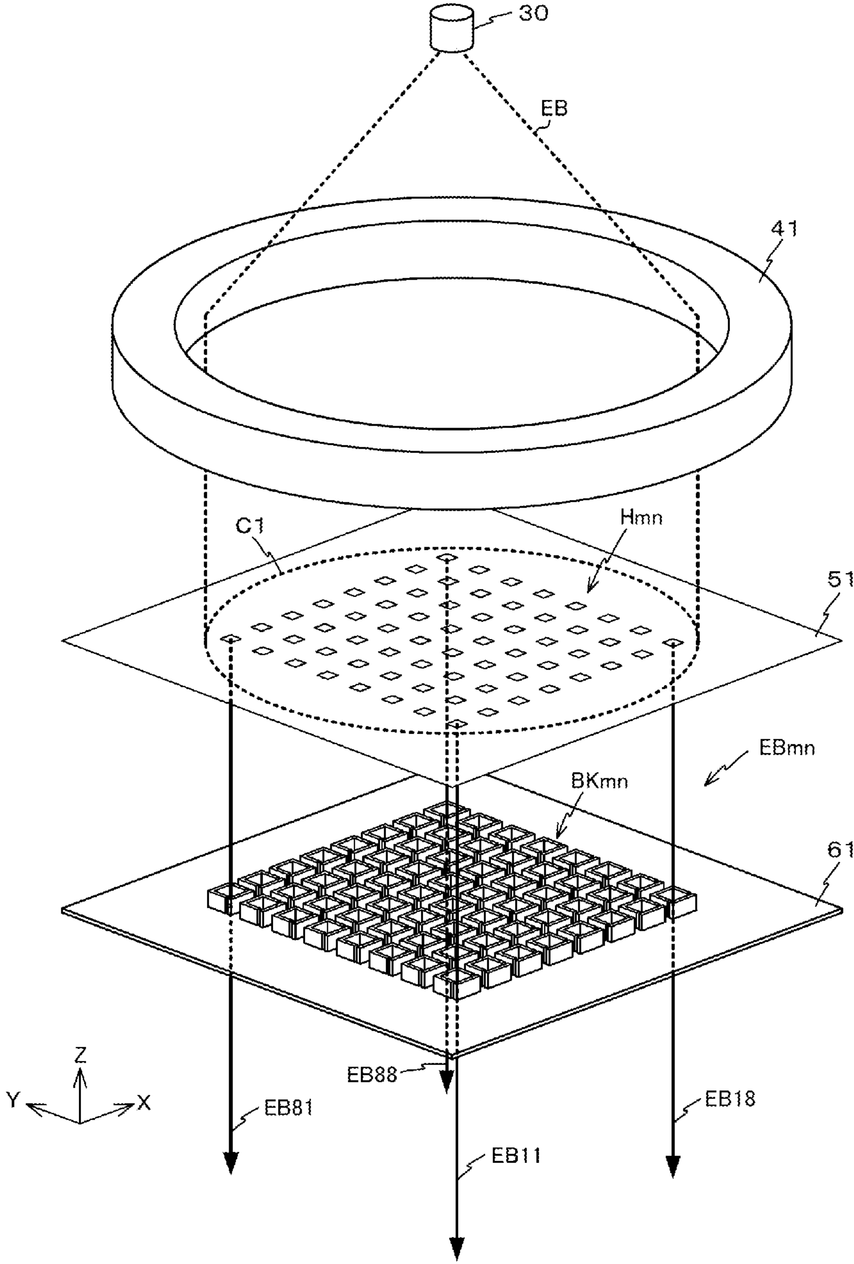


FIG.4

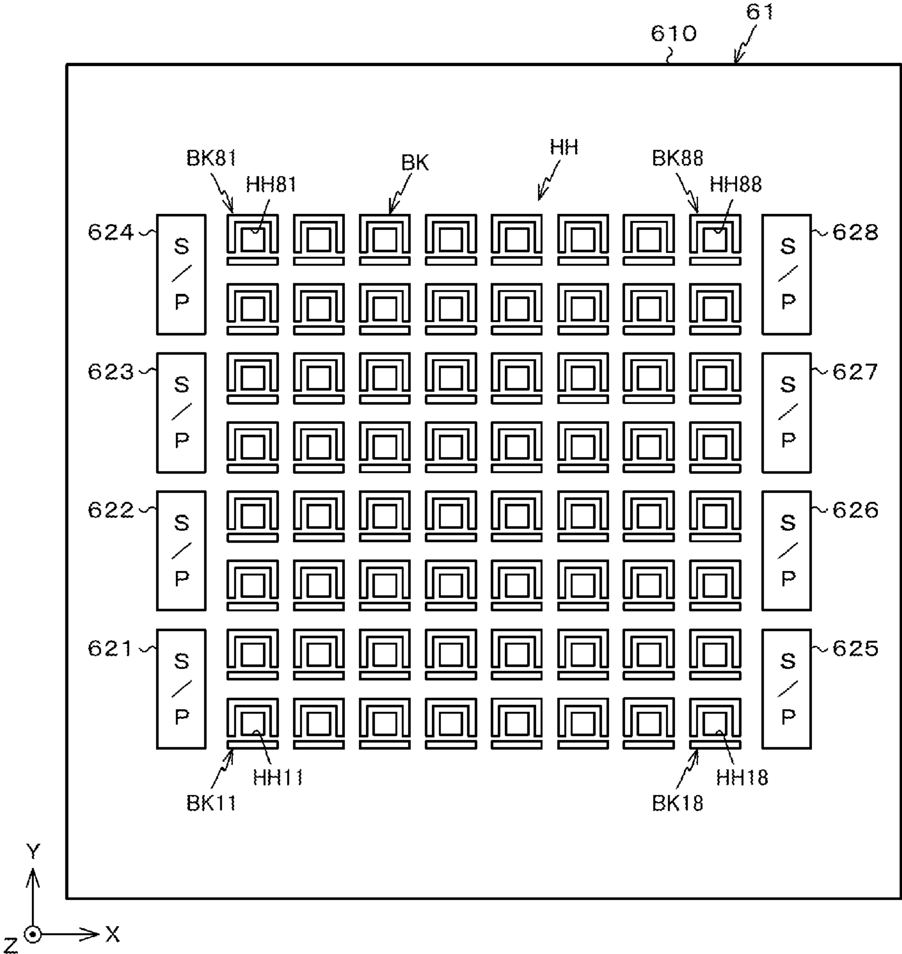


FIG.5

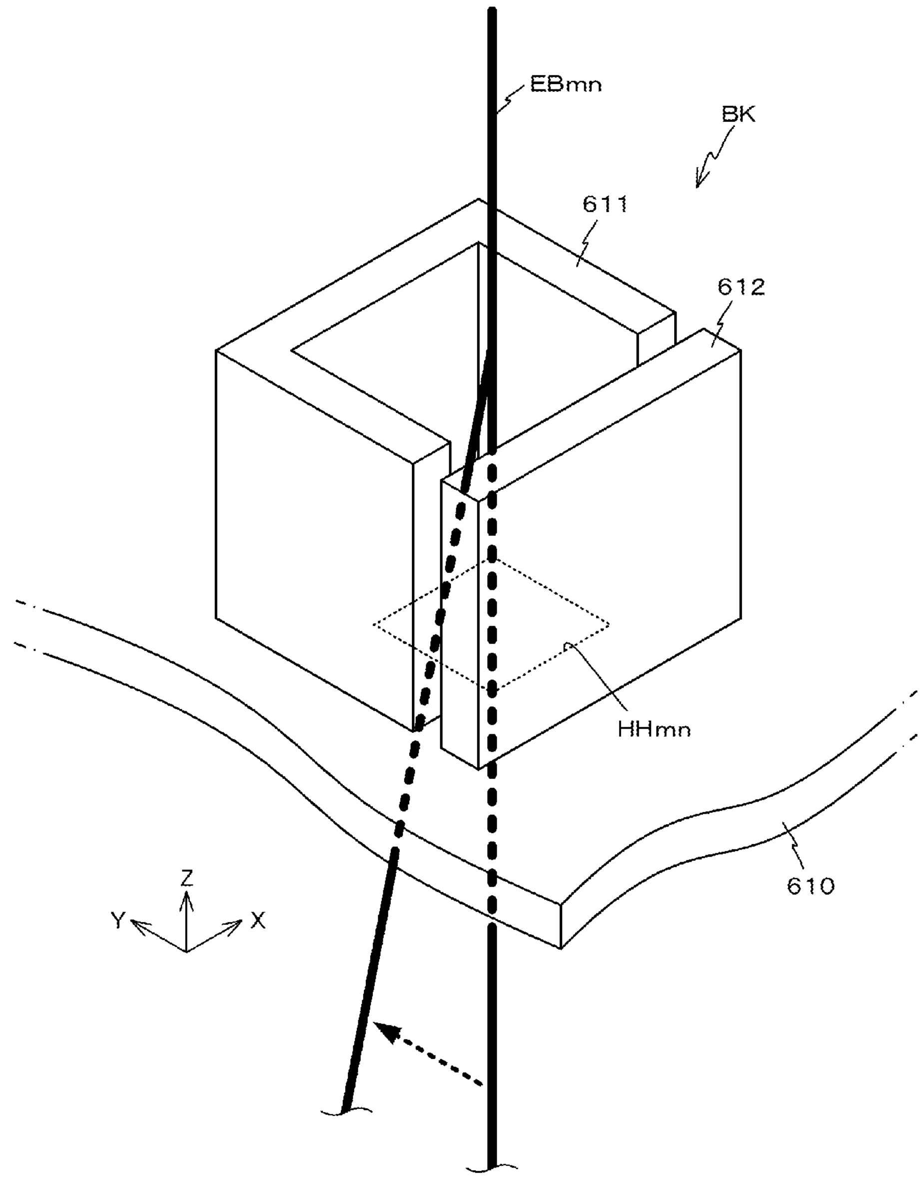


FIG.6

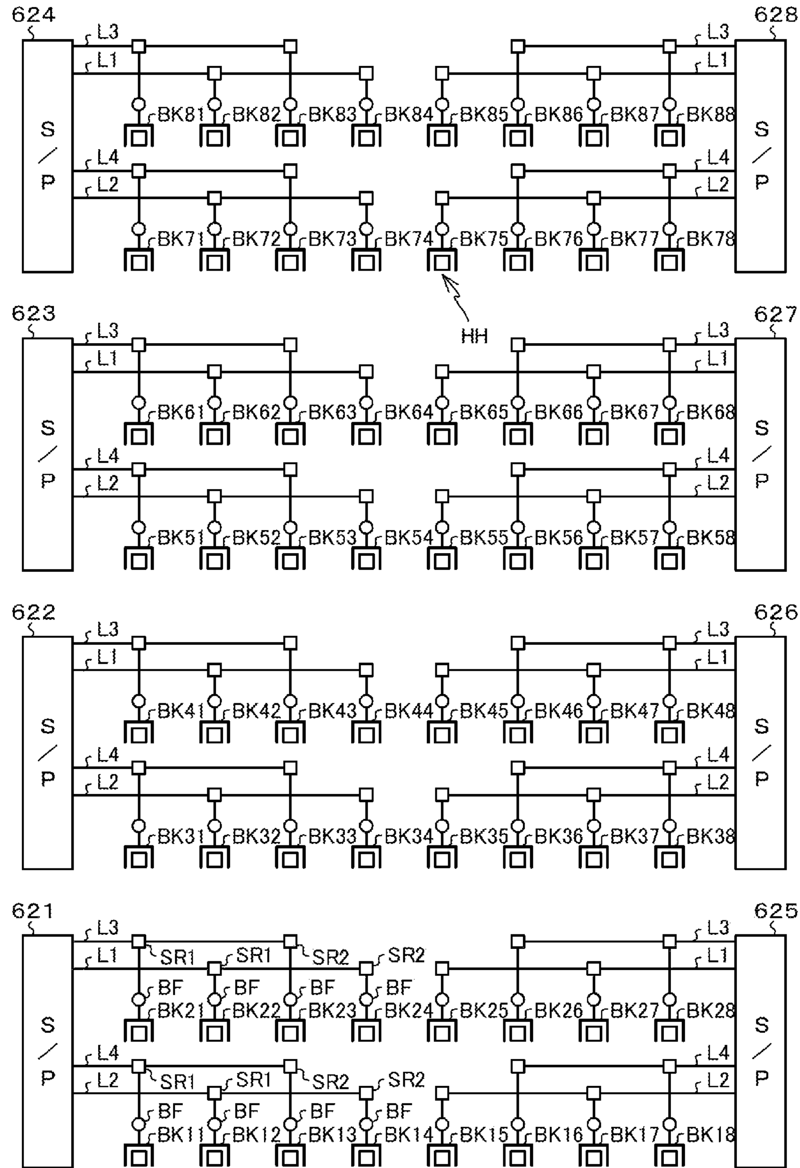


FIG.7

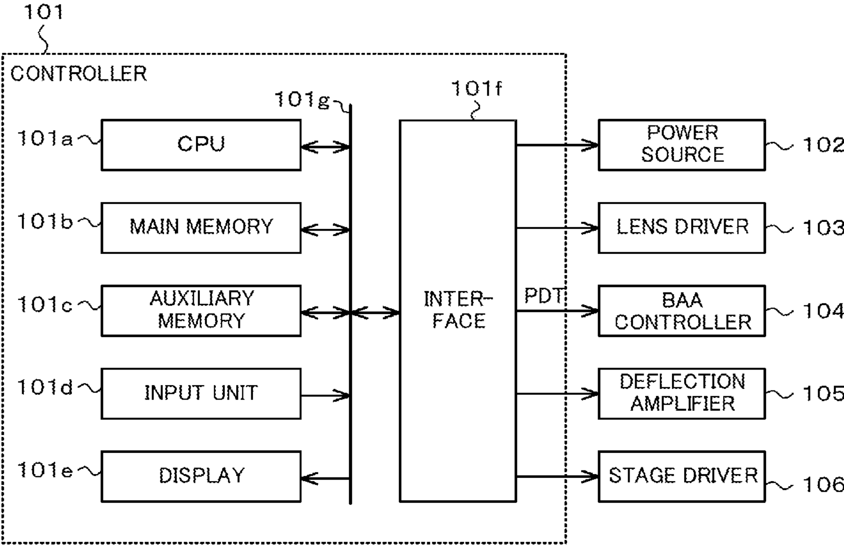


FIG.8

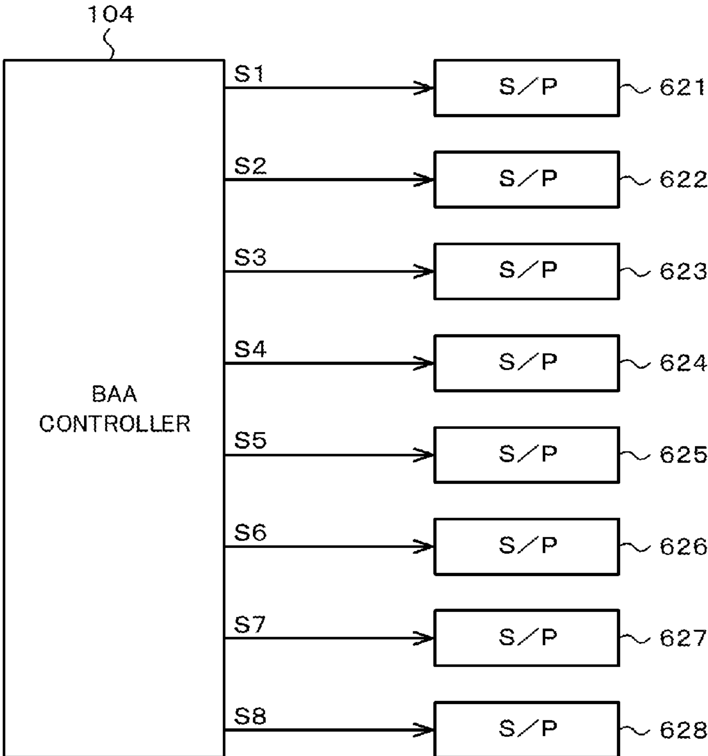
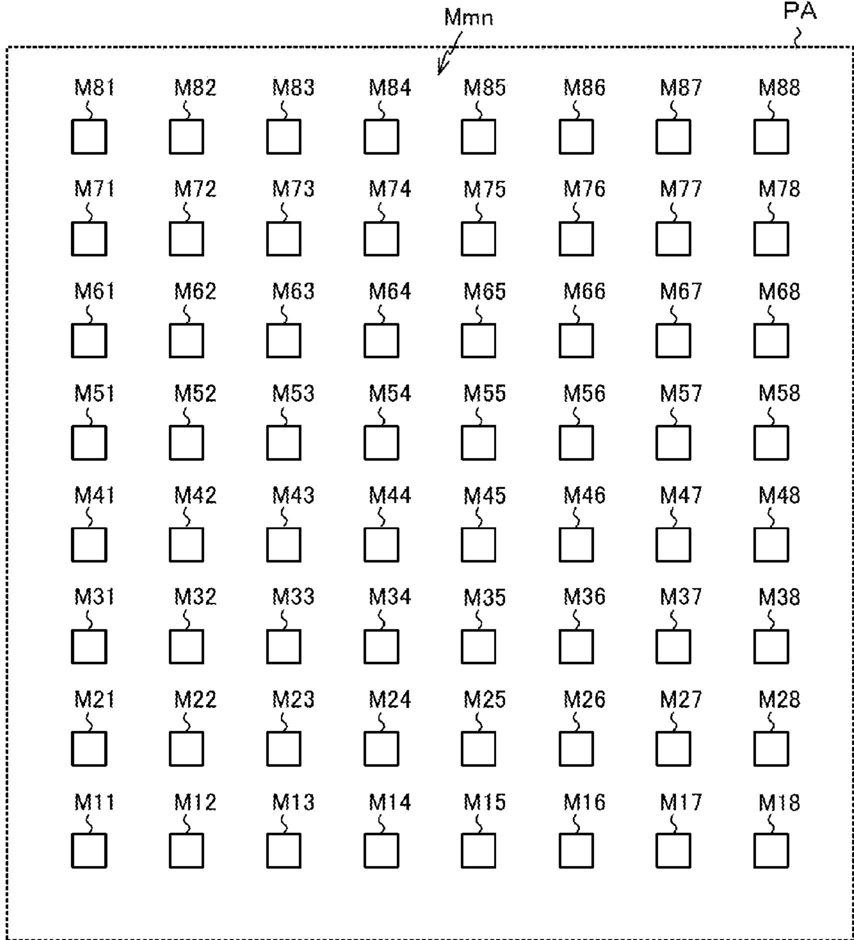


FIG.9



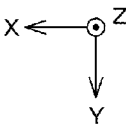


FIG.10

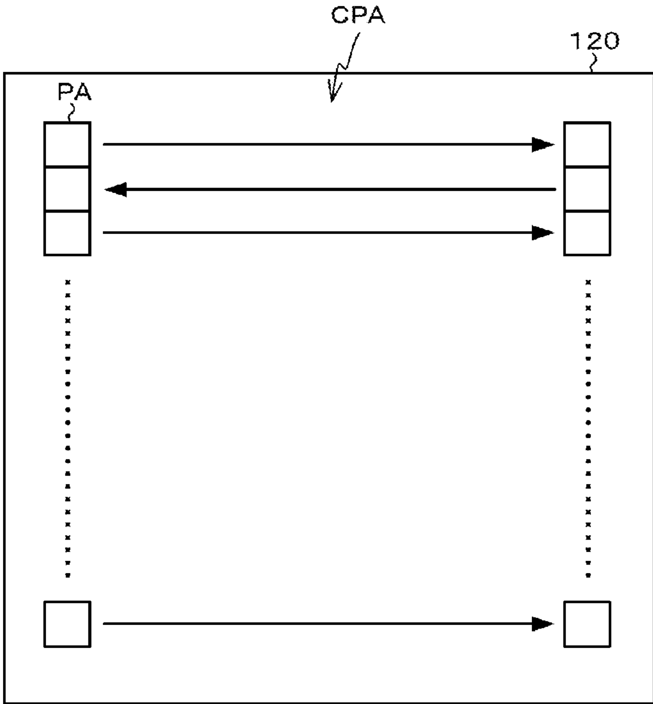


FIG.11

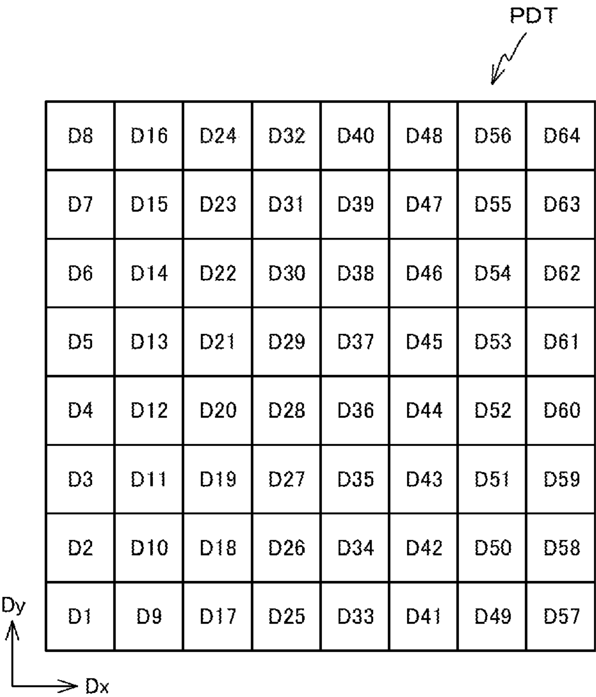


FIG.12

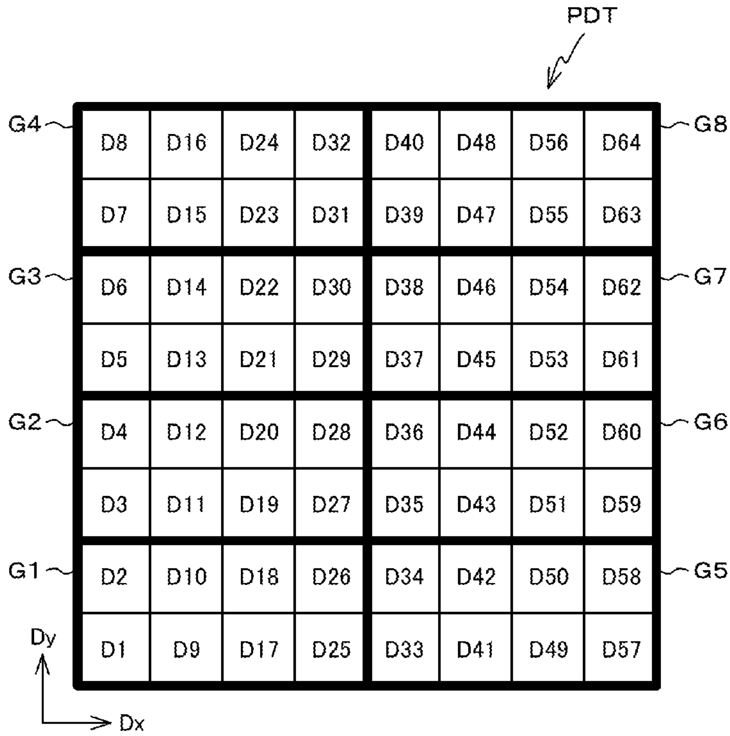


FIG.13

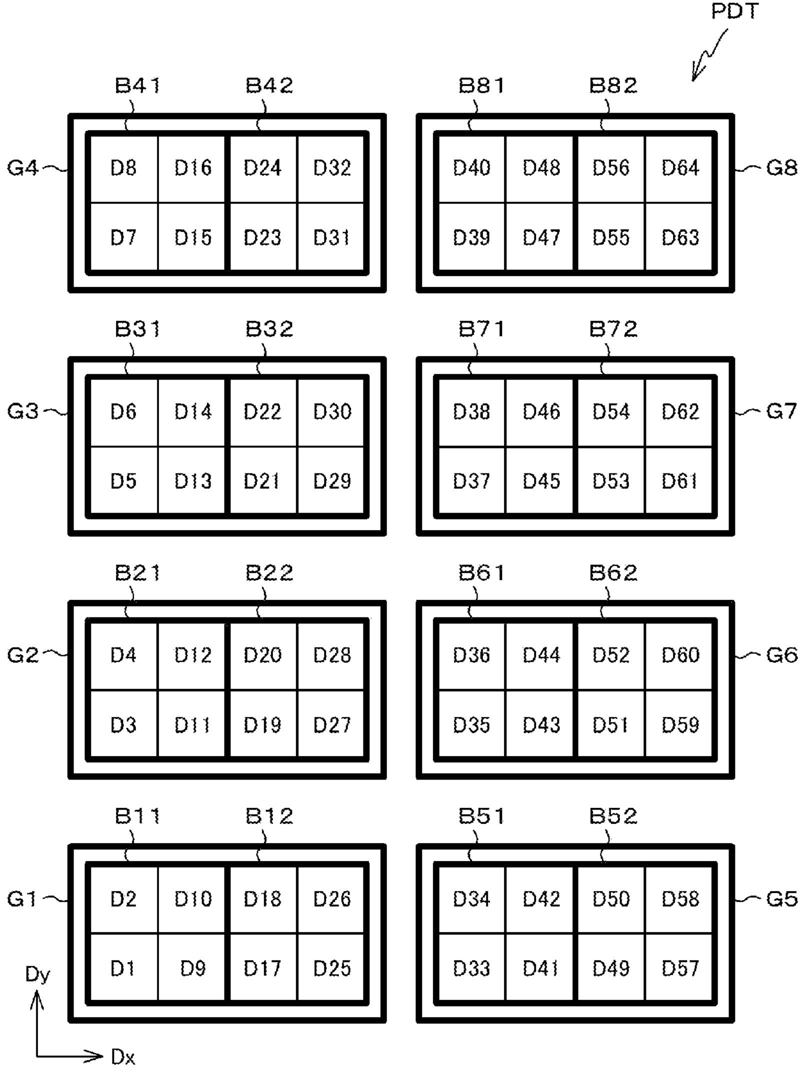


FIG.14

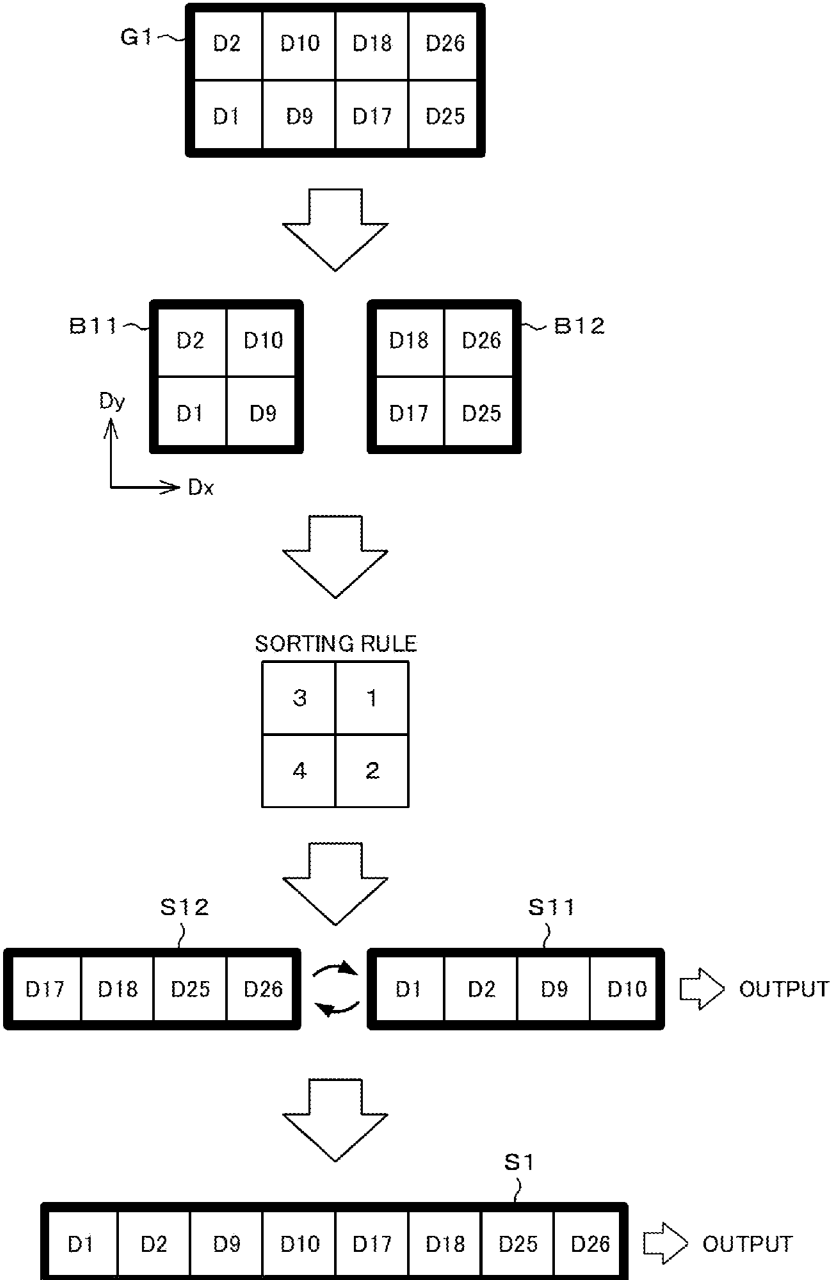


FIG.15

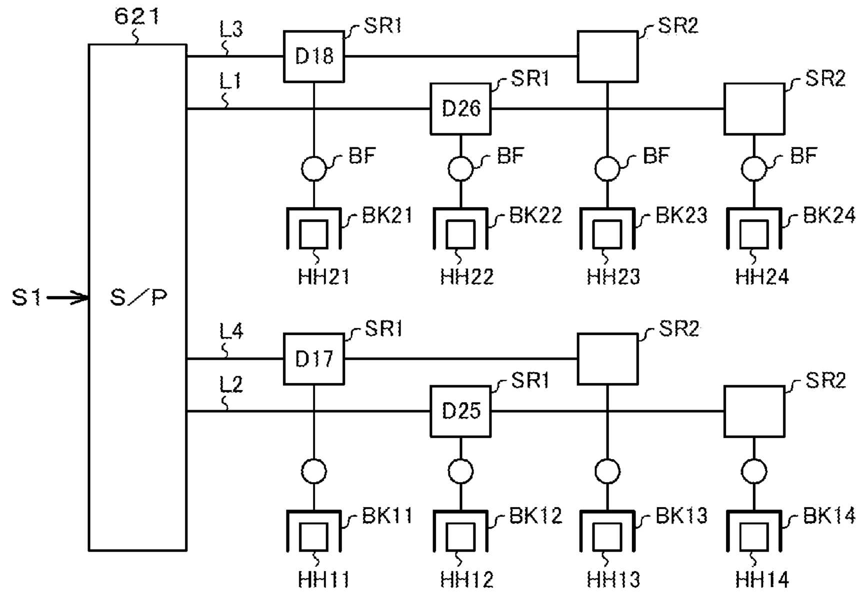


FIG.16

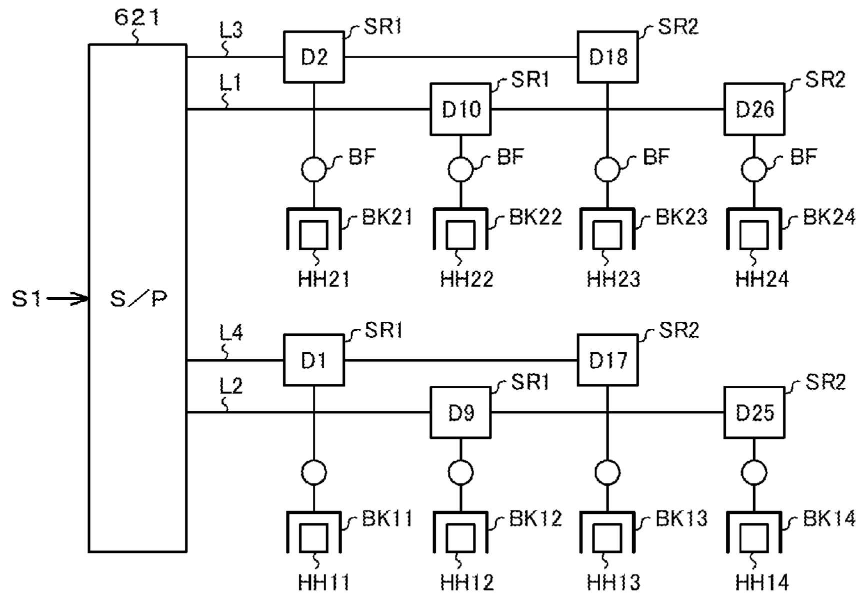
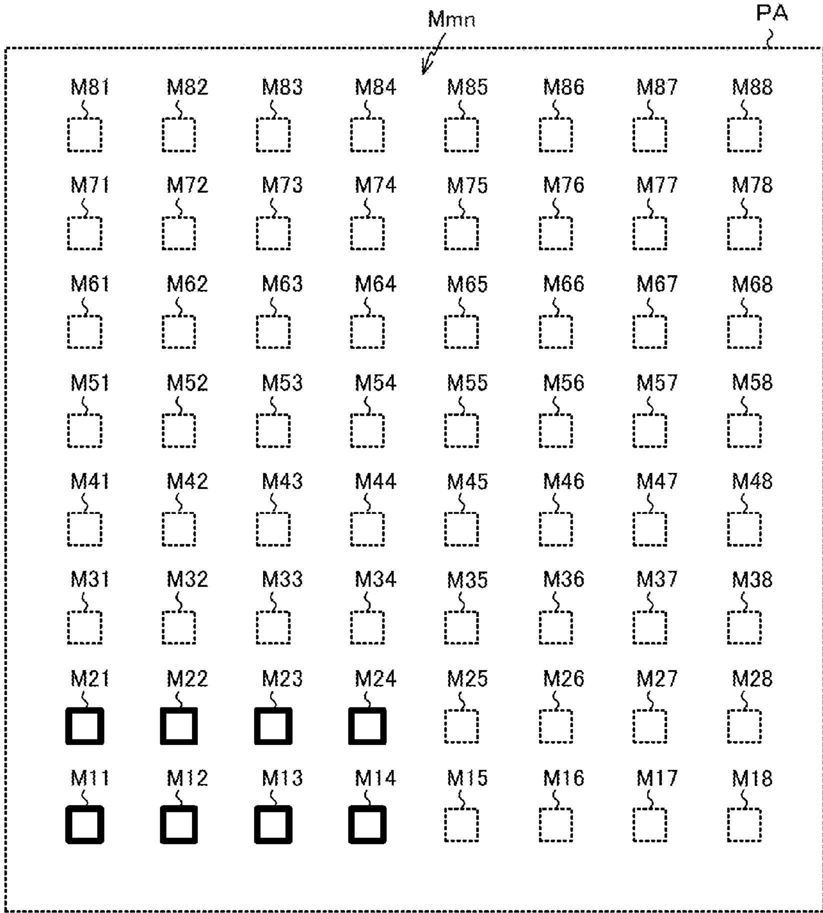


FIG.17



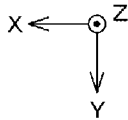


FIG.18

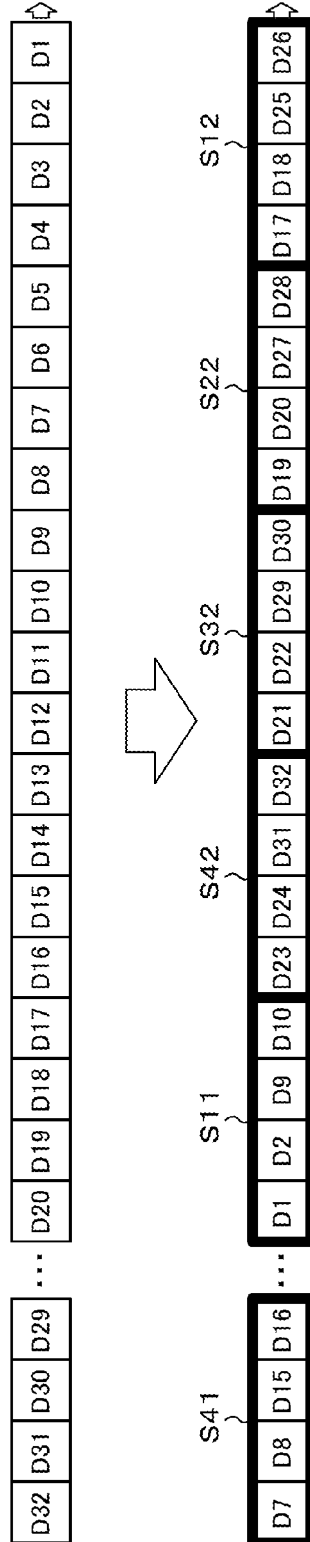


FIG.19

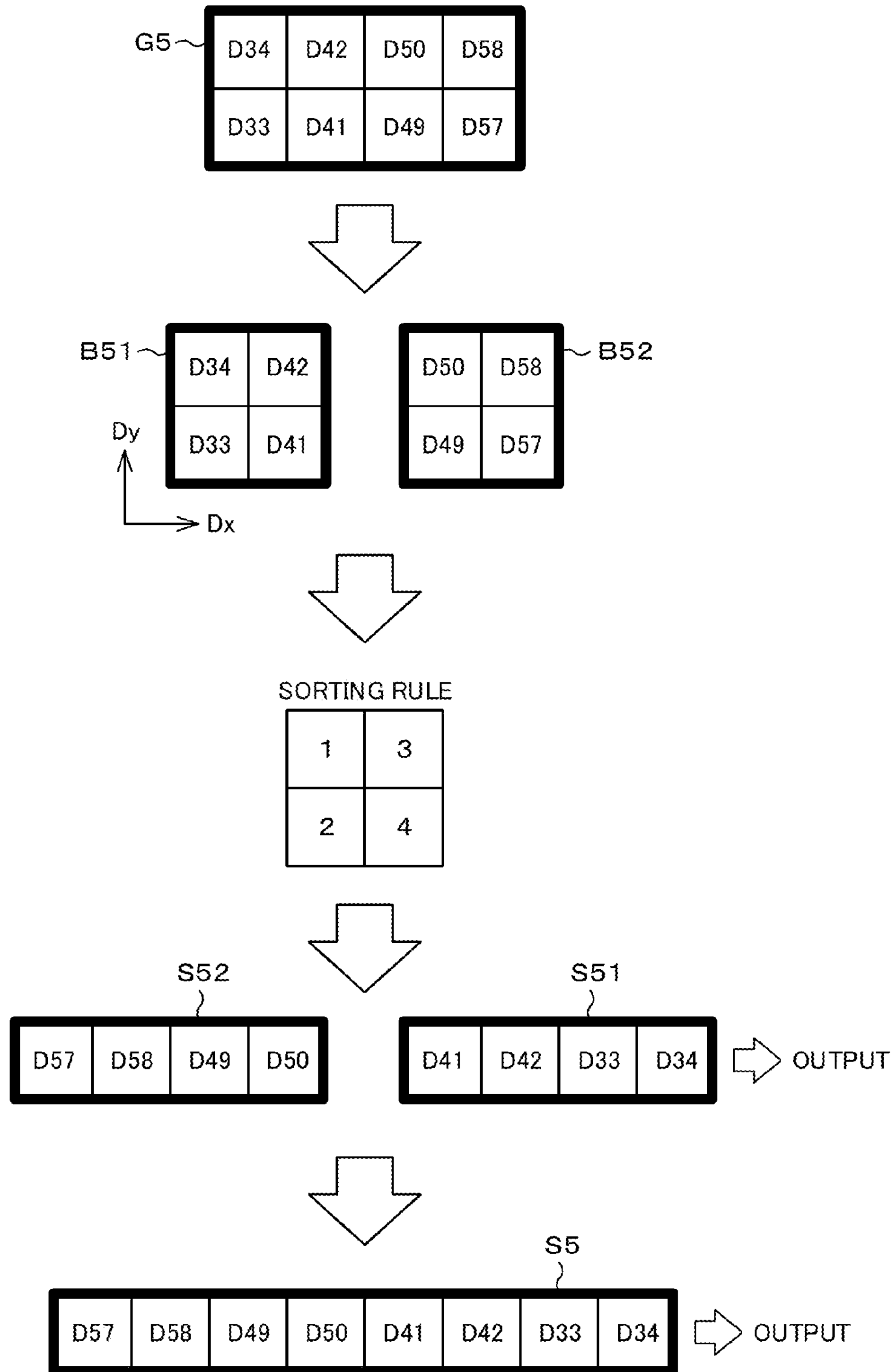


FIG.20

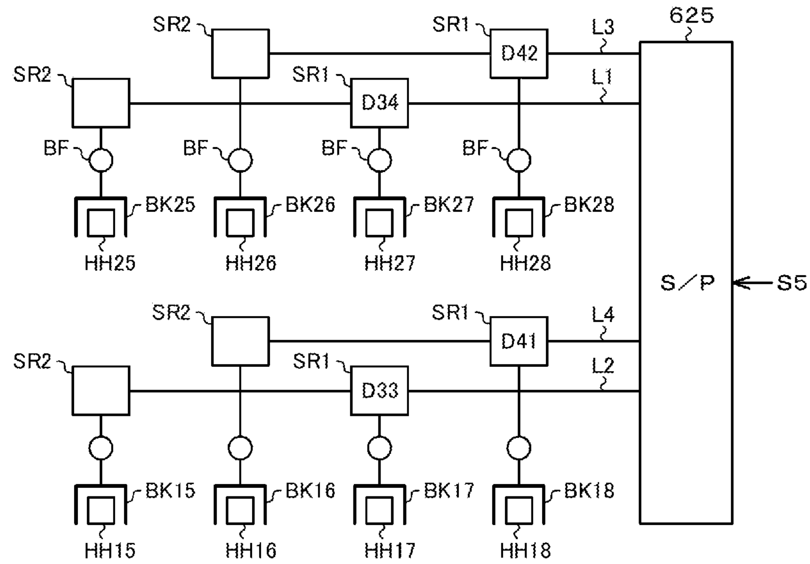


FIG.21

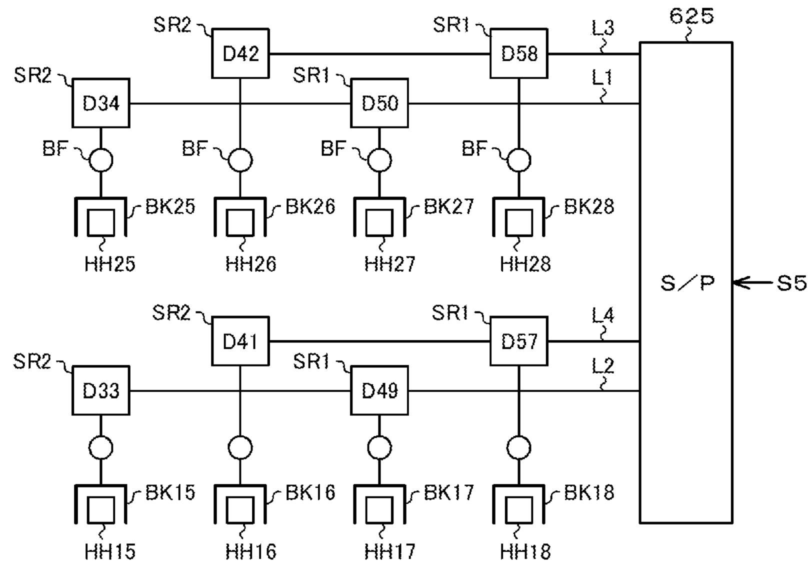
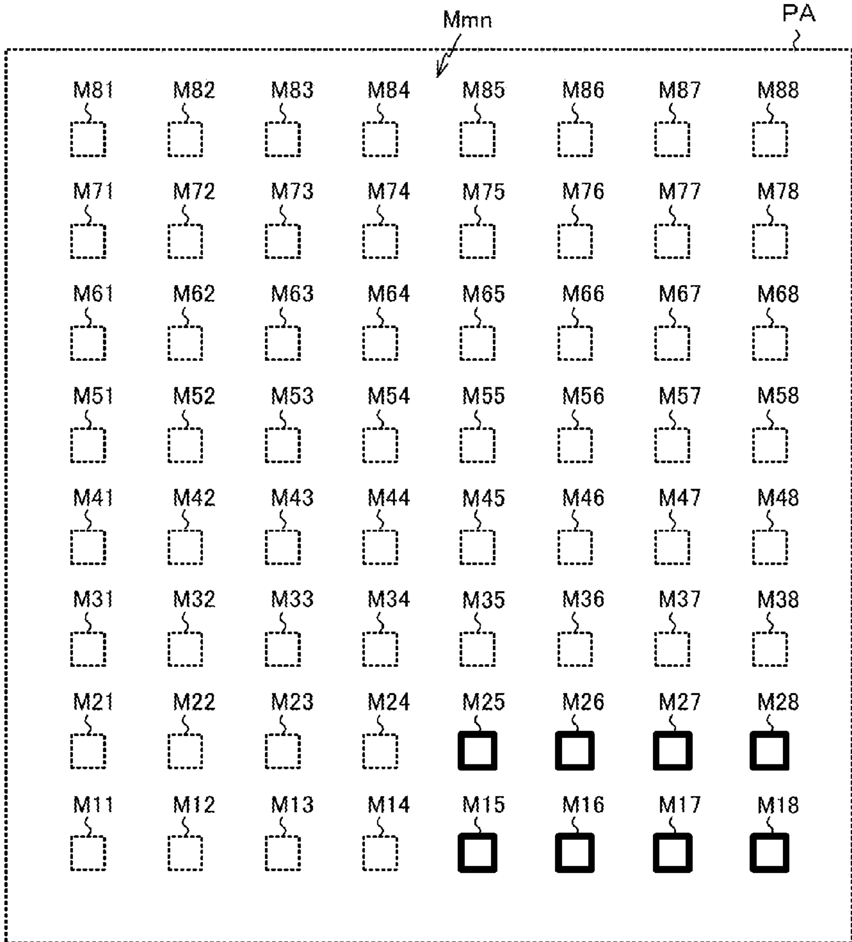


FIG.22



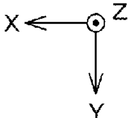


FIG.23

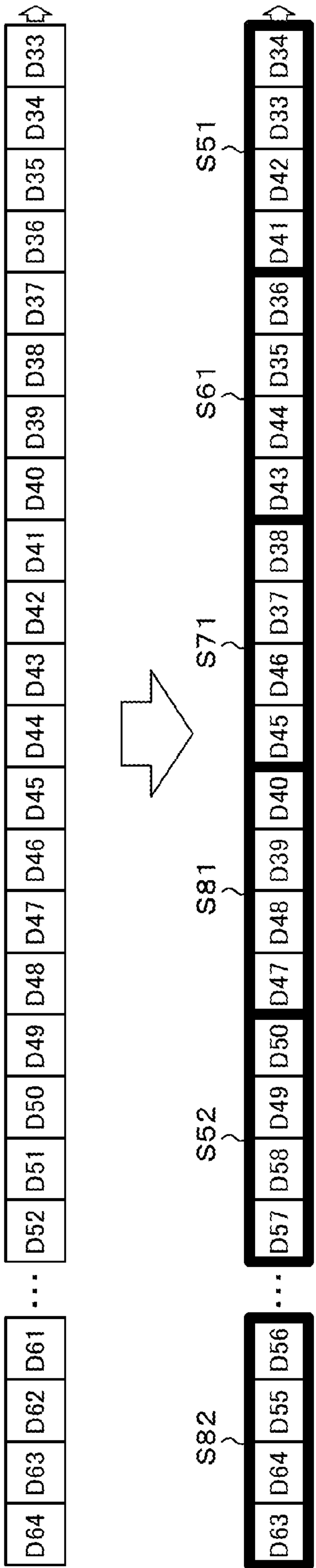


FIG.24

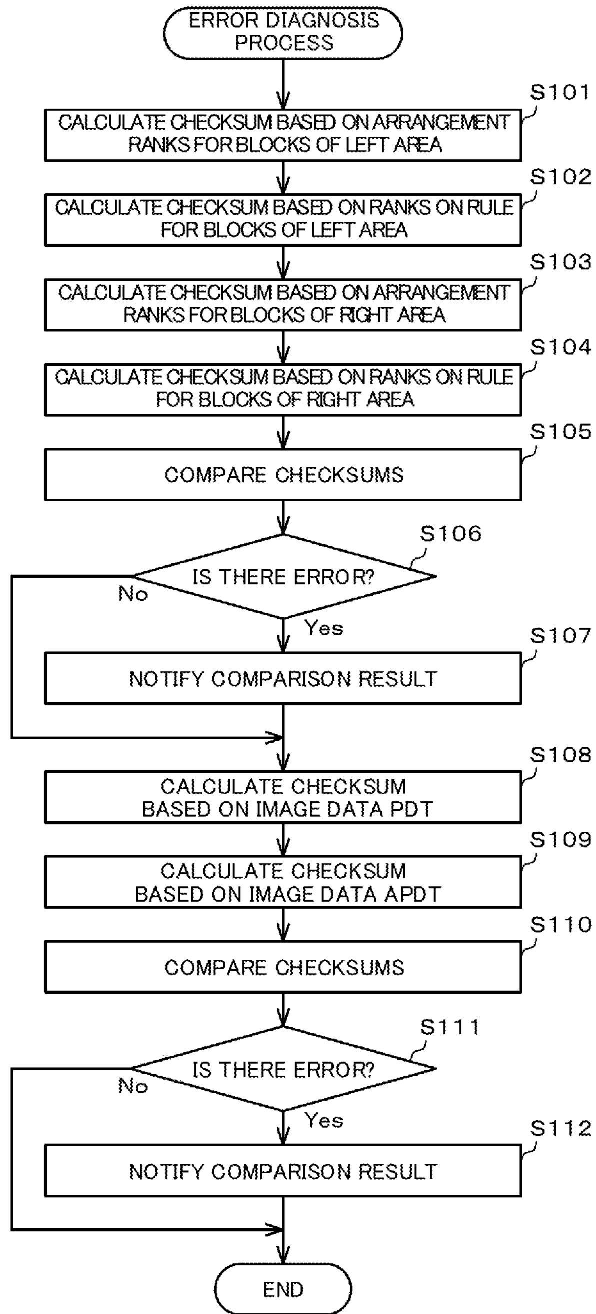


FIG.25

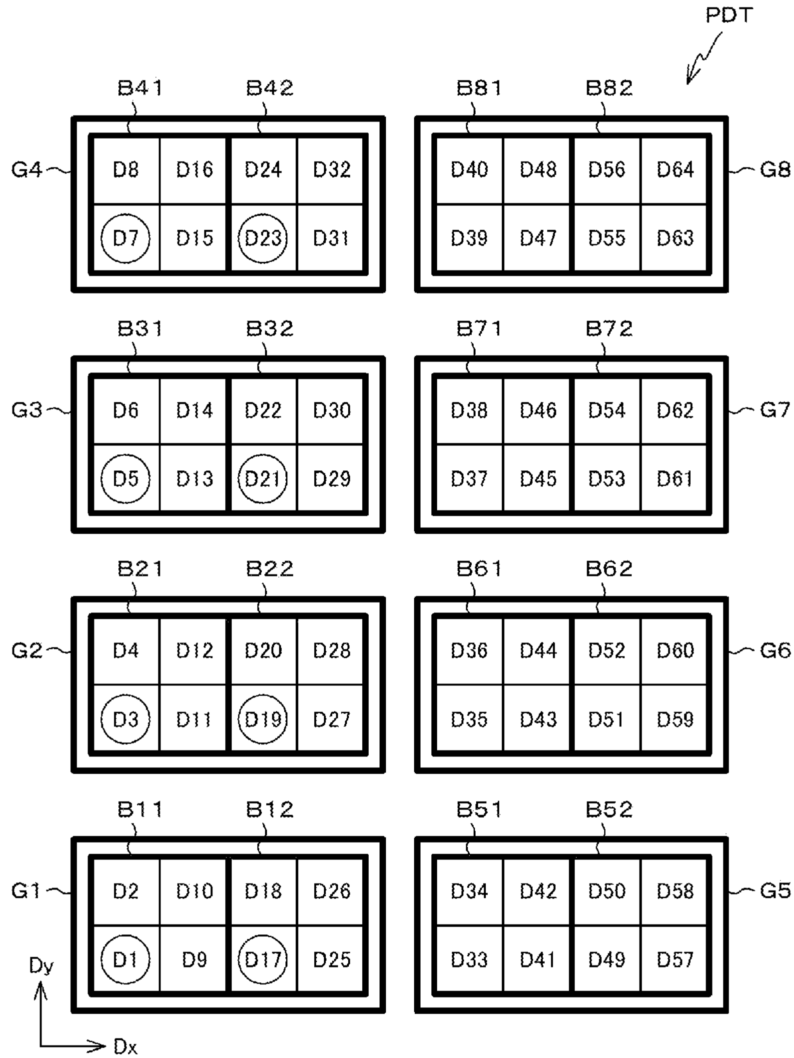


FIG.26

FIG.27

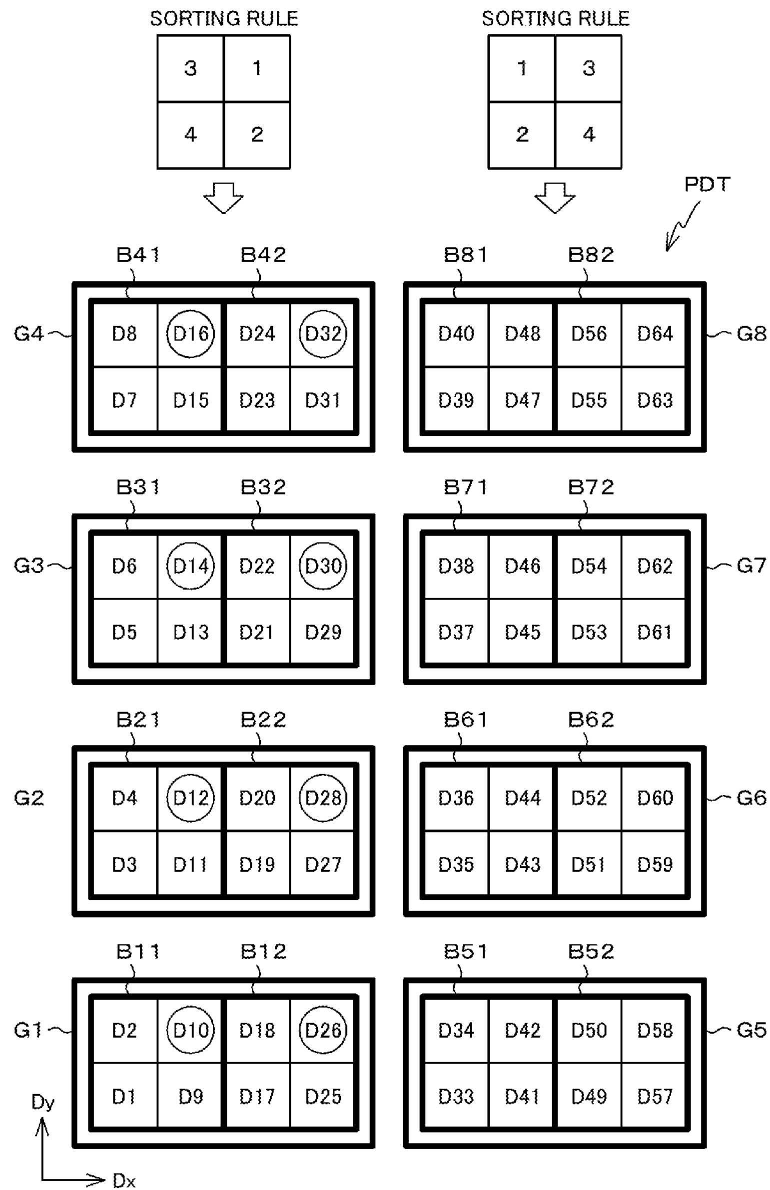


FIG.28

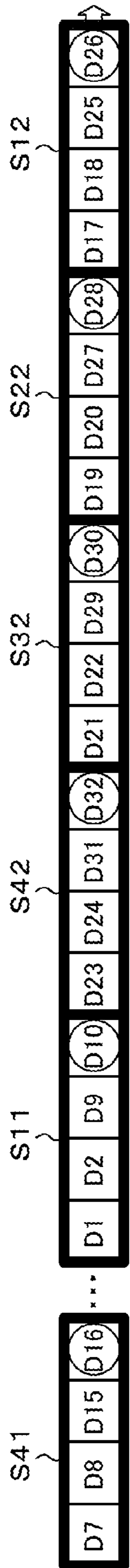


FIG.29

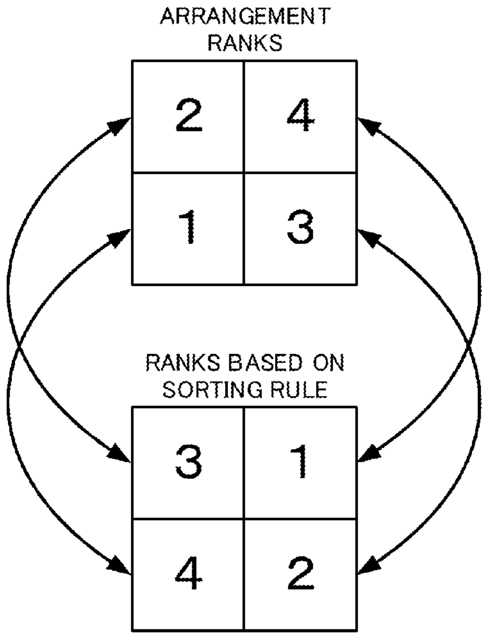


FIG.30

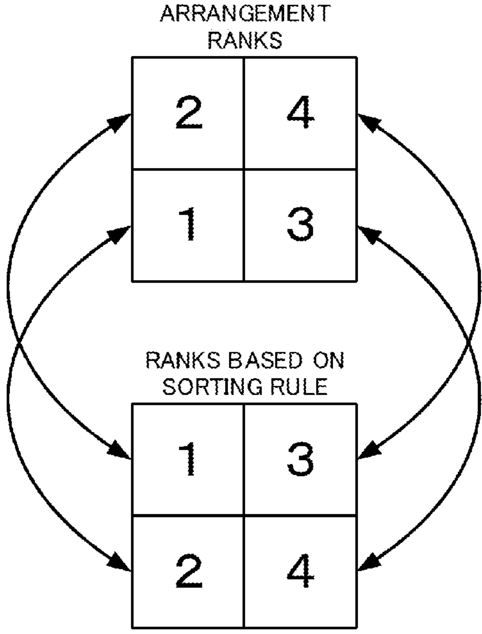


FIG.31

CHECKSUM		UNIT DATA
CS1	ACS4	D1+D3+D5+D7+D17+D19+D21+D23
CS2	ACS3	D2+D4+D6+D8+D18+D20+D22+D24
CS3	ACS2	D9+D11+D13+D15+D25+D27+D29+D31
CS4	ACS1	D10+D12+D14+D16+D26+D28+D30+D32
CS5	ACS6	D33+D35+D37+D39+D49+D51+D53+D55
CS6	ACS5	D34+D36+D38+D40+D50+D52+D54+D56
CS7	ACS8	D41+D43+D45+D47+D57+D59+D61+D63
CS8	ACS7	D42+D44+D46+D48+D58+D60+D62+D64

FIG.32

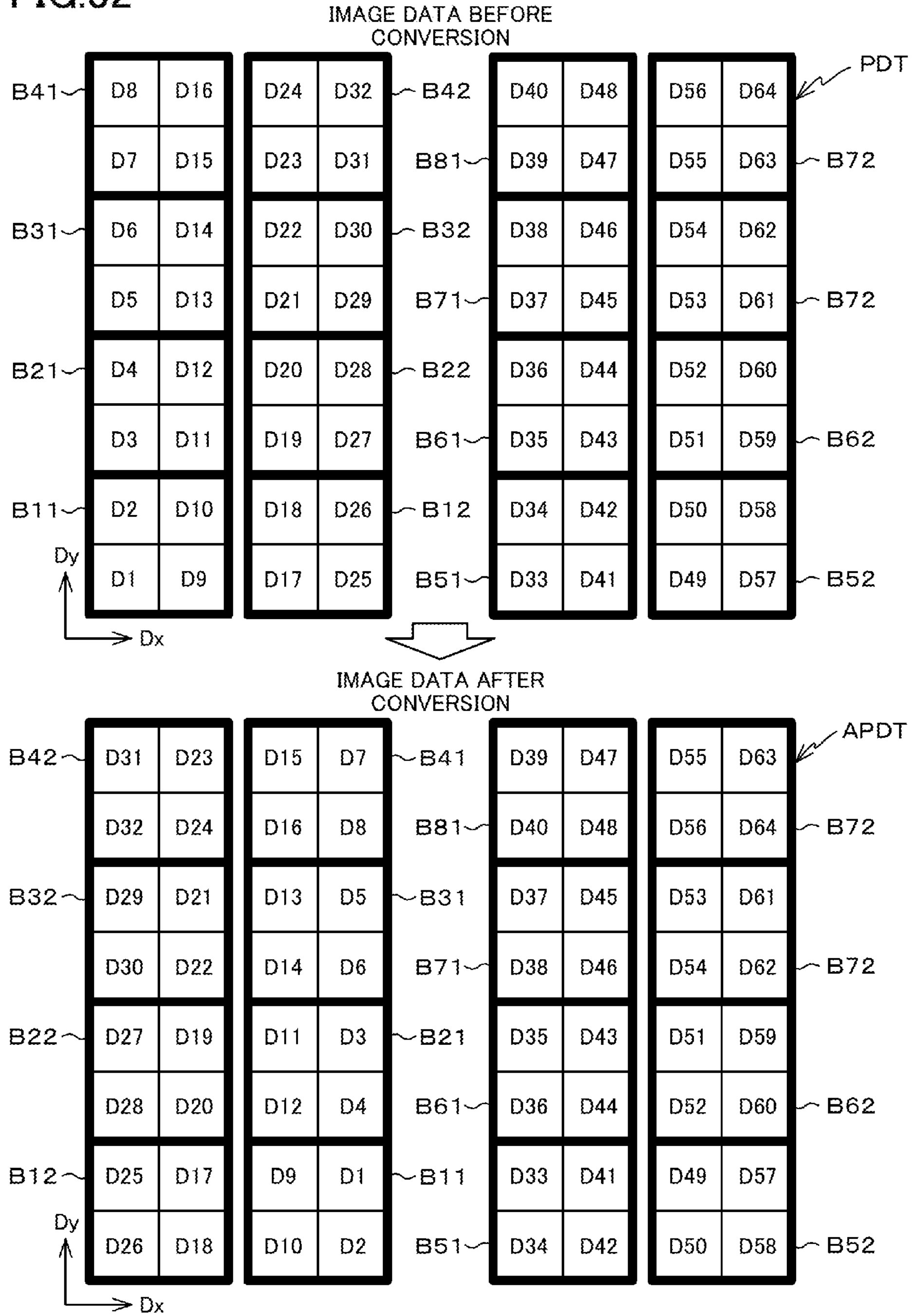


FIG.33

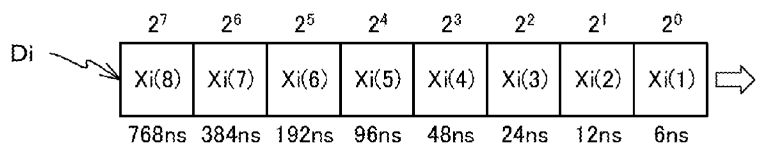
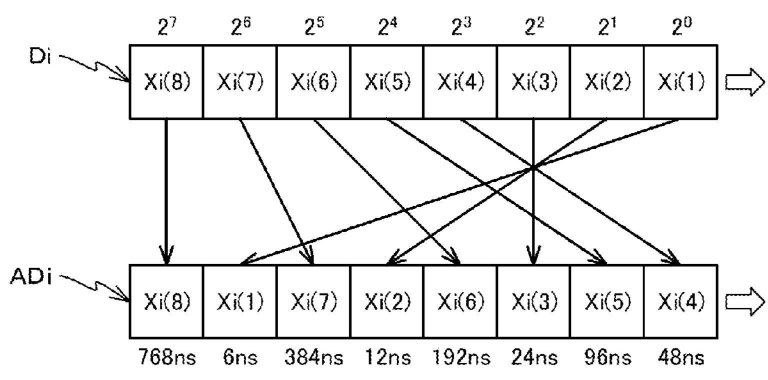


FIG.34



DIAGNOSIS METHOD, CHARGED PARTICLE BEAM LITHOGRAPHY APPARATUS, AND RECORDING MEDIUM

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Applications No. 2016-032249 filed in Japan on Feb. 23, 2016; the entire contents of which are incorporated herein by reference.

FIELD

[0002] The present disclosure relates to a diagnosis method, a charged particle beam lithography apparatus, and a recording medium.

BACKGROUND

[0003] In a semiconductor device lithography process, an original pattern formed on a mask is transferred to a wafer serving as a substrate of the semiconductor device. Drawing of the original pattern onto the mask is performed, for example, using an electron beam lithography apparatus.

[0004] In recent years, in order to improve a throughput, a multi-beam type electron beam lithography apparatus capable of drawing a pattern using a plurality of electron beams has come into use. In such a type of the electron beam lithography apparatus, an electron beam emitted from a single electron source is divided into multiple beams (multiplexed) as the electron beam passes through an aperture having a plurality of holes. The ON/OFF control of multiple electron beams are independently performed, for example, by a blanking aperture array (BAA).

[0005] Since the BAA is disposed in a vacuum lens barrel provided with an electron gun or the like for emitting an electron beam, its size is restricted. For this reason, a data format processed by the BAA is selected such that a control circuit of the BAA becomes as simple as possible. Meanwhile, image data of the pattern drawn by the electron beam lithography apparatus is designed, for example, using a computer-aided design (CAD) tool and is output in a bitmap format.

[0006] In order to perform the ON/OFF control of the electron beam using the BAA, it is necessary to convert the image data representing the pattern to be drawn into a format suitable for an interface of the BAA.

[0007] If an error occurs in conversion of the image data described above, a product yield is degraded. Thus, various techniques for avoiding such a patterning error have been proposed.

[0008] In the prior art, an error of the drawing data is detected by comparing a checksum of the data obtained before being supplied to the BAA and a checksum of the data supplied to the BAA. In the technique of Patent Document 2, a damage of the drawing data is detected by calculating and comparing an expected parity bit of the data obtained after sorting. In the technique of Patent Document 1, however, it is difficult to detect a conversion error while the damaged data can be detected. In the technique of Patent Document 2, for example, if a conversion error occurs due to a change of the data arrangement sequence, a parity check may be successful erroneously. Thus, it is difficult to detect abnormality. For this reason, if a conversion error described above occurs, a long time is necessary to perform troubleshooting. As a result, a system downtime may be prolonged.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a schematic diagram illustrating a configuration of an electron beam lithography apparatus according to an embodiment of the disclosure;

[0010] FIG. **2** is a top plan view illustrating an aperture;

[0011] FIG. **3** is a perspective view illustrating an electron gun, a lens, an aperture, and an aperture array;

[0012] FIG. **4** is a top plan view illustrating the aperture array;

[0013] FIG. **5** is an enlarged perspective view illustrating a blanker;

[0014] FIG. **6** is a wiring diagram illustrating a converter and a blanker;

[0015] FIG. **7** is a block diagram illustrating a controller;

[0016] FIG. **8** is a connection diagram illustrating a BAA controller and the converter;

[0017] FIG. **9** is a diagram illustrating a unit pattern drawn on the basis of image data;

[0018] FIG. **10** is a diagram illustrating a circuit pattern including the unit pattern;

[0019] FIG. **11** is a schematic diagram illustrating the image data;

[0020] FIG. **12** is a diagram for describing a drawing process of the circuit pattern;

[0021] FIG. **13** is a diagram for describing a drawing process of the circuit pattern;

[0022] FIG. **14** is a diagram for describing a drawing process of the circuit pattern;

[0023] FIG. **15** is a diagram for describing a drawing process of the circuit pattern;

[0024] FIG. **16** is a diagram for describing a drawing process of the circuit pattern;

[0025] FIG. **17** is a diagram for describing a drawing process of the circuit pattern;

[0026] FIG. **18** is a schematic diagram illustrating serial data based on image data;

[0027] FIG. **19** is a diagram for describing a drawing process of the circuit pattern;

[0028] FIG. **20** is a diagram for describing a drawing process of the circuit pattern;

[0029] FIG. **21** is a diagram for describing a drawing process of the circuit pattern;

[0030] FIG. **22** is a diagram for describing a drawing process of the circuit pattern;

[0031] FIG. **23** is a schematic diagram illustrating serial data based on image data;

[0032] FIG. **24** is a flowchart illustrating an error diagnosis process;

[0033] FIG. **25** is a diagram for describing a process of calculating a checksum for each arrangement rank of unit data;

[0034] FIG. **26** is a supplemental diagram for describing a method of calculating a checksum;

[0035] FIG. **27** is a diagram for describing a process of calculating a checksum according to a sorting rule;

[0036] FIG. **28** is a supplemental diagram for describing a method of calculating a checksum;

[0037] FIG. **29** is a diagram for describing a process of comparing the checksum;

[0038] FIG. **30** is a diagram for describing a process of comparing the checksum;

[0039] FIG. **31** is a diagram for describing a process of comparing the checksum;

[0040] FIG. **32** is a diagram conceptually illustrating original image data and image data equivalent to serial data;

[0041] FIG. **33** is a schematic diagram illustrating unit data; and

[0042] FIG. **34** is a diagram for describing a bit data exchange process.

DETAILED DESCRIPTION

[0043] In accordance with an aspect of the present disclosure, there is provided a method of diagnosing a conversion process for converting a format of image data including unit data corresponding to charged particle beams into a format suitable for an aperture array, the aperture array having a plurality of controllers provided to match a plurality of the charged particle beams to control the charged particle beams and a driver configured to drive the controllers, the method including: extracting the unit data having an identical first rank based on an arrangement of the unit data in the image data from the unit data of each block including a predetermined number of the unit data and calculating a first checksum of each of the first rank; extracting the unit data having an identical second rank after the conversion process from the unit data of each of the blocks and calculating a second checksum of each of the second rank; and comparing the first and second checksums.

[0044] In accordance with another aspect of the present disclosure, there is provided a charged particle beam lithography apparatus including: an aperture array having a plurality of controllers provided to match a plurality of charged particle beams to control the charged particle beams and a driver configured to drive the controllers; a converter configured to convert a format of image data having unit data corresponding to the charged particle beams into a format suitable for the aperture array; a first calculator configured to extract the unit data having an identical first rank based on the arrangement of the unit data of the image data from the unit data of each block having a predetermined number of the unit data and calculate a first checksum for each of the first rank; a second calculator configured to extract the unit data having an identical second rank after the conversion of the converter from the unit data of each of the blocks and calculate a second checksum for each of the second ranks; and a first comparator configured to compare the first checksum with the second checksum.

[0045] A computer-readable recording medium storing a program for diagnosing a conversion process for converting a format of image data including unit data corresponding to charged particle beams into a format suitable for an aperture array, the aperture array having a plurality of controllers provided to match a plurality of the charged particle beams to control the charged particle beams, and a driver configured to drive the controllers, the program causing a computer to execute: extracting the unit data having an identical first rank based on an arrangement of the unit data in the image data from the unit data of each block including a predetermined number of the unit data and calculating a first checksum of each of the first rank; extracting the unit data having an identical second rank after the conversion process from the unit data of each of the blocks and calculating a second checksum of each of the second rank; and comparing the first checksum with the second checksum.

[0046] Embodiments of the present disclosure will be described below with reference to the accompanying drawings. In the description of the embodiments, a Cartesian coordinate system composed of X, Y, and Z axes perpendicular to each other is appropriately employed.

<Configuration of Apparatus>

[0047] FIG. **1** is a schematic diagram illustrating a configuration of an electron beam lithography apparatus **10** according to an embodiment of the disclosure. The electron beam lithography apparatus **10** is an apparatus for drawing a pattern using an electron beam on a specimen **120** such as a mask or reticle coated with a resist material under the vacuum environment.

[0048] As illustrated in FIG. **1**, the electron beam lithography apparatus **10** includes an irradiator **20** that irradiates an electron beam EB onto the specimen **120**, a stage **70** used to place the specimen **120**, a vacuum chamber **80** that houses the irradiator **20** and the stage **70**, and a control system **100** that controls the irradiator **20** and the stage **70**.

[0049] The vacuum chamber **80** includes a writing chamber **80*a*** that houses the stage **70** and a lens barrel **80*b*** that houses the irradiator **20**.

[0050] The writing chamber **80*a*** is a rectangular parallelepiped hollow member and has a circular opening on its upper surface. The lens barrel **80*b*** is a cylindrical casing whose longitudinal direction is parallel to the Z-axis direction. The lens barrel **80*b*** is formed of, for example, stainless steel and is grounded. The lens barrel **80*b*** is inserted into the inside of the writing chamber **80*a*** from the opening provided on the upper surface of the writing chamber **80*a***. The internal vacuum levels of the writing chamber **80*a*** and the lens barrel **80*b*** are maintained, for example, at approximately 10^{-7} Pa.

[0051] The irradiator **20** includes an electron gun **30**, lenses **41**, **42**, and **43**, apertures **51** and **52**, an aperture array **61**, and a deflector **62**. The electron gun **30**, the lenses **41**, **42**, and **43**, the apertures **51** and **52**, the aperture array **61**, and the deflector **62** are disposed inside the lens barrel **80*b***.

[0052] The electron gun **30** is disposed in an upper part inside the lens barrel **80*b***. The electron gun **30** is, for example, a hot cathode type electron gun. The electron gun **30** includes a cathode, a Wehnelt electrode provided to surround the cathode, an anode disposed under the cathode, and the like. When a voltage is applied, the electron gun **30** ejects the electron beam EB downward.

[0053] The lens **41** is an annular electromagnetic lens and is disposed under the electron gun **30**. The lens **41** shapes the electron beam EB spreading downward so as to be parallel to a vertical direction.

[0054] The aperture **51** is a member for branching the incident electron beam EB into a plurality of electron beams EBmn. FIG. **2** is a top plan view illustrating the aperture **51**. As illustrated in FIG. **2**, the aperture **51** is a rectangular plate-shaped member. The aperture **51** is formed of, for example, a silicon-based material, and has a surface provided with a coating layer or a sputtering layer formed of, for example, chromium or the like. The aperture **51** has sixty four holes H arranged in an eight-row and eight-column matrix shape by setting a row direction to the X-axis direction and setting a column direction to the Y-axis direction. The hole H has a square shape whose each side is

parallel to the X-axis or Y-axis. The dimensions of the holes H are approximately equal to each other in the X-axis and Y-axis directions.

[0055] In this embodiment, the sixty four holes H are expressed as "Hmn," where "m" and "n" denote integers 1 to 8. The hole located in the first row closest to zero in the Y-axis direction is denoted by "H**1***n*." The holes located in the second to eighth rows are denoted by "H**2***n*" to "H**8***n*." The hole located in the first column closest to zero in the X-axis direction is denoted by "Hm**1**." The holes located in the second to eighth columns are denoted by "Hm**2**" to "Hm**8**."

[0056] FIG. **3** is a perspective view illustrating the electron gun **30**, the lens **41**, the aperture **51**, and the aperture array **61**. As illustrated in FIG. **3**, the electron beam EB ejected from the electron gun **30** is shaped by the lens **41** in parallel to the vertical axis. The shaped electron beam EB is incident to a circular area C**1** indicated by a virtual line on the upper surface of the aperture **51**. A part of the electron beams EB incident to the area C**1** are blocked by the aperture **51**, and the remaining electron beams EB pass through the holes Hmn of the aperture **51**. As a result, the electron beam EB is divided (multiplexed) into 64 electron beams traveling vertically downward.

[0057] In this embodiment, the electron beam passing through the hole Hmn of the aperture **51** will be referred to as an electron beam EBmn. Note that, in FIG. **3**, only the electron beams EB**11**, EB**18**, EB**81**, and EB**88** passing through the holes H**11**, H**18**, H**81**, and H**88**, respectively are shown representatively.

[0058] The aperture array **61** is a unit for individually blanking each electron beam EBmn. FIG. **4** is a top plan view illustrating the aperture array **61**. As illustrated in FIG. **4**, the aperture array **61** includes a substrate **610** and sixty four blankers BK provided on the upper surface (+Z-side surface) of the substrate **610**.

[0059] The substrate **610** is a square substrate formed of, for example, silicon. The substrate **610** has sixty four holes HH arranged in an eight-row and eight-column matrix shape. Each of the sixty four holes HH is positioned under each of the holes H of the aperture **51**. In this embodiment, the holes HH immediately under the holes Hmn will be expressed as "holes HHmn."

[0060] The hole HHmn is slightly larger than the hole Hmn. The electron beam EBmn passing through the hole Hmn can pass through the hole HHmn without interference of the substrate **610**.

[0061] FIG. **5** is an enlarged perspective view illustrating the blanker BK. The blanker BK includes a pair of electrodes **611** and **612** formed of, for example, metal such as copper. The electrode **611** is a member having a U-shaped X-Y cross section. The electrode **611** is disposed along the +X-side outer edge, the −X-side outer edge, and the +Y-side outer edge of the hole HHmn provided in the substrate **610**. The electrode **612** is a plate-shaped electrode and is disposed along the −Y-side outer edge of the hole HHmn. As shown in FIG. **5**, the electron beam EBmn passing through the aperture **51** passes through a gap between the electrodes **611** and **612** of the blanker BK and is then incident to the hole HHmn of the substrate **610**.

[0062] As illustrated in FIG. **4**, the blanker BK is provided in each hole HHmn. In this embodiment, the blanker BK provided in the hole HHmn will be expressed as a blanker BKmn.

[0063] The electrode **611** of the blanker BK of FIG. **5** is grounded through a circuit (not illustrated) provided in the substrate **610**. In addition, as a voltage is applied to the electrode **612**, the electron beam EBmn incident to the hole HHmn of the substrate **610** is deflected in the direction indicated by the arrow in FIG. **5**. As a result, as illustrated in FIG. **1**, the electron beam EBmn is blocked by the aperture **52**, and the electron beam EBmn has a blanked state.

[0064] FIG. **6** is a wiring diagram illustrating converters **621** to **628** and blankers BK**11** to BK**88**. As shown in FIG. **6**, in the aperture array **61**, the electrodes **612** of the blankers BK**11** to BK**14** and BK**21** to BK**24** are connected to the converter **621** through the shift registers SR**1** and SR**2** and the buffer BF. Similarly, the electrodes **612** of the blankers BK**31** to BK**34** and BK**41** to BK**44** are connected to the converter **622**. The electrodes **612** of the blankers BK**51** to BK**54** and BK**61** to BK**64** are connected to the converter **623**. The electrodes **612** of the blankers BK**71** to BK**74** and BK**81** to BK**84** are connected to the converter **624**. The electrodes **612** of the blankers BK**15** to BK**18** and BK**25** to BK**28** are connected to the converter **625**. The electrodes **612** of the blankers BK**35** to BK**38** and BK**45** to BK**48** are connected to the converter **626**. The electrodes **612** of the blankers BK**55** to BK**58** and BK**65** to BK**68** are connected to the converter **627**. The electrodes **612** of the blankers BK**75** to BK**78** and BK**85** to BK**88** are connected to the converter **628**.

[0065] The converters **621** to **628** are converters for converting serial data into parallel data. The converters **621** to **628** converts the serial data output from the control system **100** into parallel data including four data and outputs the four data. These data are output through four output lines L**1** to L**4**. The operations of the converters **621** to **628** will be described below.

[0066] Returning to FIG. **1**, the lens **42** is an annular electromagnetic lens and is disposed under the aperture array **61**. The lens **42** makes the sixty four electron beams EBmn, that are parallelized with each other by passing through the aperture array **61** and travel downward, incident to the hole of the aperture **52**.

[0067] The aperture **52** is a plate-shaped member provided with a center hole through which the electron beams EBmn pass. The aperture **52** is disposed in the vicinity of a convergence point (crossover point) of the electron beams EBmn passing through the lens **42**. As each electron beam EBmn passes through the hole of the aperture **52**, each electron beam EBmn is shaped in a shot shape. In addition, when the electron beams EBmn are deflected by the blanker BK of the aperture array **61**, the electron beams EBmn are blanked by the aperture **52**.

[0068] The deflector **62** is disposed under the aperture **52**. The deflector **62** has a plurality of pairs of electrodes arranged to face each other. The deflector **62** deflects the electron beams EBmn passing through the aperture **52** depending on a voltage applied to the electrodes. In this embodiment, for simplicity purposes, only a single pair of electrodes separated by a predetermined distance in the X-axis direction are illustrated in the drawings, the deflector **62** may deflect the electron beams EBmn in the X-axis and Y-axis directions.

[0069] The lens **43** is an annular electromagnetic lens disposed to surround the deflector **62**. The lens **43** focuses

the electron beams EBmn on a desired position of the specimen **120** placed on the stage **70** in cooperation with the deflector **62**.

[0070] The stage **70** is disposed inside the writing chamber **80***a*. The stage **70** is a stage capable of moving at least within the horizontal plane while the specimen **120** to be patterned is maintained nearly horizontally. On the upper surface of the stage **70**, a mirror Mx whose longitudinal direction is set to the Y-axis direction and a mirror My whose longitudinal direction is set to the X-axis direction are provided. A position within the horizontal plane of the stage **70** is detected with respect to the mirrors Mx and My.

[0071] The control system **100** is a system for controlling the irradiator **20** and the stage **70**. The control system **100** has a controller **101**, a power source **102**, a lens driver **103**, a BAA controller **104**, a deflection amplifier **105**, and a stage driver **106**.

[0072] FIG. **7** is a block diagram illustrating the controller **101**. As illustrated in FIG. **7**, the controller **101** is a computer having a central processing unit (CPU) **101***a*, a main memory **101***b*, an auxiliary memory **101***c*, an input unit **101***d*, a display **101***e*, an interface **101***f*, and a system bus **101***g* used to connect these elements.

[0073] The CPU **101***a* reads a program stored in the auxiliary memory **101***c* and executes the program. In addition, the CPU **101***a* integrally controls the elements of the control system **100** on the basis of the program.

[0074] The main memory **101***b* has a volatile memory such as a random access memory (RAM). The main memory **101***b* is used as a work area of the CPU **101***a*.

[0075] The auxiliary memory **101***c* has a non-volatile memory such as a read-only memory (ROM), a magnetic disc, and a semiconductor memory. The auxiliary memory **101***c* stores a program executed by the CPU **101***a*, image data PDT representing a pattern to be drawn on the specimen **120**, various parameters, and the like.

[0076] The input unit **101***d* has a pointing device such as a keyboard or a mouse. A user's instruction is input through the input unit **101***d* and is notified to the CPU **101***a* via the system bus **101***g*.

[0077] The display **10***le* has a display device such as a liquid crystal display (LCD). The display **101***e* displays information regarding a status of the electron beam lithography apparatus **10**, a lithographic pattern PDT, and the like.

[0078] The interface **101***f* has a LAN interface, a serial interface, a parallel interface, an analog interface, and the like. The power source **102**, the lens driver **103**, the BAA controller **104**, the deflection amplifier **105**, and the stage driver **106** are connected to the controller **101** through the interface **101***f*.

[0079] The controller **101** configured as described above integrally controls the power source **102**, the lens driver **103**, the BAA controller **104**, the deflection amplifier **105**, and the stage driver **106**.

[0080] Returning to FIG. **1**, the power source **102** applies a voltage to the electron gun **30** in response to an instruction from the controller **101**. As a result, the electron beam EB is ejected from the electron gun **30** downward.

[0081] The lens driver **103** controls (refractive) power of the lens **41** for the electron beam EB on the basis of the instruction from the controller **101** such that the electron beam EB spreading downward is shaped into an electron beam traveling in parallel to the vertical direction. In addition, the lens driver **103** controls power of the lens **42** such that the electron beams EBmn are converged into the center of the aperture **52**. Furthermore, the lens driver **103** controls power of the lens **43** such that the electron beams EBmn are focused on the upper surface of the specimen **120**.

[0082] Similar to the controller **101**, the BAA controller **104** is a computer having a CPU. The converters **621** to **628** are connected to the BAA controller **104** as illustrated in FIG. **8**. The BAA controller **104** creates serial data **S1** to **S8** on the basis of the image data PDT transmitted from the controller **101**. In addition, the BAA controller **104** outputs the serial data **S1** to **S8** to the converters **621** to **628**. The operation of the BAA controller **104** will be described below.

[0083] Returning to FIG. **1**, the deflection amplifier **105** generates a voltage signal on the basis of an instruction from the controller **101** and outputs the voltage signal to the electrodes of the deflector **62**. As a result, a voltage difference is generated between the electrodes of the deflector **62**. The electron beams EBmn passing through the deflector **62** are deflected as much as the voltage difference.

[0084] The stage driver **106** measures positions of the mirrors Mx and My of the stage **70** using a laser sensor (not shown) and the like and detects a position of the stage **70** on the basis of the measurement result. In addition, the stage driver **106** drives the stage **70** on the basis of an instruction from the controller **101** to move or position the specimen **120**.

<Operation of Apparatus>

[0085] In the electron beam lithography apparatus **10** described above, the controller **101** integrally controls the power source **102**, the lens driver **103**, the BAA controller **104**, the deflection amplifier **105**, and the stage driver **106**. For example, if the pattern is drawn on the specimen **120** using the electron beam lithography apparatus **10**, the CPU **101***a* of the controller **101** drives the stage **70** where the specimen **120** is placed in order to position the specimen **120** under the irradiator **20**.

[0086] The CPU **101***a* drives the power source **102** to apply a voltage to the electron gun **30**. As a result, the electron beam EB is ejected from the electron gun **30**.

[0087] As the electron beam EB is ejected from the electron gun **30**, the CPU **101***a* controls the lens **41** using the lens driver **103** to shape the electron beam EB spreading downward so as to be parallel to the vertical axis.

[0088] The electron beam EB shaped by the lens **41** travels downward and passes through the aperture **51**. As a result, the electron beam EB is branched into a plurality of (sixty four) electron beams EBmn. The electron beams EBmn pass through the blankers BKmn of the aperture array **61** and travel through holes HHmn of the substrate **610** included in the aperture array **61**.

[0089] The CPU **101***a* controls the lens **42** using the lens driver **103** such that each of the electron beams EBmn passing through the aperture array **61** is converged in the vicinity of the hole of the aperture **52**.

[0090] As each of the electron beams EBmn passes through the hole of the aperture **52**, an outer diameter and a shape of the shot are shaped. The electron beams EBmn passing through the aperture **52** are incident to the lens **43**.

[0091] The CPU **101***a* controls the lens **43** using the lens driver **103** such that the electron beams EBmn incident to the lens **43** are focused on the surface of the specimen **120** held by the stage **70**. In addition, the CPU **101***a* controls an

incident position of the electron beam EBmn to the specimen **120** by deflecting the electron beams EBmn in the X-axis or Y-axis direction using the deflection amplifier **105**.

[0092] In addition to the aforementioned operation, the CPU **101***a* outputs the image data PDT to the BAA controller **104**. The ON/OFF control of the electron beams EBmn incident to the specimen **120** is performed on the basis of the image data PDT.

[0093] FIG. **9** is a diagram illustrating a unit pattern PA drawn on the basis of the image data PDT by way of example. The unit pattern PA includes sixty four marks Mmn drawn by the sixty four electron beams EBmn. The electron beam lithography apparatus **10** draws a circuit pattern CPA including the unit pattern PA on the specimen **120** by sequentially drawing the unit pattern PA on the upper surface of the specimen **120** as indicated by the arrow in FIG. **10**.

[0094] FIG. **11** is a schematic diagram illustrating the image data PDT as an example. As illustrated in FIG. **11**, the image data PDT includes unit data D**1** to D**64** representing doses of the electron beams for drawing the sixty four marks Mmn. For example, the image data PDT is bitmap data in which the unit data D**1** to D**64** are arranged in an eight-row and eight-column matrix shape in the Dy-axis and Dx-axis directions. The image data PDT is stored in the auxiliary memory **101***c* of the controller **101** in advance. In addition, when the drawing on the specimen **120** starts, the image data is output to the BAA controller **104**.

[0095] The BAA controller **104** creates the serial data S**1** to S**8** on the basis of the image data PDT.

[0096] Specifically, the BAA controller **104** divides the unit data D**1** to D**64** of the image data PDT into eight data groups G**1** to G**8** as illustrated in FIG. **12**. As shown in FIGS. **4**, **6**, and **12**, the unit data of the data group G**1** correspond to the blankers BK**11** to BK**14** and BK**21** to BK**24**. The unit data of the data group G**2** correspond to the blankers BK**31** to BK**34** and BK**41** to BK**44**. The unit data of the data group G**3** correspond to the blankers BK**51** to BK**54** and BK**61** to BK**64**. The unit data of the data group G**4** correspond to the blankers BK**71** to BK**74** and BK**81** to BK**84**. The unit data of the data group G**5** correspond to the blankers BK**15** to BK**18** and BK**25** to BK**28**. The unit data of the data group G**6** correspond to the blankers BK**35** to BK**38** and BK**45** to BK**48**. The unit data of the data group G**7** correspond to the blankers BK**55** to BK**58** and BK**65** to BK**68**. The unit data of the data group G**8** correspond to the blankers BK**75** to BK**78** and BK**85** to BK**88**.

[0097] The BAA controller **104** divides the unit data of the data groups G**1** to G**8** into blocks of the unit data whose number is equivalent to the number of data output from the converters **621** to **628** in parallel. As illustrated in FIG. **6**, the converters **621** to **628** has four output lines L**1** to L**4**. The BAA controller **104** divides the unit data of each data group G**1** to G**8** into four-row and four-column blocks of the unit data.

[0098] For example, as illustrated in FIG. **13**, the BAA controller **104** divides the unit data of the data group G**1** into a block B**11** including the unit data D**1**, D**2**, D**9**, and D**10** and a block B**12** including the unit data D**17**, D**18**, D**25**, and D**26**.

[0099] Similarly, the BAA controller **104** divides the unit data of each data group G**2** to G**8** into blocks B**21** to B**81** and blocks B**22** to B**82**.

[0100] The block B**21** of the data group G**2** includes the unit data D**3**, D**4**, D**11**, and D**12**, and the block B**22** includes the unit data D**19**, D**20**, D**27**, and D**28**. The block B**31** of the data group G**3** includes the unit data D**5**, D**6**, D**13**, and D**14**, and the block B**32** includes the unit data D**21**, D**22**, D**29**, and D**30**. The block B**41** of the data group G**4** includes the unit data D**7**, D**8**, D**15**, and D**16**, and the block B**42** includes the unit data D**23**, D**24**, D**31**, and D**32**. The block B**51** of the data group G**5** includes the unit data D**33**, D**34**, D**41**, and D**42**, and the block B**52** includes the unit data D**49**, D**50**, D**57**, and D**58**. The block B**61** of the data group G**6** includes the unit data D**35**, D**36**, D**43**, and D**44**, and the block B**62** includes the unit data D**51**, D**52**, D**59**, and D**60**. The block B**71** of the data group G**7** includes the unit data D**37**, D**38**, D**45**, and D**46**, and the block B**72** includes the unit data D**53**, D**54**, D**61**, and D**62**. The block BS**81** of the data group G**8** includes the unit data D**39**, D**40**, D**47**, and D**48**, and the block B**82** includes the unit data D**55**, D**56**, D**63**, and D**64**.

[0101] The BAA controller **104** sorts the unit data of the block B**11** of the data group G**1** and the unit data of the block B**12** of the data group G**1** according to a predetermined rule. FIG. **14** is a schematic diagram illustrating a process of generating the serial data S**1** from the data group G**1**. The BAA controller **104** divides the data group G**1** into blocks B**11** and B**12** as illustrated in FIG. **14** and sorts the unit data of the blocks B**11** and B**12** according to the sorting rule of FIG. **14**.

[0102] The sorting rule is defined on the basis of a relationship between the converter **621** where the unit data D**1**, D**2**, D**9**, D**10**, D**17**, D**18**, D**25**, and D**26** of the block B**11** are output and the blankers BK**11** to BK**14** and BK**21** to BK**24**. For example, as illustrated by FIG. **6**, if the converter **621** firstly outputs the unit data D**10** to the output line L**1** for the blanker BK**22**, secondly outputs the unit data D**9** to the output line L**2** for the blanker BK**12**, thirdly outputs the unit data D**2** to the output line L**3** for the blanker BK**21**, and fourthly outputs the unit data D**1** to the output line L**4** for the blanker BK**11**, the BAA controller **104** creates serial data S**11** [D**10**, D**9**, D**2**, D**1**] having the unit data D**10** as a head by sorting the unit data D**1**, D**2**, D**9**, and D**10**.

[0103] Similarly, the BAA controller **104** creates serial data S**12** [D**26**, D**25**, D**18**, D**17**] having the unit data D**26** as a head by sorting the unit data D**17**, D**18**, D**25**, and D**26** of the block B**12**.

[0104] As illustrated by FIG. **6**, in the output lines L**1** to L**4** of the converter **621**, the blankers BK**13**, BK**23**, BK**14**, and BK**24** corresponding to the unit data D**17**, D**18**, D**25**, and D**26** are placed in the downstream of the blankers BK**11**, BK**21**, BK**12**, and BK**22** corresponding to the unit data D**1**, D**2**, D**9**, and D**10**. In this regard, the BAA controller **104** exchanges the sequences of the serial data S**12** and S**11** with each other and combines the exchanged sequences as illustrated in FIG. **14** so as to create serial data S**1** [D**26**, D**25**, D**18**, D**17**, D**10**, D**9**, D**2**, D**1**] having the unit data D**26** as a head. In this manner, the image data PDT is converted to create serial data S**1** suitable for the format of the converter **621**. The BAA controller **104** outputs the serial data S**1** to the converter **621**.

[0105] As the serial data S is output to the converter **621**, unit data of the serial data S**1** are sequentially output from the output lines L**1** to L**4**. As the unit data D**26**, D**25**, D**18**, and D**17** of the serial data S**1** are sequentially output, the unit data D**26**, D**25**, D**18**, and D**17** are stored in the shift register SR**1** of the output lines L**1** to L**4** as illustrated in FIG. **15**. Subsequently, when the unit data D**10**, D**9**, D**2**, and D**1** are sequentially output, the unit data D**26**, D**25**, D**18**, and D**17**

are sent to the shift register SR2 of the output lines L1 to L4 and are stored therein as illustrated in FIG. 16. In addition, the unit data D10, D9, D2, and D1 are stored in the shift register SR1 of the output lines L1 to L4.

[0106] If the unit data D1, D9, D17, D25, D2, D10, D18, and D26 are stored in both the shift registers SR1 and SR2 of the output lines L1 to L4, each of the unit data is output to the blankers BK11, BK12, BK13, BK14, BK21, BK22, BK23, and BK24 through the buffer BF. As a result, a dose of the electron beams EBmn passing through the holes HH11, HH12, HH13, HH14, HH21, HH22, HH23, and HH24 is controlled on the basis of the values of the unit data. Consequently, as illustrated in FIG. 17, the marks M11 to M14 and M21 to M24 of the unit pattern PA are drawn with a predetermined dose.

[0107] The BAA controller 104 also creates serial data S2 to S4 from the unit data of the data groups G2 to G4 and outputs them to the converters 622, 623, and 624. As a result, the marks Mm1 to Mm4 are drawn in the left half area of the unit pattern PA of FIG. 9.

[0108] FIG. 18 is a schematic diagram illustrating serial data obtained by arranging the unit data D1 to D32 on the basis of the arrangement rank of the image data PDT and serial data obtained by arranging the unit data D1 to D32 on the basis of the sorting rule. Through the process described above, the unit data D1 to D32 are converted from the serial data having the unit data D1 as a head and the unit data D32 as a tail into the serial data S11, S12, S21, S22, S31, S32, S41, and S42. In addition, the converted serial data are sequentially output one by one to the lines L1 to L4 of the converters 621 to 624 of FIG. 6. As a result, the serial data S1 to S4 are output to the converters 621 to 624, respectively.

[0109] Similarly, the BAA controller 104 sorts the unit data of the block B51 of the data group G5 and the unit data of the block B52 of the data group G5 on the basis of a predetermined rule. FIG. 19 is a schematic diagram illustrating a process of creating serial data S5 from the data group G5. The BAA controller 104 divides the data group G5 into the blocks B51 and B52 as illustrated in FIG. 19. Then, the BAA controller 104 sorts the unit data of the blocks B51 and B52 on the basis of the sorting rule illustrated in FIG. 19.

[0110] The sorting rule is defined by a relationship between the converter 625 and the blankers BK15 to BK18 and BK25 to BK28. The unit data D33, D34, D41, D42, D49, D50, D57, and D58 of the block B51 are output to the converter 625. The BAA controller 104 creates the serial data S51 [D34, D33, D42, D41] having the unit data D34 as a head by sorting the unit data D33, D34, D41, and D42.

[0111] Similarly, the BAA controller 104 creates serial data S52 [D50, D49, D58, D57] having the unit data D50 as a head by sorting the unit data D49, D50, D57, and D58 of the block B52.

[0112] As illustrated by FIG. 6, in the output lines L1 to L4 of the converter 625, the blankers BK15, BK25, BK16, and BK26 corresponding to the unit data D33, D34, D41, and D42 are placed in the downstream of the blankers BK17, BK27, BK18, and BK28 corresponding to the unit data D49, D50, D57, and D58. In this case, the BAA controller 104 combines the serial data S51 and S52 without exchanging their sequences as illustrated in FIG. 19 to create serial data S5 [D34, D33, D42, D41, D50, D49, D58, D57] having the unit data D34 as a head. In this manner, serial data S5 suitable for the format of the converter 625 is created by converting the image data PDT. The BAA controller 104 outputs the serial data S5 to the converter 625.

[0113] When the serial data S5 is output to the converter 625, the unit data of the serial data S5 are sequentially output from the output lines L1 to L4. When the unit data D34, D33, D42, and D41 of the serial data S5 are sequentially output, the unit data D34, D33, D42, and D41 are stored in the shift register SR1 of the output lines L1 to L4 as illustrated in FIG. 20. Subsequently, When the unit data D50, D49, D58, and D57 are sequentially output, the unit data D34, D33, D42, and D41 are sent to the shift register SR2 of the output lines L1 to L4 and are stored therein as illustrated in FIG. 21. In addition, the unit data D50, D49, D58, and D57 are stored in the shift register SR1 of the output lines L1 to L4.

[0114] If the unit data D33, D41, D49, D57, D34, D42, D50, and D58 are stored in both the shift registers SR1 and SR2 of the output lines L1 to L4, the unit data are output to the blankers BK15, BK16, BK17, BK18, BK25, BK26, BK27, and BK28, respectively, through the buffer BF. As a result, a dose of the electron beams EBmn passing through the holes HH15, HH16, HH17, HH18, HH25, HH26, HH27, and HH28 is controlled on the basis of the value of the unit data. Consequently, as illustrated in FIG. 22, the marks M15 to M18 and M25 to M28 of the unit pattern PA are drawn with a predetermined dose.

[0115] The BAA controller 104 also creates the serial data S6 to S8 from the unit data of the data groups G6 to G8 and outputs the serial data S6 to S8 to the converters 626, 627, and 628. As a result, the marks Mm5 to Mm8 are drawn in the right half area of the unit pattern PA of FIG. 9, so that the drawing of the unit pattern PA is completed.

[0116] FIG. 23 is a schematic diagram illustrating serial data obtained by arranging the unit data D33 to D64 on the basis of the arrangement rank of the image data PDT and serial data obtained by arranging the unit data D33 to D64 on the basis of a sorting rule. In the process described above, the unit data D33 to D64 are converted from the serial data having the unit data D33 as a head and the unit data D64 as a tail into the serial data S51, S52, S61, S62, S71, S72, S81, and S82. In addition, the converted serial data are sequentially output one by one to the lines L1 to L4 of the converters 625 to 628 of FIG. 6. As a result, the serial data S5 to S8 are output to the converters 625 to 628, respectively.

[0117] The electron beam lithography apparatus 10 consecutively draws the unit pattern PA on the upper surface of the specimen 120 as illustrated in FIG. 10 on the basis of the aforementioned method to finally obtain the circuit pattern CPA.

[0118] In the electron beam lithography apparatus 10, the unit data of the image data PDT are sorted as described above. When the unit data are sorted, a sorting error may occur, for example, if the number of the unit data of the image data PDT is too large. In this regard, in the electron beam lithography apparatus 10, a sorting error is diagnosed using a checksum. An error diagnosis process for diagnosing a sorting error will be described below with reference to FIG. 24.

<Diagnosis Process>

[0119] FIG. **24** is a flowchart illustrating an error diagnosis process. A series of processes of FIG. **24** are executed by the BAA controller **104**.

[0120] The BAA controller **104** calculates a checksum for each arrangement rank of the unit data of each block of the data groups G**1** to G**4** in the left area of the image data PDT (step S**101**).

[0121] As shown in FIGS. **25** and **26**, the BAA controller **104** calculates a checksum CS**1** by summing the values of the first unit data D**1**, D**3**, D**5**, D**7**, D**17**, D**19**, D**21**, and D**23** of each block B**11**, B**21**, B**31**, B**41**, B**12**, B**22**, B**32**, and B**42**. Similarly, the BAA controller **104** calculates checksums CS**2** to CS**4** by summing the second to fourth unit data of each block B**11**, B**21**, B**31**, B**41**, B**12**, B**22**, B**32**, and B**42**.

[0122] The following checksums CS**1** to CS**4** obtained in this manner are based on the arrangement ranks of the unit data in the image data PDT. If the checksums CS**1** to CS**4** are calculated as described below, the number of the checksums becomes equal to the number of the unit data in the block. For this reason, a data area for storing the checksums can be reduced, compared to a case where the checksum is calculated for each rank (first to eight ranks) of the data group.

$$CS1=D1+D3+D5+D7+D17+D19+D21+D23$$

$$CS2=D2+D4+D6+D8+D18+D20+D22+D24$$

$$CS3=D9+D11+D13+D15+D25+D27+D29+D31$$

$$CS4=D10+D12+D14+D16+D26+D28+D30+D32$$

[0123] The BAA controller **104** calculates checksums of each rank on the unit data sorting rule for each block of the data groups G**1** to G**4** in the left area of the image data PDT (step S**102**).

[0124] As recognized from FIGS. **27** and **28**, the BAA controller **104** calculates a checksum ACS**1** by summing the values of the first unit data D**10**, D**12**, D**14**, D**16**, D**26**, D**28**, D**30**, and D**32** on the sorting rule of each block B**11**, B**21**, B**31**, B**41**, B**12**, B**22**, B**32**, and B**42**. Similarly, the BAA controller **104** calculates checksums ACS**2** to ACS**4** by summing the second to fourth unit data of each block B**11**, B**21**, B**31**, B**41**, B**12**, B**22**, B**32**, and B**42**.

[0125] The checksums ACS**1** to ACS**4** obtained in this manner are based on the arrangement rank of the sorting rule.

$$ACS1=D26+D28+D30+D32+D10+D12+D14+D16$$

$$ACS2=D25+D27+D29+D31+D9+D11+D13+D15$$

$$ACS3=D18+D20+D22+D24+D2+D4+D6+D8$$

$$ACS4=D17+D19+D21+D23+D1+D3+D5+D7$$

[0126] The BAA controller **104** calculates checksums of each arrangement rank of the unit data for each block of the data groups G**5** to G**8** in the right area of the image data PDT of FIG. **13** (step S**103**). The following resultant checksums CS**5** to CS**8** are based on the arrangement rank of the unit data in the image data PDT.

$$CS5=D33+D35+D37+D39+D49+D51+D53+D55$$

$$CS6=D34+D36+D38+D40+D50+D52+D54+D56$$

$$CS7=D41+D43+D45+D47+D57+D59+D61+D63$$

$$CS8=D42+D44+D46+D48+D58+D60+D62+D64$$

[0127] As shown in FIG. **27**, the BAA controller **104** calculates checksums of each rank on the unit data sorting rule for each block of the data groups G**5** to G**8** in the right area of the image data PDT (step S**104**). The following resultant checksums ACS**5** to ACS**8** are based on the arrangement rank on the sorting rule.

$$ACS5=D34+D36+D38+D40+D50+D52+D54+D56$$

$$ACS6=D33+D35+D37+D39+D49+D51+D53+D55$$

$$ACS7=D42+D44+D46+D48+D58+D60+D62+D64$$

$$ACS8=D41+D43+D45+D47+D57+D59+D61+D63$$

[0128] The BAA controller **104** compares the checksums CS**1** to CS**8** and the checksums ACS**1** to ACS**8** (step S**105**).

[0129] As recognized from FIG. **29**, for the data group G**1** to G**4**, the arrangement ranks **1**, **2**, **3**, and **4** correspond to the sorting rule ranks **4**, **3**, **2**, and **1**. For this reason, it is natural that the unit data of the checksum CS**1** matches the unit data of the checksum ACS**4**, and the checksum CS**1** is equal to the checksum ACS**4** as illustrated in FIG. **31**.

[0130] Similarly, it is natural that the checksums CS**2**, CS**3**, and CS**4** are equal to the checksums ACS**3**, ACS**2**, and ACS**1**, respectively.

[0131] As recognized from FIG. **30**, for the data groups G**5** to G**8**, the arrangement ranks **1**, **2**, **3**, and **4** correspond to the sorting rule ranks **2**, **1**, **4**, and **3**. For this reason, it is natural that the unit data of the checksum CS**5** matches the unit data of the checksum ACS**6**, and the checksum CS**5** is equal to the checksum ACS**6** as illustrated in FIG. **31**.

[0132] Similarly, it is natural that the checksums CS**6**, CS**7**, and CS**8** are equal to the checksums ACS**5**, ACS**8**, and ACS**7**, respectively.

[0133] Here, the BAA controller **104** compares the corresponding checksums with each other as illustrated in FIG. **31**.

[0134] The BAA controller **104** determines whether or not an error occurs in conversion of the image data PDT on the basis of a result of the checksum comparison (step S**106**). The BAA controller **104** determines that there is an error in conversion of the image data PDT if there is a difference between the corresponding checksums (YES in step S**106**). For example, if the checksum CS**11** has a value of "X," and the checksum ACS**14** has a value of "Y" different from "X," it is determined that there is an error in conversion of the image data PDT.

[0135] Meanwhile, if the corresponding checksums have an identical value, the BAA controller **104** determines that there is no error in conversion of the image data PDT (NO in step S**106**). For example, if the checksum CS**11** has a value of "Z," and the checksum ACS**14** also has a value of "Z," it is determined that there is no error in conversion of the image data PDT.

[0136] If there is an error in conversion of the image data PDT, the BAA controller **104** notifies a result of the checksum comparison, for example, to the controller **101** (step S**107**). As a result, for example, patterning on the specimen **120** is interrupted.

[0137] FIG. **32** is a diagram conceptually illustrating the original image data PDT and image data APDT equivalent to the serial data obtained by converting the original image data PDT. As shown in FIG. **32**, in the electron beam lithography apparatus **10**, the data are output while the

positions of the blocks B11, B21, B31, and B41 in the original image data PDT are exchanged with the positions of the blocks B12, B22, B32, and B42.

[0138] In this regard, in order to diagnose an error generated by the block exchange, the BAA controller **104** calculates a checksum based on the original image data PDT (step S**108**).

[0139] Specifically, the BAA controller **104** calculates a checksum CSB**1** by summing the unit data of the blocks B**11**, B**21**, B**31**, and B**41** of the image data PDT and calculates a checksum CSB**2** by summing the unit data of the blocks B**12**, B**22**, B**32**, and B**42**. The checksum CSB**1** can be calculated on the basis of the following Equation (1). In addition, the checksum CSB**2** can be calculated on the basis of the following Equation (2).

$$CSB1=D1+D2+D9+D10+D3+D4+ \ldots +D16 \quad (1)$$

$$CSB2=D17+D18+D25+D26+D19+D20+ \ldots +D32 \quad (2)$$

[0140] The BAA controller **104** calculates a checksum based on the image data APDT equivalent to the serial data (step S**109**).

[0141] Specifically, the BAA controller **104** calculates the checksum ACSB**1** by summing the unit data of the blocks B**11**, B**21**, B**31**, and B**41** of the image data APDT and calculates the ACSB**2** by summing the unit data of the blocks B**12**, B**22**, B**32**, and B**42**. The checksum ACSB**1** can be calculated on the basis of the following Equation (3). The checksum ACSB**2** can be calculated on the basis of the following Equation (4).

$$ACSB1=D10+D9+D2+D1+D12+D11+ \ldots +D7 \quad (3)$$

$$ACSB2=D26+D25+D18+D17+D28+D27+ \ldots +D23 \quad (4)$$

[0142] The BAA controller **104** compares the checksums CSB**1** and CSB**2** and the checksums ACSB**1** and ACSB**2** (step S**110**).

[0143] As shown in FIG. **32**, it is natural that the checksum CSB**1** representing a sum of the unit data of the blocks B**11**, B**21**, B**31**, and B**41** of the image data PDT is equal to the checksum ACSB**1** representing a sum of the unit data of the blocks B**11**, B**21**, B**31**, and B**41** of the image data APDT. Similarly, it is natural that the checksum CSB**2** representing a sum of the unit data of the blocks B**12**, B**22**, B**32**, and B**42** of the image data PDT is equal to the checksum ACSB**2** representing a sum of the unit data of the blocks B**12**, B**22**, B**32**, and B**42** of the image data APDT.

[0144] Then, the BAA controller **104** determines whether or not an error is generated from the block exchange process on the basis of a result of the checksum comparison (step S**111**). If there is a difference between the corresponding checksums, the BAA controller **104** determines that there is an error in conversion of the image data PDT (YES in step S**111**). For example, if the checksum CSB**1** has a value of "X," and the checksum ACSB**1** has a value of "Y" different from "X," it is determined that there is an error in the block exchange process.

[0145] Meanwhile, if the values of the corresponding checksums are equal to each other, the BAA controller **104** determines that there is no error in the block exchange process (NO in step S**111**). For example, if the checksum CSB**1** has a value of "Z," and the checksum ACSB**1** has the identical value of "Z," it is determined that there is no error in the block exchange process.

[0146] If there is an error in the block exchange process, the BAA controller **104** notifies the controller **101** of a result of the checksum comparison, for example, (step S**112**). As a result, for example, pattering on the specimen **120** is interrupted.

[0147] If the process of step S**112** is terminated, or it is determined that there is no error in step S**111**, the BAA controller **104** terminates the error diagnosis process.

[0148] As described above, according to this embodiment, the checksum is calculated for each rank of the unit data contained in the blocks of the image data PDT (steps S**101** to S**104**). For this reason, it is possible to diagnose an error generated in parallel/serial conversion of the image data PDT by comparing the checksums (step S**105**). As a result, it is possible to detect a conversion error with high accuracy and improve a patterning resolution.

[0149] According to this embodiment, when the image data PDT is converted into the image data APDT, the checksum is calculated for each group of the exchanged blocks as illustrated in FIG. **32** (steps S**108** and S**109**). For this reason, by comparing the checksums (step S**110**), it is possible to diagnose an error generated in the block exchange process. As a result, it is possible to detect a conversion error with high accuracy and improve a patterning resolution.

[0150] As described above, according to this embodiment, a diagnosis can be performed for each particular process such as parallel/serial conversion of the image data PDT or the block exchange process. Therefore, it is possible to easily specify when a patterning error is generated during the processing and reduce a downtime of the system.

[0151] While embodiments according to the present disclosure have been described, they are not intended to limit the scope of the present disclosure. For example, although a dose of the electron beams EBmn is determined on the basis of the values of the unit data D**1** to D**64**, various other methods may also be employed to control the dose of the electron beams EBmn. For example, the dose of the electron beams EBmn may be controlled in an ON/OFF manner on the basis of the values of the unit data D**1** to D**64**. In addition, the unit data D**1** to D**64** may have a bit length of several bits to several tens of bits, and the electron beam irradiation time may be controlled depending on the bit value. As a result, marks Mmn having various gradations can be formed. An example of the dose control will be described below.

<Dose Control>

[0152] FIG. **33** is a schematic diagram illustrating unit data Di (where "i"=1 to 64). The unit data Di (where "i"=1 to 64) are, for example, 8-bit data, and first to eighth bit data are set to Xi(**1**) to Xi(**8**), respectively. The bit data Xi(**1**) to Xi(**8**) has a value of "1" or "0." The irradiation time of the electron beam EBmn is allocated to the bit data Xi(**1**) to Xi(**8**). In the electron beam lithography apparatus **10**, for example, the irradiation times 6 ns, 12 ns, 24 ns, 48 ns, 96 ns, 192 ns, 384 ns, and 768 ns are allocated to the bit data Xi(**1**) to Xi(**8**), respectively, as illustrated in FIG. **33**. For this reason, the irradiation time IT (ns) shown in the unit data Di can be represented as the following Equation (5). For example, if the unit data Di (Xi(**1**) to Xi(**8**)) is set to [10100000], the irradiation time IT becomes 30 ns (=6·1+24·1).

$$IT=6Xi(1)+12Xi(2)+24Xi(3)+48Xi(4)+96Xi(5)+192Xi(6)+384Xi(7)+768Xi(8) \quad (5)$$

[0153] The BAA controller **104** sorts the bit data of the unit data Di on the basis of a predetermined rule. For example, if the ON/OFF control of the electron beams EBmn is performed sequentially from the first bit of the bit data Xi(**1**) to the eighth bit of the bit data Xi(**8**), the ON/OFF switching control of the electron beam EBmn for every short interval such as 6 ns, 12 ns, or 24 ns may be necessary in the first half. In this regard, the BAA controller **104** performs the exchange process of the bit data Xi(**1**) to Xi(**8**) of the unit data Di on the basis of a predetermined rule.

[0154] For example, the BAA controller **104** combines the bit data Xi1 representing "6 ns" and the bit data Xi8 representing "768 ns" as illustrated in FIG. **34**. Similarly, the bit data Xi(**2**) representing "12 ns" and the bit data Xi(**7**) representing "384 ns" are combined. The bit data Xi(**3**) representing "24 ns" and the bit data Xi(**6**) representing "192 ns" are combined. The bit data Xi(**4**) representing "48 ns" and the bit data Xi(**5**) representing "96 ns" are combined. As a result, the unit data Di is converted into unit data ADi [Xi(**4**), Xi(**5**), Xi(**3**), Xi(**6**), Xi(**2**), Xi(**7**), Xi(**1**), and Xi(**8**)].

[0155] From the converters **621** to **628**, the data DXi(**4**) to DXi(**8**) corresponding to the first bit of the bit data Xi(**4**) to the eighth bit of the bit data Xi(**8**) of the unit data ADi are sequentially output. Note that the data DXi(**1**) to DXi(**8**) are data for turning on the electron beam EBmn only for the irradiation time allocated to the bit data Xi(l) to Xi(**8**).

[0156] For example, the converter **621** outputs data DX**26**(**4**), DX**25**(**4**), DX**18**(**4**), and DX**17**(**4**) corresponding to the first bits X**26**(**4**), X**25**(**4**), X**18**(**4**), and X**17**(**4**) of the unit data D**26**, D**25**, D**18**, and D**17**, respectively, to the output lines L**1** to L**4**. Then, the converter **621** outputs data DX**10**(**4**), DX**9**(**4**), DX**2**(**4**), and DX**1**(**4**) corresponding to the first bits X**10**(**4**), X**9**(**4**), X**2**(**4**), and X**1**(**4**) of the unit data D**10**, D**9**, D**2**, and D**1**, respectively, to the output lines L**1** to L**4**. Similarly, the converter **621** repeats the above described operation for the second and subsequent bits of the unit data D**26**, D**25**, D**18**, D**17**, D**10**, D**9**, D**2**, and D**1**.

[0157] If the converters **621** to **628** repeat the above described operation for each bit data of the unit data Di, a mark Mmn having a predetermined gradation is formed.

<Diagnosis Process>

[0158] The BAA controller **104** calculates a checksum before and after the bit data exchange process of the unit data Di. For example, the value VDi of the unit data Di itself can be expressed as the following Equation (6). Therefore, the checksum CSD before the sorting of the unit data Di can be obtained using the following Equation (7).

$$VDi=2^7Xi(8)+2^6Xi(7)+2^5Xi(6)+2^4Xi(5)+2^3Xi(4)+2^2Xi(3)+2^1Xi(2)+2^0Xi(1) \quad (6)$$

$$CSD = (X1(8)+X2(8)+\ldots X64(8))\times 2^7+(X1(7)+X2(7)+\ldots X64(7))\times 2^6+(X1(6)+X2(6)+\ldots X64(6))\times 2^5+(X1(5)+X2(5)+\ldots X64(5))\times 2^4+(X1(4)+X2(4)+\ldots X64(4))\times 2^3+ \quad (7)$$

-continued

$$(X1(3)+X2(3)+\ldots X64(3))\times 2^2+(X1(2)+X2(2)+\ldots X64(2))\times 2^1+(X1(1)+X2(1)+\ldots X64(1))\times 2^0 = k8\times 2^7+k7\times 2^6+k6\times 2^5+k5\times 2^4+k4\times 2^3+k3\times 2^2+k2\times 2^1+k1\times 2^0$$

[0159] The BAA controller **104** calculates the checksum ACSD for the unit data ADi [Xi(**8**), Xi(**1**), Xi(**7**), Xi(**2**), Xi(**6**), Xi(**3**), Xi(**5**), and Xi(**4**)] created by exchanging the bit data Xi(**1**) to Xi(**8**) of the unit data Di.

[0160] Specifically, the BAA controller **104** first calculates a sum Σ(j) of the bit data of the (j)th rank (j=1 to 8) from the bit data Xi(**1**) to Xi(**64**) of the sixty four unit data ADi on the basis of the following Equations (8) to (15).

$$\Sigma(1)=X1(4)+X2(4)+\ldots+X64(4) \quad (8)$$

$$\Sigma(2)=X1(5)+X2(5)+\ldots+X64(5) \quad (9)$$

$$\Sigma(3)=X1(3)+X2(3)+\ldots+X64(3) \quad (10)$$

$$\Sigma(4)=X1(6)+X2(6)+\ldots+X64(6) \quad (11)$$

$$\Sigma(5)=X1(2)+X2(2)+\ldots+X64(2) \quad (12)$$

$$\Sigma(6)=X1(7)+X2(7)+\ldots+X64(7) \quad (14)$$

$$\Sigma(7)=X1(1)+X2(1)+\ldots+X64(1) \quad (13)$$

$$\Sigma(8)=X1(8)+X2(8)+\ldots+X64(8) \quad (15)$$

[0161] As recognized by comparing Equations (8) to (15) with Equation (7), if the exchange process of the bit data Xi(**1**) to Xi(**8**) is successful, the sum Σ(**1**) is equal to a coefficient "k**4**." Similarly, the sum Σ(**2**) is equal to the coefficient "k**5**." The sum Σ(**3**) is equal to the coefficient "k**3**." The sum Σ(**4**) is equal to the coefficient "k**6**." The sum Σ(**5**) is equal to the coefficient "k**2**." The sum Σ(**6**) is equal to the coefficient "k**7**." The sum Σ(**7**) is equal to the coefficient "k**1**." The sum Σ(**8**) is equal to the coefficient "k**8**."

[0162] In this regard, the BAA controller **104** calculates the checksum ACSD using the following Equation (16).

$$ACSD=\Sigma(8)\times 2^7+\Sigma(7)\times 2^6+\Sigma(6)\times 2^5+\Sigma(5)\times 2^4+\Sigma(4)\times 2^3+\Sigma(3)\times 2^2+\Sigma(2)\times 2^1+\Sigma(1)\times 2^0 \quad (16)$$

[0163] The BAA controller **104** compares the checksums CSD and ACSD calculated as described above. If both the checksums CSD and ACSD are equal to each other, the BAA controller **104** determines that the exchange process of the bit data Xi(**1**) to Xi(**8**) is successful. Otherwise, if the checksums CSD and ACSD have different values as a result of comparison, the BAA controller **104** determines that there is an error in the exchange process of the bit data Xi(**1**) to Xi(**8**). In this case, the patterning on the specimen **120** may be interrupted. As a result, it is possible to improve a patterning resolution.

[0164] While the embodiments of the present disclosure and their modifications have been described, it would be appreciated that they are not intended to limit the scope of the present disclosure. For example, although the electron beam lithography apparatus draws a pattern using sixty four electron beams EBmn in the above described embodiments, the electron beam lithography apparatus **10** may draw a

pattern using sixty five or more electron beams or sixty three or less electron beams without a particular limitation.

[0165] In the embodiments described above, the unit data Di of the image data PDT are divided into eight data groups G**1** to G**8** as illustrated in FIG. **12**. Alternatively, the unit data may be divided into seven or less data groups or nine or more data groups depending on the number of unit data of the image data PDT without a particular limitation.

[0166] In the embodiments described above, each of the converters **621** to **628** outputs eight unit data as illustrated in FIG. **6**. Alternatively, one converter may process nine or more unit data depending on a specification of the converter without a particular limitation.

[0167] In the embodiments described above, the BAA controller **104** executes the error diagnosis process of FIG. **24**. Alternatively, the error diagnosis process may be executed by devices other than the BAA controller **104** such as the controller **101** or any external device without a particular limitation.

[0168] The functions of the BAA controller **104** according to each embodiment of the disclosure may be implemented in a dedicated hardware device or a typical computer system. The program executed by the BAA controller **104** may be distributed while being stored in a computer-readable recording medium such as a flexible disk, a compact disc read-only memory (CD-ROM), a digital versatile disk (DVD). Alternatively, the program may also be installed in the BAA controller **104** via the Internet.

[0169] A part of or the entirety of the programs described above may be executed, for example, on a server, and information relating to execution thereof may be received by the BAA controller **104** through a communication network to execute the error diagnosis process.

[0170] While several embodiments according to the present invention have been described, they are just for exemplary purposes and are not intended to limit the scope of the invention. These novel embodiments may be embodied in various other forms, and various omissions, substitutions, or modifications may also be possible without departing from the scope and spirit of the invention. Such various embodiments or modifications should be construed as being included in the scope and spirit of the invention contained in the attached claims and equivalents thereof.

1. A method of diagnosing a conversion process for converting a format of image data including unit data corresponding to charged particle beams into a format suitable for an aperture array, the aperture array having a plurality of controllers provided to match a plurality of the charged particle beams to control the charged particle beams and a driver configured to drive the controllers, the method comprising:

extracting the unit data having an identical first rank based on an arrangement of the unit data in the image data from the unit data of each block including a predetermined number of the unit data and calculating a first checksum of each of the first rank;

extracting the unit data having an identical second rank after the conversion process from the unit data of each of the blocks and calculating a second checksum of each of the second rank; and

comparing the first and second checksums.

2. The method according to claim **1**, wherein the driver is provided in each group having a predetermined number of the controllers, further comprising dividing the unit data into the blocks having the unit data corresponding to an output of the driver.

3. The method according to claim **1**, wherein the number of the unit data in each of the blocks is identical one anther between the blocks.

4. The method according to claim **1**, further comprising:

dividing each of the blocks into a first block and a second block;

calculating a third checksum based on the unit data included in the first block;

calculating a fourth checksum based on the unit data included in the second block; and

comparing the third checksum with the fourth checksum.

5. The method according to claim **4**, wherein a count of the unit data of the first block is equal to a count of the unit data of the second block.

6. The method according to claim **1**, wherein the plurality of unit data include a plurality of bit data arranged based on predetermined ranks,

the method further comprising:

calculating a sum of values of the plurality of unit data as a fifth checksum;

summing the bit data of the unit data for each of the predetermined ranks;

calculating a sixth checksum based on a result of the summing; and

comparing the fifth checksum with the sixth checksum.

7. The method according to claim **6**, wherein a time for defining a dose of the charged particle beam is allocated to the bit data.

8. The method according to claim **6**, wherein the bit data are paired, and

the bit data are arranged such that a difference of the dose defined by the pair of the bit data is minimized between the pair of bit data.

9. A charged particle beam lithography apparatus comprising:

an aperture array having a plurality of controllers provided to match a plurality of charged particle beams to control the charged particle beams and a driver configured to drive the controllers;

a converter configured to convert a format of image data having unit data corresponding to the charged particle beams into a format suitable for the aperture array;

a first calculator configured to extract the unit data having an identical first rank based on the arrangement of the unit data of the image data from the unit data of each block having a predetermined number of the unit data and calculate a first checksum for each of the first rank;

a second calculator configured to extract the unit data having an identical second rank after the conversion of the converter from the unit data of each of the blocks and calculate a second checksum for each of the second ranks; and

a first comparator configured to compare the first checksum with the second checksum.

10. The charged particle beam lithography apparatus according to claim **9**, wherein the driver is provided in each group having a predetermined number of the controllers, and

the unit data are divided into the blocks having the unit data matching the output of the driver.

11. The charged particle beam lithography apparatus according to claim **9**, wherein each of the blocks is divided into a first block and a second block, further comprising:
a third calculator configured to calculate a third checksum based on the unit data of the first block;
a fourth calculator configured to calculate a fourth checksum based on the unit data of the second block; and
a second comparator configured to compare the third checksum with the fourth checksum.

12. The charged particle beam lithography apparatus according to claim **9**, wherein the plurality of unit data include a plurality of bit data arranged based on predetermined ranks, further comprising:
a fifth calculator configured to calculate a sum of values of the plurality of unit data as a fifth checksum;
a summer configured to sum the bit data of the unit data for each of the predetermined rank;
a sixth calculator configured to calculate a sixth checksum based on a result of the summing of the summer; and
a third comparator configured to compare the fifth checksum with the sixth checksum.

13. The charged particle beam lithography apparatus according to claim **12**, wherein a time for defining a dose of the charged particle beam is allocated to the bit data.

14. The charged particle beam lithography apparatus according to claim **12**, wherein the bit data are paired, and
the bit data are arranged such that a difference of the dose defined by the pair of bit data is minimized between the pair of bit data.

15. A computer readable recording medium storing a program for diagnosing a conversion process for converting a format of image data including unit data corresponding to charged particle beams into a format suitable for an aperture array, the aperture array having a plurality of controllers provided to match a plurality of the charged particle beams to control the charged particle beams, and a driver configured to drive the controllers, wherein
the program causes a computer to execute:
extracting the unit data having an identical first rank based on an arrangement of the unit data in the image data from the unit data of each block including a predetermined number of the unit data and calculating a first checksum of each of the first rank;
extracting the unit data having an identical second rank after the conversion process from the unit data of each of the blocks and calculating a second checksum of each of the second rank; and
comparing the first checksum with the second checksum.

16. The computer readable recording medium according to claim **15**, wherein the driver is provided in each group having a predetermined number of the controllers, further comprising dividing the unit data into the blocks having the unit data corresponding to an output of the driver.

17. The computer readable recording medium according to claim **15**,
wherein the program causes the computer to further execute:
dividing each of the blocks into a first block and a second block;
calculating a third checksum based on the unit data included in the first block;
calculating a fourth checksum based on the unit data included in the second block; and
comparing the third checksum with the fourth checksum.

18. The computer readable recording medium according to claim **15**,
wherein the plurality of unit data include a plurality of bit data arranged based on predetermined ranks,
the program causes the computer to further execute:
calculating a sum of values of the plurality of unit data as a fifth checksum;
summing the bit data of the unit data for each of the predetermined ranks;
calculating a sixth checksum based on a result of the summing; and
comparing the fifth checksum with the sixth checksum.

19. The computer readable recording medium according to claim **18**, wherein a time for defining a dose of the charged particle beam is allocated to the bit data.

20. The computer readable recording medium according to claim **18**, wherein, the bit data are paired, and
the bit data are arranged such that a difference of the dose defined by the pair of the bit data is minimized between the pair of bit data.

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