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(54) **IMAGING ELEMENT AND IMAGING DEVICE**

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(57) **ABSTRACT**

An imaging element (**10**) according to an embodiment of the present disclosure includes: an imaging section (**11**) in which a plurality of pixels (**110**) individually including a photoelectric conversion element is arranged in a matrix; a convolution circuit (**20**, **20**A) that performs convolution processing on a plurality of pixel signals, which are analog signals each output from the plurality of pixels (**110**), on a basis of a convolution coefficient; and a pooling circuit (**150**) that performs pooling processing on the plurality of pixel signals that has been subjected to the convolution processing.

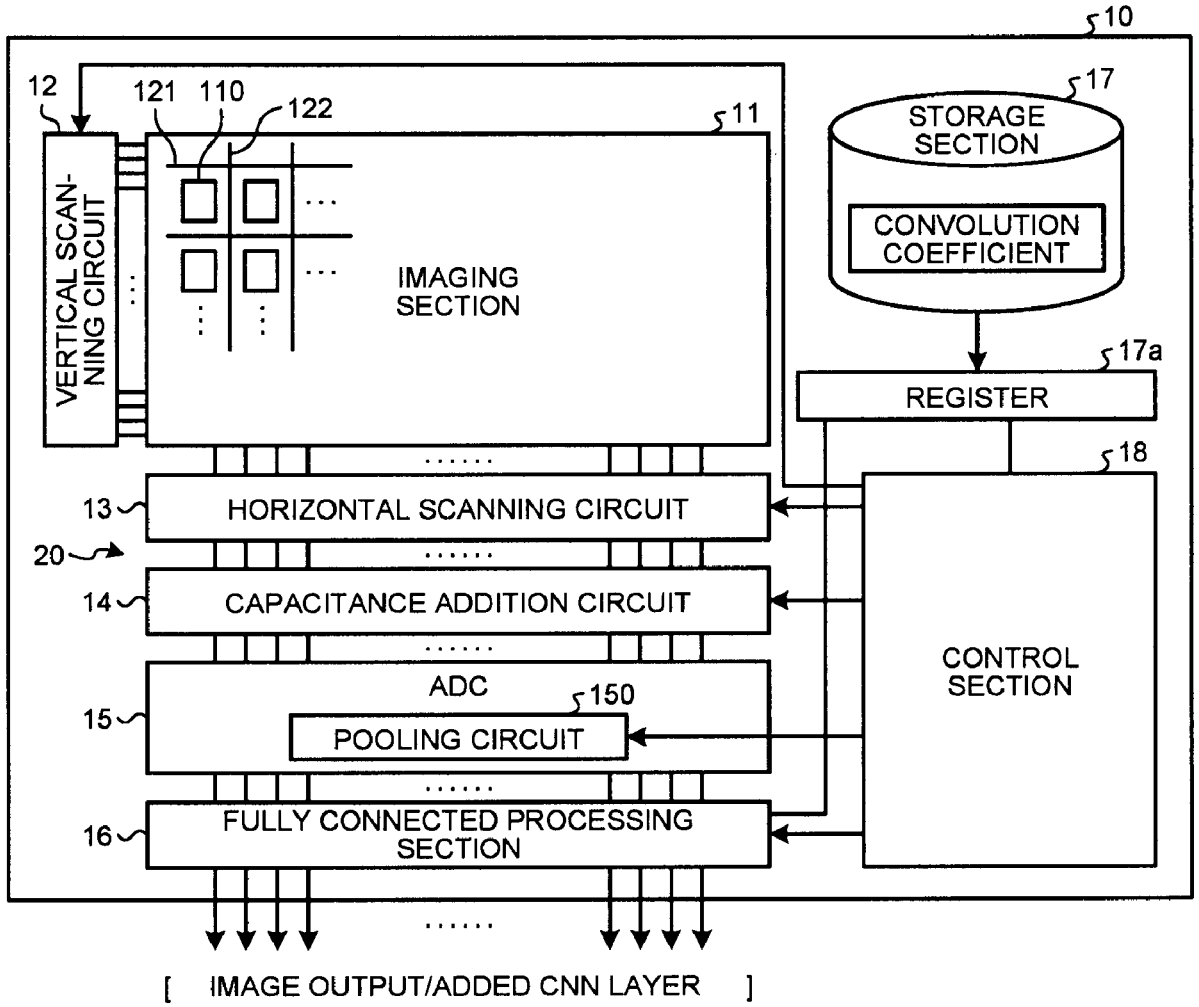


FIG.1

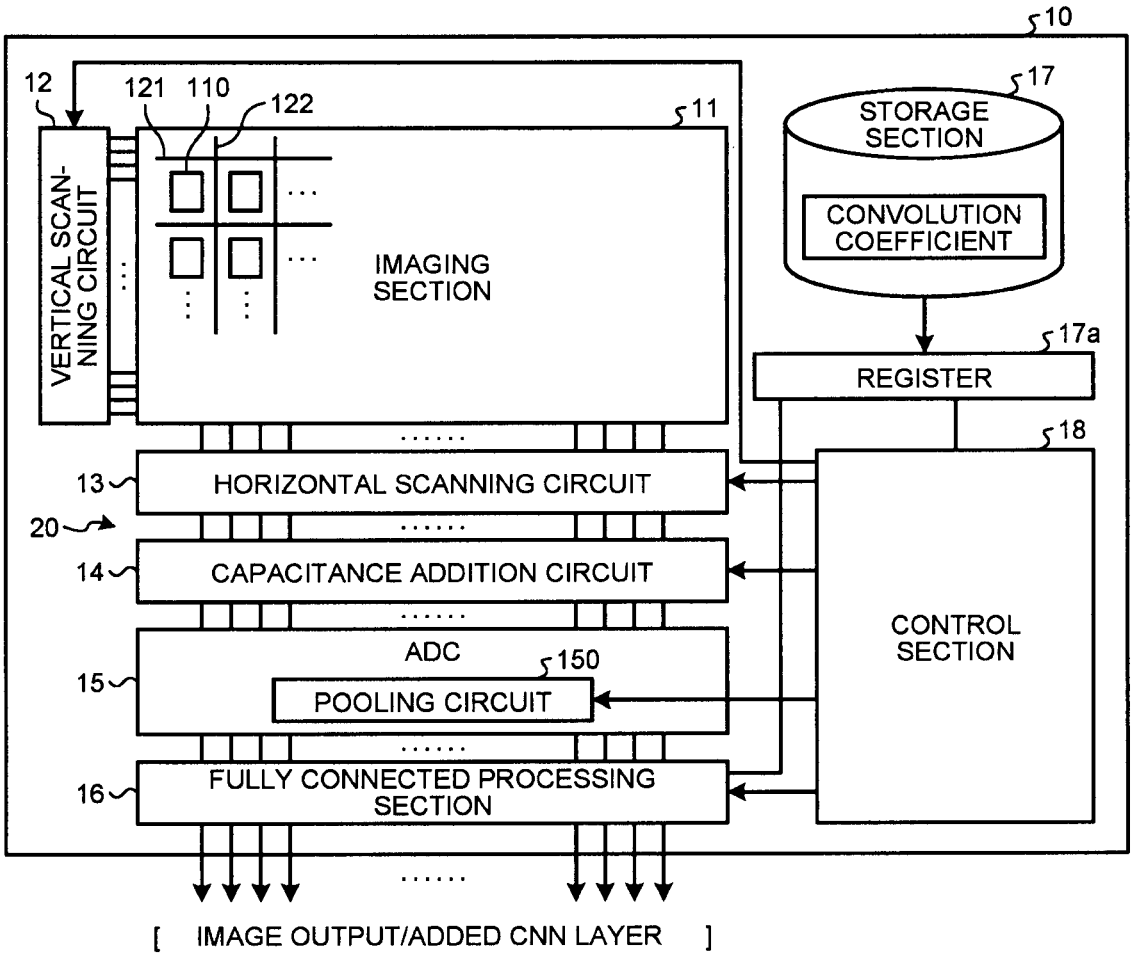

10
12
121
110
122
11
17
STORAGE SECTION
CONVOLUTION COEFFICIENT
VERTICAL SCANNING CIRCUIT
IMAGING SECTION
17a
REGISTER
18
13
HORIZONTAL SCANNING CIRCUIT
20
14
CAPACITANCE ADDITION CIRCUIT
ADC
150
15
POOLING CIRCUIT
CONTROL SECTION
16
FULLY CONNECTED PROCESSING SECTION
[IMAGE OUTPUT/ADDED CNN LAYER]

FIG.2

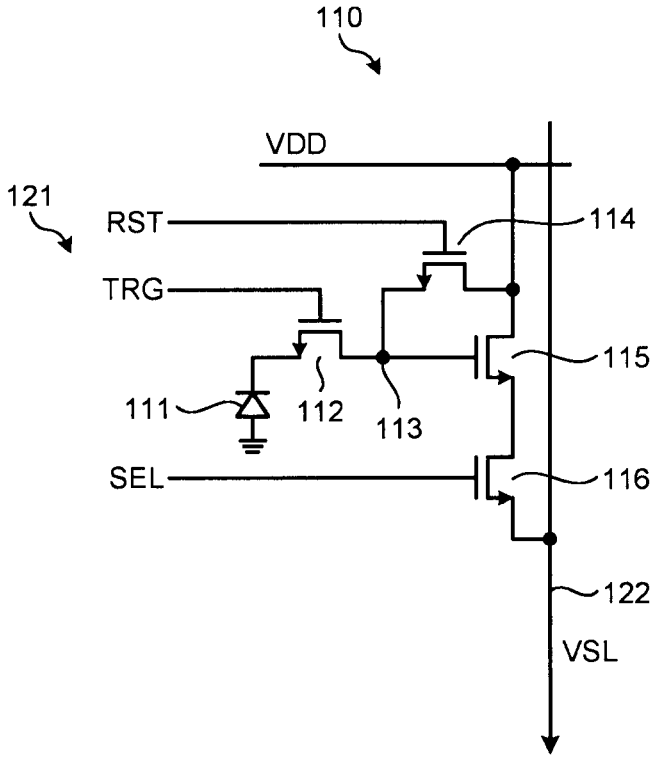


FIG.3

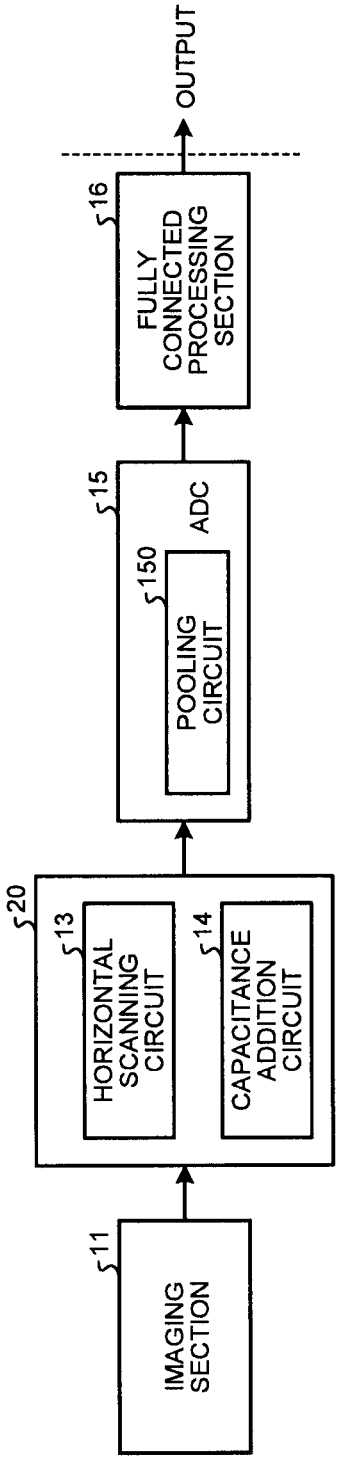

OUTPUT
16
FULLY CONNECTED PROCESSING SECTION
15
ADC
150
POOLING CIRCUIT
20
13
HORIZONTAL SCANNING CIRCUIT
14
CAPACITANCE ADDITION CIRCUIT
11
IMAGING SECTION

FIG.4

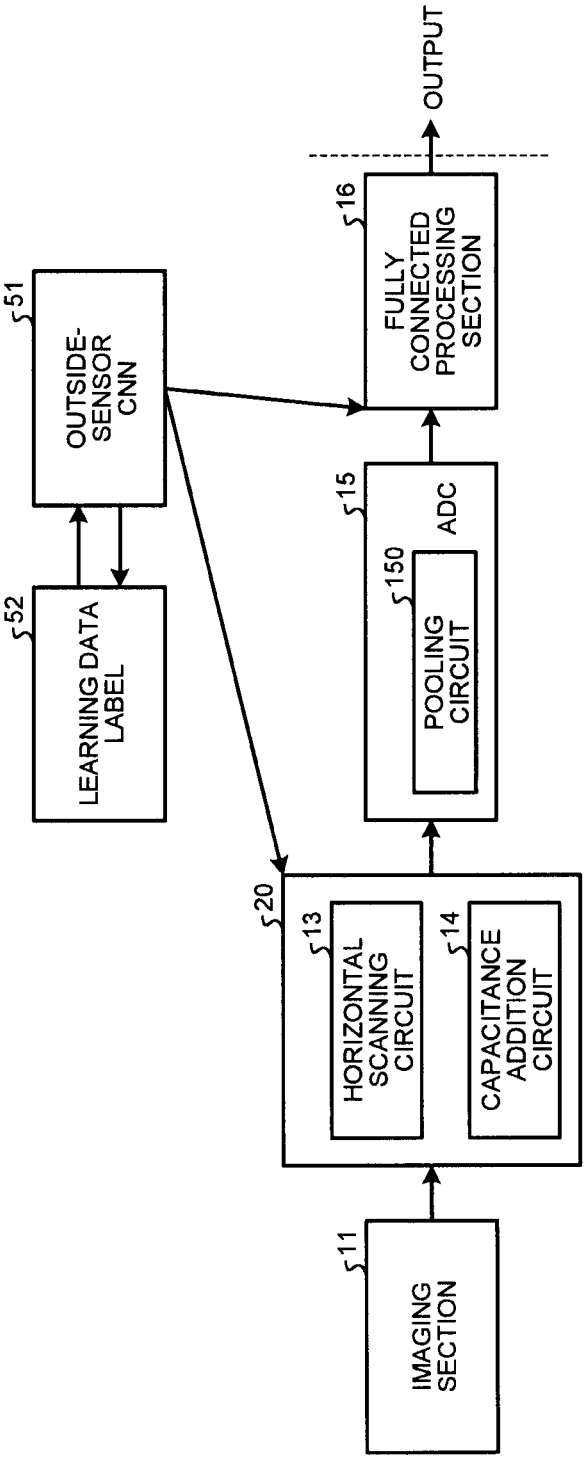

OUTPUT
16
FULLY CONNECTED PROCESSING SECTION
51
OUTSIDE-SENSOR CNN
52
LEARNING DATA LABEL
15
ADC
150
POOLING CIRCUIT
20
13
HORIZONTAL SCANNING CIRCUIT
14
CAPACITANCE ADDITION CIRCUIT
11
IMAGING SECTION

FIG.5

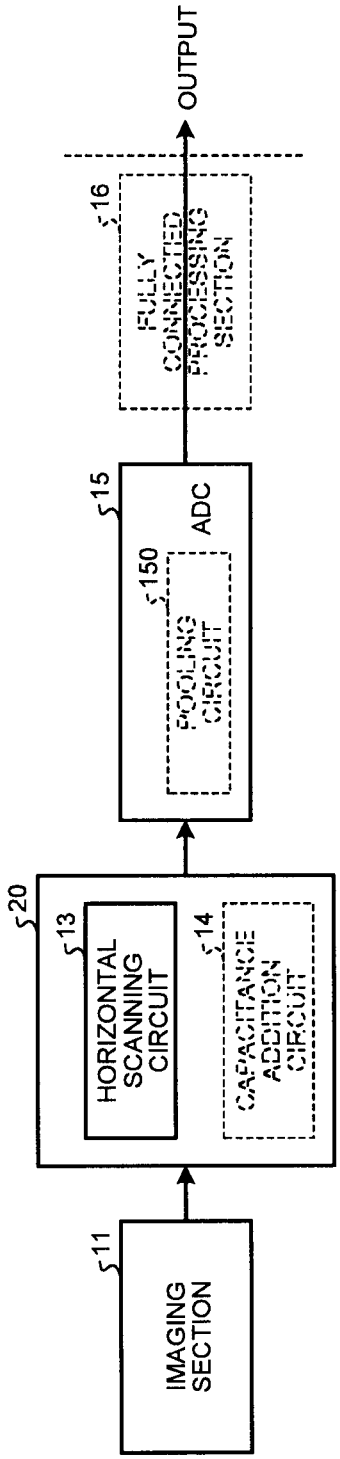

OUTPUT
16
FULLY CONNECTED PROCESSING SECTION
15
ADC
150
POOLING CIRCUIT
20
13
HORIZONTAL SCANNING CIRCUIT
14
CAPACITANCE ADDITION CIRCUIT
11
IMAGING SECTION

FIG.6

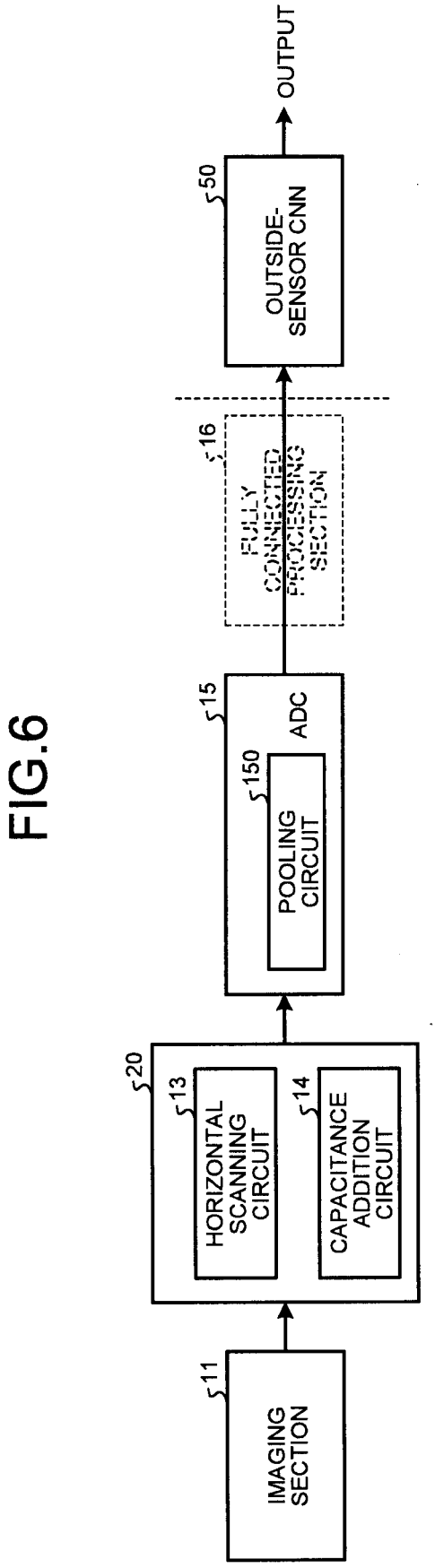
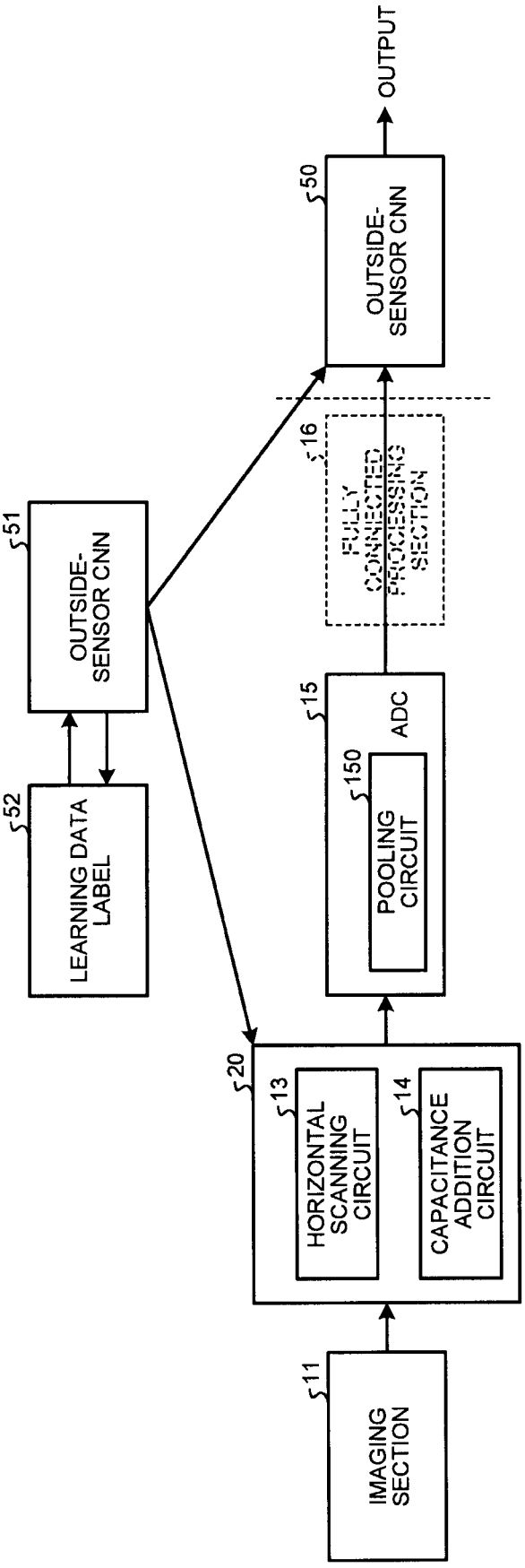

OUTPUT
50
OUTSIDE-SENSOR CNN
16
FULLY CONNECTED PROCESSING SECTION
15
ADC
150
POOLING CIRCUIT
20
13
HORIZONTAL SCANNING CIRCUIT
14
CAPACITANCE ADDITION CIRCUIT
11
IMAGING SECTION

FIG.7


OUTPUT
50
OUTSIDE-SENSOR CNN
16
FULLY CONNECTED PROCESSING SECTION
51
OUTSIDE-SENSOR CNN
15
ADC
150
POOLING CIRCUIT
52
LEARNING DATA LABEL
20
13
HORIZONTAL SCANNING CIRCUIT
14
CAPACITANCE ADDITION CIRCUIT
11
IMAGING SECTION

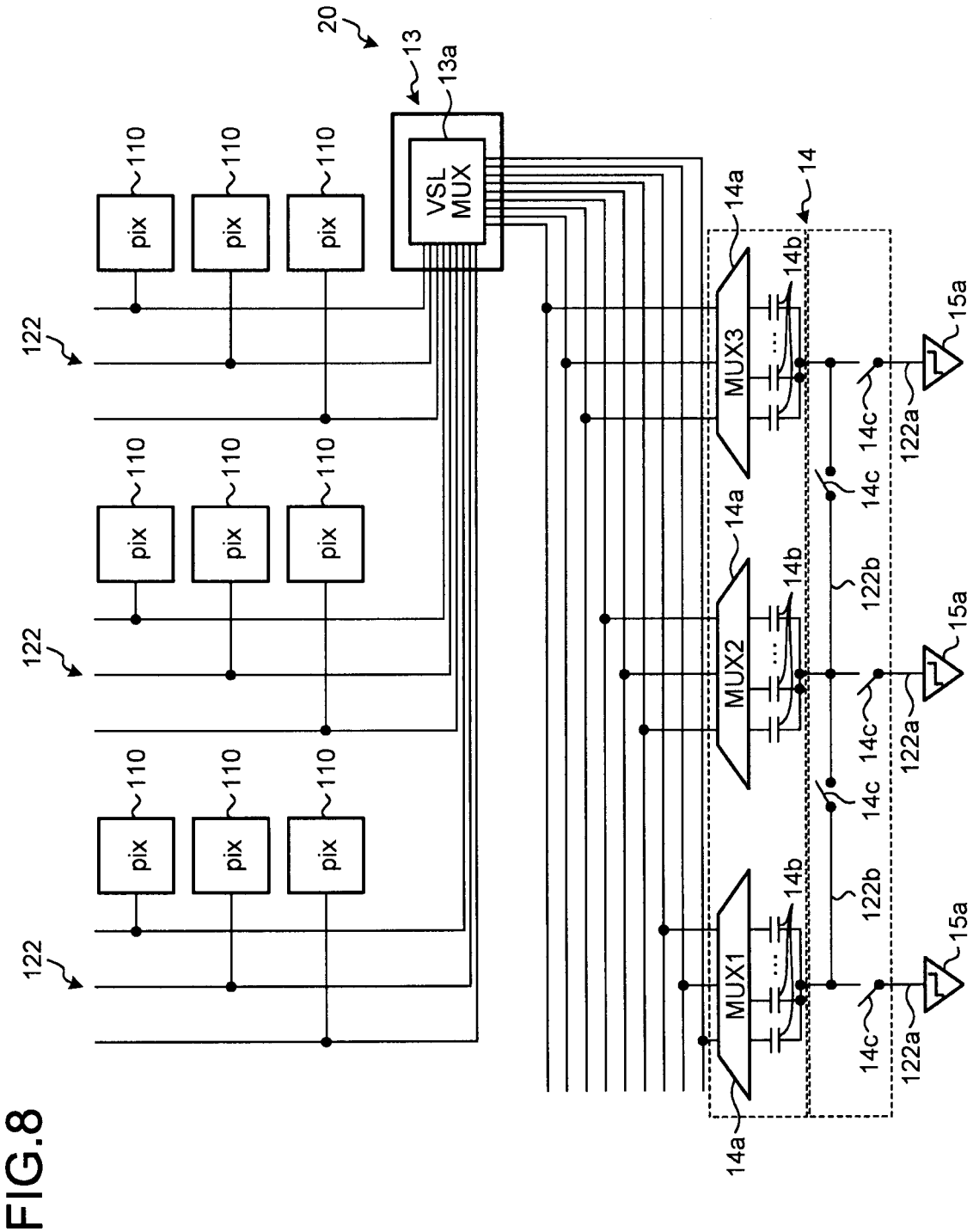

20
13
13a
VSL MUX
pix
110
122
14
14a
14b
14c
MUX3
MUX2
MUX1
122a
122b
15a

FIG.8

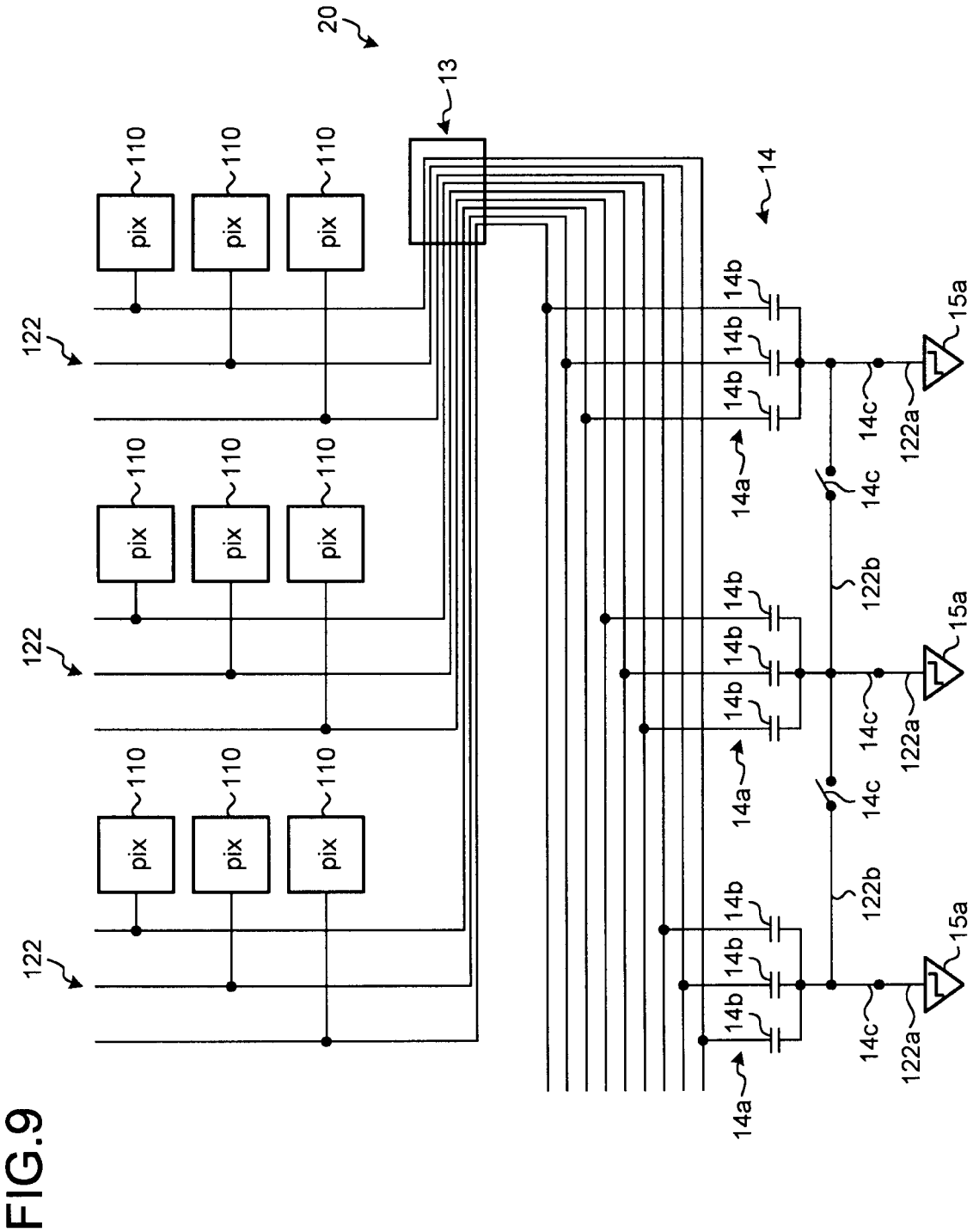


FIG.9

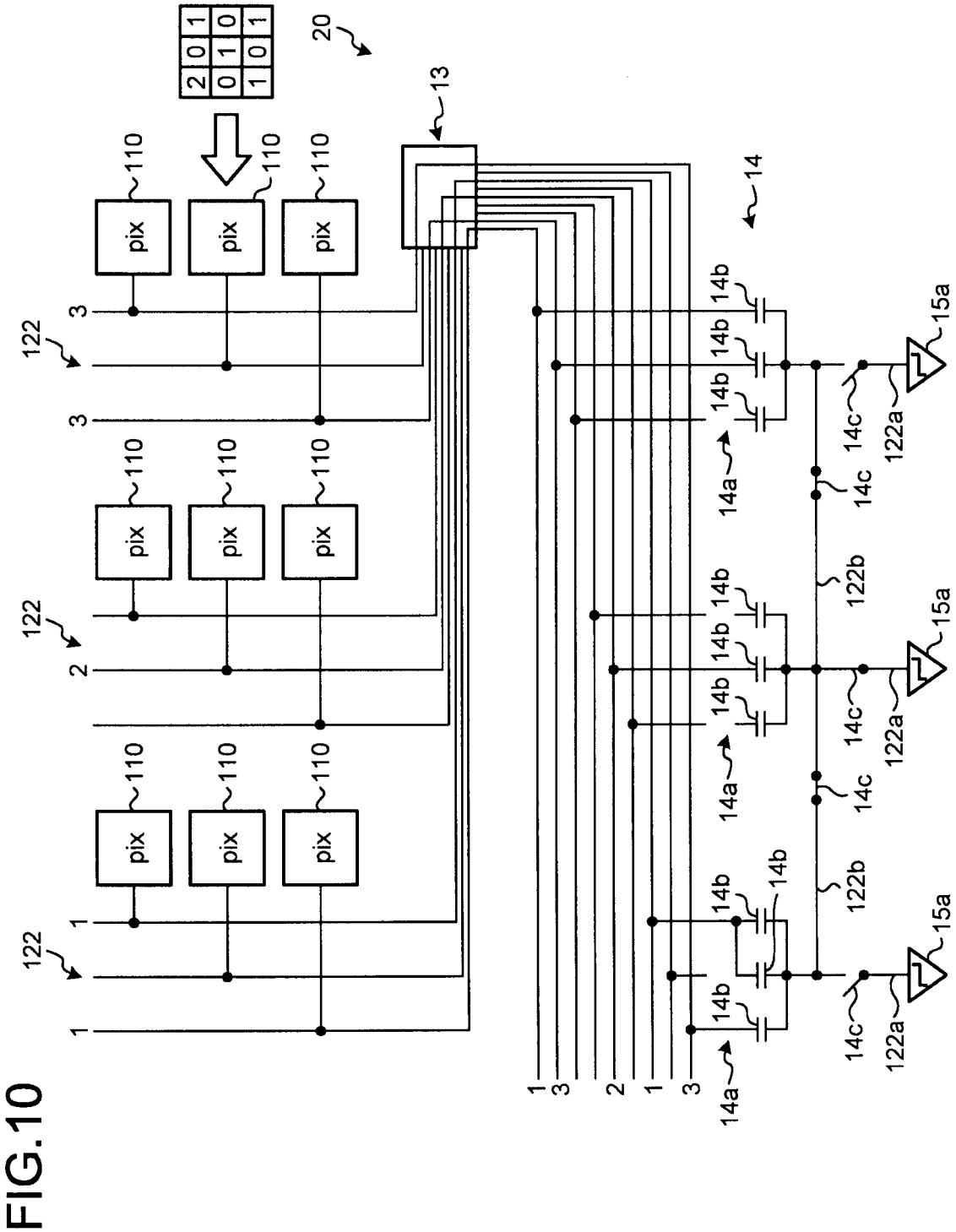
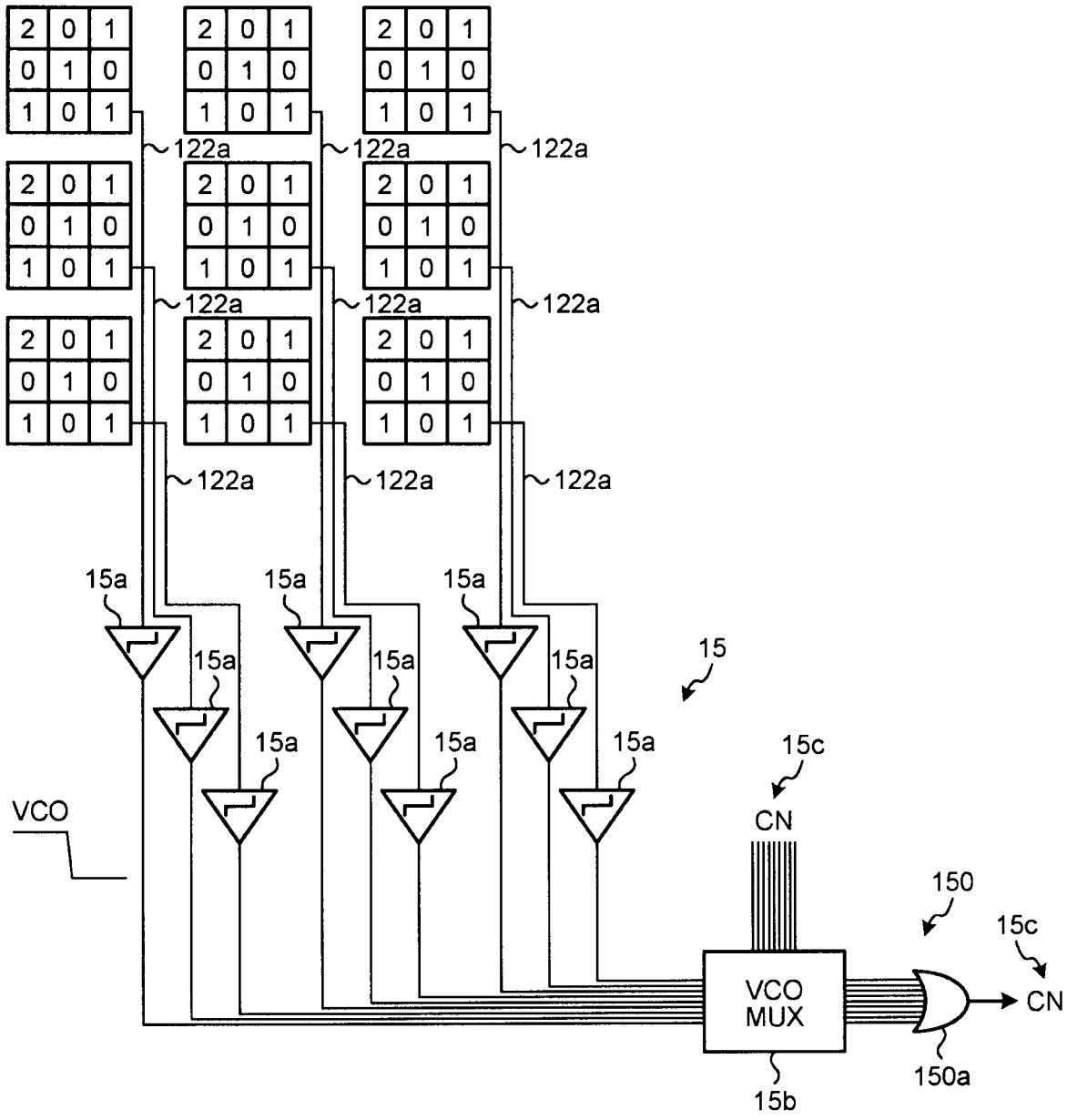


FIG.10

FIG.11



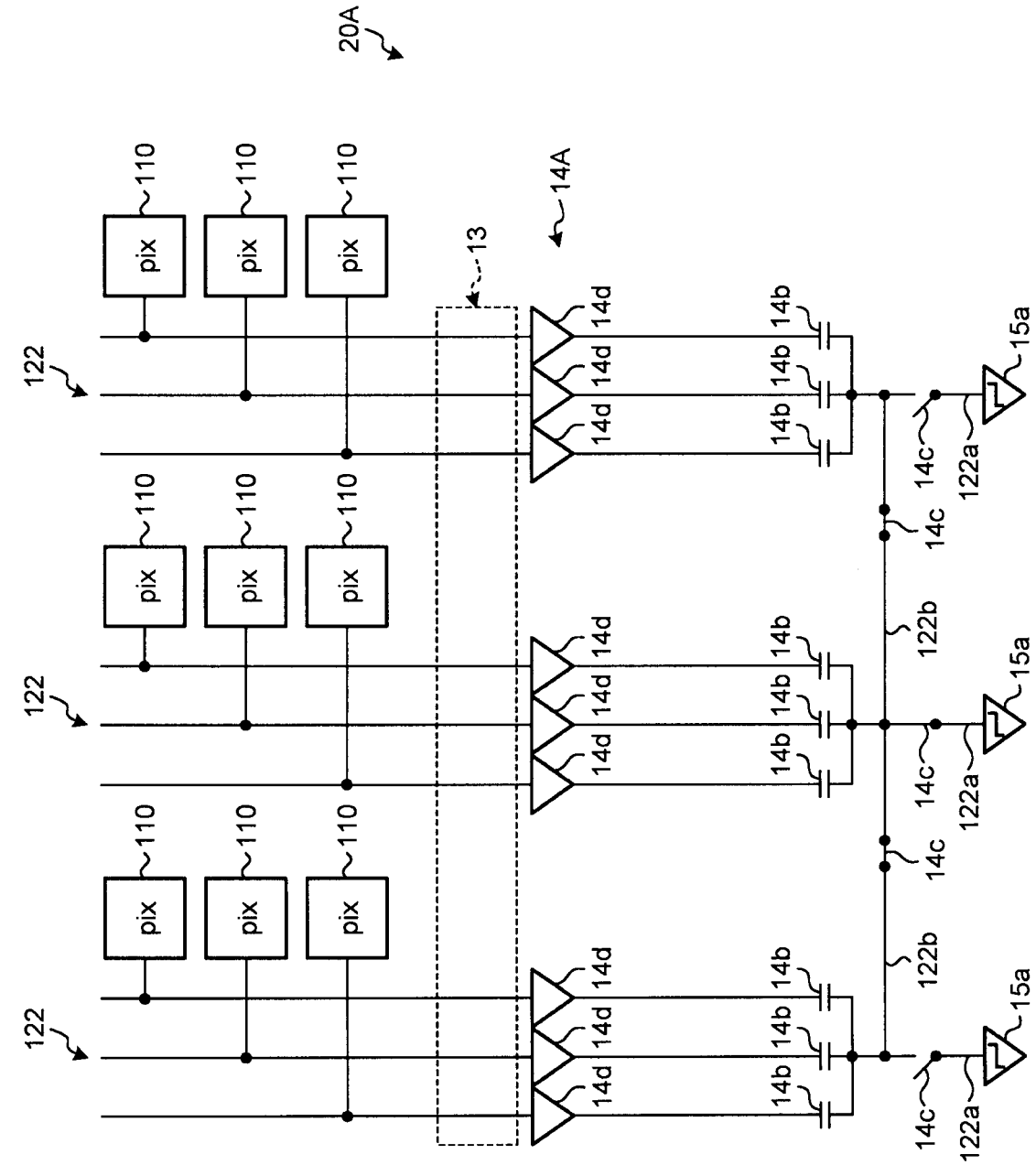


FIG.12

FIG.13

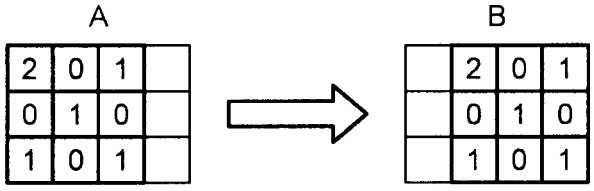


FIG.14

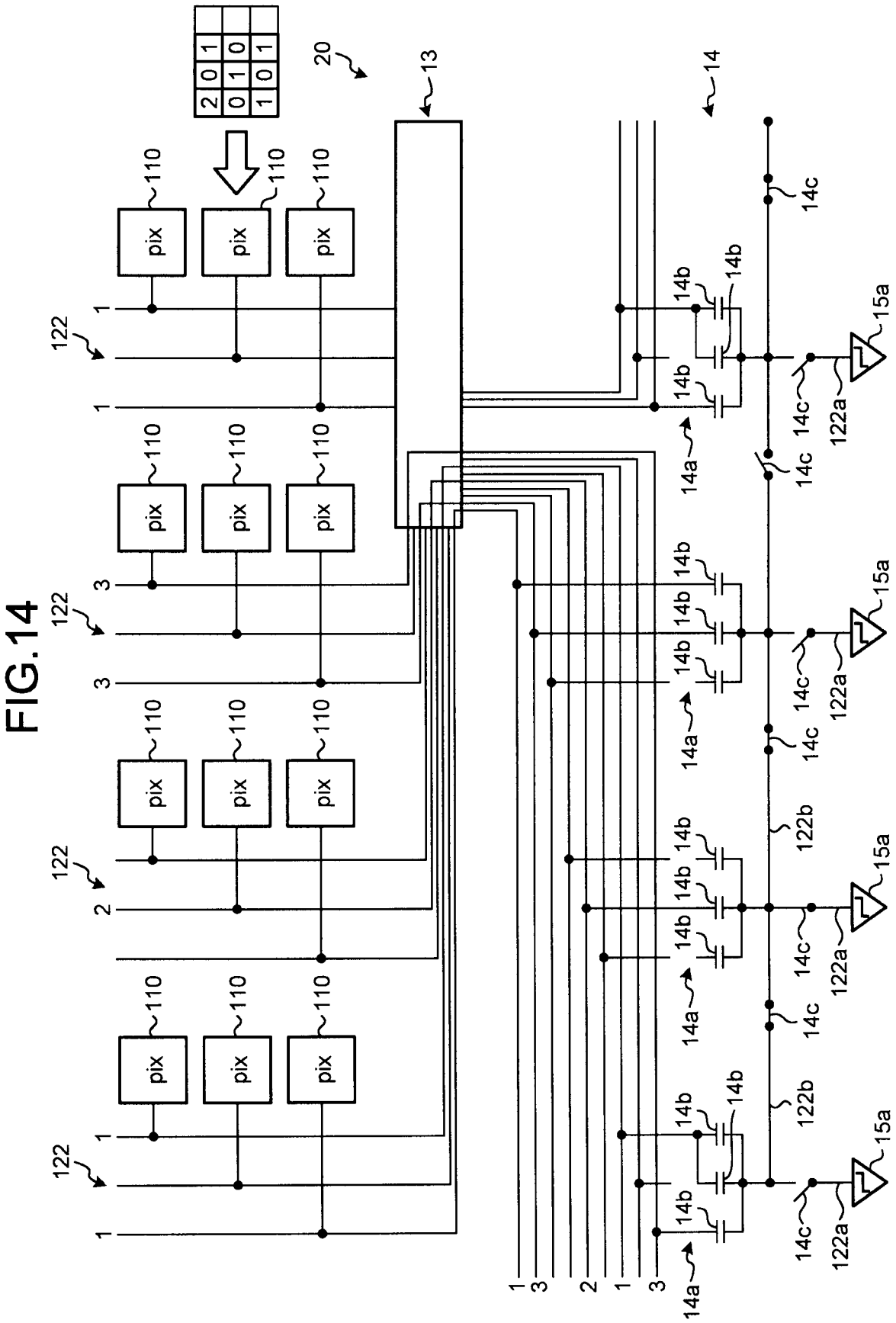


FIG.15

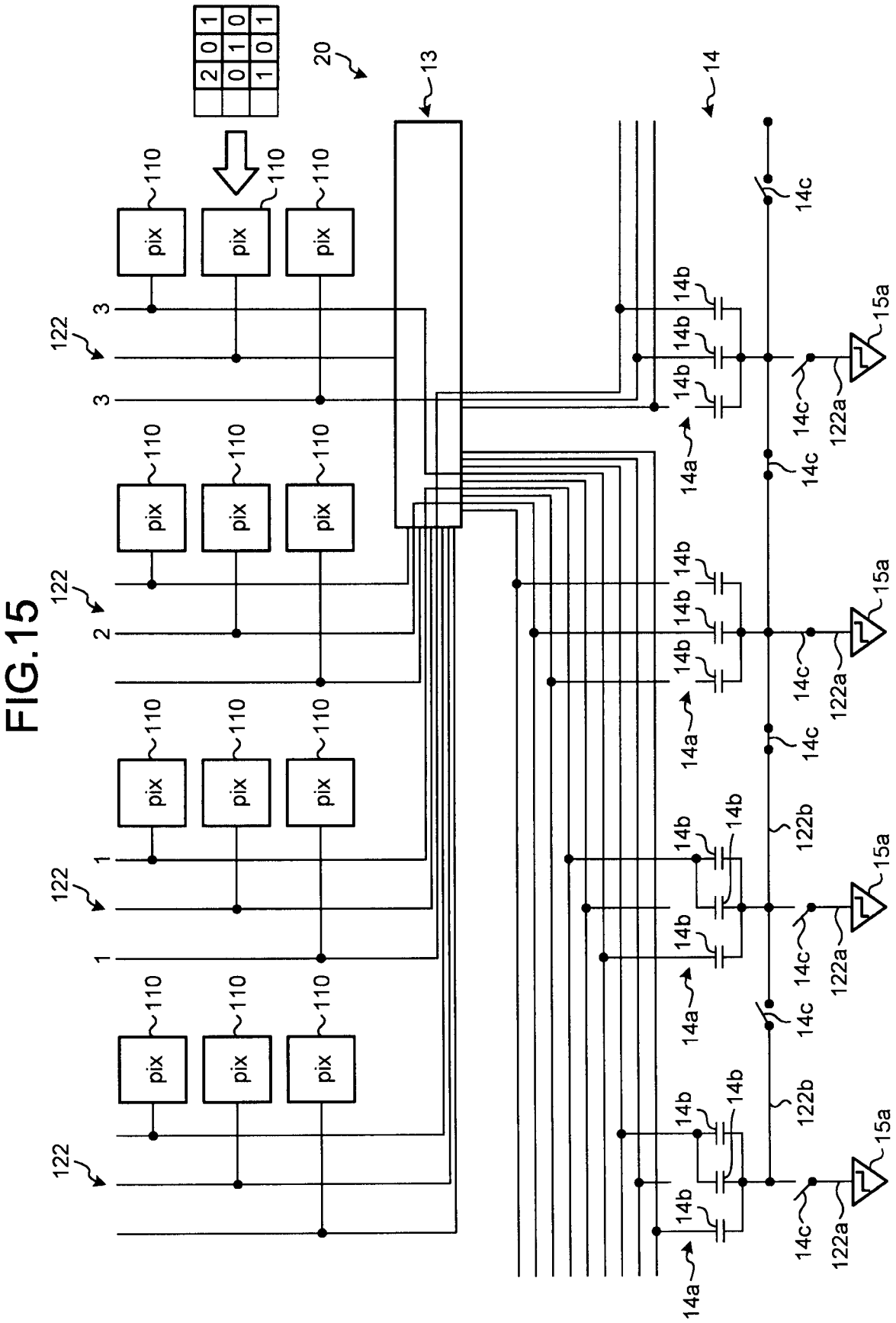


FIG.16

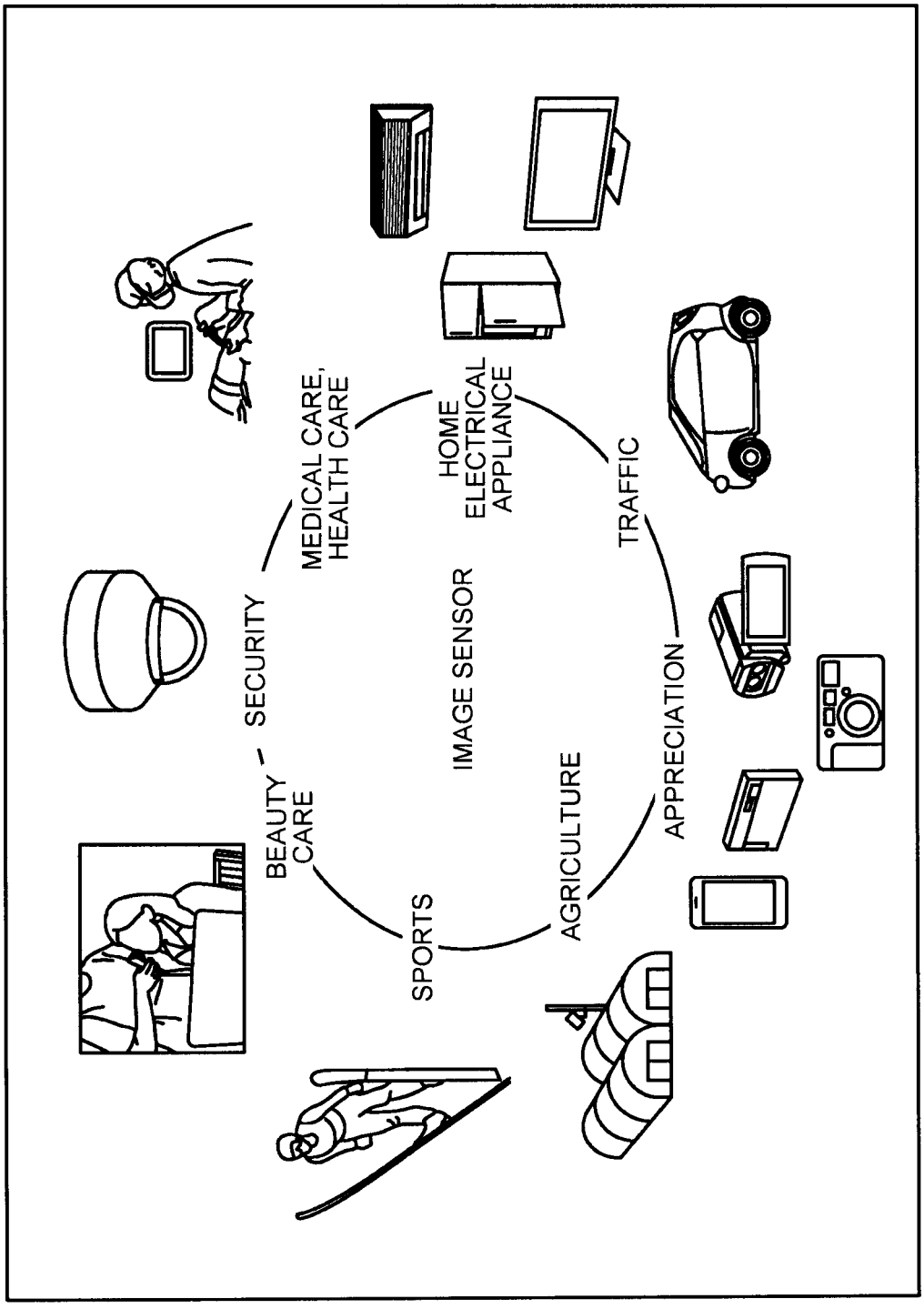


IMAGE SENSOR
MEDICAL CARE, HEALTH CARE
HOME ELECTRICAL APPLIANCE
TRAFFIC
APPRECIATION
AGRICULTURE
SPORTS
BEAUTY CARE
SECURITY

FIG.17

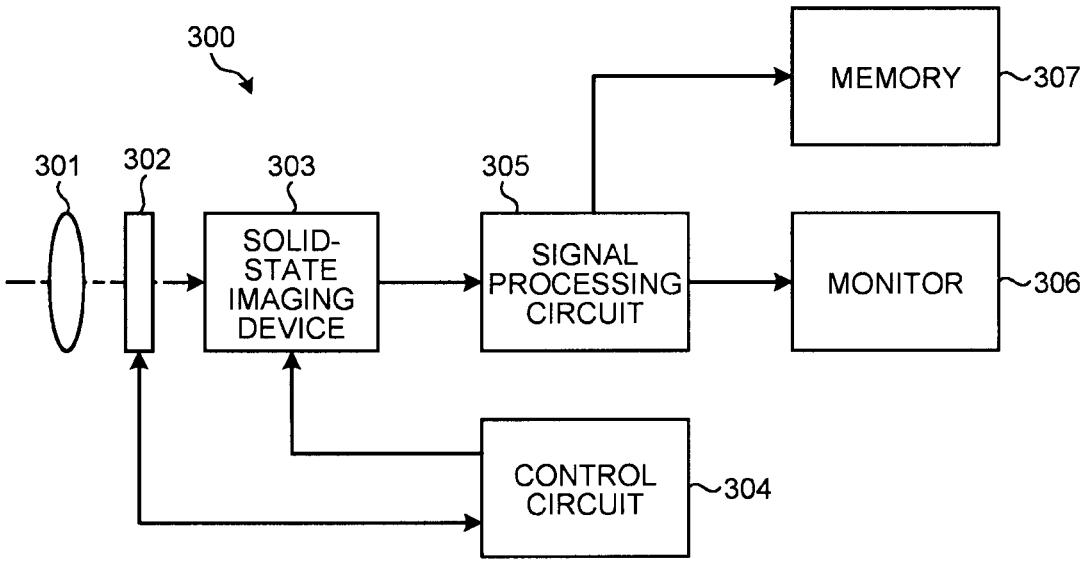

300
301
302
303
305
SOLID-STATE IMAGING DEVICE
SIGNAL PROCESSING CIRCUIT
MEMORY
307
MONITOR
306
CONTROL CIRCUIT
304

FIG.18

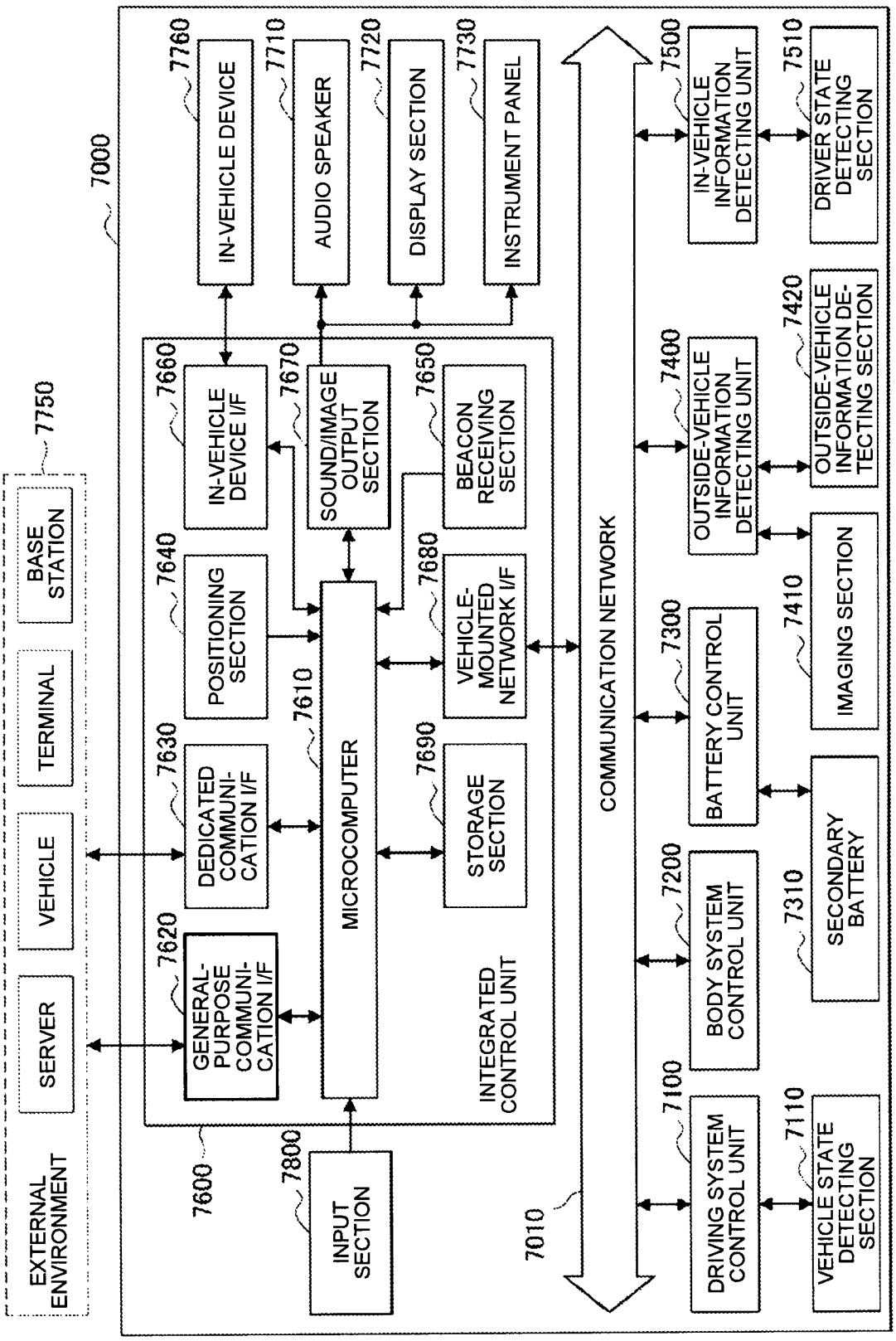
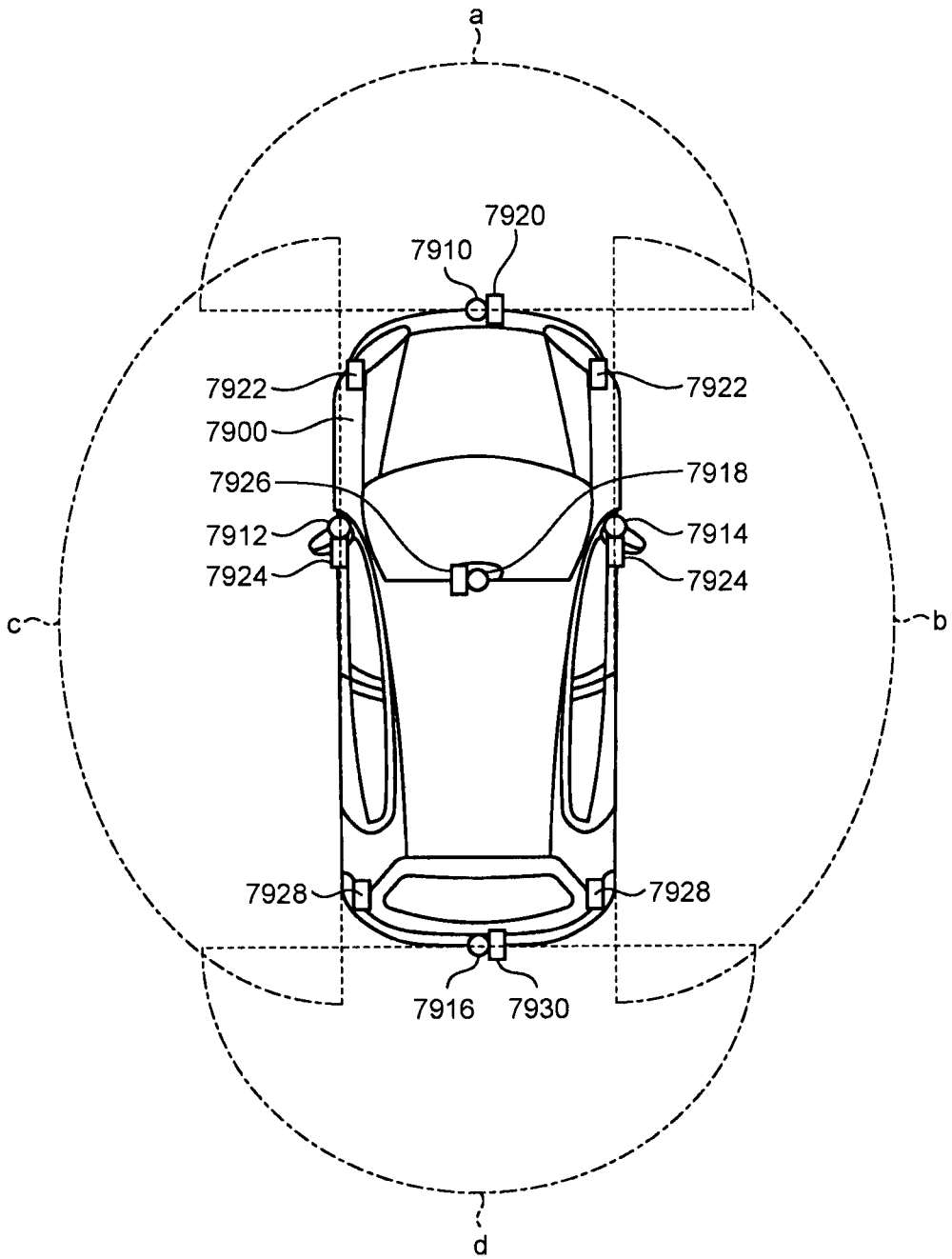

EXTERNAL ENVIRONMENT
SERVER
VEHICLE
TERMINAL
BASE STATION
7750
7000
7760
IN-VEHICLE DEVICE
7710
AUDIO SPEAKER
7720
DISPLAY SECTION
7730
INSTRUMENT PANEL
7660
IN-VEHICLE DEVICE I/F
7670
SOUND/IMAGE OUTPUT SECTION
7650
BEACON RECEIVING SECTION
7640
POSITIONING SECTION
7680
VEHICLE-MOUNTED NETWORK I/F
7630
DEDICATED COMMUNI-CATION I/F
7610
MICROCOMPUTER
7690
STORAGE SECTION
7620
GENERAL-PURPOSE COMMUNI-CATION I/F
7600
INTEGRATED CONTROL UNIT
7800
INPUT SECTION
7010
COMMUNICATION NETWORK
7500
IN-VEHICLE INFORMATION DETECTING UNIT
7510
DRIVER STATE DETECTING SECTION
7400
OUTSIDE-VEHICLE INFORMATION DETECTING UNIT
7420
OUTSIDE-VEHICLE INFORMATION DE-TECTING SECTION
7300
BATTERY CONTROL UNIT
7410
IMAGING SECTION
7200
BODY SYSTEM CONTROL UNIT
7310
SECONDARY BATTERY
7100
DRIVING SYSTEM CONTROL UNIT
7110
VEHICLE STATE DETECTING SECTION

FIG.19


a
7920
7910
7922
7922
7900
7926
7918
7912
7914
7924
7924
c
b
7928
7928
7916
7930
d

IMAGING ELEMENT AND IMAGING DEVICE

FIELD

[0001] The present disclosure relates to an imaging element and an imaging device.

BACKGROUND

[0002] Convolutional neural networks (CNNs) are actively used in the field of image recognition. In the CNN processing, a received input image reaches a fully connected layer (FC layer) through a convolution layer and a pooling layer. For example, when an image is output from a contact image sensor (CIS) and image recognition (for example, character recognition and object recognition) using a CNN is performed, a system outside the CIS is essential. In addition, the CNN may require a high-specification graphics processing unit (GPU) depending on a processing content. When real-time processing is intended to be performed, an image recognition system may become large.

CITATION LIST

Patent Literature

[0003] Patent Literature 1: JP 2012-227695 A

SUMMARY

Technical Problem

[0004] In order to simplify an image recognition system, implementing a CNN in CIS logic processing is conceivable. Convolution and pooling operation are, however, bottlenecks. Performing processing in a realistic time is difficult. A lead time for recognizing an image is increased. Therefore, it is demanded to shorten the lead time for recognizing an image while simplifying the image recognition system.

[0005] Therefore, the present disclosure provides an imaging element and an imaging device capable of simplifying an image recognition system and shortening a lead time.

Solution to Problem

[0006] An imaging element according to an embodiment of the present disclosure includes: an imaging section in which a plurality of pixels individually including a photoelectric conversion element is arranged in a matrix; a convolution circuit that performs convolution processing on a plurality of pixel signals, which are analog signals each output from the plurality of pixels, on a basis of a convolution coefficient; and a pooling circuit that performs pooling processing on the plurality of pixel signals that has been subjected to the convolution processing.

BRIEF DESCRIPTION OF DRAWINGS

[0007] FIG. **1** is a block diagram depicting an example of a schematic configuration of an imaging element according to a first embodiment.

[0008] FIG. **2** is a circuit diagram depicting an example of a schematic configuration of a pixel according to the first embodiment.

[0009] FIG. **3** is a block diagram depicting a flow of CNN operation of the imaging element according to the first embodiment.

[0010] FIG. **4** is a block diagram depicting a flow of CNN learning related to the CNN operation in FIG. **3**.

[0011] FIG. **5** is a block diagram depicting a flow of a normal image output operation of the imaging element according to the first embodiment.

[0012] FIG. **6** is a block diagram depicting a flow of a variation of the CNN operation of the imaging element according to the first embodiment.

[0013] FIG. **7** is a block diagram depicting a flow of the CNN learning related to the CNN operation in FIG. **6**.

[0014] FIG. **8** depicts an example of a schematic configuration of a convolution circuit based on a convolution filter according to the first embodiment.

[0015] FIG. **9** depicts an example of operation of the convolution circuit at the time of performing the normal image output processing according to the first embodiment.

[0016] FIG. **10** depicts an example of operation of the convolution circuit at the time of performing the convolution processing according to the first embodiment.

[0017] FIG. **11** depicts an example of a schematic configuration of an AD conversion circuit including a pooling circuit according to the first embodiment.

[0018] FIG. **12** depicts an example of a schematic configuration of the convolution circuit based on the convolution filter according to the second embodiment.

[0019] FIG. **13** depicts slide of a convolution filter according to a third embodiment.

[0020] FIG. **14** is a first diagram depicting an example of the operation of the convolution circuit at the time of performing the convolution processing according to the third embodiment.

[0021] FIG. **15** is a second diagram depicting an example of the operation of the convolution circuit at the time of performing the convolution processing according to the third embodiment.

[0022] FIG. **16** depicts a usage example in which an imaging element according to each embodiment is used.

[0023] FIG. **17** depicts an example of a schematic configuration of an imaging device.

[0024] FIG. **18** is a block diagram depicting an example of schematic configuration of a vehicle control system.

[0025] FIG. **19** is a diagram of assistance in explaining an example of installation positions of an outside-vehicle information detecting section and an imaging section.

DESCRIPTION OF EMBODIMENTS

[0026] Embodiments of the present disclosure will be described in detail below with reference to the drawings. Incidentally, in the following embodiments, the same reference signs are attached to the same parts, so that duplicate description will be omitted.

[0027] In addition, the present disclosure will be described in accordance with the following item order.

[0028] 1. First Embodiment

[0029] 1-1. Example of Schematic Configuration of Imaging Element

[0030] 1-2. Example of Schematic Configuration of Pixel

[0031] 1-3. CNN Operation Example and Normal Image Output Operation Example of Imaging Element

[0032] 1-4. Example of Schematic Configuration of Convolution Circuit

1. First Embodiment

[0041] <1-1. Example of Schematic Configuration of Imaging Device>

[0042] FIG. **1** is a block diagram depicting an example of a schematic configuration of an imaging element **10** according to a first embodiment. As depicted in FIG. **1**, the imaging element **10** includes an imaging section (pixel array section) **11**, a vertical scanning circuit **12**, a horizontal scanning circuit **13**, a capacitance addition circuit (addition circuit) **14**, an analog to digital (AD) conversion circuit **15**, a fully connected processing section **16**, a storage section **17**, and a control section **18**. The imaging element **10** is, for example, a complementary metal oxide semiconductor (CMOS) image sensor. The imaging element **10** is incorporated in various imaging devices such as a CIS, for example.

[0043] The imaging section **11** includes a plurality of pixels **110** capable of performing photoelectric conversion. These pixels **110** are arranged in a two-dimensional lattice pattern in a vertical direction (column direction) and a horizontal direction (row direction). In FIG. **1**, an arrangement in the vertical direction is defined as a column, and an arrangement in the horizontal direction is defined as a row. Each row is also referred to as a line. Each column is also referred to as a column. A pixel signal line **121** is connected to each pixel **110** for each row. A vertical signal line **122** is connected to each pixel **110** for each column. Each pixel signal line **121** is connected to the vertical scanning circuit **12**. Each vertical signal line **122** is connected to the horizontal scanning circuit **13**. For example, the pixel signal line **121** or the vertical signal line **122** includes a plurality of signal lines.

[0044] Under the control of the control section **18**, the vertical scanning circuit **12** transmits various signals such as a drive pulse for reading a pixel signal from a pixel **110** to the imaging section **11** via each pixel signal line **121**. For example, the vertical scanning circuit **12** supplies various signals such as a drive pulse to each pixel **110** via the pixel signal line **121** for each line, and causes each pixel **110** to output a pixel signal to the vertical signal line **122**. That is, each pixel **110** is driven for each line by a drive signal supplied from the vertical scanning circuit **12** via the pixel signal line **121**. The vertical scanning circuit **12** includes, for example, a shift register and an address decoder.

[0045] Under the control of the control section **18**, the horizontal scanning circuit **13** scans the pixel signal output (read) by each pixel **110** in the horizontal direction (line direction), and outputs each pixel signal to the capacitance addition circuit **14**. In addition, under the control of the control section **18**, the horizontal scanning circuit **13** controls the connection between each vertical signal line **122** and the capacitance addition circuit **14** in accordance with processing to be executed. For example, when normal image output processing of outputting a normal image is performed, the horizontal scanning circuit **13** connects all the vertical signal lines **122** with the capacitance addition circuit **14**. In addition, when CNN processing is performed, the horizontal scanning circuit **13** controls the connection between each vertical signal line **122** and the capacitance addition circuit **14** on the basis of a convolution coefficient stored in the storage section **17** (details will be described later).

[0046] Under the control of the control section **18**, the capacitance addition circuit **14** outputs the pixel signal output from each pixel **110** to the AD conversion circuit (ADC) **15** in accordance with the processing to be executed. For example, when the normal image output processing is performed, the capacitance addition circuit **14** outputs straight each pixel signal output from the horizontal scanning circuit **13** to the AD conversion circuit **15** (bypass). In addition, when the CNN processing is performed, the capacitance addition circuit **14** adds (for example, weights and adds) each pixel signal output from the horizontal scanning circuit **13** on the basis of the convolution coefficient stored in the storage section **17**, and outputs the result to the AD conversion circuit **15** (details will be described later).

[0047] Here, the horizontal scanning circuit **13** and the capacitance addition circuit **14** function as a convolution circuit **20** that performs convolution processing on individual pixel signals output from the respective pixels **110**. In normal CNN processing, an input image reaches a fully connected layer (FC layer) through a convolution layer and a pooling layer. In the convolution layer, a feature amount is extracted from the input image on the basis of the convolution coefficient (convolution filter). For example, the convolution filter is sequentially applied to the input image to extract the feature amount. The convolution circuit **20** executes processing related to the convolution layer (convolution processing) in an analog manner. The convolution circuit **20** is an analog circuit.

[0048] The AD conversion circuit **15** performs AD conversion processing on each pixel signal output from the capacitance addition circuit **14**, that is, a pixel signal output from each pixel **110**, and outputs each pixel signal, which is a digital signal, to the fully connected processing section **16**. Various AD conversion circuits can be used as the AD conversion circuit **15**.

[0049] The AD conversion circuit **15** includes a pooling circuit **150**. Under the control of the control section **18**, the pooling circuit **150** performs pooling processing on a pixel signal output from each pixel **110** in accordance with the processing to be executed. For example, when the normal image output processing is performed, the pooling circuit **150** outputs straight each pixel signal to the fully connected processing section **16** (bypass). In addition, when the CNN processing is performed, the AD conversion circuit **15** performs the pooling processing on each pixel signal, and outputs each pixel signal that has been subjected to the pooling processing to the fully connected processing section **16**. The pooling circuit **150** performs the pooling processing on each pixel signal that has been subjected to the convolution processing (details will be described later).

[0050] Here, in the normal CNN processing, in the pooling layer, a maximum value or an average value is extracted in a predetermined number (for example, 3×3) of windows. A feature amount is extracted from the input image. In the case, a data amount is reduced. The pooling circuit **150** executes processing related to the pooling layer (convolution

processing) in an analog manner. The pooling circuit **150** and the AD conversion circuit **15** are analog circuits.

[0051] Under the control of the control section **18**, the fully connected processing section **16** outputs each pixel signal, which is a digital signal output from the AD conversion circuit **15**, to the outside of an element (sensor) in accordance with the processing to be executed. For example, when the normal image output processing is performed, the fully connected processing section **16** outputs straight each pixel signal to the outside of the element (bypass). In addition, when the CNN processing is performed, the fully connected processing section **16** performs fully connected processing on each pixel signal, and outputs each pixel signal that has been subjected to the fully connected processing to the outside of the element.

[0052] Here, in the normal CNN processing, outputs from the pooling layer are collected in the fully connected layer. The fully connected processing section **16** logically executes the processing related to the fully connected layer (fully connected processing). The fully connected processing section **16** is, for example, a digital circuit (logic circuit).

[0053] Incidentally, the pixel signal output from the fully connected processing section **16** is input to, for example, an external device such as a signal processing section. For example, the external device generates a pixel signal of a digital signal, that is, pixel data, performs various kinds of processing on the pixel data, and finally generates the image data.

[0054] The storage section **17** stores various kinds of data such as a convolution coefficient (convolution filter). For example, a random access memory (RAM) and a flash memory are used as the storage section **17**. The convolution coefficient read from the storage section **17** is temporarily set in a register **17***a*.

[0055] The control section **18** controls each section such as the vertical scanning circuit **12**, the horizontal scanning circuit **13**, the capacitance addition circuit **14**, the pooling circuit **150**, and the fully connected processing section **16**. For example, the control section **18** controls the horizontal scanning circuit **13**, the capacitance addition circuit **14**, and the like on the basis of a convolution coefficient set in a register **18***a*. For example, a processor such as a central processing unit (CPU) is used as the control section **18**. The CPU includes a read only memory (ROM), a RAM, and the like. The CPU controls operations of each circuit and each section by using the RAM as a work memory in accordance with a program preliminarily stored in the ROM.

[0056] <1-2. Example of Schematic Configuration of Pixel>

[0057] FIG. **2** depicts an example of a schematic configuration of the pixel **110** according to the first embodiment. As depicted in FIG. **2**, the pixel **110** includes a photoelectric conversion element **111**, a trigger transistor **112**, a reset transistor **114**, an amplification transistor **115**, and a selection transistor **116**. For example, a PN-junction photodiode is used as the photoelectric conversion element **111**. In addition, for example, an N-type metal oxide semiconductor (MOS) transistor is used as the trigger transistor **112**, the reset transistor **114**, the amplification transistor **115**, and the selection transistor **116**.

[0058] The pixel signal line **121** is connected to such a pixel **110**. The pixel signal line **121** supplies a reset pulse RST, a transfer pulse TRG, and a selection signal SEL to the pixel **110**. Therefore, the pixel signal line **121** includes a plurality of signal lines.

[0059] The photoelectric conversion element **111** photoelectrically converts incident light into charges (electrons here) in an amount corresponding to an amount of light. A cathode of the photoelectric conversion element **111** is connected to ground. An anode of the photoelectric conversion element **111** is connected to a drain of the trigger transistor **112**.

[0060] A source of the trigger transistor **112** is connected to a floating diffusion layer **113**. The transfer pulse TRG is supplied to a gate of the trigger transistor **112**. The trigger transistor **112** is turned on (closed) when the transfer pulse TRG is in a high state, and is turned off (opened) when the transfer pulse TRG is in a low state. Charges output from the photoelectric conversion element **111** are supplied to the floating diffusion layer **113** with the trigger transistor **112** being in an on state. The floating diffusion layer **113** accumulates the charges supplied from the photoelectric conversion element **111**. The floating diffusion layer **113** generates a voltage in accordance with an amount of the accumulated charges.

[0061] A source of the reset transistor **114** is connected to the floating diffusion layer **113**. A power supply VDD for the pixel **110** is connected to a drain of the reset transistor **114**. The reset pulse RST is supplied to a gate of the reset transistor **114**. The reset transistor **114** is turned on when the reset pulse RST is in a high state, and is turned off when the reset pulse RST is in a low state.

[0062] A gate of the amplification transistor **115** is connected to the floating diffusion layer **113**. The power supply VDD is connected to a drain of the amplification transistor **115**. A drain of the selection transistor **116** is connected to a source of the amplification transistor **115**. A source of the selection transistor **116** is connected to a vertical signal line (VSL) **122**. The selection signal SEL is supplied to a gate of the selection transistor **116**. The selection transistor **116** is turned on when the selection signal SEL is in the high state, and is turned off when the selection signal SEL is in the low state.

[0063] In such configuration, in an initial state, each of the selection signal SEL, the reset pulse RST, and the transfer pulse TRG is in the low state. In addition, the photoelectric conversion element **111** is exposed, and the trigger transistor **112** is turned off by the transfer pulse TRG in the low state. Therefore, charges generated by the exposure are accumulated in the photoelectric conversion element **111**.

[0064] When the selection signal SEL is set to the high state, the selection transistor **116** is turned on. The reset pulse RST is set to the high state, and the charges of the floating diffusion layer **113** are discharged to the power supply VDD. This causes the potential of the floating diffusion layer **113** to be reset to a predetermined potential. After a predetermined time has elapsed since the reset pulse RST was returned to the low state, the transfer pulse TRG is set to the high state. Charges accumulated in the photoelectric conversion element **111** by exposure are supplied to and accumulated in the floating diffusion layer **113**. A voltage corresponding to the charges accumulated in the floating diffusion layer **113** is generated. The voltage is amplified by the amplification transistor **115**, and output to the vertical signal line **122** as a pixel signal via the selection transistor **116**.

[0065] <1-3. CNN Operation Example and Normal Image Output Operation Example of Imaging Element>

[0066] FIG. **3** is a block diagram depicting a flow of CNN operation of the imaging element **10** according to the first embodiment. In the CNN operation, as depicted in FIG. **3**, the imaging section **11** acquires each pixel signal (analog signal). The horizontal scanning circuit **13** and the capacitance addition circuit **14** (convolution circuit **20**) perform the convolution processing on each pixel signal on the basis of the convolution coefficient (convolution filter). The pooling circuit **150** in the AD conversion circuit **15** executes the pooling processing on each pixel signal that has been subjected to the convolution processing. The fully connected processing section **16** executes the fully connected processing on each pixel signal that has been subjected to the pooling processing. Each pixel signal (pixel signal and classification label) that has been subjected to the CNN processing is output. The imaging element **10** can complete the CNN processing in the sensor. Incidentally, there is a plurality of types of convolution filters, and a feature amount to be extracted changes depending on a convolution filter to be applied.

[0067] Here, FIG. **4** is a block diagram depicting a flow of CNN learning related to the CNN operation in FIG. **3**. In order to achieve the CNN operation in FIG. **3**, as depicted in FIG. **4**, an outside-sensor CNN **51**, which is a system outside the sensor, preliminarily learns a CNN, and the storage section **17** preliminarily stores the convolution coefficient and a fully connected processing coefficient. The outside-sensor CNN **51** can learn the CNN (convolution layer to pooling layer to fully connected layer) on the basis of learning data and a label **52**, and acquire the convolution coefficient and the fully connected processing coefficient. The convolution circuit **20** performs convolution processing on the basis of the convolution coefficient stored in the storage section **17**. In addition, the fully connected processing section **16** performs the fully connected processing on the basis of the fully connected processing coefficient stored in the storage section **17**. In the examples of FIGS. **3** and **4**, the convolution processing, the pooling processing, and the fully connected processing are executed in the sensor. Incidentally, the outside-sensor CNN **51** may include both or any one of hardware and software.

[0068] FIG. **5** is a block diagram depicting a flow of a normal image output operation of the imaging element **10** according to the first embodiment. In the normal image output operation, as depicted in FIG. **5**, the imaging section **11**, the horizontal scanning circuit **13**, and the AD conversion circuit **15** (excluding pooling circuit **150**) operate to output a normal image (to output all pixels). All pieces of the CNN-based processing are bypassed. The capacitance addition circuit **14**, the pooling circuit **150**, and the fully connected processing section **16** do not operate. This causes a normal image that has not been subjected to the CNN processing to be output.

[0069] Incidentally, although, in the examples of FIGS. **3** and **4**, the fully connected processing section **16** is provided in the sensor (imaging element **10**), this is not a limitation. FIG. **6** is a block diagram depicting a flow of a variation of the CNN operation of the imaging element **10** according to the first embodiment. As depicted in FIG. **6**, instead of the fully connected processing section **16**, an outside-sensor CNN **50** that performs the fully connected processing may be provided outside the sensor. That is, the fully connected processing may be performed outside the sensor.

[0070] Here, FIG. **7** is a block diagram depicting a flow of the CNN learning related to the CNN operation in FIG. **6**. In order to achieve the CNN operation in FIG. **6**, as depicted in FIG. **7**, an outside-sensor CNN **51**, which is a system outside the sensor, preliminarily learns a CNN, and the storage section **17** preliminarily stores the convolution coefficient (first layer). Then, the outside-sensor CNN **50** executes the CNN processing in the first and subsequent layers. In this case, convolution processing in the first layer is executed in the sensor, and subsequent pieces of processing is executed outside the sensor.

[0071] Incidentally, the CNN operation and the normal image output operation may be switched by a user, for example. The user operates an input section (for example, switch and button) to cause the control section **18** to switch the CNN operation and the normal image output operation. The input section is electrically connected to the control section **18**. The input section receives an input operation from the user, and transmits an input signal (switching instruction signal) to the control section **18** in response to the input operation. The control section **18** switches the CNN operation and the normal image output operation in response to the input signal.

[0072] For example, the control section **18** switches an operation mode from the CNN operation to the normal image output operation in response to an input signal for restricting the CNN operation, and restricts (prohibits) the convolution processing and the pooling processing. In contrast, the control section **18** switches the operation mode from the normal image output operation to the CNN operation in response to an input signal for permitting the CNN operation, and permits the convolution processing and the pooling processing. This allows the user to be given a selection right to select whether or not to execute the CNN operation, and can improve convenience for the user.

[0073] <1-4. Example of Schematic Configuration of Convolution Circuit>

[0074] FIG. **8** depicts an example of a schematic configuration of the convolution circuit **20** based on the convolution filter according to the first embodiment. As depicted in FIG. **8**, the horizontal scanning circuit **13** includes a multiplexer **13***a*. Each vertical signal line **122** of each column is connected to the multiplexer **13***a*. The multiplexer **13***a* selects, by switching (VSL connection/disconnection switch), a column to which each vertical signal line **122** is to be connected. The control section **18** controls the multiplexer **13***a*.

[0075] The capacitance addition circuit **14** includes a plurality of multiplexers **14***a*, a plurality of capacitors **14***b*, and a plurality of switches **14***c*. Each multiplexer **14***a* is connected to the multiplexer **13***a* of the horizontal scanning circuit **13** via a predetermined number (three in FIG. **8**) of vertical signal lines **122**. Each capacitor **14***b* is connected to a multiplexer **14***a* at one end. Each capacitor **14***b* is connected to one signal line **122***a* at the other end for each multiplexer **14***a*. Each multiplexer **14***a* changes the connection of the capacitor **14***b*, and sets an addition ratio (addition capacitance setting). The control section **18** controls these multiplexers **14***a*.

[0076] A signal line **122***a* is provided for each multiplexer **14***a*. These signal lines **122***a* are connected to adjacent signal lines **122***a* via connection lines **122***b*. Each switch **14***c* is individually provided in each signal line **122***a*, and is

individually provided in each connection line **122***b*. The control section **18** controls on/off of these switches **14***c*.

[0077] FIG. **9** depicts an example of operation of the convolution circuit **20** at the time of performing the normal image output processing according to the first embodiment. In the normal image output processing, as depicted in FIG. **9**, the horizontal scanning circuit **13** connects all the vertical signal lines **122** to the capacitance addition circuit **14** without disconnection. In addition, the capacitance addition circuit **14** connects all the vertical signal lines **122** to the signal lines **122***a* via the multiplexers **14***a* and the capacitors **14***b*. In the case, switches **14***c* connect all the signal lines **122***a* without connecting the connection lines **122***b*.

[0078] FIG. **10** depicts an example of operation of the convolution circuit **20** at the time of performing the convolution processing according to the first embodiment. In the convolution processing, as depicted in FIG. **10**, the horizontal scanning circuit **13** controls the connection between each vertical signal line **122** and the capacitance addition circuit **14** with the multiplexer **13***a* on the basis of the convolution filter. In addition, the capacitance addition circuit **14** controls the connection between each vertical signal line **122** and each signal line **122***a* with each multiplexer **14***a* and each capacitor **14***b* on the basis of the convolution filter. In the case, adjacent three signal lines **122***a* are defined as one set. Each switch **14***c* connects (laterally connects) the connection lines **122***b* for each set, and connects a central one signal line **122***a*. Incidentally, similar connection processing is performed in each pixel **110** other than each pixel **110** in FIG. **10**.

[0079] In the example of FIG. **10**, in a 3×3 convolution filter, "first row: 2, 0, and 1, second row: 0, 1, and 0, and third row: 1, 0, and 1" is established. The horizontal scanning circuit **13** and the capacitance addition circuit **14** achieve the convolution filter (number of matrices and each numerical value). The capacitance addition circuit **14** includes each multiplexer **14***a* and each capacitor **14***b* for setting the convolution coefficient. For example, in the 3×3 convolution filter in FIG. **10**, two is provided in the first row and the first column. A pixel (upper left pixel) **110** in the first row and the first column in FIG. **10** is connected to two capacitors **14***b* via the vertical signal line **122**. Similarly, zero is provided in the first row and the second column. The pixel **110** in the first row and the second column in FIG. **10** is not connected to the capacitor **14***b*. One is provided in the first row and the third column. The pixel **110** in the first row and the third column in FIG. **10** is connected to one capacitor **14***b*. In the second and third rows, connection/disconnection between the pixel **110** and the capacitor **14***b* is similarly performed.

[0080] Here, like the convolution filter depicted in FIG. **10**, a convolution filter including 0 (0 filter) can be achieved by the horizontal scanning circuit **13** and the capacitance addition circuit **14**. This allows achievement of the 0 filter with simple configuration. Incidentally, a larger number of capacitors **14***b* of the capacitance addition circuit **14** increase the degree of freedom of the convolution coefficient (convolution filter).

[0081] <1-5. Example of Schematic Configuration of AD Conversion Circuit Including Pooling Circuit>

[0082] FIG. **11** depicts an example of a schematic configuration of the AD conversion circuit **15** including the pooling circuit **150** according to the first embodiment. As depicted in FIG. **11**, the AD conversion circuit **15** includes a plurality of comparators **15***a*, a multiplexer **15***b*, and a plurality of counters **15***c* (CN). For example, an AD conversion circuit using a voltage controlled oscillator (VCO) is used as the AD conversion circuit **15**. Each comparator **15***a* is provided in each signal line **122***a*. The multiplexer **15***b* is connected to each signal line **122***a*. Each counter **15***c* is connected to a subsequent stage (downstream side of signal flow) of the multiplexer **15***b*.

[0083] The pooling circuit **150** includes an OR circuit **150***a*. The OR circuit **150***a* is provided between the multiplexer **15***b* and the counter **15***c*. The pooling circuit **150** performs maximum value pooling processing (max pooling processing) on pixel signals output from the comparators **15***a* by using the OR circuit **150***a*. Note, however, that the pooling processing is not limited to the maximum value pooling processing. For example, average value pooling processing may be used.

[0084] When the normal image output processing is performed, the multiplexer **15***b* sends straight the pixel signal output from the comparators **15***a* to the counter **15***c* (CN). In addition, when the CNN processing is performed, the multiplexer **15***b* sends the pixel signals output from the comparators **15***a* to the OR circuit **150***a*. The OR circuit **150***a* performs the maximum value pooling processing on each pixel signal, and sends each image signal that has been subjected to the pooling processing to the counters **15***c* (CN). Each pixel signal output from the counter **15***c* is a digital signal. The control section **18** controls the multiplexer **15***b*.

[0085] <1-6. Actions/Effects>

[0086] As described above, according to the first embodiment, an operation related to the convolution processing and the pooling processing can be processed in an analog manner by incorporating the convolution processing and the pooling processing of the CNN processing in the imaging element **10**, and a processing time can be speeded up. For example, the scales of a memory, a logic circuit, and the like can be reduced by achieving the convolution processing and the pooling processing in an analog circuit. In addition, a load of logic processing can be reduced, and a lead time can be shortened. Thus, an image recognition system can be simplified, and a lead time can be shortened.

2. Second Embodiment

[0087] Next, a convolution circuit **20**A according to a second embodiment will be described with reference to FIG. **12**. FIG. **12** depicts an example of a schematic configuration of the convolution circuit **20**A based on the convolution filter according to the second embodiment. Differences from the first embodiment will be mainly described below, and other descriptions will be omitted.

[0088] As depicted in FIG. **12**, the convolution circuit **20**A according to the second embodiment includes a capacitance addition circuit (addition circuit) **14**A partially different from that of the first embodiment. The capacitance addition circuit **14**A includes a plurality of amplifiers (column amplifiers) **14***d* for setting a convolution coefficient in addition to the plurality of capacitors **14***b* and the plurality of switches **14***c* according to the first embodiment. These amplifiers **14***d* are provided for each vertical signal line **122**. A gain of an amplifier **14***d* is changed to achieve a convolution filter. For example, when a convolution filter has a numerical value of two, the gain of the amplifier **14***d* is doubled. Such an amplifier **14***d* is used to achieve a convolution filter. Inci-

dentally, although the capacitance ratio of the capacitor **14***b* is fixed, element configuration can be simplified as compared with that in a case of addition by the capacitance ratio.

[0089] As described above, according to the second embodiment, the configuration of the imaging element **10** can be simplified by using the plurality of amplifiers **14***d* as a part of the capacitance addition circuit **14**A of the convolution circuit **20**A, so that an image recognition system can be simplified. Incidentally, according to the second embodiment, the same effects as those of the first embodiment can be obtained.

3. Third Embodiment

[0090] Next, convolution processing (including slide processing) according to a third embodiment will be described with reference to FIGS. **13** to **15**. Differences from the first embodiment will be mainly described below, and other descriptions will be omitted.

[0091] FIG. **13** depicts slide of a convolution filter according to the third embodiment. As depicted in FIG. **13**, in the third embodiment, the convolution filter is horizontally shifted in a predetermined movement amount. In the example of FIG. **13**, the predetermined movement amount (stride) is one, and the convolution filter is slid from A to B with movement amount=1. Incidentally, the slide means shifting the convolution filter, and the stride is a unit indicating a movement amount in which the convolution filter is shifted.

[0092] FIG. **14** is a first diagram depicting an example of operation of the convolution circuit **20** at the time of performing the convolution processing according to the third embodiment. FIG. **15** is a second diagram depicting an example of the operation of the convolution circuit **20** at the time of performing the convolution processing according to the third embodiment. As depicted in FIGS. **14** and **15**, the horizontal scanning circuit **13** and the capacitance addition circuit **14** according to the third embodiment have configurations similar to those of the first embodiment. In addition, the horizontal scanning circuit **13** and the capacitance addition circuit **14** can execute the convolution processing including the slide processing.

[0093] As depicted in FIG. **14**, in the convolution processing, the horizontal scanning circuit **13** controls the connection between each vertical signal line **122** and the capacitance addition circuit **14** on the basis of the convolution filter. In addition, the capacitance addition circuit **14** controls the connection between each vertical signal line **122** and each signal line **122***a* with each multiplexer **14***a* and each capacitor **14***b* on the basis of the convolution filter. In the case, adjacent three signal lines **122***a* are defined as one set. Each switch **14***c* connects (laterally connects) the connection lines **122***b* for each set, and connects a central one signal line **122***a*. In the example of FIG. **14**, in a 3×3 convolution filter, "first row: 2, 0, and 1, second row: 0, 1, and 0, and third row: 1, 0, and 1" is established. The horizontal scanning circuit **13** and the capacitance addition circuit **14** achieve the convolution filter (number of matrices and each numerical value).

[0094] As depicted in FIG. **15**, when the convolution filter is shifted with movement amount=1 (see FIG. **13**), the horizontal scanning circuit **13** controls the connection between each vertical signal line **122** and the capacitance addition circuit **14** on the basis of the convolution filter and the movement amount. In addition, the capacitance addition circuit **14** controls the connection between each vertical signal line **122** and each signal line **122***a* with each multiplexer **14***a* and each capacitor **14***b* on the basis of the convolution filter and the movement amount. In the case, a set in which three signal lines **122***a* are combined is shifted by one of the signal lines **122***a*. Each switch **14***c* connects (laterally connects) the connection lines **122***b* for each set, and connects a central one signal line **122***a*. This causes the convolution filter to slide in the horizontal direction (row direction). Such slide is repeated in the imaging section **11**.

[0095] As described above, according to the third embodiment, the convolution processing including the slide processing can be performed, so that variations of the convolution processing can be increased, and convenience can be improved for a user. Incidentally, according to the third embodiment, the same effects as those of the first embodiment can be obtained.

[0096] Although, in the above-described third embodiment, a form, in which convolution is performed by not simultaneously but separately performing AD conversion when a convolution filter A and a convolution filter B are simultaneously subjected to AD conversion, is adopted since a column circuit needs to be added, this is not a limitation. For example, a column circuit such as a vertical column may be added to simultaneously perform the AD conversion in the convolution filter A and the convolution filter B.

[0097] In addition, although, in the above-described third embodiment, the convolution filter is shifted in the horizontal direction (row direction), this is not a limitation. For example, the convolution filter may be shifted in the vertical direction (column direction). Also in this case, the convolution filter can be vertically shifted by adding a column circuit such as a vertical column.

4. Other Embodiments

[0098] Incidentally, although, in each of the above-described embodiments, one convolution layer and one pooling layer are provided, and one piece of convolution processing and one piece of pooling processing are performed, this is not a limitation. For example, multiple convolution layers and multiple pooling layers may be provided, and a plurality of numbers of times of convolution processing and a plurality of numbers of times of pooling processing may be repeatedly performed.

[0099] In addition, the imaging element **10** according to each of the above-described embodiments may be formed on one chip. Alternatively, the imaging element **10** may be divided and formed on a plurality of chips. Further, the imaging element **10** may be formed as a laminated structure obtained by bonding these chips. For example, the imaging element **10** may have a structure in which a light receiving chip and a circuit chip are vertically laminated (two-layer laminated structure). The light receiving chip includes the imaging section **11**. The circuit chip includes the storage section **17** and the control section **18**.

5. Application Example

[0100] Next, an application example of the imaging element **10** according to each embodiment will be described. FIG. **16** depicts a usage example in which the imaging element **10** according to each embodiment is used.

[0101] For example, as described below, the above-described imaging element **10** can be used in various cases in

which light such as visible light, infrared light, ultraviolet light, and X-rays are sensed. For example, as depicted in FIG. **16**, the imaging element **10** is used for a "device that captures an image provided for appreciation, such as a digital camera and a portable device with a camera function", a "device provided for traffic, such as a vehicle-mounted sensor, a monitoring camera, and a distance measurement sensor, the vehicle-mounted sensor photographing, for example, the front, back, surroundings, and inside of an automobile for safe driving such as automatic stop, recognition of the state of a driver, and the like, the monitoring camera monitoring a traveling vehicle and a road, the distance measurement sensor measuring, for example, a distance between vehicles", a "device provided for a home electrical appliance, such as a TV, a refrigerator, and an air conditioner, for photographing a gesture of a user and operating a device according to the gesture", a "device provided for medical care or health care, such as an endoscope and a device that performs angiography by receiving infrared light", a "device provided for security, such as a monitoring camera for security and a camera for person authentication", a "device provided for beauty care, such as a skin measuring instrument that photographs skin and a microscope that photographs a scalp", a "device provided for sports, such as an action camera and a wearable camera for sports", a "device provided for agriculture, such as a camera for monitoring the states of fields and crops", and the like.

[0102] For example, the above-described imaging element **10** can be applied to various electronic devices, such as an imaging device including a digital still camera and a digital video camera, a mobile phone having an imaging function, and other devices having an imaging function.

[0103] FIG. **17** is a block diagram depicting a configuration example of an imaging device **300** as an electronic device to which the technology according to the present disclosure can be applied. The imaging device **300** includes an optical system **301**, a shutter device **302**, a solid-state imaging device **303**, a control circuit (control section) **304**, a signal processing circuit **305**, a monitor **306**, and a memory **307**. The imaging device **300** can capture a still image and a moving image.

[0104] The optical system **301** includes one or a plurality of lenses. The optical system **301** guides light (incident light) from a subject to the solid-state imaging device **303**, and forms an image of the light on a light receiving surface of the solid-state imaging device **303**.

[0105] The shutter device **302** is disposed between the optical system **301** and the solid-state imaging device **303**. The shutter device **302** controls a light application period and a light shielding period for the solid-state imaging device **303** under the control of the control circuit **304**.

[0106] The solid-state imaging device **303** includes, for example, a package including the above-described imaging element **10**. The solid-state imaging device **303** accumulates signal charges for a certain period in accordance with light whose image is formed on the light receiving surface via the optical system **301** and the shutter device **302**. The signal charges accumulated in the solid-state imaging device **303** are transferred in accordance with a drive signal (timing signal) supplied from the control circuit **304**.

[0107] The control circuit **304** outputs a drive signal for controlling transfer operation of the solid-state imaging device **303** and shutter operation of the shutter device **302** to drive the solid-state imaging device **303** and the shutter device **302**.

[0108] The signal processing circuit **305** performs various types of signal processing on the signal charges output from the solid-state imaging device **303**. An image (image data) obtained by signal processing performed by the signal processing circuit **305** is supplied to be displayed on the monitor **306**, or supplied to be stored (recorded) in the memory **307**.

[0109] Also in the imaging device **300** configured as described above, an image recognition system can be simplified and a lead time can be shortened by applying the above-described imaging element **10** as the solid-state imaging device **303**.

6. Applications

[0110] In addition, the technology according to the present disclosure can be applied to various products. For example, the technology according to the present disclosure may be achieved as a device such as an electronic device mounted in any type of mobile body, such as an automobile, an electric vehicle, a hybrid electric vehicle, a motorcycle, a bicycle, a personal mobility, an airplane, a drone, a ship, a robot, a construction machine, and an agricultural machine (tractor). In addition, for example, the technology according to the present disclosure may be applied to an endoscopic surgical system, a microscopic surgical system, and the like.

[0111] FIG. **18** is a block diagram depicting an example of schematic configuration of a vehicle control system **7000** as an example of a mobile body control system to which the technology according to an embodiment of the present disclosure can be applied. The vehicle control system **7000** includes a plurality of electronic control units connected to each other via a communication network **7010**. In the example in FIG. **18**, the vehicle control system **7000** includes a driving system control unit **7100**, a body system control unit **7200**, a battery control unit **7300**, an outside-vehicle information detecting unit **7400**, an in-vehicle information detecting unit **7500**, and an integrated control unit **7600**. The communication network **7010** connecting the plurality of control units to each other may, for example, be a vehicle-mounted communication network compliant with an arbitrary standard such as controller area network (CAN), local interconnect network (LIN), local area network (LAN), FlexRay (registered trademark), or the like.

[0112] Each of the control units includes: a microcomputer that performs arithmetic processing according to various kinds of programs; a storage section that stores the programs executed by the microcomputer, parameters used for various kinds of operations, or the like; and a driving circuit that drives various kinds of control target devices. Each of the control units further includes: a network interface (I/F) for performing communication with other control units via the communication network **7010**; and a communication I/F for performing communication with a device, a sensor, or the like within and without the vehicle by wire communication or radio communication. A functional configuration of the integrated control unit **7600** illustrated in FIG. **18** includes a microcomputer **7610**, a general-purpose communication I/F **7620**, a dedicated communication I/F **7630**, a positioning section **7640**, a beacon receiving section **7650**, an in-vehicle device I/F **7660**, a sound/image output section **7670**, a vehicle-mounted network I/F **7680**, and a storage section

7690. The other control units similarly include a microcomputer, a communication I/F, a storage section, and the like.

[0113] The driving system control unit **7100** controls the operation of devices related to the driving system of the vehicle in accordance with various kinds of programs. For example, the driving system control unit **7100** functions as a control device for a driving force generating device for generating the driving force of the vehicle, such as an internal combustion engine, a driving motor, or the like, a driving force transmitting mechanism for transmitting the driving force to wheels, a steering mechanism for adjusting the steering angle of the vehicle, a braking device for generating the braking force of the vehicle, and the like. The driving system control unit **7100** may have a function as a control device of an antilock brake system (ABS), electronic stability control (ESC), or the like.

[0114] The driving system control unit **7100** is connected with a vehicle state detecting section **7110**. The vehicle state detecting section **7110**, for example, includes at least one of a gyro sensor that detects the angular velocity of axial rotational movement of a vehicle body, an acceleration sensor that detects the acceleration of the vehicle, and sensors for detecting an amount of operation of an accelerator pedal, an amount of operation of a brake pedal, the steering angle of a steering wheel, an engine speed or the rotational speed of wheels, and the like. The driving system control unit **7100** performs arithmetic processing using a signal input from the vehicle state detecting section **7110**, and controls the internal combustion engine, the driving motor, an electric power steering device, the brake device, and the like.

[0115] The body system control unit **7200** controls the operation of various kinds of devices provided to the vehicle body in accordance with various kinds of programs. For example, the body system control unit **7200** functions as a control device

1. An imaging element comprising:
an imaging section in which a plurality of pixels individually including a photoelectric conversion element is arranged in a matrix;
a convolution circuit that performs convolution processing on a plurality of pixel signals, which are analog signals each output from the plurality of pixels, on a basis of a convolution coefficient; and
a pooling circuit that performs pooling processing on the plurality of pixel signals that has been subjected to the convolution processing.

2. The imaging element according to claim **1**, further comprising
a fully integrated processing section that performs fully integrated processing on the plurality of pixel signals that has been subjected to the pooling processing.

3. The imaging element according to claim **1**,
wherein the convolution circuit includes:
a horizontal scanning circuit that selects a plurality of pixels from which the pixel signals are output from the plurality of pixels on a basis of the convolution coefficient; and
an addition circuit that adds the plurality of pixel signals each output from the plurality of pixels that has been selected, on a basis of the convolution coefficient.

4. The imaging element according to claim **3**,
wherein the addition circuit includes
a multiplexer for setting the convolution coefficient and a plurality of capacitors.

5. The imaging element according to claim **3**,
wherein the addition circuit includes
a plurality of amplifiers for setting the convolution coefficient.

6. The imaging element according to claim **1**, further comprising
a storage section that stores the convolution coefficient.

7. The imaging element according to claim **1**, further comprising
a control section that controls the convolution circuit and the pooling circuit on a basis of the convolution coefficient.

8. The imaging element according to claim **7**,
wherein the control section restricts or permits the convolution processing and the pooling processing in response to an input signal input to the control section.

9. The imaging element according to claim **1**,
wherein the convolution coefficient is a convolution filter, and
the convolution circuit shifts the convolution filter in a predetermined movement amount, and performs the convolution processing.

10. The imaging element according to claim **1**,
wherein the convolution coefficient is a convolution filter including zero.

11. An imaging device comprising:
an imaging element; and
an optical system that forms an image of light on a light receiving surface of the imaging element,
wherein the imaging element includes:
an imaging section in which a plurality of pixels individually including a photoelectric conversion element is arranged in a matrix;
a convolution circuit that performs convolution processing on a plurality of pixel signals, which are analog signals each output from the plurality of pixels, on a basis of a convolution coefficient; and
a pooling circuit that performs pooling processing on the plurality of pixel signals that has been subjected to the convolution processing.

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