(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 4 270 496 A1**

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(43) Date of publication:
01.11.2023 Bulletin 2023/44

(21) Application number: **21943828.0**

(22) Date of filing: **22.10.2021**

(51) International Patent Classification (IPC):
H01L 33/06 *(2010.01)* ***H01L 33/14*** *(2010.01)*
H01L 33/38 *(2010.01)*

(52) Cooperative Patent Classification (CPC):
H01L 33/06; H01L 33/14; H01L 33/38

(86) International application number:
PCT/CN2021/125522

(87) International publication number:
WO 2022/252476 (08.12.2022 Gazette 2022/49)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(30) Priority: **31.05.2021 CN 202110603573**

(71) Applicant: **BOE Technology Group Co., Ltd.**
Beijing 100015 (CN)

(72) Inventors:
- **QIN, Bin**
  Beijing 100176 (CN)
- **PENG, Kuanjun**
  Beijing 100176 (CN)
- **LIU, Weixing**
  Beijing 100176 (CN)
- **ZHANG, Fangzhen**
  Beijing 100176 (CN)
- **DONG, Xue**
  Beijing 100176 (CN)
- **PENG, Jintao**
  Beijing 100176 (CN)
- **TENG, Wanpeng**
  Beijing 100176 (CN)
- **LI, Xiaolong**
  Beijing 100176 (CN)
- **SUN, Shuang**
  Beijing 100176 (CN)
- **CHEN, Wanzhi**
  Beijing 100176 (CN)
- **YUAN, Guangcai**
  Beijing 100176 (CN)
- **JIA, Qian**
  Beijing 100176 (CN)

(74) Representative: **Cohausz & Florack**
Patent- & Rechtsanwälte
Partnerschaftsgesellschaft mbB
Bleichstraße 14
40211 Düsseldorf (DE)

(54) LIGHT-EMITTING DEVICE, LIGHT-EMITTING SUBSTRATE, AND METHOD FOR MANUFACTURING LIGHT-EMITTING DEVICE

(57) A light-emitting device, a light-emitting substrate, and a method for manufacturing the light-emitting device. The light-emitting device comprises at least one light-emitting structure. The light-emitting structure comprises: a first semiconductor layer (21); a light-emitting layer (3); a second semiconductor layer (22), doping ions of the second semiconductor layer (22) and a first semiconductor layer (21) being oppositely charged; a barrier structure (4) provided with an opening for exposing the second semiconductor layer (22), the orthographic projection of the opening on the base substrate (1) being located in the orthographic projection of the light-emitting layer (3) on the base substrate (1), and the area of the opening being smaller than that of the light-emitting layer (3); and a landing electrode (6) located on the side of the barrier structure (4) facing away from the second semiconductor layer (22), the landing electrode (6) being in contact with the second semiconductor layer (22) by means of the opening.

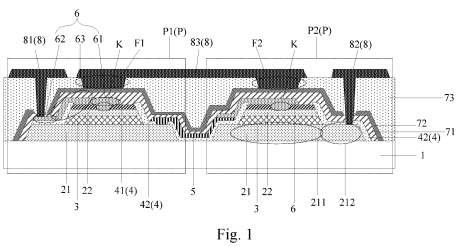

Fig. 1

EP 4 270 496 A1

Description

Cross Reference to Related Applications

[0001] This application claims the priority of Chinese patent application No. 202110603573.3, filed to China Patent Office on May 31, 2021, and entitled "LIGHT-EMITTING DEVICE, LIGHT-EMITTING SUBSTRATE, AND METHOD FOR MANUFACTURING LIGHT-EMITTING DEVICE", the entire contents of which are incorporated herein by reference.

Field

[0002] The present disclosure relates to the technical field of semiconductors, in particular to a light-emitting device, a light-emitting substrate, and a method for manufacturing the light-emitting device.

Background

[0003] Light-emitting diode (LED) display refers to a technology that traditional LEDs are arrayed and miniaturized, and then subjected to addressing and mass transfer to a circuit substrate to form ultra-small pitch LEDs, and the length of millimeter-level LEDs is further miniaturized to micron-level, so as to achieve ultra-high pixels and ultra-high resolution, which can adapt to screens of various sizes in theory. Generally, an LED growth backplate includes sapphire, a GaN layer on a Si chip, SiC, and so on. Compared with organic light-emitting display and liquid crystal display, the LED display has the advantages of higher luminous efficiency, better display effects, and lower power, and thus becomes a research hotspot in the display industry.

Summary

[0004] The present disclosure provides a light-emitting device, a light-emitting substrate, and a method for manufacturing the light-emitting device. The light-emitting device includes a base substrate, and at least one light-emitting structure located on one side of the base substrate; wherein the light-emitting structure includes: a first semiconductor layer; a light-emitting layer located on the side, facing away from the base substrate, of the first semiconductor layer; a second semiconductor layer located on the side, facing away from the first semiconductor layer, of the light-emitting layer, wherein doping ions of the second semiconductor layer and the first semiconductor layer are oppositely charged; a barrier structure located on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein the barrier structure is provided with an opening for exposing the second semiconductor layer, an orthographic projection of the opening on the base substrate is located in an orthographic projection of the light-emitting layer on the base substrate, and an area of the opening is smaller than that of the light-emitting layer; and a landing electrode located on the side, facing away from the second semiconductor layer, of the barrier structure, wherein the landing electrode is in contact with the second semiconductor layer through the opening.

[0005] In one possible embodiment, an orthographic projection of the second semiconductor layer on the base substrate and the orthographic projection of the light-emitting layer on the base substrate substantially coincide with each other; the barrier structure includes a third semiconductor layer and a passivation layer located on the side, facing away from the second semiconductor layer, of the third semiconductor layer, wherein doping ions of the third semiconductor layer and the second semiconductor layer are oppositely charged; and the third semiconductor layer is provided with a first sub-opening for exposing a part of the second semiconductor layer, and the passivation layer is provided with a second sub-opening for exposing the third semiconductor layer and the first sub-opening; and the landing electrode is in contact with the second semiconductor layer through the first sub-opening of the third semiconductor layer.

[0006] In one possible embodiment, an orthographic projection of the second semiconductor layer on the base substrate and the orthographic projection of the light-emitting layer on the base substrate substantially coincide with each other; the barrier structure includes a passivation layer; wherein the passivation layer is provided with a third sub-opening for exposing a part of the second semiconductor layer; and the landing electrode is in contact with the second semiconductor layer through the third sub-opening of the passivation layer.

[0007] In one possible embodiment, a thickness of the second semiconductor layer is 2-4% of a thickness of the first semiconductor layer.

[0008] In one possible embodiment, an orthographic projection of the second semiconductor layer on the base substrate is located in the orthographic projection of the light-emitting layer on the base substrate, and an area of the orthographic projection of the second semiconductor layer on the base substrate is smaller than that of the orthographic projection of the light-emitting layer on the base substrate; the barrier structure includes a passivation layer; wherein the passivation layer is provided with a fourth sub-opening for exposing at least part of the second semiconductor layer; and the landing electrode is in contact with the second semiconductor layer through the fourth sub-opening of the passivation layer.

[0009] In one possible embodiment, an orthographic projection of the fourth sub-opening on the base substrate and the orthographic projection of the second semiconductor layer on the base substrate substantially coincide with each other.

[0010] In one possible embodiment, an area of the second semiconductor layer is one fifth to four fifths of an area of the light-emitting layer.

[0011] In one possible embodiment, the light-emitting device includes at least two of the light-emitting struc-

tures connected in series with each other; and the light-emitting device further includes an encapsulation layer located on the side, facing away from the barrier structure, of the landing electrode, and the at least two light-emitting structures connected in series with each other are integrally encapsulated by the encapsulation layer.

[0012] In one possible embodiment, the light-emitting device includes a first light-emitting structure and a second light-emitting structure which are connected in series with each other; and the light-emitting device further includes a bridge electrode located between the barrier structure and the landing electrode; the first semiconductor layer of the first light-emitting structure and the landing electrode of the second light-emitting structure are electrically connected by the bridge electrode.

[0013] In one possible embodiment, the barrier structure at least includes a passivation layer; and one end of the bridge electrode is electrically connected with the first semiconductor layer of the first light-emitting structure through a via hole penetrating the passivation layer, and the other end of the bridge electrode is in direct contact and electrically connected with the landing electrode of the second light-emitting structure.

[0014] In one possible embodiment, the light-emitting device further includes a connection pad layer located on the side, facing away from the second semiconductor layer, of the encapsulation layer, wherein the connection pad layer includes a first connection electrode pad electrically connected with the landing electrode of the first light-emitting structure, and a second connection electrode pad electrically connected with the first semiconductor layer of the second light-emitting structure.

[0015] In one possible embodiment, the landing electrode of the first light-emitting structure includes a first contact portion in contact with the second semiconductor layer, a first landing portion, and a first connection portion connecting the first contact portion and the first landing portion; wherein an orthographic projection of the first landing portion on the base substrate does not overlap with the orthographic projection of the light-emitting layer on the base substrate; the first connection electrode pad is electrically connected with the first landing portion through a via hole; and the first semiconductor layer of the second light-emitting structure is provided with an overlapping portion which overlaps with the light-emitting layer, and an extension portion extending from the overlapping portion, and the second connection electrode pad is electrically connected with the extension portion through a via hole.

[0016] In one possible embodiment, the light-emitting device further includes a heat dissipation layer located between the encapsulation layer and the landing electrode; wherein an orthographic projection of the heat dissipation layer on the base substrate at least covers an orthographic projection of the opening of the first light-emitting structure on the base substrate, and an orthographic projection of the opening of the second light-emitting structure on the base substrate.

[0017] In one possible embodiment, the connection pad layer further includes a heat dissipation pad which is in a conducting relationship with the heat dissipation layer, and an orthographic projection of the heat dissipation pad on the base substrate at least covers the orthographic projection of the opening of the first light-emitting structure on the base substrate, and covers the orthographic projection of the opening of the second light-emitting structure on the base substrate.

[0018] In one possible embodiment, the encapsulation layer is provided with a first encapsulation opening and a second encapsulation opening; wherein an orthographic projection of the first encapsulation opening on the base substrate covers the orthographic projection of the opening of the first light-emitting structure on the base substrate, and an orthographic projection of the second encapsulation opening on the base substrate covers the orthographic projection of the opening of the second light-emitting structure on the base substrate; and the heat dissipation pad is in contact with the thermal dissipation layer through the first encapsulation opening and the second encapsulation opening.

[0019] In one possible embodiment, the heat dissipation pad includes a first heat dissipation pad covering the opening of the first light-emitting structure, and a second heat dissipation pad covering the opening of the second light-emitting structure, wherein the first heat dissipation pad and the second heat dissipation pad are integrally connected; and a center of the first connection electrode pad, a center of the second connection electrode pad, a center of the first heat dissipation pad, and a center of the second heat dissipation pad enclose a rectangle; and the center of the first connection electrode pad and the center of the second connection electrode pad are respectively located at two vertices on one diagonal line of the rectangle, and the center of the first heat dissipation pad and the center of the second heat dissipation pad are respectively located at two vertices on the other diagonal line of the rectangle.

[0020] In one possible embodiment, a reflective layer is also arranged between the heat dissipation layer and the landing electrode.

[0021] An embodiment of the present disclosure also provides a light-emitting substrate, including a driving backplane and the light-emitting devices provided by the embodiment of the present disclosure disposed on one side of the driving backplane.

[0022] In one possible embodiment, the driving backplane includes driving structures in one-to-one correspondence with the light-emitting devices, wherein each driving structure includes a first electrode, a second electrode, and a heat dissipation electrode; wherein each first electrode is in bound connection with the corresponding first connection electrode pad, each second electrode is in bound connection with the corresponding second connection electrode pad, and each heat dissipation electrode is in bound connection with the corresponding heat dissipation pad.

[0023] In one possible embodiment, the driving backplate further includes heat dissipation connection electrodes, wherein the heat dissipation electrodes of the different driving structures are electrically connected to each other through the heat dissipation connection electrodes.

[0024] An embodiment of the present disclosure also provides a method for manufacturing a light-emitting device, including: forming a first semiconductor layer on one side of a base substrate;

forming a light-emitting layer on the side, facing away from the base substrate, of the first semiconductor layer; forming a second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer; forming a barrier structure provided with an opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein an orthographic projection of the opening on the base substrate is located in an orthographic projection of the light-emitting layer on the base substrate, and an area of the opening is smaller than that of the light-emitting layer; and forming a landing electrode on the side, facing away from the second semiconductor layer, of the barrier structure such that the landing electrode is in contact with the second semiconductor layer through the opening.

[0025] In one possible embodiment, the forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer includes: forming a third semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein doping ions of the third semiconductor layer and the second semiconductor layer are oppositely charged; patterning the third semiconductor layer to form a first sub-opening for exposing a part of the second semiconductor layer; and forming a passivation layer provided with a second sub-opening on the side, facing away from the second semiconductor layer, of the third semiconductor layer, wherein the second sub-opening exposes the third semiconductor layer and the first sub-opening.

[0026] In one possible embodiment, the forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer includes: forming a passivation layer on the side, facing away from the light-emitting layer, of the second semiconductor layer; and patterning the passivation layer to form a third sub-opening for exposing a part of the second semiconductor layer such that the landing electrode is in contact with the second semiconductor layer through the third sub-opening.

[0027] In one possible embodiment, the forming the second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer includes forming a second semiconductor layer of which an orthographic projection on the base substrate is located in the orthographic projection of the light-emitting layer on the base substrate on the side, facing away from the first semiconductor layer, of the light-emitting layer, and an area of the orthographic projection of the second semiconductor layer on the base substrate is smaller than that of the orthographic projection of the light-emitting layer on the base substrate; and the forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer includes: forming a passivation layer on the side, facing away from the light-emitting layer, of the second semiconductor layer; and patterning the passivation layer to form a fourth sub-opening for exposing the second semiconductor layer such that the landing electrode is in contact with the second semiconductor layer through the fourth sub-opening, wherein an orthographic projection of the fourth sub-opening on the base substrate and the orthographic projection of the second semiconductor layer on the base substrate substantially coincide with each other.

Brief Description of the Drawings

[0028]

Fig. 1 is a first schematic sectional view of a light-emitting device according to an embodiment of the present disclosure;

Fig. 2 is a second schematic sectional view of the light-emitting device according to the embodiment of the present disclosure;

Fig. 3 is a third schematic sectional view of the light-emitting device according to the embodiment of the present disclosure;

Fig. 4 is a schematic top view of a connection pad layer according to an embodiment of the present disclosure;

Fig. 5 is a schematic sectional view of a light-emitting substrate according to an embodiment of the present disclosure;

Fig. 6 is a schematic top view of a driving backplane according to an embodiment of the present disclosure;

Fig. 7 is a schematic flow chart of manufacturing of a light-emitting device according to an embodiment of the present disclosure;

Fig. 8A is a schematic sectional view after forming a second semiconductor layer 22;

Fig. 8B is a top view of a single film layer of a light-emitting layer 3;

Fig. 8C is a top view of a single film layer of a second semiconductor layer 22;

Fig. 9A is a schematic sectional view after forming a third semiconductor layer 41;

Fig. 9B is a top view of a single film layer of the third semiconductor layer 41;

Fig. 10A is a schematic sectional view after forming

a landing electrode 6;

Fig. 10B is a top view of a single film layer of a passivation layer 42;

Fig. 10C is a top view of a single film layer of a bridge electrode 5;

Fig. 10D is a top view of a single film layer of the landing electrode 6;

Fig. 11A is a schematic sectional view after forming an encapsulation layer 73;

Fig. 11B is a top view of a single film layer of a reflective layer 71;

Fig. 11C is a top view of a single film layer of a heat dissipation layer 72;

Fig. 11D is a top view of a single film layer of the encapsulation layer 73;

Fig. 12A is a schematic sectional view of Fig. 12C along a dashed line E1F1;

Fig. 12B is a top view of a single film layer of a connection pad layer 8;

Fig. 12C is a first top view of the overall light-emitting device;

Fig. 13A is a schematic sectional view of FIG. 13B along a dashed line E2F2;

Fig. 13B is a second top view of the overall light-emitting device;

Fig. 14A is a schematic sectional view of Fig. 14B along a dashed line E3F3;

Fig. 14B is a third top view of the overall light-emitting device;

Fig. 15A is a schematic sectional view of Fig. 15B along a dashed line E4F4; and

Fig. 15B is a fourth top view of the overall light-emitting device.

Detailed Description of the Embodiments

[0029] In order to make the objectives, technical solutions, and advantages of the embodiments of the present disclosure clearer, the technical solutions of the embodiments of the present disclosure will be described clearly and completely with reference to accompanying drawings of the embodiments of the present disclosure. Apparently, the described embodiments are some, not all, of the embodiments of the present disclosure. Based on the described embodiments of the present disclosure, all other embodiments obtained those of ordinarily skill in the art without creative work fall within the protection scope of the present disclosure.

[0030] Unless otherwise defined, technical or scientific terms used in the present disclosure shall have the ordinary meaning as understood by those of ordinary skill in the art to which the present disclosure belongs. "First", "second" and similar words used in the present disclosure do not represent any order, quantity, or importance, but are merely used to distinguish different components. "Include" or "comprise" and other similar words mean that an element or an item preceding the word cover elements or items and their equivalents listed after the word without excluding other elements or items. "Connection" or "connected" and other similar words may include electrical connection, direct or indirect, instead of being limited to physical or mechanical connection. "Upper", "lower", "left", "right", etc. are only used to indicate a relative position relationship, and the relative position relationship may also change accordingly when an absolute position of a described object changes.

[0031] To keep the following description of the embodiments of the present disclosure clear and concise, the present disclosure omits detailed descriptions of well-known functions and well-known components.

[0032] It is found through a test of the photoelectric properties of LEDs that the luminous efficiency of the LEDs and the density of current passing through a light-emitting region of the LEDs have a relationship as shown in Fig. 1. The luminous efficiency of the LEDs increases with the increase of the current density, and shows a trend of luminous efficiency saturation after reaching a certain degree. Further, compared with a gray scale required by a mainstream display screen at this stage, it is found that application of the luminous efficiency of the LEDs by a LED display panel is far from reaching a high-efficiency light-emitting region of the LEDs at present. As shown in Fig. 1, if a light-emitting region of L255 is reduced to 25%, the luminous efficiency of the LEDs is increased by about 20%, and accordingly, the power consumption of backplanes of the LEDs can be reduced on the basis of maintaining the excellent display quality. Therefore, reducing a light-emitting area of the LEDs and increasing the current density in a certain manner to improve the luminous efficiency become a new idea of reducing power consumption of the LED display panel.

[0033] In view of this, referring to Figs. 1, 2, and 3, an embodiment of the present disclosure provides a light-emitting device, including: a base substrate 1, and at least one light-emitting structure P located on one side of the base substrate 1; wherein the light-emitting structure P includes:

a first semiconductor layer 21;

a light-emitting layer 3 located on the side, facing away from the base substrate 1, of the first semiconductor layer 21; wherein in particular, the light-emitting layer may be a multiple quantum well (MQW) layer; and the base substrate 1 is configured to grow a semiconductor layer and a light-emitting layer, for example, the base substrate 1 may be a sapphire substrate;

a second semiconductor layer 22 located on the side, facing away from the first semiconductor layer 21, of the light-emitting layer 3, wherein doping ions of the second semiconductor layer 22 and the first semiconductor layer 21 are oppositely charged; specifically, for example, the first semiconductor layer 21 can be an n-doped semiconductor layer, and the second semiconductor layer 22 can be a p-doped semiconductor layer; specifically, a material of the first

semiconductor layer 21 may be n-doped GaN, and a material of the second semiconductor layer 22 may be p-doped GaN;

a barrier structure 4 located on the side, facing away from the light-emitting layer 3, of the second semiconductor layer 22, wherein the barrier structure 4 is provided with an opening K for exposing the second semiconductor layer 22, an orthographic projection of the opening K on the base substrate 1 is located in an orthographic projection of the light-emitting layer 3 on the base substrate 1, and an area of the opening K is smaller than that of the light-emitting layer 3; and

a landing electrode 6 located on the side, facing away from the second semiconductor layer 22, of the barrier structure 4, wherein the landing electrode 6 is in contact with the second semiconductor layer 22 through the opening K.

[0034] In some embodiments of the present disclosure, the side, facing away from the light-emitting layer 3, of the second semiconductor layer 22 is provided with the barrier structure 4, the barrier structure 4 is provided with the opening K for exposing the second semiconductor layer 22, the orthographic projection of the opening K on the base substrate 1 is located in the orthographic projection of the light-emitting layer 3 on the base substrate 1, and the area of the opening K is smaller than that of the light-emitting layer 3, the landing electrode 6 is in contact with the second semiconductor layer 22 through the opening K, the opening K for exposing the second semiconductor layer 22 of the barrier structure 4 forms an effective light-emitting region, an area of the effective light-emitting region is smaller than that of the original light-emitting layer 3, so that a light-emitting region of the light-emitting device is reduced, the luminous efficiency of the light-emitting device can be improved under the condition that the applied gray scale voltage is the same, and the power consumption of the light-emitting device is reduced on the basis of maintaining the excellent display quality.

[0035] In a specific implementation, the barrier structure 4 can be formed in different ways, and specific examples are given below.

[0036] For example, in one possible embodiment, referring to in Fig. 1, an orthographic projection of the second semiconductor layer 22 on the base substrate 1 and the orthographic projection of the light-emitting layer 3 on the base substrate 1 substantially coincide with each other; the barrier structure 4 includes a third semiconductor layer 41, and a passivation layer 42 located on the side, facing away from the second semiconductor layer 22, of the third semiconductor layer 41, wherein doping ions of the third semiconductor layer 41 and the second semiconductor layer 22 are oppositely charged; in particular, for example, when the second semiconductor layer 22 is an n-doped semiconductor layer, the third semiconductor layer 41 specifically may be a p-doped semiconductor layer, and further, when a material of the second semiconductor layer 22 may be n-doped GaN, a material of the third semiconductor layer 41 specifically may be p-doped GaN; the third semiconductor layer 41 is provided with a first sub-opening K1 for exposing a part of the second semiconductor layer 22, the passivation layer 42 is provided with a second sub-opening K2 for exposing the third semiconductor layer 41 and the first sub-opening K1; and the landing electrode 6 is in contact with the second semiconductor layer 22 through the first sub opening K1 of the third semiconductor layer 41. In the embodiment of the present disclosure, by forming the third semiconductor layer 41 of which doping ions, and doping ions of the second semiconductor layer 22 are oppositely charged, the third semiconductor layer 41 and the second semiconductor layer 22 form a reverse PN junction when the light-emitting structure P is operated, thereby blocking the flow of carriers (for example, electrons), forming an effective light-emitting region in a region where the first sub-opening K1 is located, and lowering the light-emitting region of the light-emitting device.

[0037] In some embodiments, the third semiconductor layer 41 may be an electron blocking layer.

[0038] For another example, in one possible embodiment, referring to Fig. 2, the orthographic projection of the second semiconductor layer 22 on the base substrate 1 and the orthographic projection of the light-emitting layer 3 on the base substrate 1 substantially coincide with each other; the barrier structure 4 includes a passivation layer 42; the passivation layer 42 is provided with a third sub-opening K3 for exposing a part of the second semiconductor layer 22; and the landing electrode 6 is in contact with the second semiconductor layer 22 through the third sub opening K3 of the passivation layer 42. In the embodiment of the present disclosure, by reducing the size of the third sub-opening K3 of the passivation layer 42, the control of the effective light-emitting region is then achieved, and thus, a way of reducing the light-emitting region is simple and easy to implement.

[0039] In particular, a thickness of the second semiconductor layer 22 is 2-4% of a thickness of the first semiconductor layer. In some embodiments of the present disclosure, by reducing the size of the third sub-opening K3 of the passivation layer 42 to reduce the effective light-emitting region, the thickness of the second semiconductor layer 22 is 2-4% of the thickness of the first semiconductor layer, excessive lateral diffusion of current in the second semiconductor layer 22 can be avoided, and the current can enter the light-emitting layer 3 as soon as possible, so as to have a higher luminous efficiency.

[0040] For another example, in one possible embodiment, the orthographic projection of the second semiconductor layer 22 on the base substrate 1 is located in the orthographic projection of the light-emitting layer 3 on the base substrate 1, and an area of the orthographic projection of the second semiconductor layer 22 on the base

substrate 1 is smaller than that of the orthographic projection of the light-emitting layer 3 on the base substrate 1; the barrier structure 4 includes a passivation layer 42; the passivation layer 42 is provided with a fourth sub-opening K4 for exposing at least part of the second semiconductor layer 22; and the landing electrode 6 is in contact with the second semiconductor layer 22 through the fourth sub-opening K4 of the passivation layer 42. In the embodiment of the present disclosure, by reducing the area of the second semiconductor layer 22, the control of the effective light-emitting region is then achieved, and thus, a way of reducing the light-emitting region is simple and easy to implement.

[0041] In particular, the reduction of the effective light-emitting region may be achieved only by reducing the area of the second semiconductor layer 22, e.g., referring to Fig. 3, an orthographic projection of the fourth sub-opening K4 on the base substrate 1 and the orthographic projection of the second semiconductor layer 22 on the base substrate 1 substantially coincide with each other. In particular, it is also possible to reduce the size of the fourth sub-opening K4 of the passivation layer 42 while reducing the area of the second semiconductor layer 22. For example, making the orthographic projection of the fourth sub-opening K4 on the base substrate 1 to be smaller than the orthographic projection of the second semiconductor layer 22 on the base substrate 1 can further reduce the effective light-emitting region.

[0042] In particular, referring to Fig. 3, an area of the second semiconductor layer 22 is one fifth to four fifths of an area of the light-emitting layer 3. In some embodiments of the present disclosure, since the area of the second semiconductor layer 22 is one fifth to four fifths of the area of the light-emitting layer 3, the reduction of the effective light-emitting region can be achieved by reducing the area of the second semiconductor layer 22, while avoiding a situation that the effective light-emitting region is too small and the light output is too small, affecting normal use of the light-emitting device.

[0043] In one possible embodiment, referring to Figs. 1, 2, and 3, the light-emitting device includes at least two light-emitting structures P connected in series with each other; the light-emitting device further includes an encapsulation layer 73 located on the side, facing away from the barrier structure 4, of the landing electrode 6, and the at least two light-emitting structures P connected in series with each other are integrally encapsulated by the encapsulation layer 73. In the embodiment of the present disclosure, the light-emitting device includes at least two light-emitting structures P connected in series with each other, in an active LED driving circuit, in a current path of VDD→VSS, the light-emitting device is equivalent to connecting two light-emitting structures in series, the light-emitting device has a higher crossover voltage, the voltage of a transistor in the driving circuit is reduced, and a high-voltage light-emitting device is formed, which can greatly reduce the cost of the light-emitting device, reduce the current of the circuit and reduce the power consumption.

[0044] In one possible embodiment, referring to Figs. 1, 2, and 3, the light-emitting device includes a first light-emitting structure P1 and a second light-emitting structure P2 which are connected in series with each other; the light-emitting device further includes a bridge electrode 5 located between the barrier structure 4 and the landing electrode 6; the first semiconductor layer 21 of the first light-emitting structure P1 and the landing electrode 6 of the second light-emitting structure P2 are electrically connected by the bridge electrode 5, thereby realizing series connection of different light-emitting structures P.

[0045] In particular, referring to Figs. 1, 2, and 3, the barrier structure 4 at least includes a passivation layer 42; one end of the bridge electrode 5 is electrically connected with the first semiconductor layer 21 of the first light-emitting structure P1 by a via hole penetrating the passivation layer 42, and the other end of the bridge electrode 5 is in direct contact and electrically connected with the landing electrode 6 of the second light-emitting structure P2.

[0046] In one possible embodiment, referring to Figs. 1, 2, and 3, the light-emitting device further includes a connection pad layer 8 located on the side, facing away from the second semiconductor layer 22, of the encapsulation layer 73, wherein the connection pad layer 8 includes a first connection electrode pad 81 electrically connected with the landing electrode 6 of the first light-emitting structure P1, and a second connection electrode pad 82 electrically connected with the first semiconductor layer 21 of the second light-emitting structure P2, thus leading out different electrode terminals of the two light-emitting structures P connected in series with each other.

[0047] In one possible embodiment, referring to Figs. 1, 2, and 3, the landing electrode 6 of the first light-emitting structure P1 includes a first contact portion 61 in contact with the second semiconductor layer 22, a first landing portion 62, and a first connection portion 63 connecting the first contact portion 61 and the first landing portion 62; wherein an orthographic projection of the first landing portion 62 on the base substrate 1 does not overlap with the orthographic projection of the light-emitting layer 3 on the base substrate 1; the first connection electrode pad 81 is electrically connected with the first landing portion 62 through a via hole, thereby moving the lead-out position of the landing electrode 6 in the first light-emitting structure P1 out of the effective light-emitting region, thereby improving the luminous efficiency; the first semiconductor layer 21 of the second light-emitting structure P2 is provided with an overlapping portion 211 which overlaps with the light-emitting layer 3, and an extension portion 212 extending from the overlapping portion 211, and the second connection electrode pad 82 is electrically connected with the extension portion 212 through a via hole, thereby moving the lead-out position of the first semiconductor layer 21 in the second light-emitting structure P2 out of the effective light-emitting

region, thereby improving the luminous efficiency. Compared with a situation that when the lead-out position of the landing electrode 6 in the first light-emitting structure P1 and the lead-out position of the first semiconductor layer 21 in the second light-emitting structure P2 are still in the effective light-emitting region, the proportion of via holes increases, and when the effective light-emitting region of the light-emitting structure P is reduced, the luminous efficiency of the light-emitting structure P decreases, in the embodiment of the present disclosure, by moving the lead-out positions out of the effective light-emitting region, the problem that the luminous efficiency may be reduced after the effective light-emitting region of the light-emitting structure P is reduced can be improved.

[0048] In one possible embodiment, the light-emitting device further includes a heat dissipation layer 72 located between the encapsulation layer 73 and the landing electrode 6; an orthographic projection of the heat dissipation layer 72 on the base substrate 1 at least covers an orthographic projection of the opening K of the first light-emitting structure P1 on the base substrate 1, and an orthographic projection of the opening K of the second light-emitting structure P2 on the base substrate 1. In some embodiments of the present disclosure, the light-emitting device further includes the heat dissipation layer 72 located between the encapsulation layer 73 and the landing electrode 6, which can effectively dissipate heat generated by the light-emitting structure P.

[0049] In one possible embodiment, the connection pad layer 8 further includes a heat dissipation pad 83 which is in a conducting relationship with the heat dissipation layer 72, and an orthographic projection of the heat dissipation pad 83 on the base substrate 1 at least covers the orthographic projection of the opening K1 of the first light-emitting structure P1 on the base substrate 1, and covers the orthographic projection of the opening of the second light-emitting structure P2 on the base substrate 1. After reducing the effective light-emitting region of the light-emitting structure P, although the luminous efficiency of the light-emitting structure P is improved, heat generation points are more concentrated, and heat is more easily accumulated to the light-emitting region, in the embodiment of the present disclosure, the connection pad layer 8 further includes the heat dissipation pad 83 which is in a conducting relationship with the heat dissipation layer 72, which can quickly and efficiently dissipate heat generated by the light-emitting structure P after the effective light-emitting region is reduced, reduce the junction temperature of the light-emitting structure P, and avoid the reduction of luminous efficiency or burning of the light-emitting structure P.

[0050] In one possible embodiment, the encapsulation layer 73 is provided with a first encapsulation opening F1 and a second encapsulation opening F2; wherein an orthographic projection of the first encapsulation opening F1 on the base substrate 1 covers the orthographic projection of the opening K of the first light-emitting structure P1 on the base substrate 1, and an orthographic projection of the second encapsulation opening F2 on the base substrate 1 covers the orthographic projection of the opening K of the second light-emitting structure P2 on the base substrate 1; and the heat dissipation pad 83 is in contact with the heat dissipation layer 72 through the first encapsulation opening F1 and the second encapsulation opening F2. In the embodiment of the present disclosure, by providing the first encapsulation opening F1 and the second encapsulation opening F2 at the openings K to make the heat dissipation pad 83 and the heat dissipation layer 72 conductive at the effective light-emitting region, the length of a heat dissipation channel can be shortened, so that the heat generated by the light-emitting structure P can be quickly and effectively dissipated.

[0051] In one possible embodiment, referring to Fig. 4, the heat dissipation pad 83 includes a first heat dissipation pad 831 covering the opening K of the first light-emitting structure P1, and a second heat dissipation pad 832 covering the opening K of the second light-emitting structure P2, wherein the first heat dissipation pad 831 and the second heat dissipation pad 832 are integrally connected; a center O1 of the first connection electrode pad 81, a center O2 of the second connection electrode pad 82, a center O3 of the first heat dissipation pad 831, and a center O4 of the second heat dissipation pad 832 enclose a rectangle; and the center O1 of the first connection electrode pad 81 and the center O2 of the second connection electrode pad 82 are respectively located at two vertices on one diagonal line k1 of the rectangle, and the center O3 of the first heat dissipation pad 831 and the center O4 of the second heat dissipation pad 832 are respectively located at two vertices on the other diagonal line k2 of the rectangle.

[0052] In one possible embodiment, referring to Figs. 1, 2 and 3, a reflective layer 71 is also arranged between the heat dissipation layer 8 and the landing electrode 6. About 50% of light emitted from the light-emitting layer 3 faces away from the side of the base substrate 1, so the reflective layer 71, which may in particular be a distributed Bragg reflector (DBR), is required to reflect the light facing away from the base substrate 1 back to the base substrate 1 to improve the light emission of the light-emitting structure P. In particular, the reflective layer 71 may adopt a 1/4 wavelength reflector of desired light composed of superimposed SiO2 and TiO2.

[0053] Based on the same inventive concept, referring to Fig. 5, an embodiment of the present disclosure also provides a light-emitting substrate, including a driving backplane 200 and the light-emitting devices provided by embodiments of the present disclosure disposed on one side of the driving backplane 200.

[0054] In one possible embodiment, referring to Figs. 5 and 6, the driving backplane 200 includes driving structures 23 in one-to-one correspondence with the light-emitting devices, wherein each driving structure 23 includes a first electrode 231, a second electrode 232, and

a heat dissipation electrode 233; wherein each first electrode 231 is in bound connection with the corresponding first connection electrode pad 81, each second electrode 232 is in bound connection with the corresponding second connection electrode pad 82, and the heat dissipation electrode 233 is in bound connection with the corresponding heat dissipation pad 83.

[0055] In one possible embodiment, referring to Fig. 6, the driving backplate 200 further includes heat dissipation connection electrodes 234, wherein the heat dissipation electrodes 233 of the different driving structures 23 are electrically connected to each other through the heat dissipation connection electrodes 234.

[0056] In one possible embodiment, the driving backplate 200 may further includes a driving base substrate 21, the driving structures 23 are located on one side of the driving base substrate 21, a driving layer 22 is also arranged between the driving base substrate 21 and the driving structures 23, and the driving layer 22 may in particular be a composite layer including a plurality of film layers. The driving layer 22 may include a first power supply line 221, a second power supply line 222, and a drive circuit 223. The first power supply line 221 may in particular be a VDD power supply line, and the second power supply line 222 may in particular be a VSS power supply line. The drive circuit 223 may specifically include a thin film transistor and a capacitor.

[0057] Based on the same inventive concept, referring to Fig. 7, an embodiment of the present disclosure also provides a method for manufacturing a light-emitting device, including:

step S100, forming a first semiconductor layer on one side of a base substrate;

step S200, forming a light-emitting layer on the side, facing away from the base substrate, of the first semiconductor layer;

step S300, forming a second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer;

step S400, forming a barrier structure provided with an opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein an orthographic projection of the opening on the base substrate is in an orthographic projection of the light-emitting layer on the base substrate, and an area of the opening is smaller than that of the light-emitting layer; and

step S500, forming a landing electrode on the side, facing away from the second semiconductor layer, of the barrier structure such that the landing electrode is in contact with the second semiconductor layer through the opening.

[0058] In one possible embodiment, an effective light-emitting region can be reduced by forming a third semiconductor layer 41, and in particular the step S400, i.e., forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer includes:

step S411, forming a third semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein doping ions of the third semiconductor layer and the second semiconductor layer are oppositely charged;

step S412, patterning the third semiconductor layer to form a first sub-opening for exposing a part of the second semiconductor layer; and

step S413, forming a passivation layer provided with a second sub-opening on the side, facing away from the second semiconductor layer, of the third semiconductor layer, wherein the second sub-opening exposes the third semiconductor layer and the first sub-opening.

[0059] In one possible embodiment, the effective light-emitting region can be reduced by adjusting the size of the opening of the passivation layer, and in particular the step S400, i.e., forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer includes:

step S421, forming a passivation layer on the side, facing away from the light-emitting layer, of the second semiconductor layer; and

step S422, patterning the passivation layer to form a third sub-opening for exposing a part of the second semiconductor layer such that the landing electrode is in contact with the second semiconductor layer through the third sub-opening.

[0060] In one possible embodiment, the effective light-emitting region can be reduced by adjusting an area of the second semiconductor layer, and in particular the step S300, i.e., forming the second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer includes: forming a second semiconductor layer of which an orthographic projection on the base substrate is located in the orthographic projection of the light-emitting layer on the base substrate on the side, facing away from the first semiconductor layer, of the light-emitting layer, and an area of the orthographic projection of the second semiconductor layer on the base substrate is smaller than that of the orthographic projection of the light-emitting layer on the base substrate.

[0061] Correspondingly, the step S400 of forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer includes:

step S431, forming a passivation layer on the side, facing away from the light-emitting layer, of the second semiconductor layer; and

step S432, patterning the passivation layer to form a fourth sub-opening for exposing the second semiconductor layer such that the landing electrode is in contact with the second semiconductor layer through the fourth sub-opening, wherein an orthographic projection of the fourth sub-opening on the base substrate and the orthographic projection of the second semiconductor layer on the base substrate substantially coincide with each other.

[0062] In order to more clearly understand the method for manufacturing the light-emitting device provided by the embodiment of the present disclosure, further description is made as follows by specific embodiments.

[0063] In one possible embodiment, taking the addition of the third semiconductor layer (a current blocker, CB) to reduce an effective light-emitting area, and the manufacture of a corresponding heat dissipation channel of a driving backplane as an example, a detailed explanation is given:

step 1: a base film layer of a light-emitting structure P is manufactured on a base substrate 1 (e.g., a sapphire substrate), a manufacturing method can be in particular a conventional manufacturing process for LED chips, which will not be described here, including the manufacture of three layers of n-GaN (as the first semiconductor layer 21), a quantum well (MQW, as the light-emitting layer 3), and p-GaN (as the second semiconductor layer 22), and as shown in Figs. 8A, 8B, and 8C, Fig. 8A is a schematic sectional view after forming the second semiconductor layer 22, Fig. 8B is a top view of a single film layer of the light-emitting layer 3, and Fig. 8C is a top view of a single film layer of the second semiconductor layer 22;

step 2, the third semiconductor layer 41 (an electron blocking layer) is manufactured, and an opening K defining a light-emitting region is formed, the electron blocking layer is made of n-doped GaN or other materials, during operation of the LED, the electron blocking layer and p-GaN form a reverse PN junction to block the flow of electrons, and the opening K of the electron blocking layer normally emits light, thereby defining the size of the light-emitting region, as shown in Fig. 9A and Fig. 9B, the opening K in Fig. 9B shows an effective light-emitting region of the LED, wherein Fig. 9A is a schematic sectional view after forming the third semiconductor layer 41, and Fig. 9B is a top view of a single film layer of the third semiconductor layer 41;

step 3, the passivation layer 42 is manufactured, and the bridge electrode 5, and the landing electrode 6 are manufactured, light-emitting structures P at two sides are connected, in this step, two sub-LEDs (light-emitting structures P) connected in series are manufactured inside the same LED (the light-emitting device), after all connections are completed, a n-electrode of the left sub-LED will be connected to a p-electrode of the right sub-LED, forming a high voltage LED (in an AMLED driving circuit, in a current path of VDD→VSS, the LED is equivalent to connecting two LEDs in series, and the LED has a higher crossover voltage, thus becoming the high voltage LED); the landing electrode 6 (made of a material which may specifically be indium tin oxide) is subjected to landing by the bridge electrode 5 to form a potential connection, the landing electrode 6 of the left sub-LED connected to the p electrode extends beyond the light-emitting region, so as to subsequently keep the p electrode away from the light-emitting region with respect to via holes 711 of the reflective layer 71 to avoid affecting the light emission of the LED, and as shown in Figs. 10A, 10B, 10C, and 10D, Fig. 10A is a schematic sectional view after forming the landing electrode 6, Fig. 10B is a top view of a single film layer of the passivation layer 42, Fig. 10C is a top view of a single film layer of the bridge electrode 5, and Fig. 10D is a top view of a single film layer of the landing electrode 6;

step 4, the reflective layer 71 is manufactured, about 50% of light emitted from the quantum well (the light-emitting layer 3) faces away from the side of the base substrate 1 (sapphire) when the LED is in operation, so the reflective layer 71, which may in particular be a distributed Bragg reflector (DBR), is required to reflect the light facing away from the base substrate 1 back to the sapphire side, improving the light emission of the LED, and a 1/4 wavelength reflector of desired light composed of superimposed SiO_2 and TiO_2 can be adopted; however, when a conventional LED is connected to the p electrode, it is necessary to land p-GaN in the light-emitting region through via holes formed after etching the DBR, metal of the p electrode absorbs part of photons to reduce the luminous efficiency, and in the embodiments of the present disclosure, after reducing the effective light-emitting region of the LED, the proportion of via holes increases, and the luminous efficiency of the LED is reduced instead, so there is a need of a certain method to move via holes of the p-electrode out of the light-emitting region and manufacture a relatively complete DBR to improve the light emission; the heat dissipation layer 72 (heat sink) is manufactured on an outer layer of the DBR, wrapping the entire LED and leaving via holes for subsequent Pad (a connection pad layer 8) connection electrodes; the LED is encapsulated through the encapsulation layer 73 and Pad metal vias are etched for subsequent connection of the heat dissipation channel and the electrode, and as shown in Figs. 11A, 11B, 11C, and 11D, Fig. 11A is a schematic sectional view after forming the encapsulation layer 73, Fig. 11B is a top

view of a single film layer of the reflective layer 71, Fig. 11C is a top view of a single film layer of the heat dissipation layer 72, and Fig. 11D is a top view of a single film layer of the encapsulation layer 73; and

step 5, manufacture of the connection pad layer 8 is completed, the heat dissipation layer 72 directly facing the opening K is connected through the first encapsulation opening F1 and the second encapsulation opening F2 of the encapsulation layer 73 to form a heat dissipation channel, the corresponding electrodes are connected to form an electrical connection of the n and p electrodes of the LED, and as shown in Fig. 12A, Fig. 12B, and Fig. 12C, Fig. 12A is a schematic sectional view after forming the connection pad layer 8, Fig. 12B is a top view of a single film layer of the connection pad layer 8, and Fig. 12C is a top view of the overall light-emitting device, and Fig. 12A may be a schematic sectional view of Fig. 12C along a dashed line E1F1.

[0064] In another possible implementation, the size of the effective light-emitting region can be controlled by adjusting the size of the third sub-opening of the passivation layer 42, in this embodiment, the thickness of p-GaN can be reduced, excessive lateral diffusion of current in p-GaN is avoided, and the current enters the quantum well as soon as possible; a via area of the third sub-opening K3 of the passivation layer 42 is a landing area of the landing electrode 6 and p-GaN, i.e. the effective light-emitting region, wherein Fig. 13A is a schematic sectional view after forming the connection pad layer 8, Fig. 13B is a top view of the overall light-emitting device, and Fig. 13A can be a schematic sectional view of Fig. 13B along a dashed line E2F2; and a specific manufacture process for film layers may be similar to that in the above embodiment, which will not be repeated in the embodiments of the present disclosure.

[0065] In another possible embodiment, the area of the second semiconductor layer 22 (p-GaN) is reduced by etching, limiting the effective light-emitting region; in specific implementation, a situation that the quantum well layer is etched, resulting in the formation of a structure aligned with p-GaN can be avoided, and a situation that if being aligned, a leakage channel is formed through a lattice structure where the edges of p-GaN, the quantum well, and n-GaN are damaged is avoided, thereby reducing the luminous efficiency of the LED, wherein Fig. 14A is a schematic sectional view after forming the connection pad layer 8, Fig. 14B is a top view of the overall light-emitting device, and Fig. 14A can be a schematic sectional view of Fig. 14B along a dashed line E3F3; and a specific manufacture process for film layers may be similar to that in the above embodiment, which will not be repeated in the embodiments of the present disclosure.

[0066] In another possible embodiment, the connection pad layer 8 may also not be provided with the heat dissipation pad 83, taking the addition of the third semiconductor layer (a current blocker, CB) to reduce an effective light-emitting area, and the manufacture of a corresponding heat dissipation channel of a driving backplane as an example, a structural schematic diagram of the manufactured light-emitting device is specifically shown in Figs. 15A, and 15B, wherein Fig. 15A is a schematic sectional view after forming the connection pad layer 8, and Fig. 15B is a top view of the overall light-emitting device, and Fig. 15A may be a schematic sectional view of Fig. 15B along a dashed line E4F4; and a specific manufacture process for film layers may be similar to that in the above embodiment, which will not be repeated in the embodiments of the present disclosure.

[0067] The beneficial effects of the embodiments of the present disclosure are as follows: in the embodiments of the present disclosure, the side, facing away from the light-emitting layer 3, of the second semiconductor layer 22 is provided with the barrier structure 4, the barrier structure 4 is provided with the opening K for exposing the second semiconductor layer 22, the orthographic projection of the opening K on the base substrate 1 is located in the orthographic projection of the light-emitting layer 3 on the base substrate 1, and the area of the opening K is smaller than that of the light-emitting layer 3, the landing electrode 6 is in contact with the second semiconductor layer 22 through the opening K, the opening K for exposing the second semiconductor layer 22 of the barrier structure 4 forms an effective light-emitting region, an area of the effective light-emitting region is smaller than that of the original light-emitting layer 3, so that a light-emitting region of the light-emitting device is reduced, the luminous efficiency of the light-emitting device can be improved under the condition that the applied gray scale voltage is the same, and the power consumption of the light-emitting device is reduced on the basis of maintaining the excellent display quality.

[0068] Although preferred embodiments of the present disclosure have been described, those skilled in the art can make additional changes and modifications to these embodiments once they know the basic inventive concepts. Therefore, the appended claims are intended to be explained as including the preferred embodiments and all changes and modifications falling within the scope of the present disclosure.

[0069] It will be apparent to those skilled in the art that various changes and modifications can be made to the embodiments of the present disclosure without departing from the spirit or scope of the embodiments of the present disclosure. Thus, if these changes and modifications of the embodiments of the present disclosure fall within the scope of the claims of the present disclosure and their equivalents, the present disclosure is also intended to include these changes and modifications.

Claims

1. A light-emitting device, comprising: a base sub-

strate, and at least one light-emitting structure on one side of the base substrate; wherein the light-emitting structure comprises:

a first semiconductor layer;
a light-emitting layer on a side, facing away from the base substrate, of the first semiconductor layer;
a second semiconductor layer on a side, facing away from the first semiconductor layer, of the light-emitting layer, wherein doping ions of the second semiconductor layer and the first semiconductor layer are oppositely charged;
a barrier structure on a side, facing away from the light-emitting layer, of the second semiconductor layer, wherein the barrier structure is provided with an opening for exposing the second semiconductor layer, an orthographic projection of the opening on the base substrate is in an orthographic projection of the light-emitting layer on the base substrate, and an area of the opening is smaller than an area of the light-emitting layer; and
a landing electrode on a side, facing away from the second semiconductor layer, of the barrier structure, wherein the landing electrode is in contact with the second semiconductor layer through the opening.

2. The light-emitting device according to claim 1, wherein an orthographic projection of the second semiconductor layer on the base substrate and the orthographic projection of the light-emitting layer on the base substrate substantially coincide with each other;

the barrier structure comprises a third semiconductor layer and a passivation layer on a side, facing away from the second semiconductor layer, of the third semiconductor layer, wherein doping ions of the third semiconductor layer and the second semiconductor layer are oppositely charged; and the third semiconductor layer is provided with a first sub-opening for exposing a part of the second semiconductor layer, and the passivation layer is provided with a second sub-opening for exposing the third semiconductor layer and the first sub-opening; and
the landing electrode is in contact with the second semiconductor layer through the first sub-opening of the third semiconductor layer.

3. The light-emitting device according to claim 1, wherein an orthographic projection of the second semiconductor layer on the base substrate and the orthographic projection of the light-emitting layer on the base substrate substantially coincide with each other;

the barrier structure comprises a passivation layer; wherein the passivation layer is provided with a third sub-opening for exposing a part of the second semiconductor layer; and
the landing electrode is in contact with the second semiconductor layer through the third sub-opening of the passivation layer.

4. The light-emitting device according to claim 3, wherein a thickness of the second semiconductor layer is 2-4% of a thickness of the first semiconductor layer.

5. The light-emitting device according to claim 1, wherein an orthographic projection of the second semiconductor layer on the base substrate is in the orthographic projection of the light-emitting layer on the base substrate, and an area of the orthographic projection of the second semiconductor layer on the base substrate is smaller than an area of the orthographic projection of the light-emitting layer on the base substrate;

the barrier structure comprises a passivation layer; wherein the passivation layer is provided with a fourth sub-opening for exposing at least part of the second semiconductor layer; and
the landing electrode is in contact with the second semiconductor layer through the fourth sub-opening of the passivation layer.

6. The light-emitting device according to claim 5, wherein an orthographic projection of the fourth sub-opening on the base substrate and the orthographic projection of the second semiconductor layer on the base substrate substantially coincide with each other.

7. The light-emitting device according to claim 6, wherein an area of the second semiconductor layer is one fifth to four fifths of an area of the light-emitting layer.

8. The light-emitting device according to any one of claims 1 to 7, wherein the light-emitting device comprises at least two of the light-emitting structures connected in series with each other; and
the light-emitting device further comprises an encapsulation layer on a side, facing away from the barrier structure, of the landing electrode, and the at least two light-emitting structures connected in series with each other are integrally encapsulated by the encapsulation layer.

9. The light-emitting device according to claim 8, wherein the light-emitting device comprises a first light-emitting structure and a second light-emitting structure which are connected in series with each

other; and
the light-emitting device further comprises a bridge electrode between the barrier structure and the landing electrode; the first semiconductor layer of the first light-emitting structure and the landing electrode of the second light-emitting structure are electrically connected by the bridge electrode.

10. The light-emitting device according to claim 9, wherein the barrier structure at least comprises a passivation layer; and
one end of the bridge electrode is electrically connected with the first semiconductor layer of the first light-emitting structure through a via hole penetrating the passivation layer, and the other end of the bridge electrode is in direct contact and electrically connected with the landing electrode of the second light-emitting structure.

11. The light-emitting device according to claim 10, further comprising a connection pad layer on a side, facing away from the second semiconductor layer, of the encapsulation layer, wherein the connection pad layer comprises a first connection electrode pad electrically connected with the landing electrode of the first light-emitting structure, and a second connection electrode pad electrically connected with the first semiconductor layer of the second light-emitting structure.

12. The light-emitting device according to claim 11, wherein the landing electrode of the first light-emitting structure comprises a first contact portion in contact with the second semiconductor layer, a first landing portion, and a first connection portion connecting the first contact portion and the first landing portion; wherein an orthographic projection of the first landing portion on the base substrate does not overlap with the orthographic projection of the light-emitting layer on the base substrate; the first connection electrode pad is electrically connected with the first landing portion through a via hole; and
the first semiconductor layer of the second light-emitting structure is provided with an overlapping portion which overlaps with the light-emitting layer, and an extension portion extending from the overlapping portion, and the second connection electrode pad is electrically connected with the extension portion through a via hole.

13. The light-emitting device according to claim 11, further comprising a heat dissipation layer between the encapsulation layer and the landing electrode; wherein an orthographic projection of the heat dissipation layer on the base substrate at least covers an orthographic projection of the opening of the first light-emitting structure on the base substrate, and covers an orthographic projection of the opening of the second light-emitting structure on the base substrate.

14. The light-emitting device according to claim 13, wherein the connection pad layer further comprises a heat dissipation pad which is in a conducting relationship with the heat dissipation layer, and an orthographic projection of the heat dissipation pad on the base substrate at least covers the orthographic projection of the opening of the first light-emitting structure on the base substrate, and covers the orthographic projection of the opening of the second light-emitting structure on the base substrate.

15. The light-emitting device according to claim 14, wherein the encapsulation layer is provided with a first encapsulation opening and a second encapsulation opening; wherein an orthographic projection of the first encapsulation opening on the base substrate covers the orthographic projection of the opening of the first light-emitting structure on the base substrate, and an orthographic projection of the second encapsulation opening on the base substrate covers the orthographic projection of the opening of the second light-emitting structure on the base substrate; and
the heat dissipation pad is in contact with the thermal dissipation layer through the first encapsulation opening and the second encapsulation opening.

16. The light-emitting device according to claim 14, wherein the heat dissipation pad comprises a first heat dissipation pad covering the opening of the first light-emitting structure, and a second heat dissipation pad covering the opening of the second light-emitting structure, wherein the first heat dissipation pad and the second heat dissipation pad are integrally connected; and
a center of the first connection electrode pad, a center of the second connection electrode pad, a center of the first heat dissipation pad, and a center of the second heat dissipation pad enclose a rectangle; and the center of the first connection electrode pad and the center of the second connection electrode pad are respectively located at two vertices on one diagonal line of the rectangle, and the center of the first heat dissipation pad and the center of the second heat dissipation pad are respectively located at two vertices on the other diagonal line of the rectangle.

17. The light-emitting device according to claim 13, wherein a reflective layer is arranged between the heat dissipation layer and the landing electrode.

18. A light-emitting substrate, comprising a driving backplane and the light-emitting devices according to any one of claims 1 to 17 disposed on one side of the driving backplane.

19. The light-emitting substrate according to claim 18, wherein the driving backplane comprises driving structures in one-to-one correspondence with the light-emitting devices, wherein each of the driving structures comprises a first electrode, a second electrode, and a heat dissipation electrode; wherein each first electrode is in bound connection with the corresponding first connection electrode pad, each second electrode is in bound connection with the corresponding second connection electrode pad, and each heat dissipation electrode is in bound connection with the corresponding heat dissipation pad.

20. The light-emitting substrate according to claim 19, wherein the driving backplane further comprises heat dissipation connection electrodes, wherein the heat dissipation electrodes of different driving structures are electrically connected to each other through the heat dissipation connection electrodes.

21. A method for manufacturing a light-emitting device, comprising:

forming a first semiconductor layer on one side of a base substrate;
forming a light-emitting layer on the side, facing away from the base substrate, of the first semiconductor layer;
forming a second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer;
forming a barrier structure provided with an opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein an orthographic projection of the opening on the base substrate is located in an orthographic projection of the light-emitting layer on the base substrate, and an area of the opening is smaller than an area of the light-emitting layer; and
forming a landing electrode on the side, facing away from the second semiconductor layer, of the barrier structure such that the landing electrode is in contact with the second semiconductor layer through the opening.

22. The manufacturing method according to claim 21, wherein the forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer comprises:

forming a third semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein doping ions of the third semiconductor layer and the second semiconductor layer are oppositely charged;
patterning the third semiconductor layer to form a first sub-opening for exposing a part of the second semiconductor layer; and
forming a passivation layer provided with a second sub-opening on the side, facing away from the second semiconductor layer, of the third semiconductor layer, wherein the second sub-opening exposes the third semiconductor layer and the first sub-opening.

23. The manufacturing method according to claim 21, wherein the forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer comprises:

forming a passivation layer on the side, facing away from the light-emitting layer, of the second semiconductor layer; and
patterning the passivation layer to form a third sub-opening for exposing a part of the second semiconductor layer such that the landing electrode is in contact with the second semiconductor layer through the third sub-opening.

24. The manufacturing method according to claim 21, wherein the forming the second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer comprises: forming a second semiconductor layer of which an orthographic projection on the base substrate is in the orthographic projection of the light-emitting layer on the base substrate on the side, facing away from the first semiconductor layer, of the light-emitting layer, and an area of the orthographic projection of the second semiconductor layer on the base substrate is smaller than an area of the orthographic projection of the light-emitting layer on the base substrate; and the forming the barrier structure provided with the opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer comprises:

forming a passivation layer on the side, facing away from the light-emitting layer, of the second semiconductor layer; and
patterning the passivation layer to form a fourth sub-opening for exposing the second semiconductor layer such that the landing electrode is in contact with the second semiconductor layer through the fourth sub-opening, wherein an orthographic projection of the fourth sub-opening on the base substrate and the orthographic projection of the second semiconductor layer on the base substrate substantially coincide with each other.

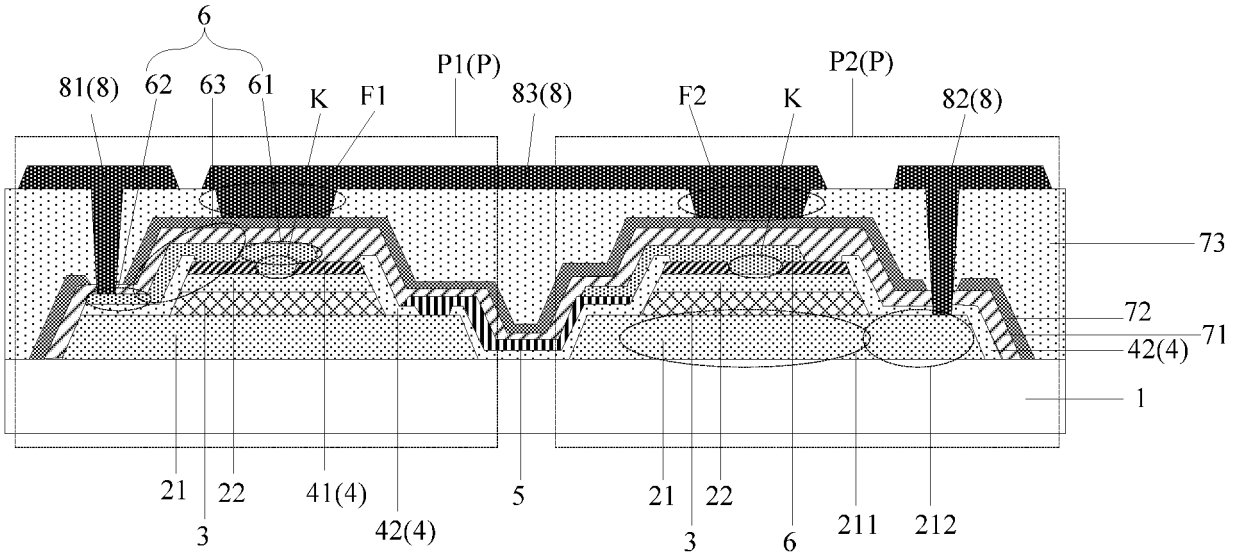
6
81(8)
62
63
61
K
F1
P1(P)
83(8)
F2
K
P2(P)
82(8)
73
72
71
42(4)
1
21
22
41(4)
5
21
22
3
42(4)
3
6
211
212

Fig. 1

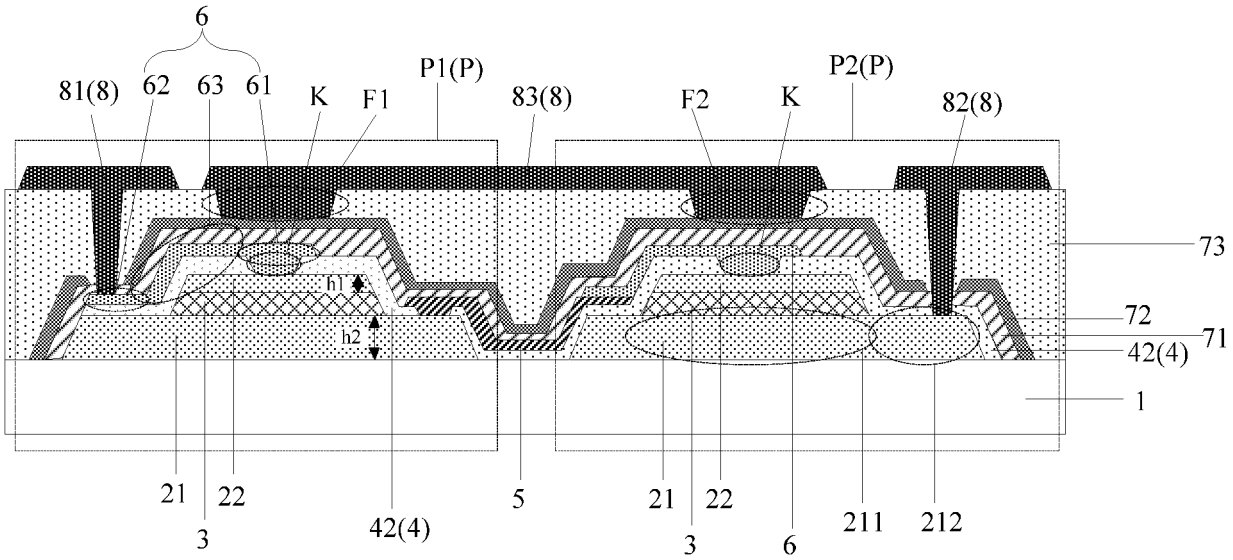
6
81(8)
62
63
61
K
F1
P1(P)
83(8)
F2
K
P2(P)
82(8)
73
h1
h2
72
71
42(4)
1
21
22
5
21
22
3
42(4)
3
6
211
212

Fig. 2

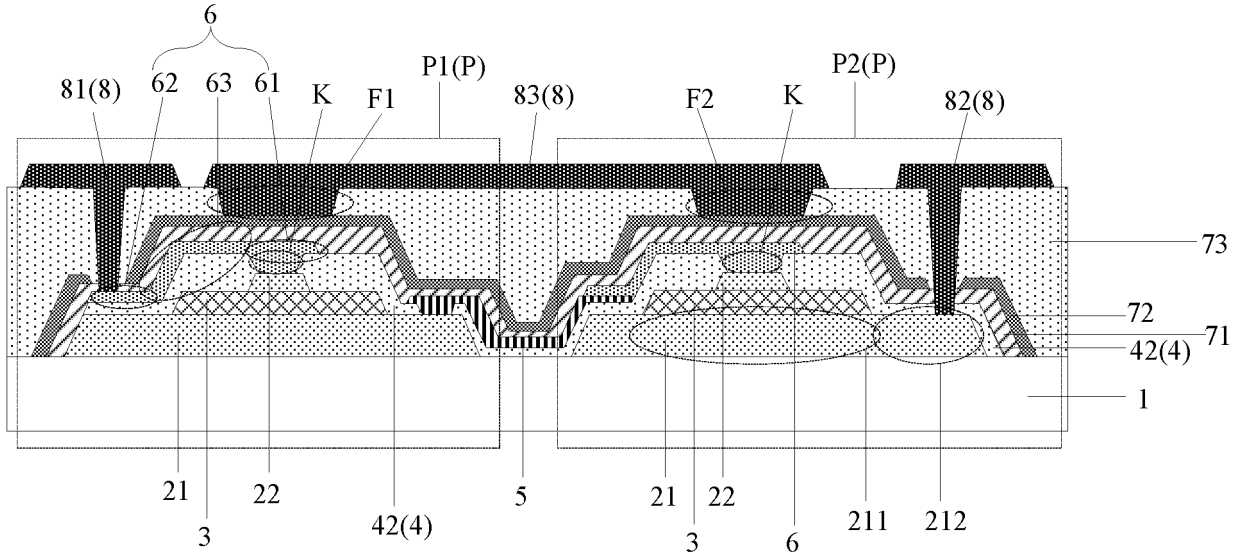
6
81(8)
62
63
61
K
F1
P1(P)
83(8)
F2
K
P2(P)
82(8)
73
72
71
42(4)
1
21
3
22
42(4)
5
21
3
22
6
211
212

Fig. 3

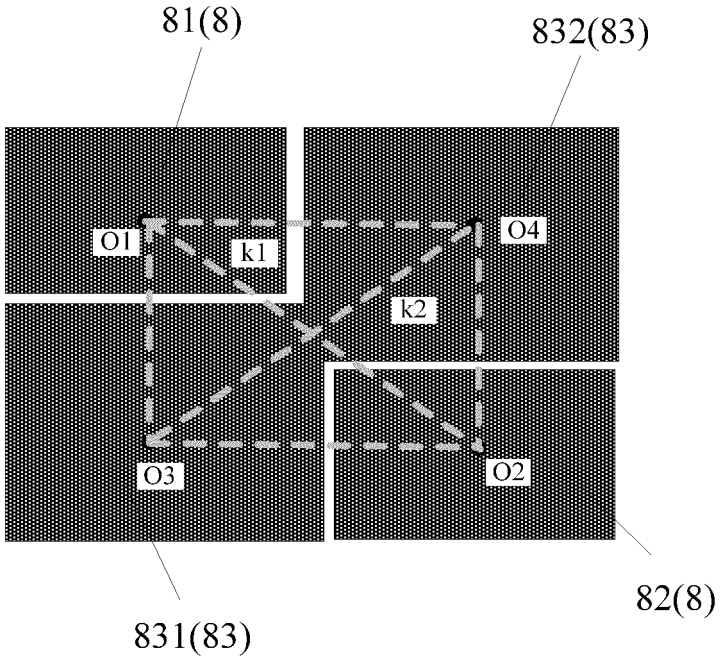
81(8)
832(83)
O1
k1
O4
k2
O3
O2
831(83)
82(8)

Fig. 4

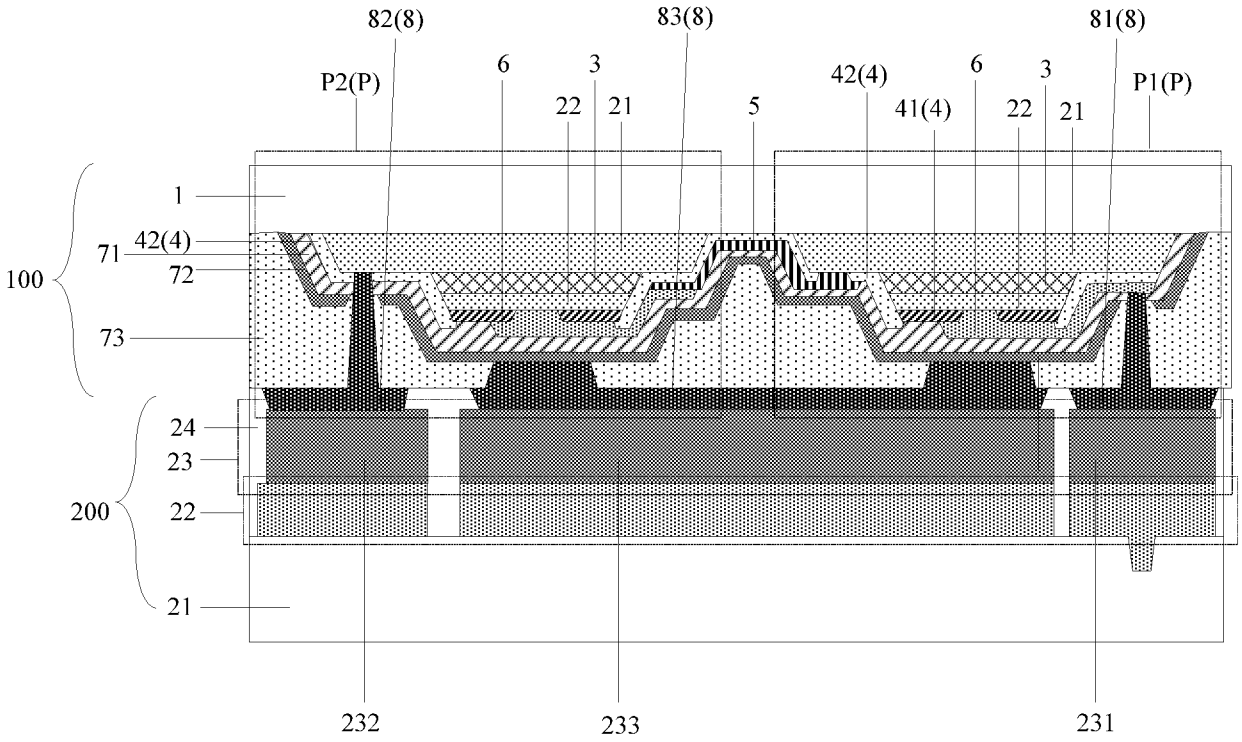
82(8)
83(8)
81(8)
P2(P)
6
3
22
21
5
42(4)
41(4)
6
3
22
21
P1(P)
1
71
42(4)
72
100
73
24
23
200
22
21
232
233
231

Fig. 5

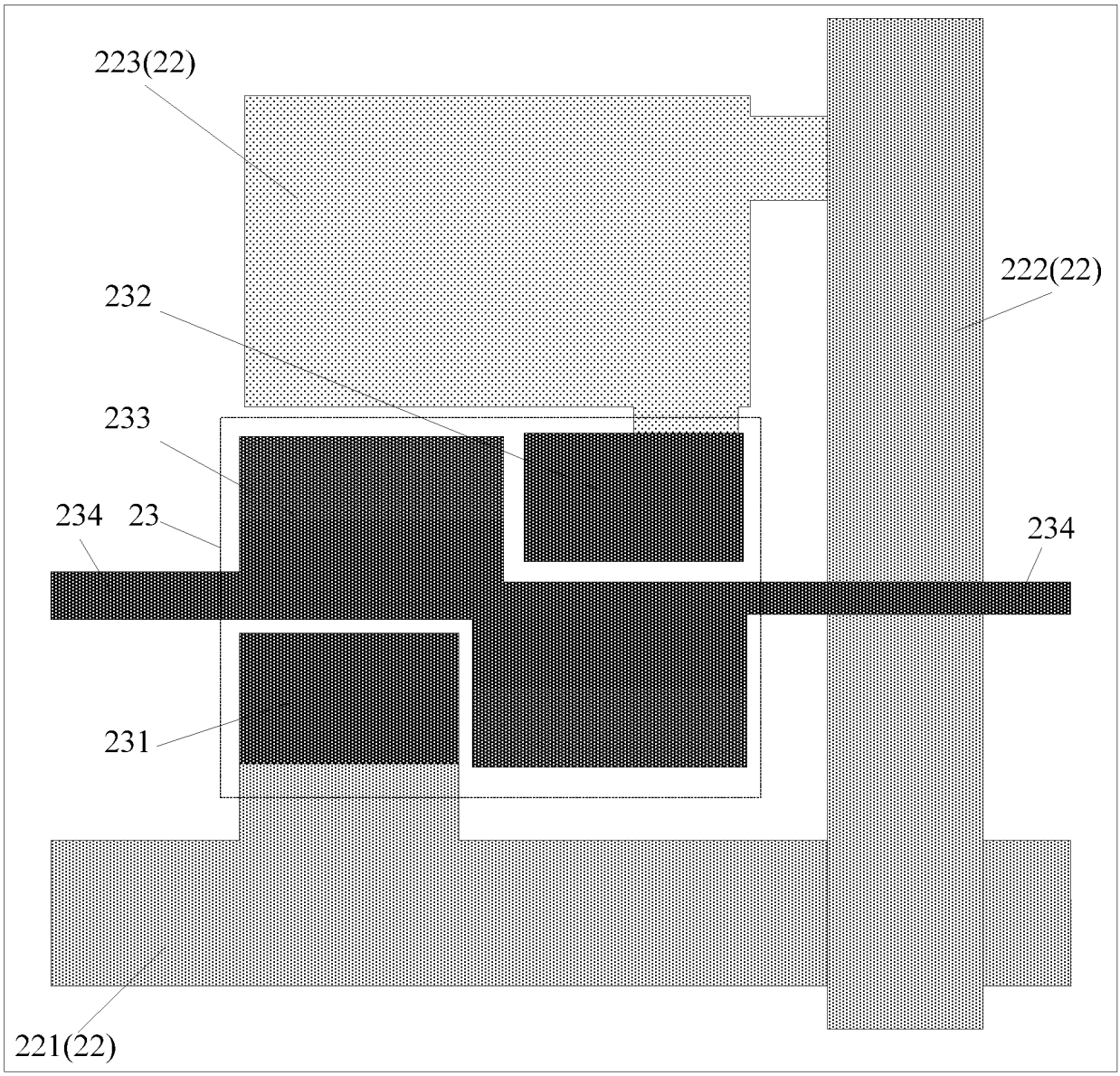

Fig. 6

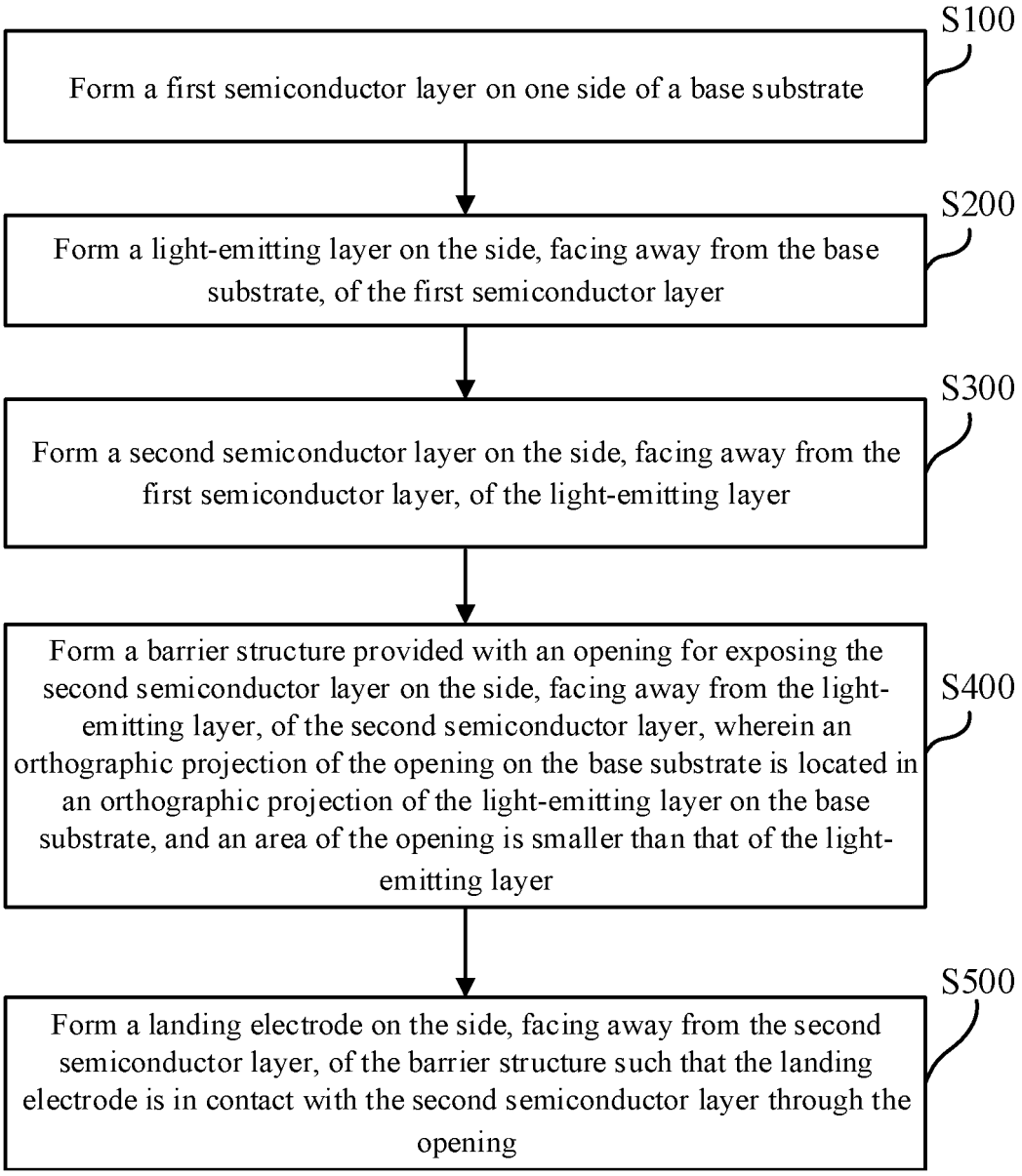
S100
Form a first semiconductor layer on one side of a base substrate
S200
Form a light-emitting layer on the side, facing away from the base substrate, of the first semiconductor layer
S300
Form a second semiconductor layer on the side, facing away from the first semiconductor layer, of the light-emitting layer
S400
Form a barrier structure provided with an opening for exposing the second semiconductor layer on the side, facing away from the light-emitting layer, of the second semiconductor layer, wherein an orthographic projection of the opening on the base substrate is located in an orthographic projection of the light-emitting layer on the base substrate, and an area of the opening is smaller than that of the light-emitting layer
S500
Form a landing electrode on the side, facing away from the second semiconductor layer, of the barrier structure such that the landing electrode is in contact with the second semiconductor layer through the opening

Fig. 7

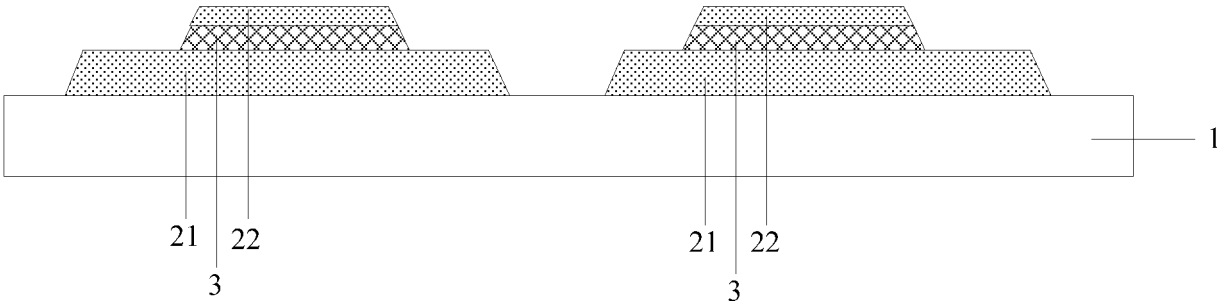

Fig. 8A

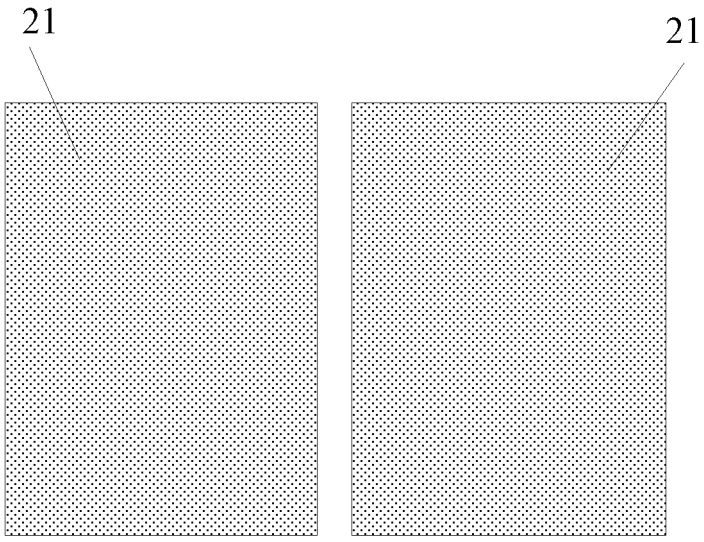

Fig. 8B

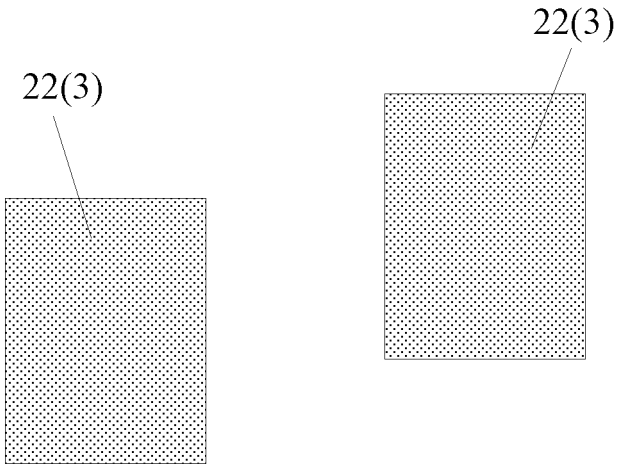

Fig. 8C

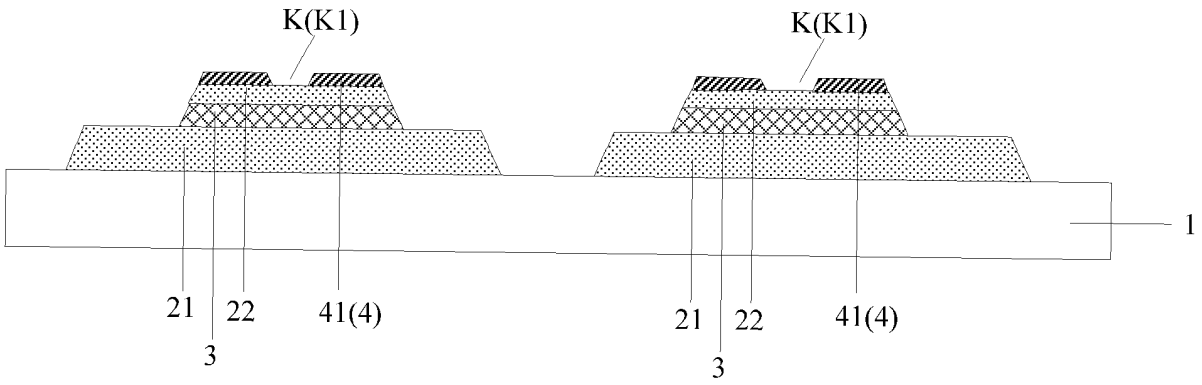

Fig. 9A

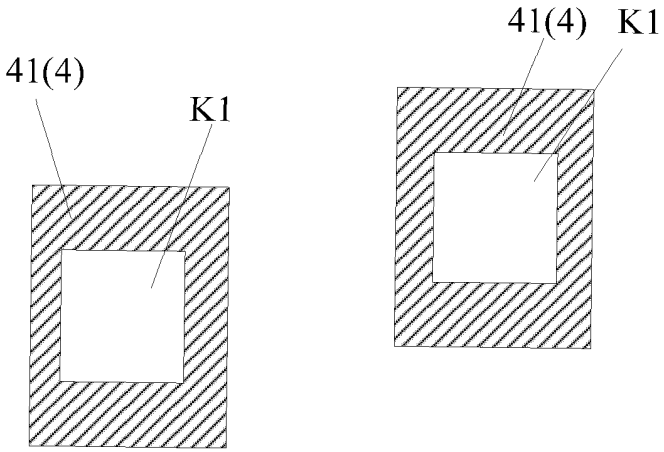

Fig. 9B

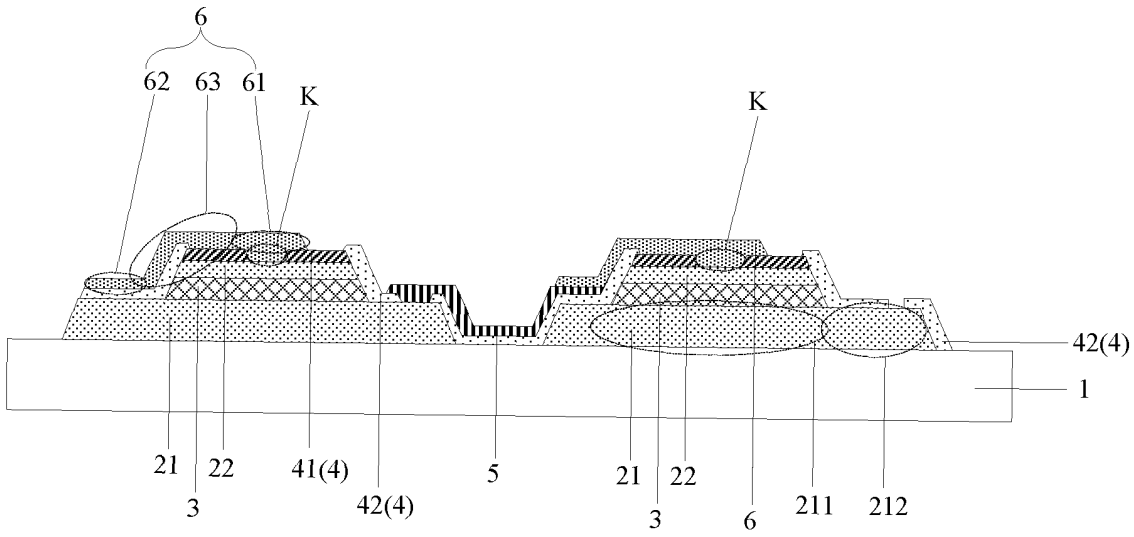

Fig. 10A

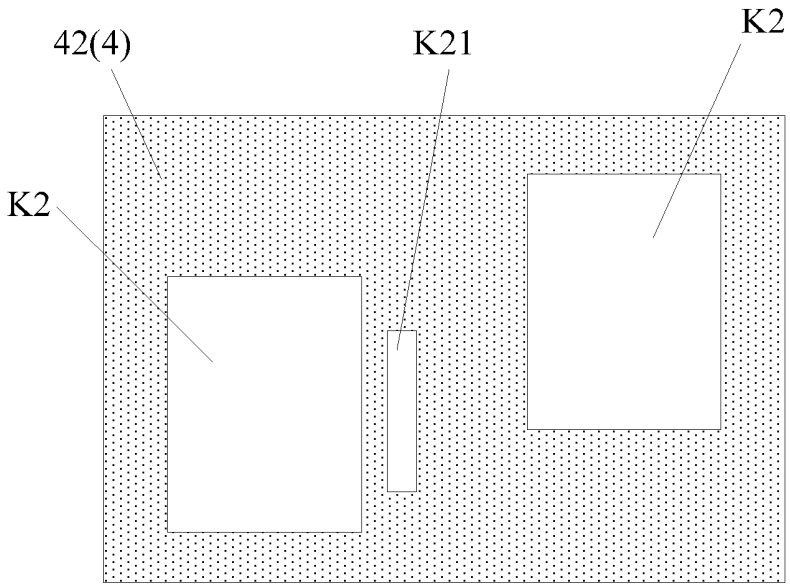

Fig. 10B

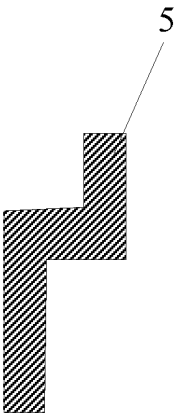

Fig. 10C

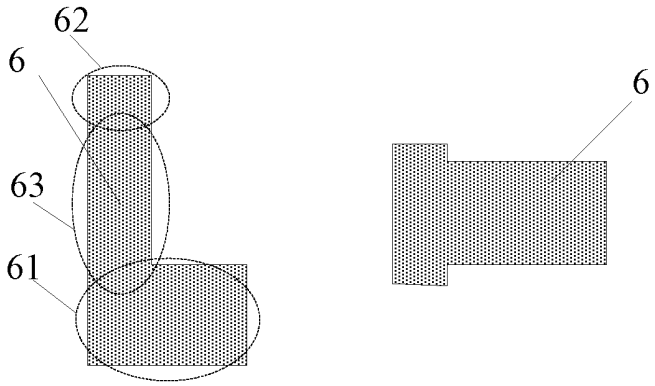

Fig. 10D

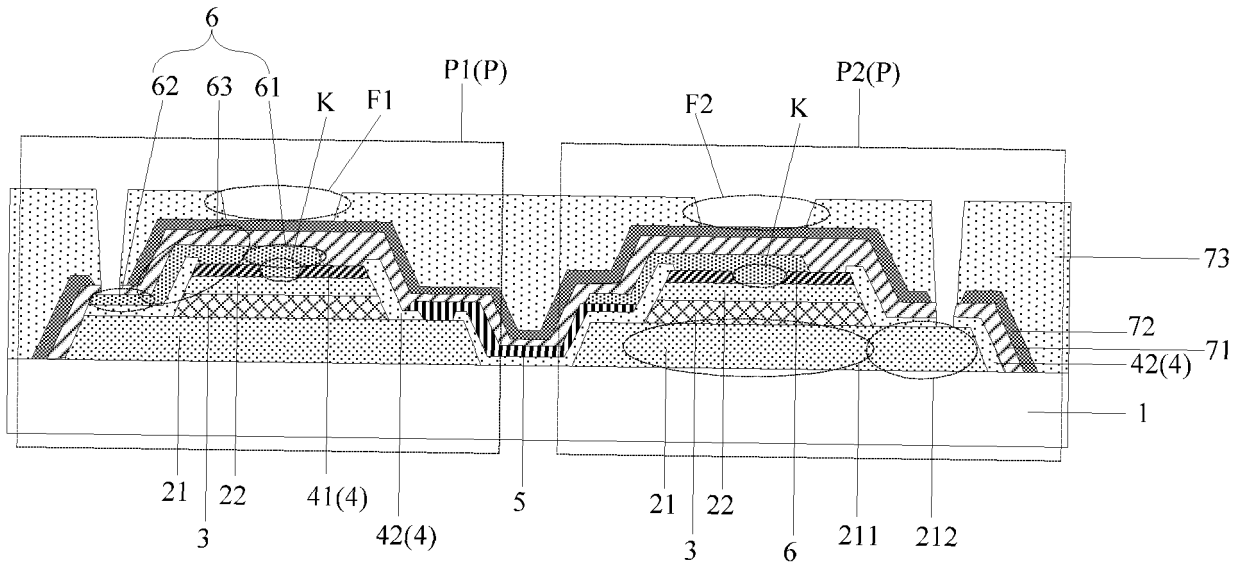

Fig. 11A

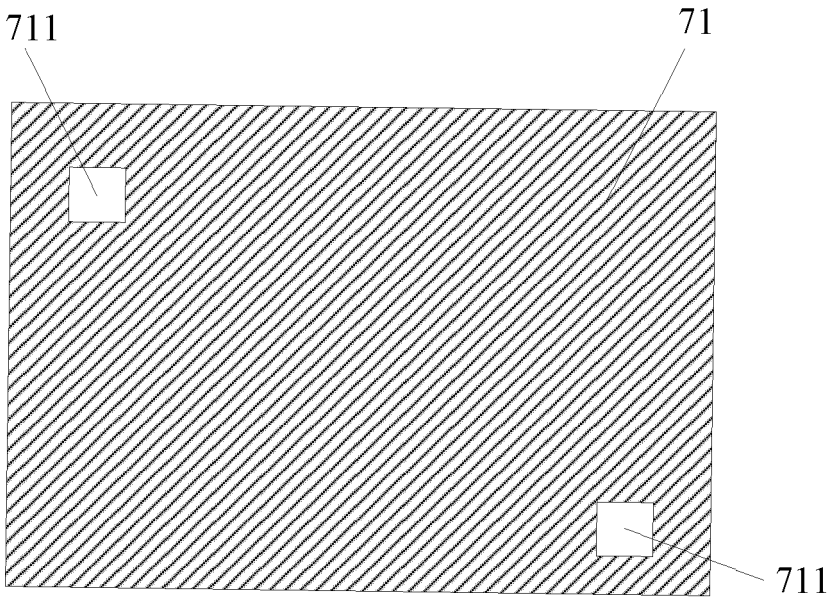

Fig. 11B

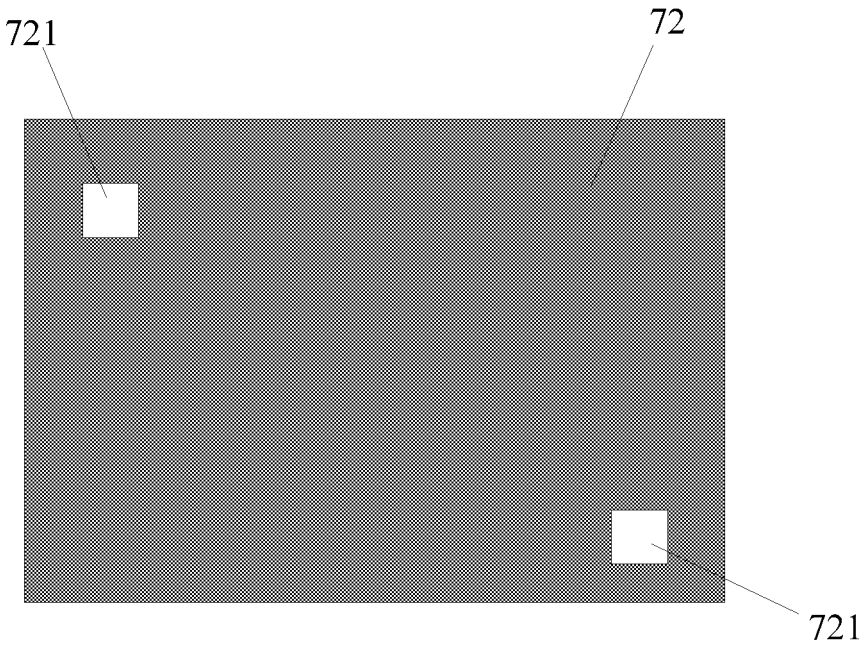

Fig. 11C

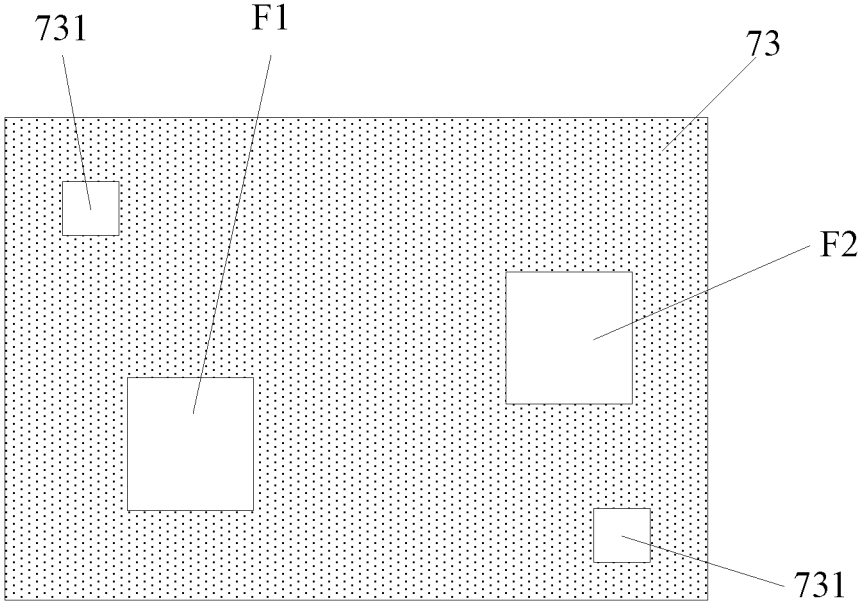

Fig. 11D

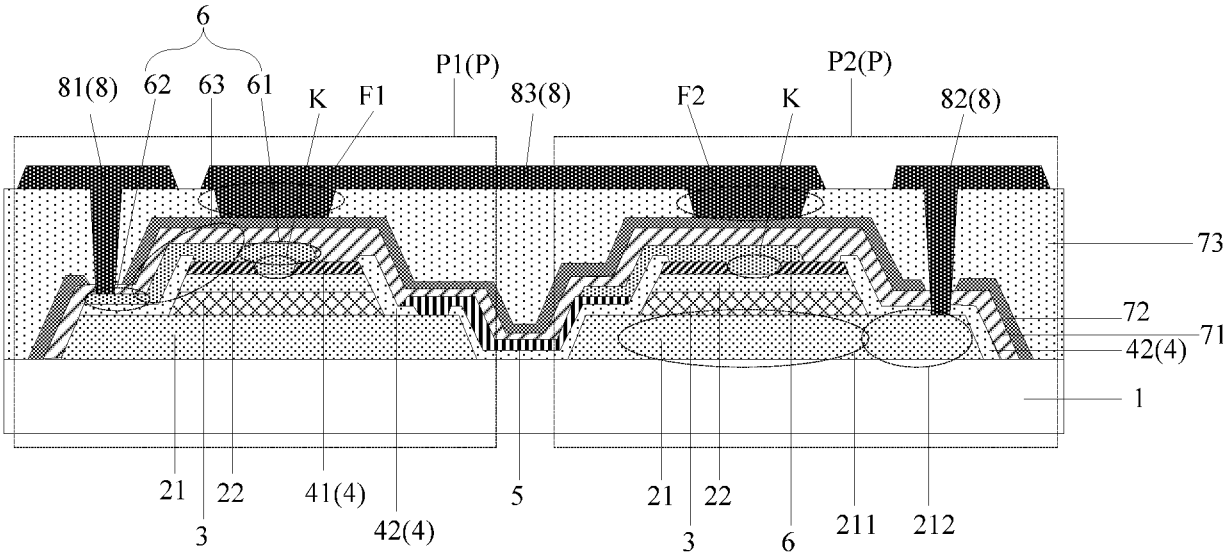

Fig. 12A

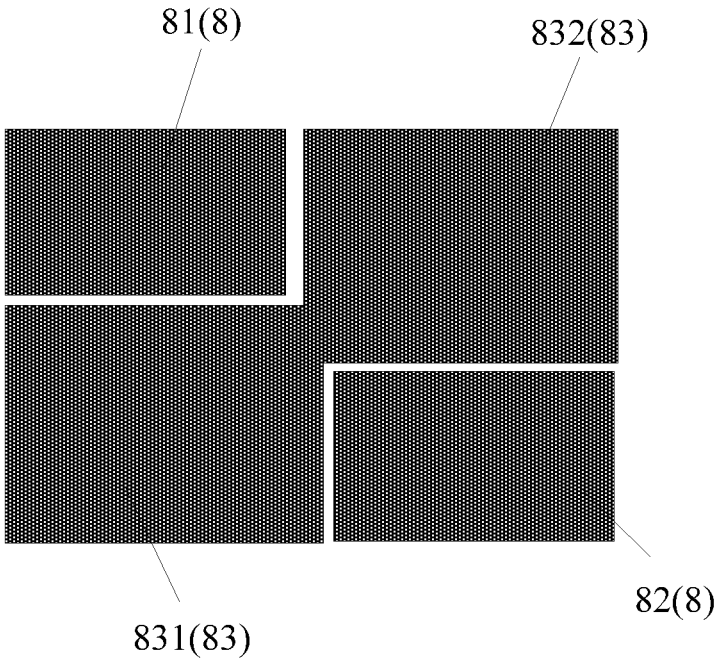

Fig. 12B

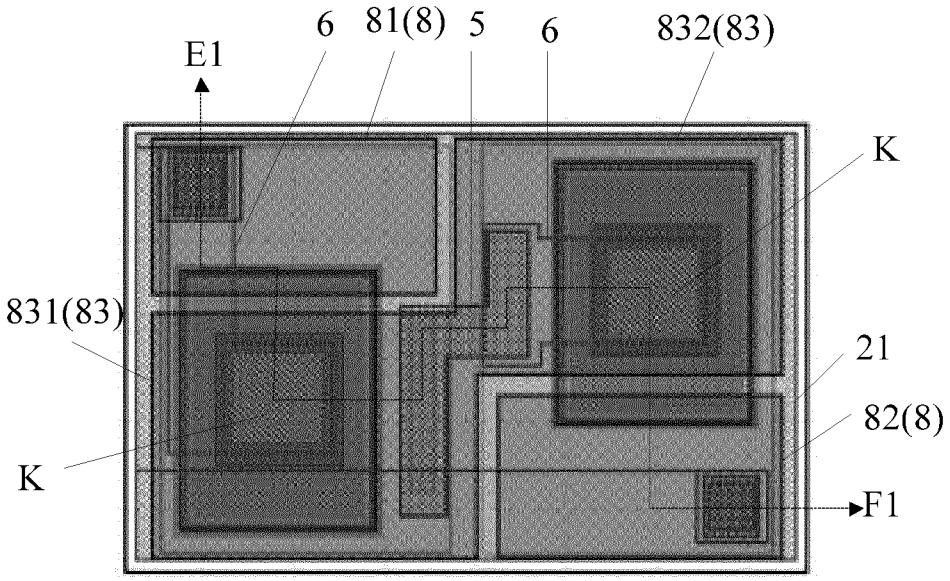

Fig. 12C

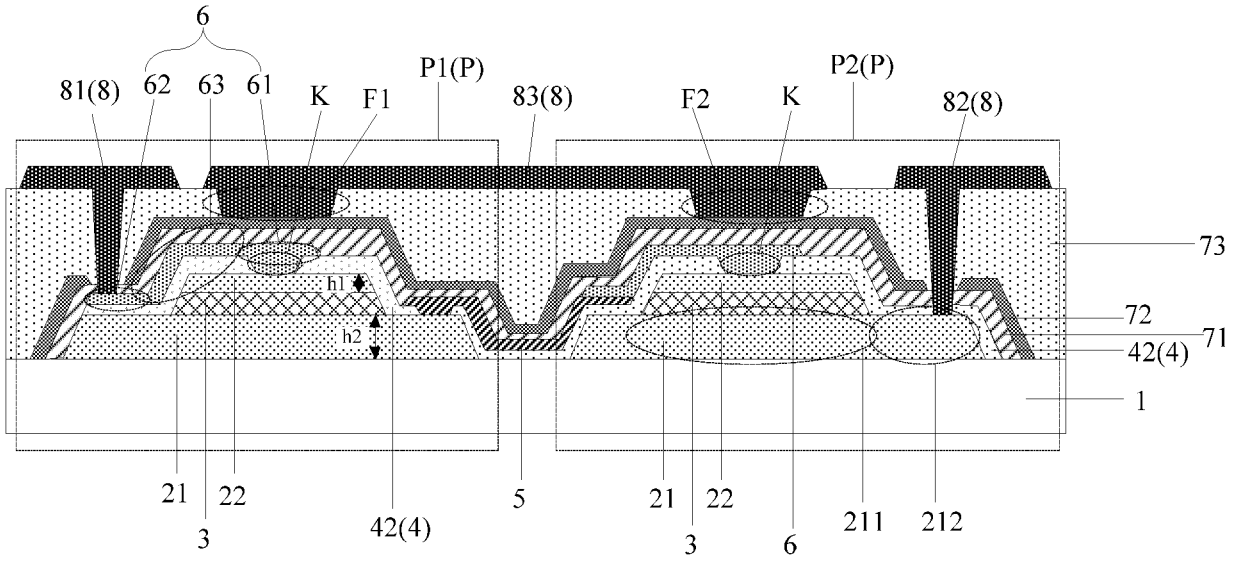

Fig. 13A

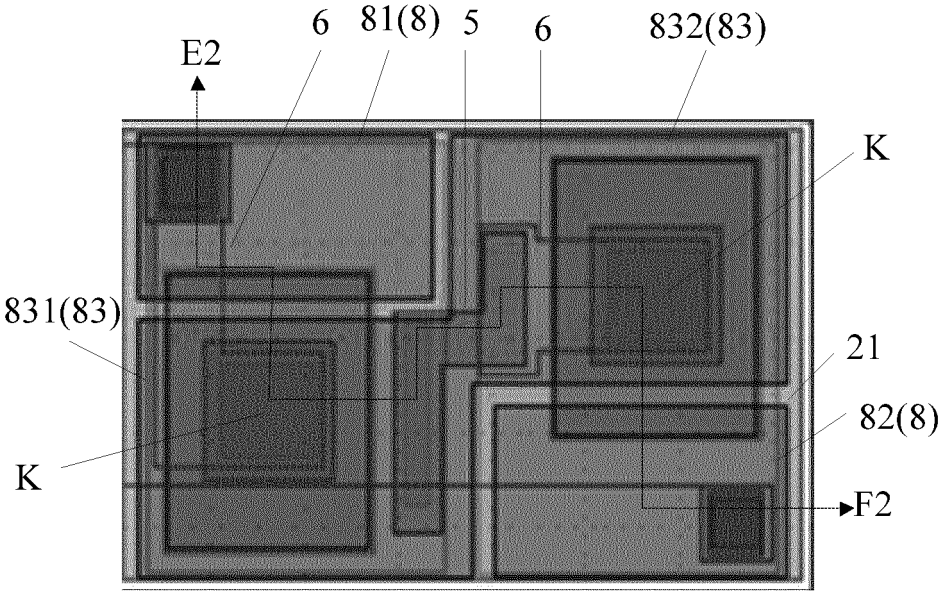

Fig. 13B

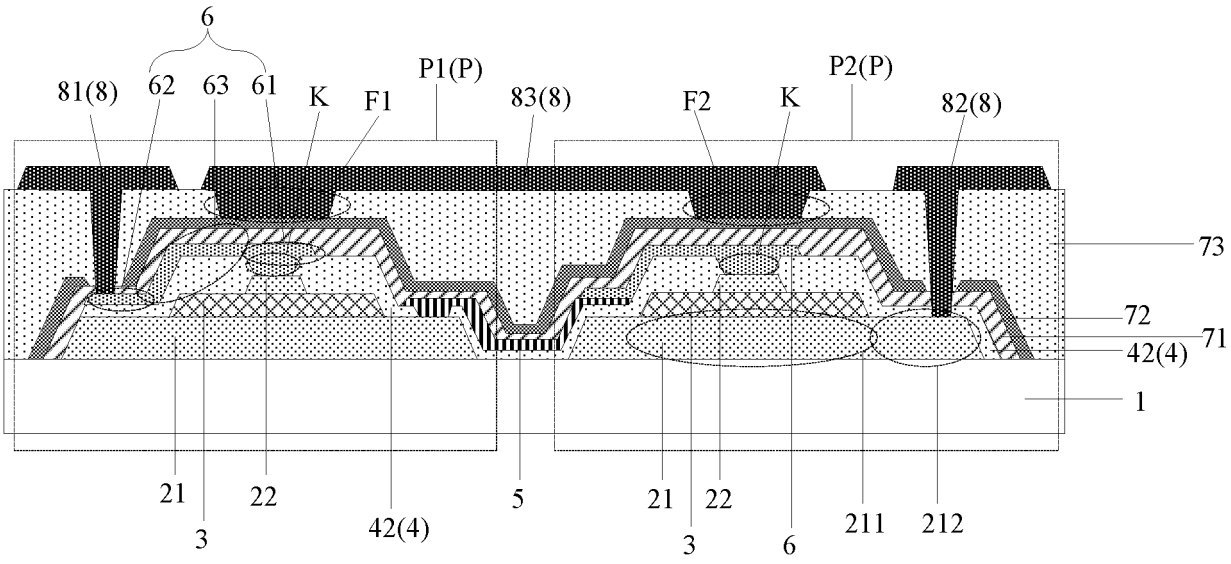

Fig. 14A

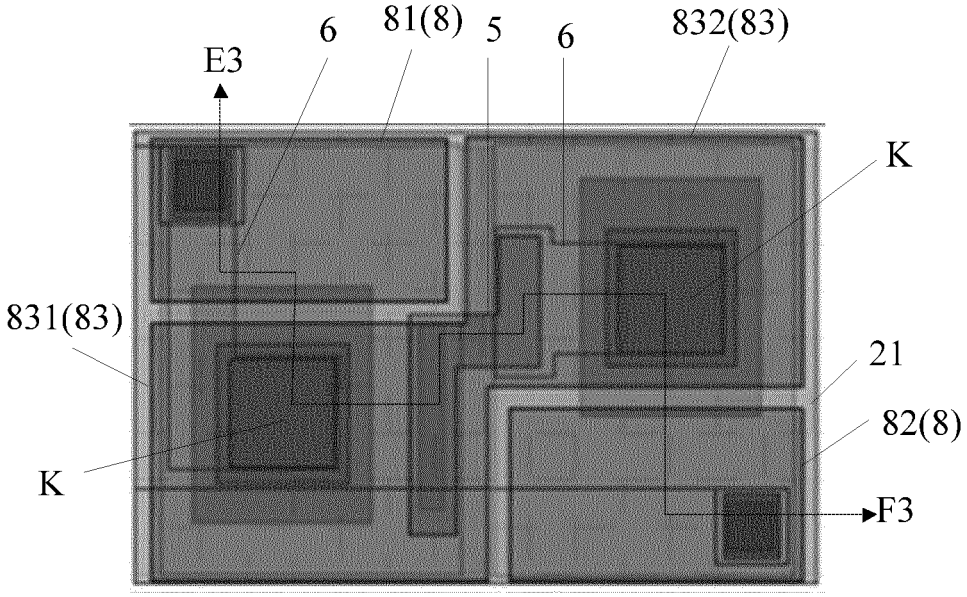

Fig. 14B

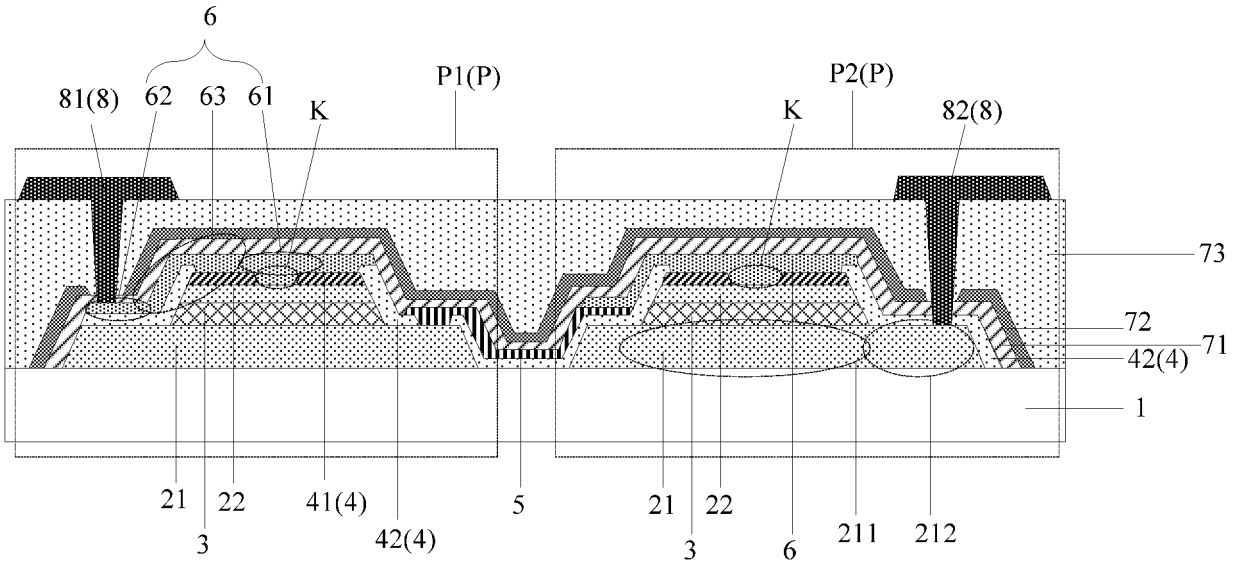

Fig. 15A

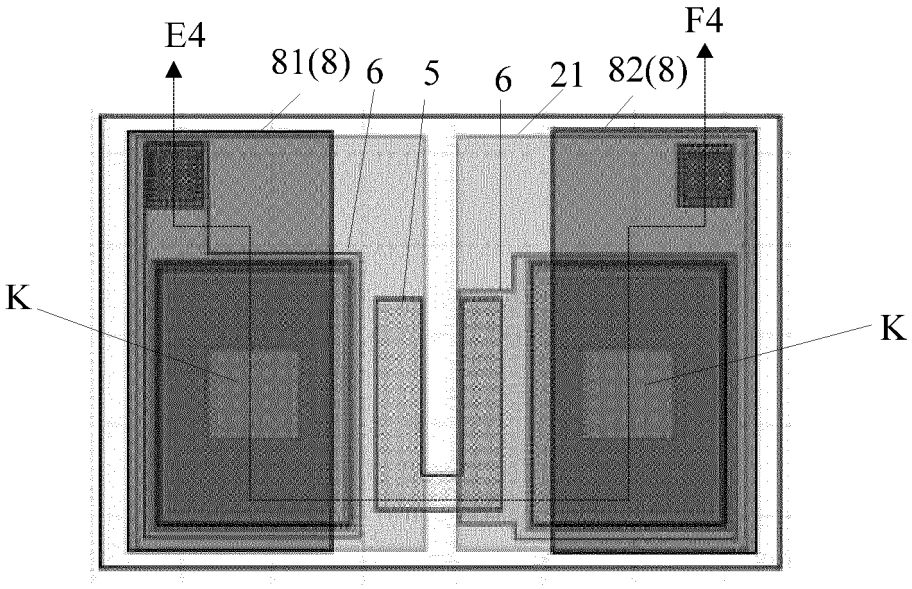

Fig. 15B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2021/125522

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/06(2010.01)i; H01L 33/14(2010.01)i; H01L 33/38(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS; CNTXT; CNKI; VEN; USTXT; WOTXT; EPTXT: 发光, 二极管, 二极体, 有效, 面积, 区域, 边缘, 边沿, 降低, 减小, 缩小, LED, area, edge, reduc+, decreas+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 113270522 A (BOE TECHNOLOGY GROUP CO., LTD.) 17 August 2021 (2021-08-17) description, paragraphs [0050]-[0095], and figures 1-11	1-3, 5-12, 18, 21-24
X	CN 106981550 A (GUANGDONG UNIVERSITY OF TECHNOLOGY) 25 July 2017 (2017-07-25) description, paragraphs [0016]-[0027], and figures 1-8	1, 3, 8-15, 17-20, 21, 23
Y	CN 106981550 A (GUANGDONG UNIVERSITY OF TECHNOLOGY) 25 July 2017 (2017-07-25) description, paragraphs [0016]-[0027], and figures 1-8	2, 5-15, 17-20, 22, 24
Y	CN 110212069 A (HC SEMITEK (ZHEJIANG) CORP.) 06 September 2019 (2019-09-06) description, paragraphs [0033]-[0081], and figures 1-6	2, 5-15, 17-20, 22, 24
X	TW 201407829 A (HELIO OPTOELECTRONICS CORP.) 16 February 2014 (2014-02-16) description, page 5, second-to-last paragraph to page 8, paragraph 1, and figure 1	1, 3, 8-12, 18, 21, 23
Y	TW 201407829 A (HELIO OPTOELECTRONICS CORP.) 16 February 2014 (2014-02-16) description, page 5, second-to-last paragraph to page 8, paragraph 1, and figure 1	2, 5-12, 18, 22, 24
A	CN 102386178 A (APT ELECTRONICS (GUANGZHOU) LIMITED) 21 March 2012 (2012-03-21) entire document	1-24

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 2022	**27 January 2022**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2021/125522

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	113270522	A	17 August 2021	None			
CN	106981550	A	25 July 2017	CN	207116465	U	16 March 2018
CN	110212069	A	06 September 2019	CN	110212069	B	10 November 2020
TW	201407829	A	16 February 2014	None			
CN	102386178	A	21 March 2012	CN	102386178	B	02 December 2015

Form PCT/ISA/210 (patent family annex) (January 2015)

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- CN 202110603573 **[0001]**