US 20180091676A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2018/0091676 A1**

SUZUKI (43) **Pub. Date: Mar. 29, 2018**

(54) **IMAGE READING APPARATUS**

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(21) Appl. No.: **15/714,143**

(22) Filed: **Sep. 25, 2017**

(30) **Foreign Application Priority Data**

Sep. 29, 2016 (JP) 2016-190810

Publication Classification

(51) **Int. Cl.**

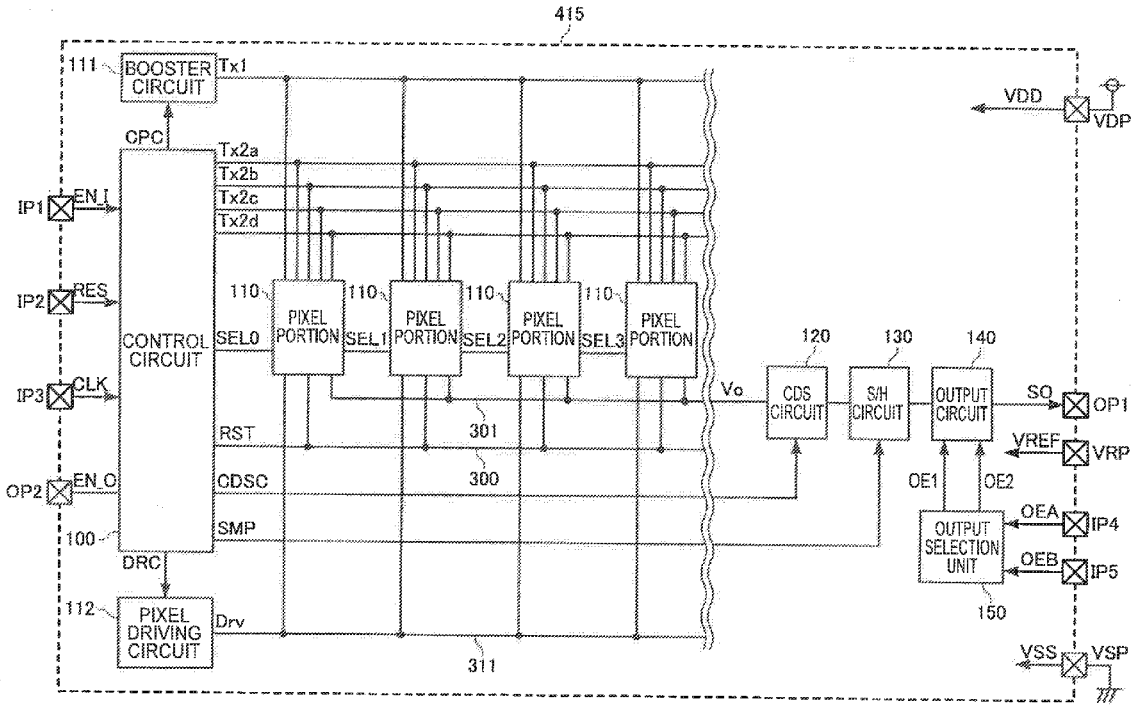
H04N 1/00	(2006.01)
H04N 1/40	(2006.01)
H04N 1/409	(2006.01)

(52) **U.S. Cl.**

CPC ***H04N 1/00904*** (2013.01); ***H04N 1/40056*** (2013.01); ***H04N 1/409*** (2013.01); *H04N 1/0306* (2013.01); *H04N 2201/0081* (2013.01); *H04N 1/00907* (2013.01); ***H04N 1/40068*** (2013.01)

(57) **ABSTRACT**

A first image reading chip for reading an image of a first surface of a medium includes a first pixel portion that outputs a first pixel signal, a first output circuit that outputs a signal based on the first pixel signal, and a first output selection unit that selects a first drive capability as a drive capability of the first output circuit, and a second image reading chip for reading an image of a second surface of a medium includes a second pixel portion that outputs a second pixel signal, a second output circuit that outputs a signal based on the second pixel signal, and a second output selection unit that selects a second drive capability as a drive capability of the second output circuit.



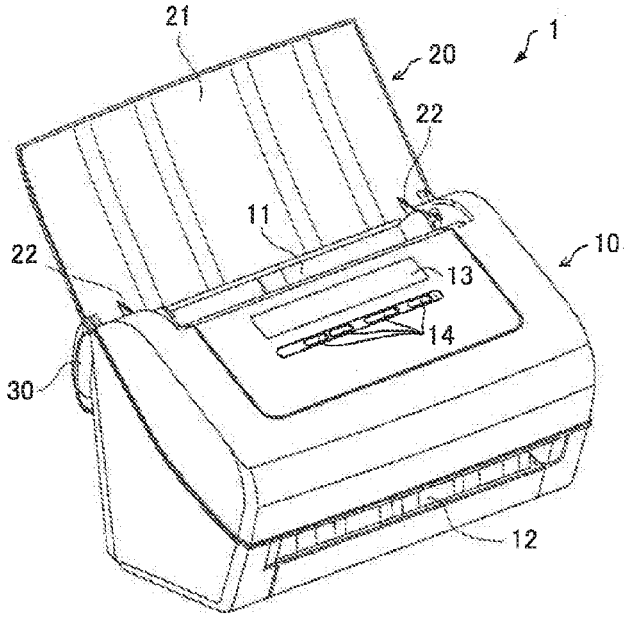

21
20
1
22
11
10
22
13
14
30
12

FIG. 1

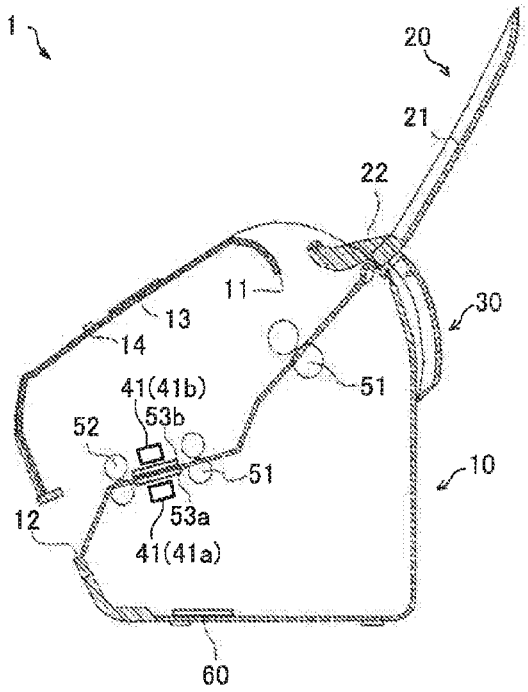

1
20
21
22
11
13
14
30
41(41b)
53b
52
51
51
10
12
53a
41(41a)
60

FIG. 2

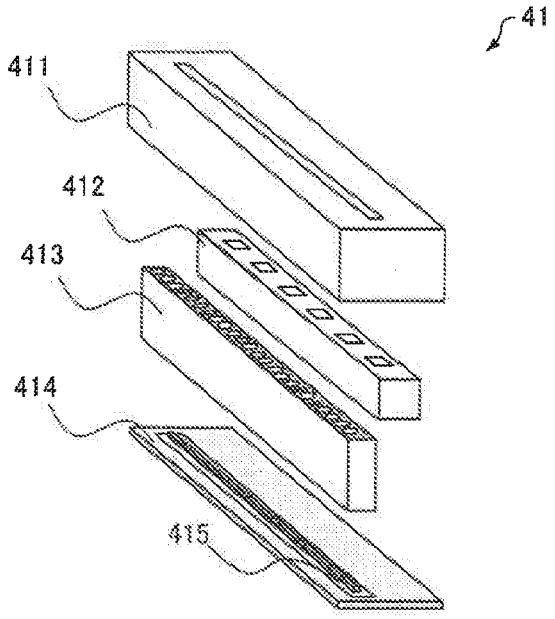


FIG. 3

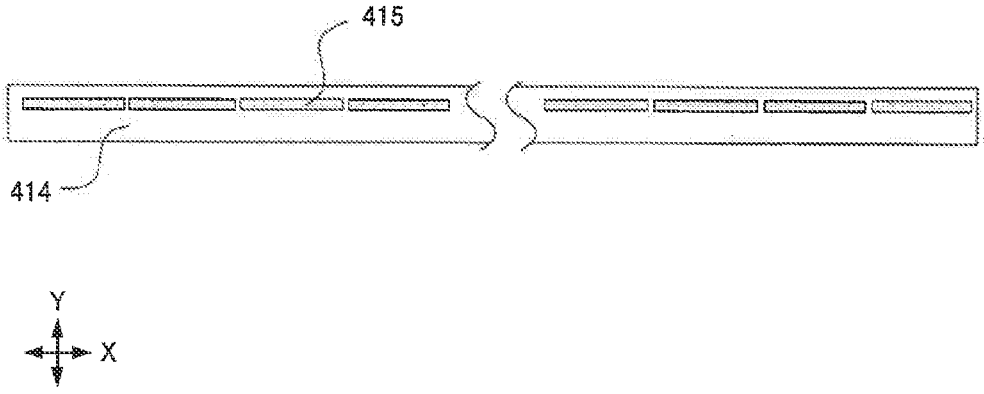


FIG. 4

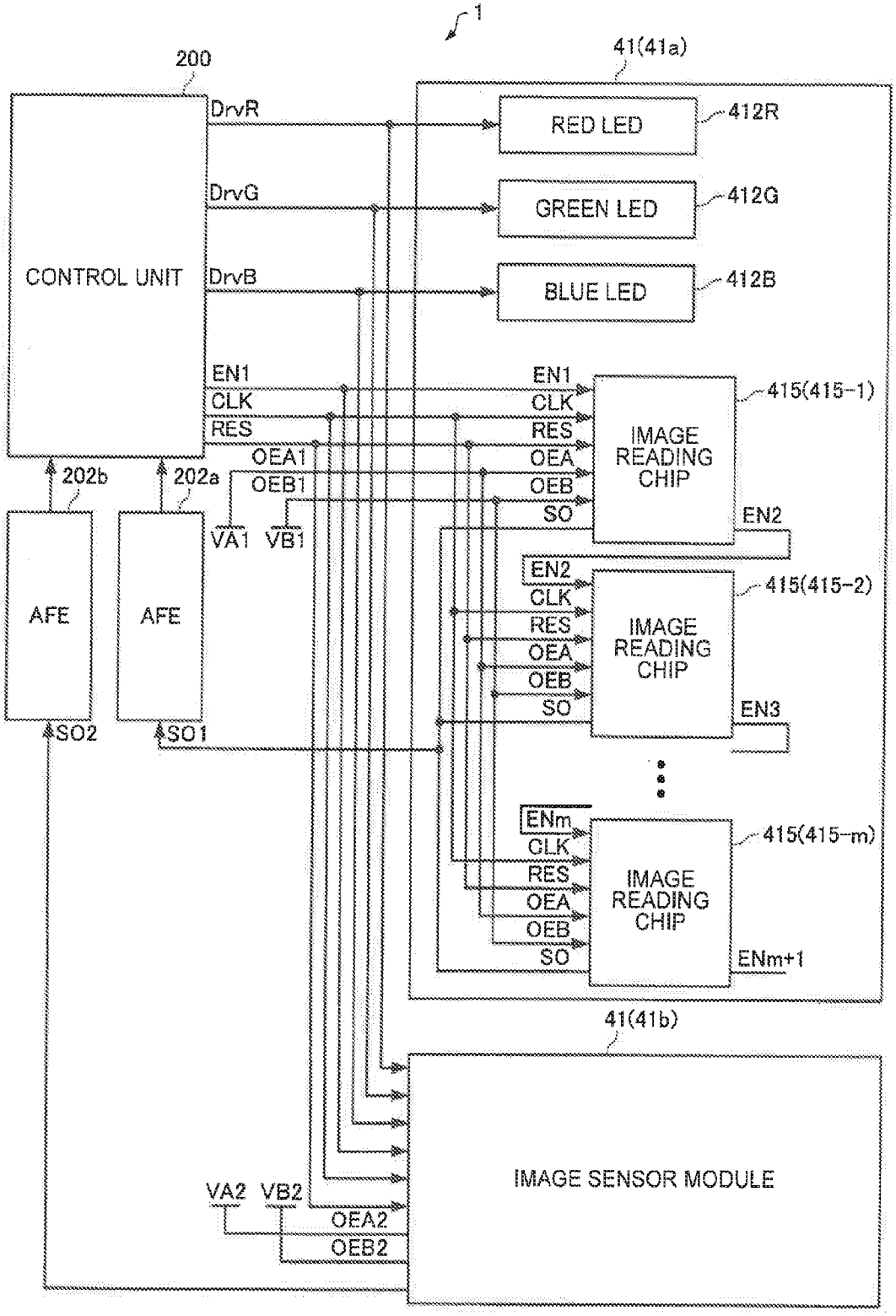

1
200
41(41a)
CONTROL UNIT
DrvR
DrvG
DrvB
RED LED
412R
GREEN LED
412G
BLUE LED
412B
EN1
CLK
RES
OEA1
OEB1
202b
202a
VA1
VB1
AFE
AFE
SO2
SO1
EN1
CLK
RES
OEA
OEB
SO
IMAGE READING CHIP
415(415-1)
EN2
EN2
CLK
RES
OEA
OEB
SO
IMAGE READING CHIP
415(415-2)
EN3
ENm
CLK
RES
OEA
OEB
SO
IMAGE READING CHIP
415(415-m)
ENm+1
41(41b)
IMAGE SENSOR MODULE
VA2
VB2
OEA2
OEB2

FIG. 5

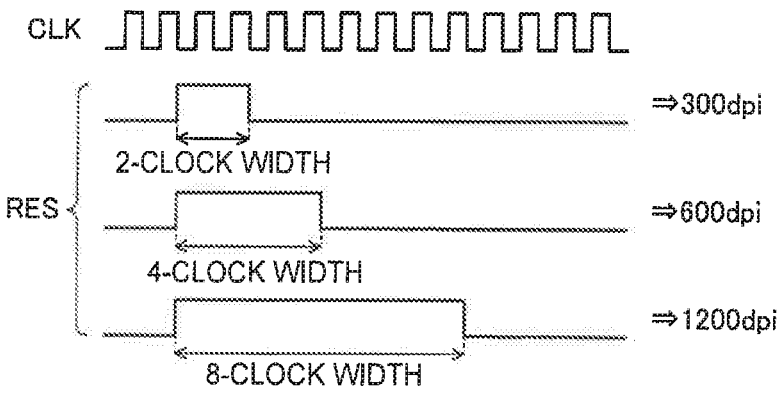

CLK
RES
⇒300dpi
2-CLOCK WIDTH
⇒600dpi
4-CLOCK WIDTH
⇒1200dpi
8-CLOCK WIDTH

FIG. 6

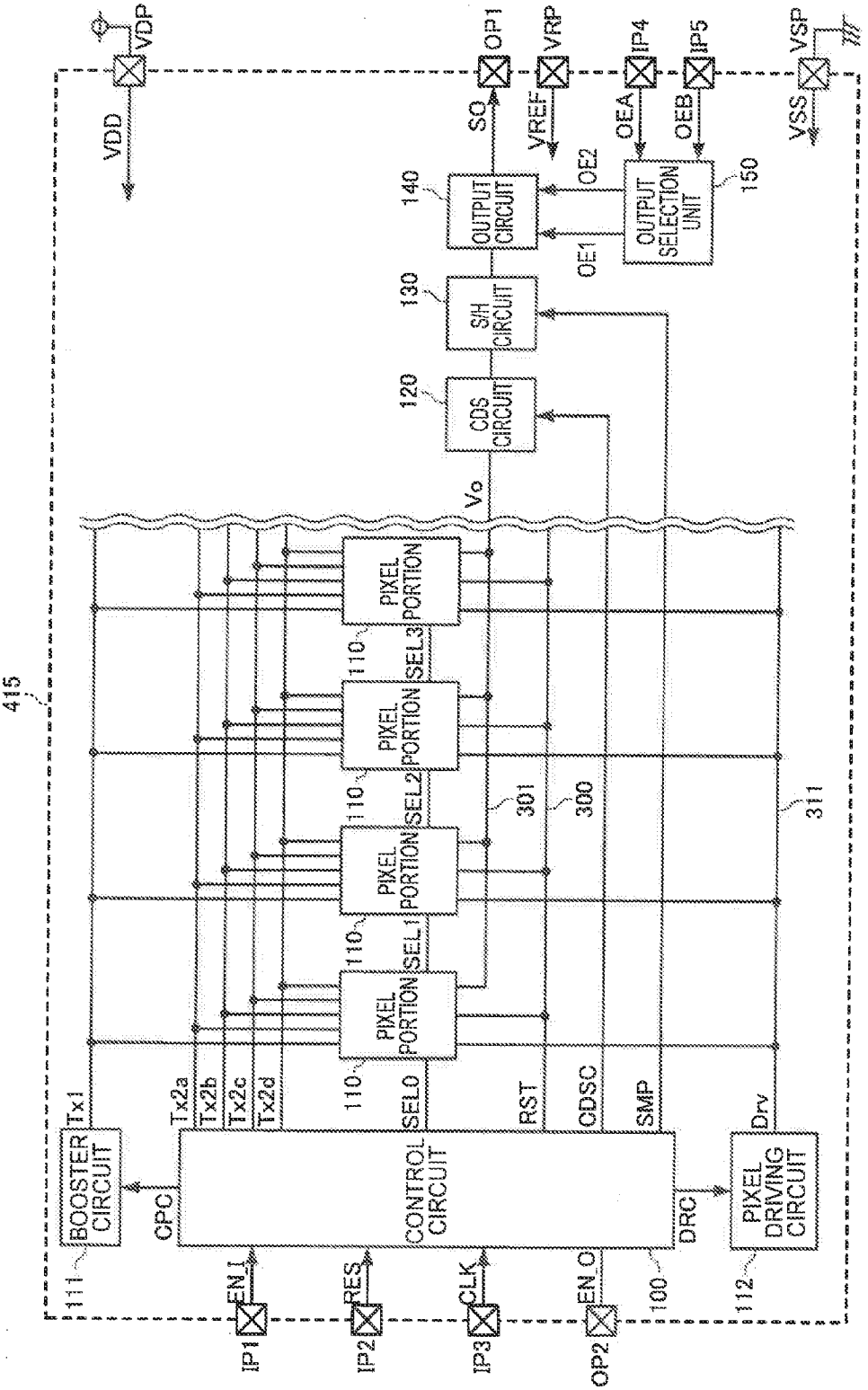

VDP
VDD
OP1
VRP
IP4
IP5
VSP
SO
VREF
OEA
OEB
VSS
OE2
OE1
140
OUTPUT CIRCUIT
OUTPUT SELECTION UNIT
150
130
S/H CIRCUIT
120
CDS CIRCUIT
Vo
PIXEL PORTION
110
SEL3
SEL2
SEL1
SEL0
301
300
311
415
Tx1
Tx2a
Tx2b
Tx2c
Tx2d
RST
CDSC
SMP
Drv
BOOSTER CIRCUIT
CPC
CONTROL CIRCUIT
DRC
PIXEL DRIVING CIRCUIT
111
112
100
EN_I
RES
CLK
EN_O
IP1
IP2
IP3
OP2

FIG. 7

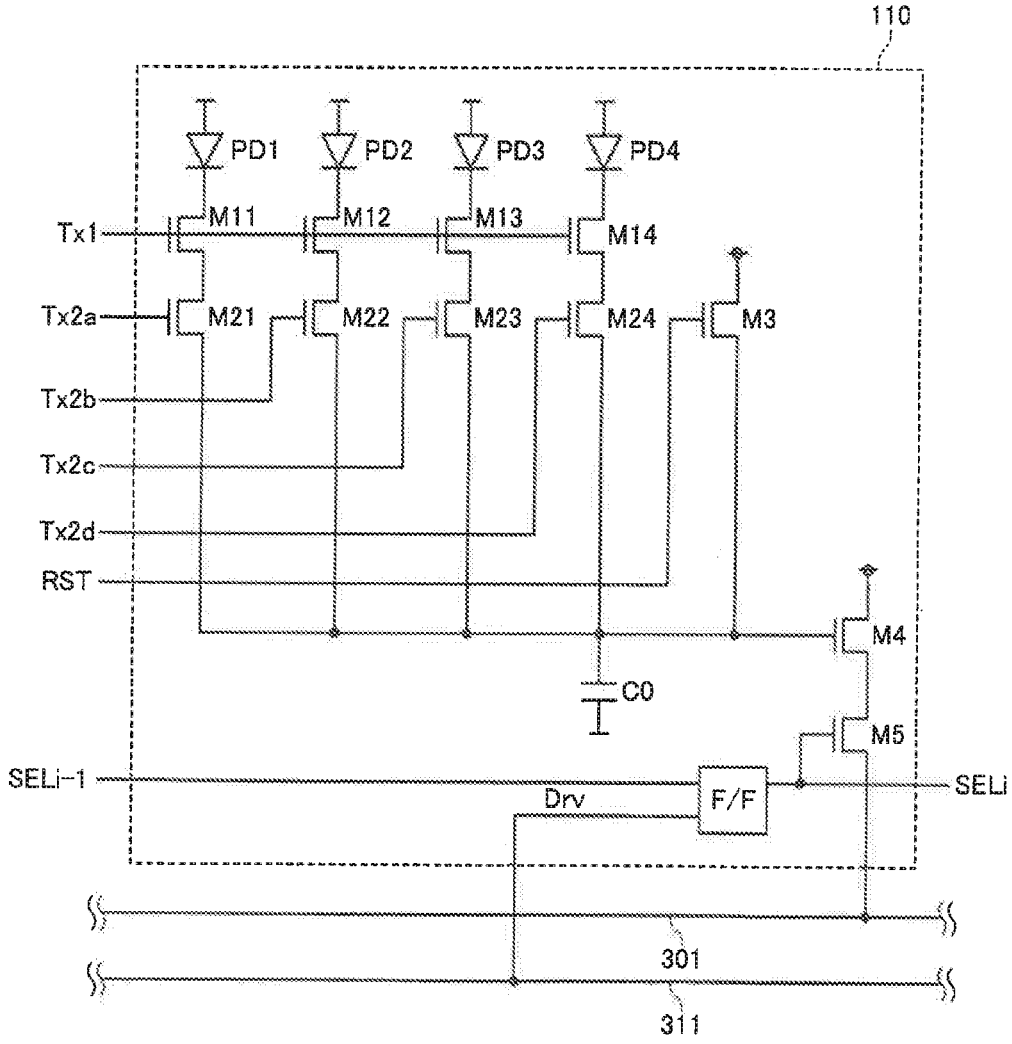

110
PD1
PD2
PD3
PD4
M11
M12
M13
M14
Tx1
Tx2a
M21
M22
M23
M24
M3
Tx2b
Tx2c
Tx2d
RST
M4
C0
M5
SELi-1
Drv
F/F
SELi
301
311

FIG. 8

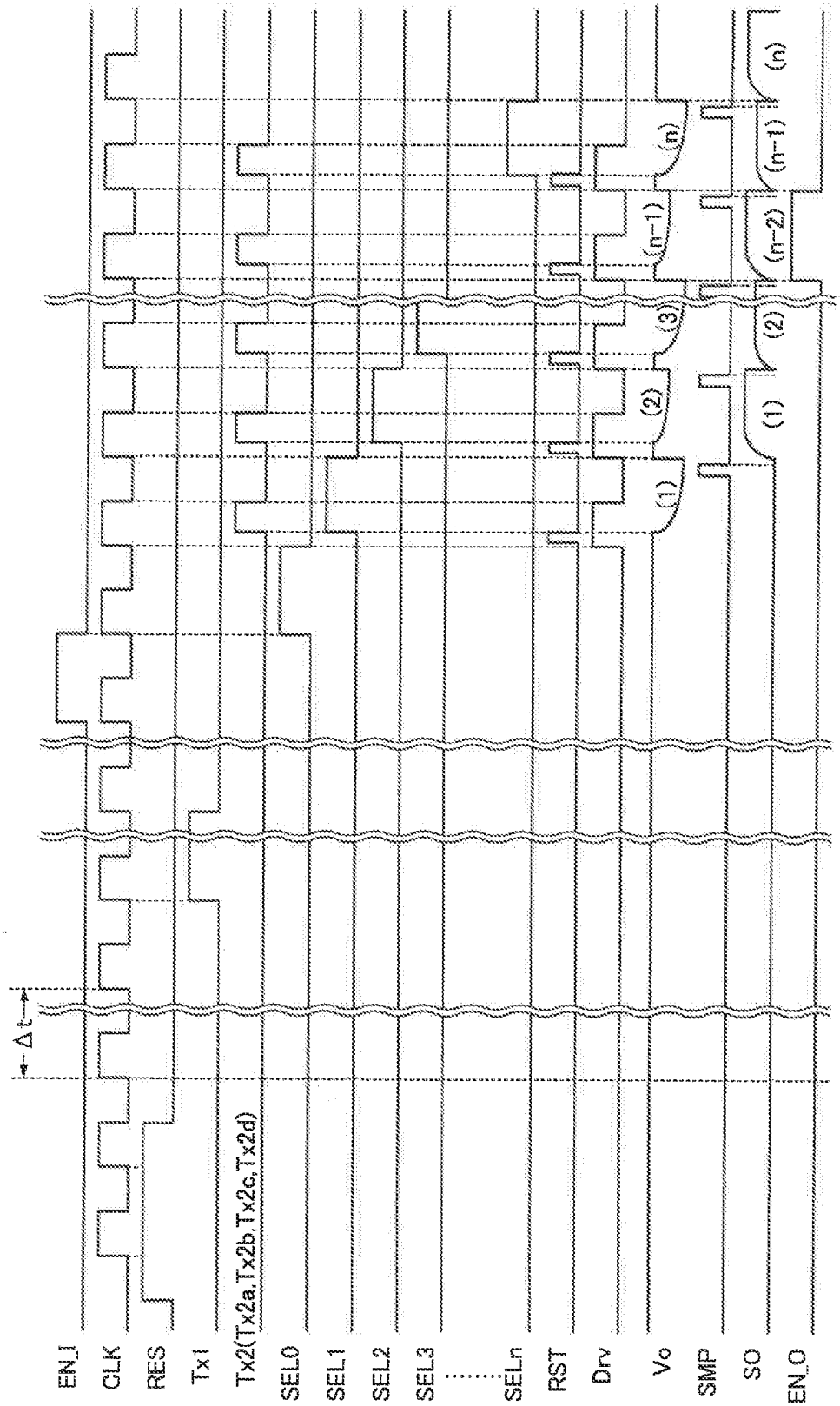

EN_I
CLK
RES
Tx1
Tx2(Tx2a,Tx2b,Tx2c,Tx2d)
SEL0
SEL1
SEL2
SEL3
SELn
RST
Drv
Vo
SMP
SO
EN_O
Δt
(1)
(2)
(3)
(n-1)
(n)
(1)
(2)
(n-2)
(n-1)
(n)

FIG. 9

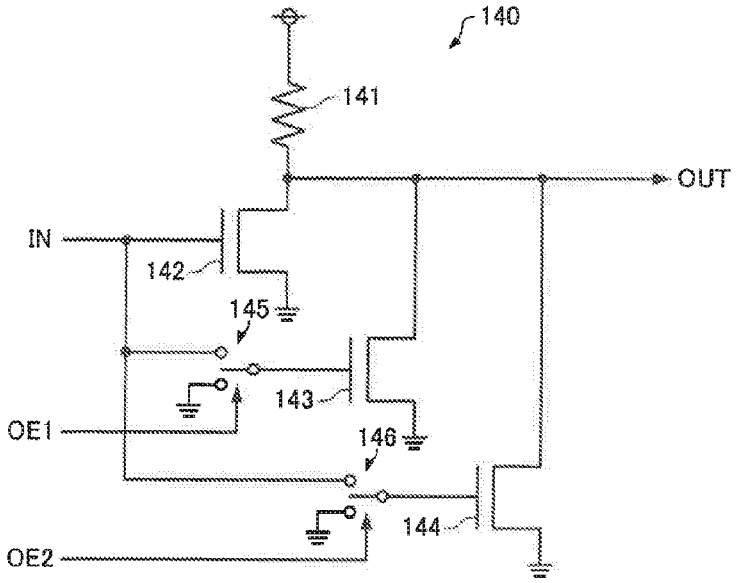

140
141
OUT
IN
142
145
143
OE1
146
144
OE2

FIG. 10

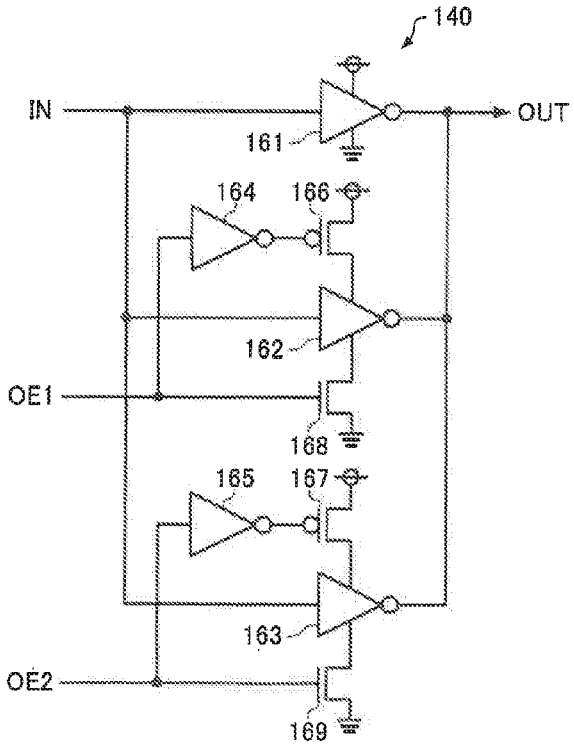

140
IN
OUT
161
164
166
162
OE1
168
165
167
163
OE2
169

FIG. 11

OEA	OEB	OE1	OE2
L	L	L	L
H	L	H	L
L	H	H	H

FIG. 12

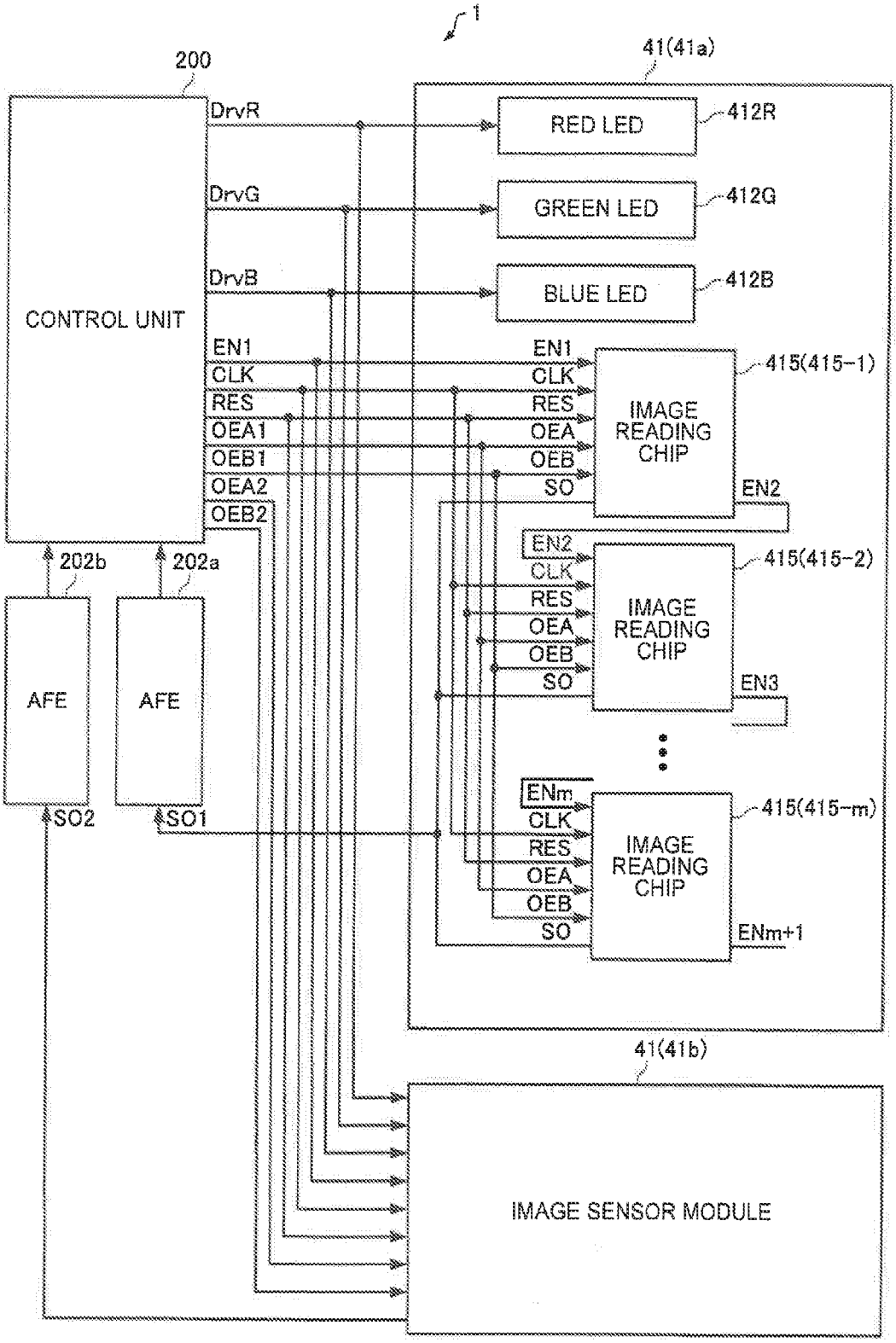

1
200
41(41a)
CONTROL UNIT
DrvR
DrvG
DrvB
RED LED
GREEN LED
BLUE LED
412R
412G
412B
EN1
CLK
RES
OEA1
OEB1
OEA2
OEB2
EN1
CLK
RES
OEA
OEB
SO
IMAGE READING CHIP
415(415-1)
EN2
EN2
CLK
RES
OEA
OEB
SO
IMAGE READING CHIP
415(415-2)
EN3
ENm
CLK
RES
OEA
OEB
SO
IMAGE READING CHIP
415(415-m)
ENm+1
202b
202a
AFE
AFE
SO2
SO1
41(41b)
IMAGE SENSOR MODULE

FIG. 13

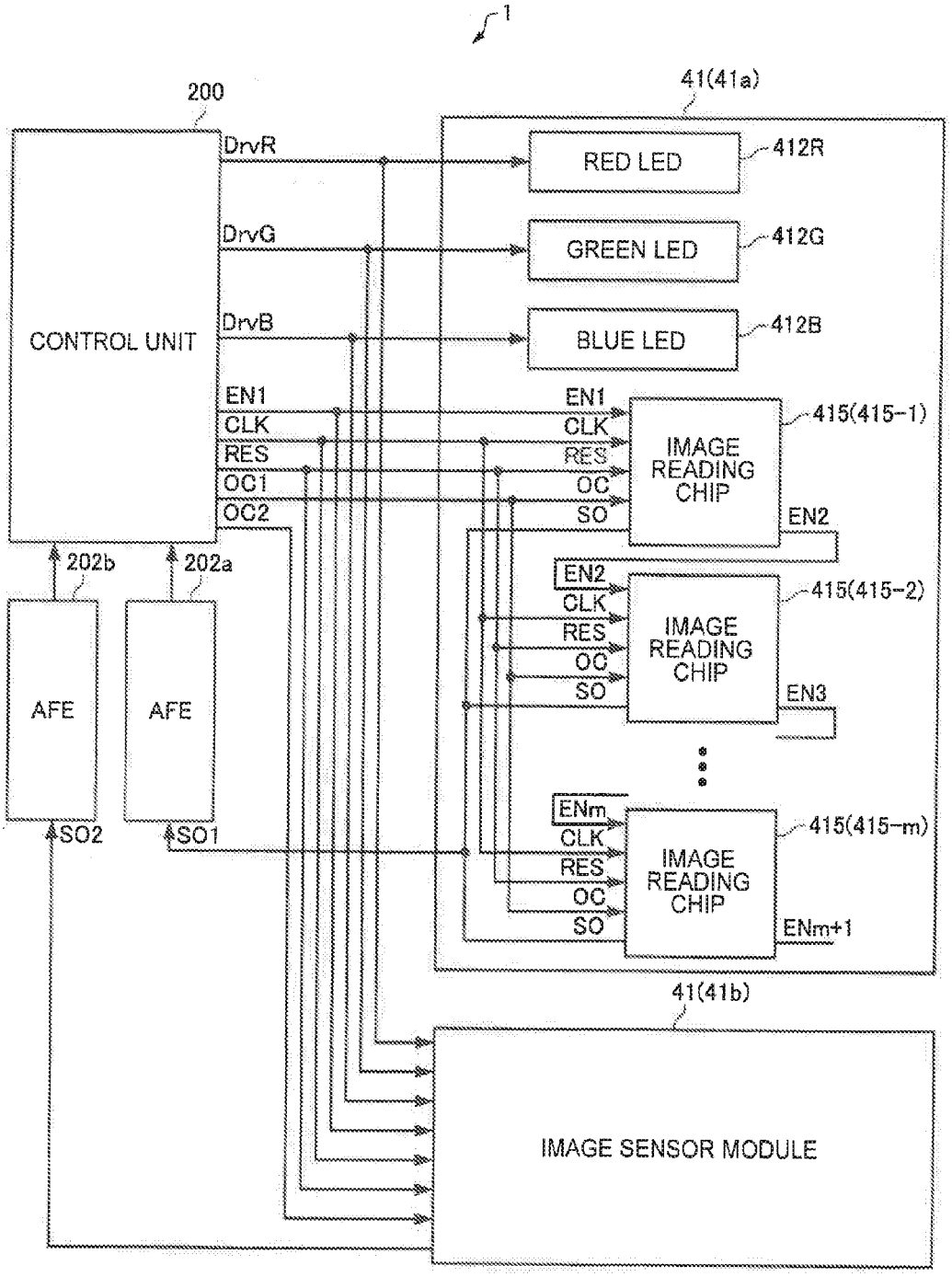

1
200
41(41a)
CONTROL UNIT
DrvR
DrvG
DrvB
EN1
CLK
RES
OC1
OC2
RED LED
412R
GREEN LED
412G
BLUE LED
412B
IMAGE READING CHIP
415(415-1)
415(415-2)
415(415-m)
EN2
EN3
ENm
ENm+1
SO
OC
202b
202a
AFE
AFE
SO2
SO1
41(41b)
IMAGE SENSOR MODULE

FIG. 14

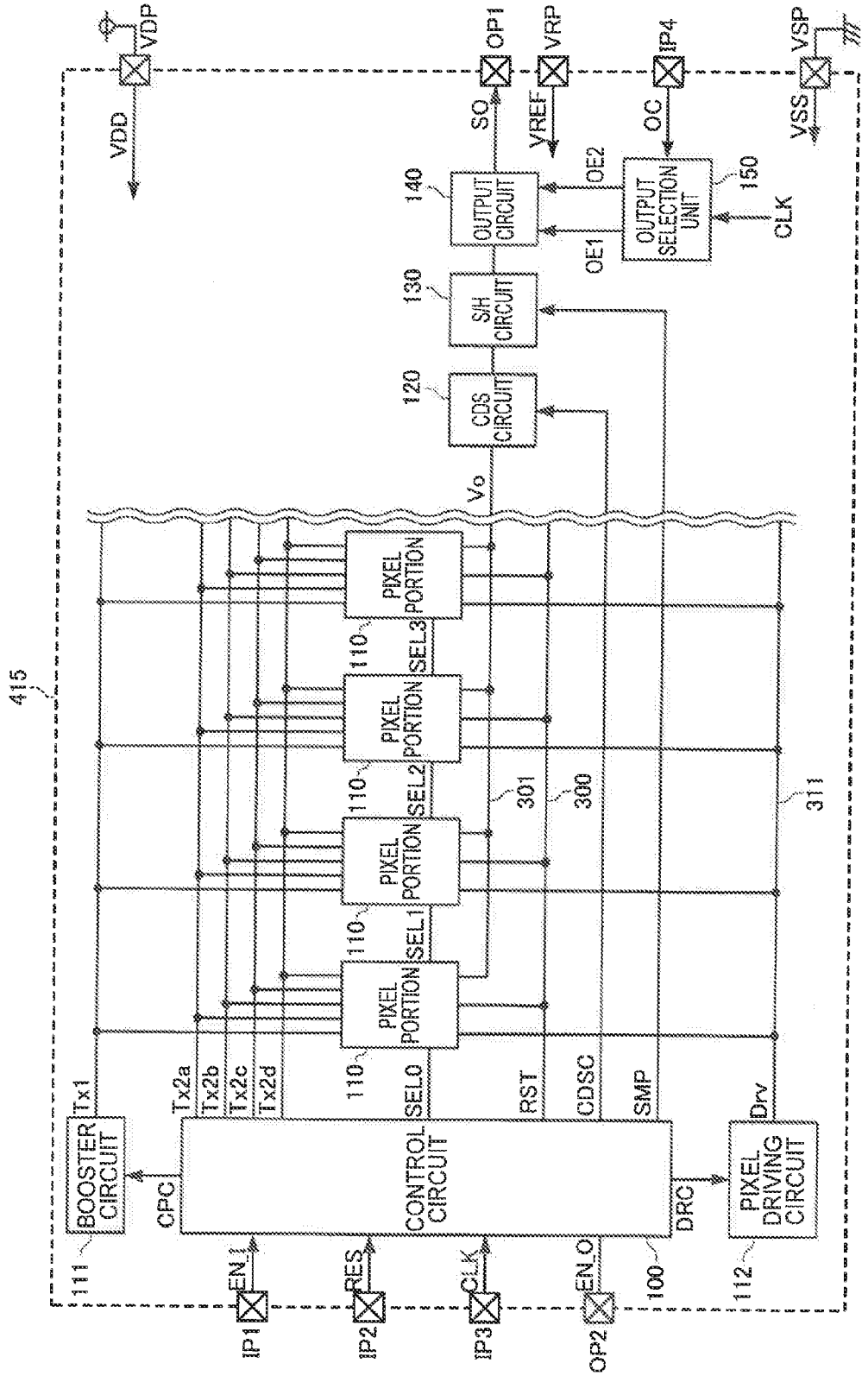

415
VDP
VDD
OP1
SO
VRP
VREF
IP4
OC
VSP
VSS
140
OUTPUT CIRCUIT
OE2
OE1
OUTPUT SELECTION UNIT
150
CLK
130
S/H CIRCUIT
120
CDS CIRCUIT
Vo
PIXEL PORTION
110
SEL3
SEL2
SEL1
SEL0
301
300
311
Tx1
Tx2a
Tx2b
Tx2c
Tx2d
RST
CDSC
SMP
Drv
BOOSTER CIRCUIT
111
CPC
CONTROL CIRCUIT
DRC
PIXEL DRIVING CIRCUIT
112
100
IP1
EN_I
IP2
RES
IP3
CLK
OP2
EN_O

FIG. 15

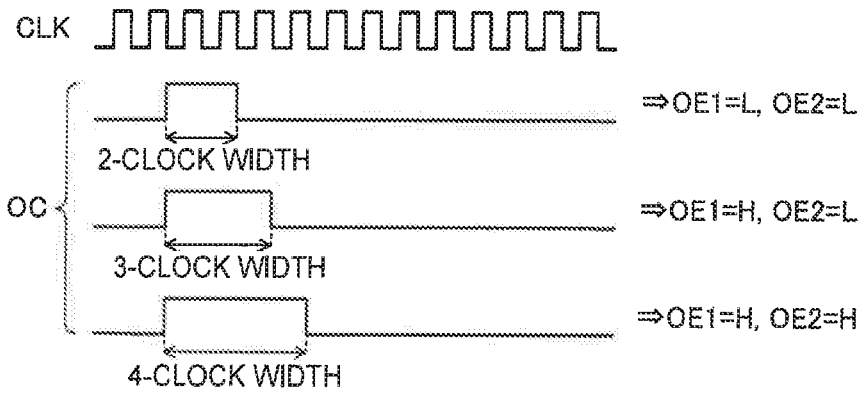

CLK
OC
2-CLOCK WIDTH
⇒OE1=L, OE2=L
3-CLOCK WIDTH
⇒OE1=H, OE2=L
4-CLOCK WIDTH
⇒OE1=H, OE2=H

FIG. 16

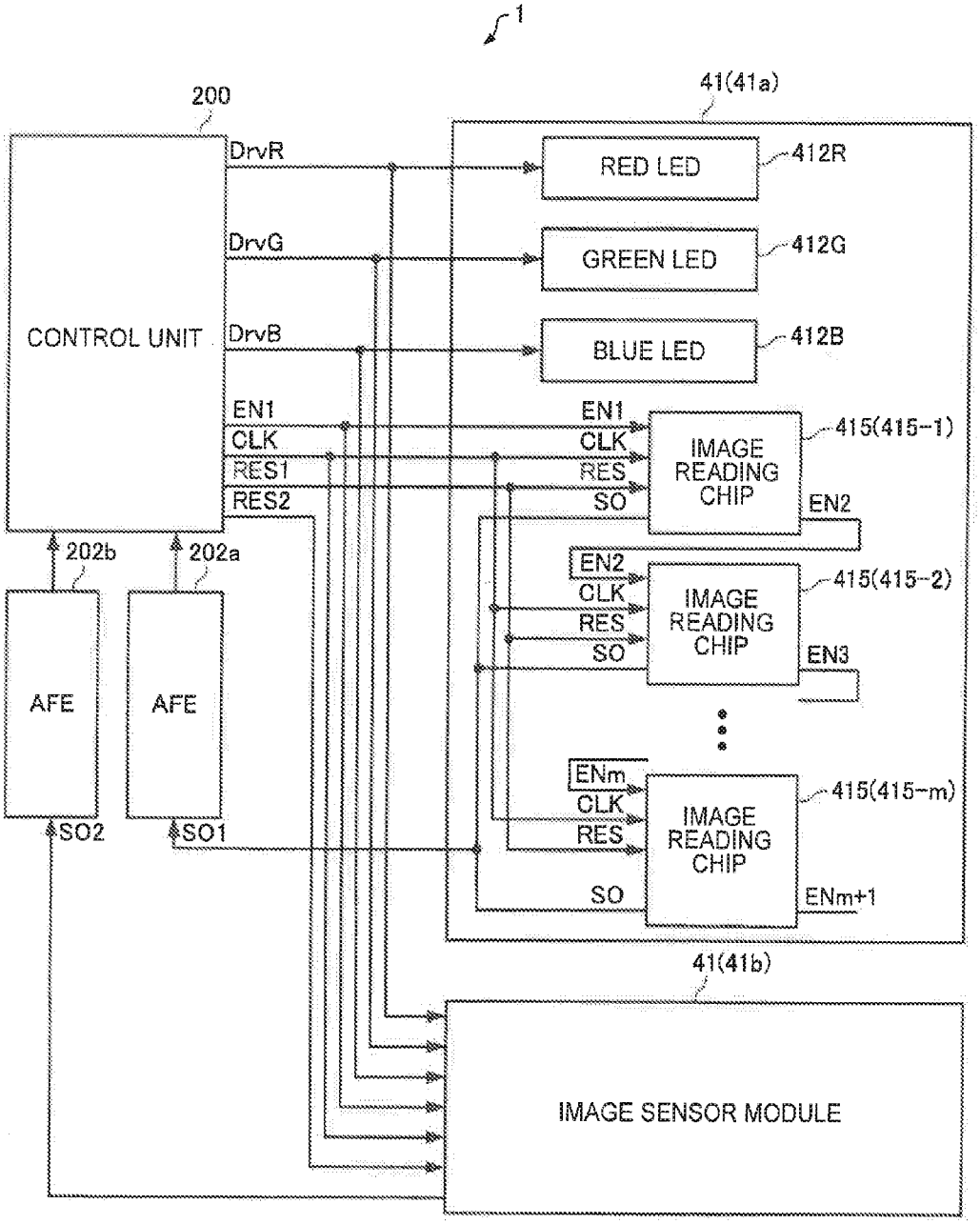

1
200
41(41a)
CONTROL UNIT
DrvR
DrvG
DrvB
EN1
CLK
RES1
RES2
RED LED
412R
GREEN LED
412G
BLUE LED
412B
EN1
CLK
RES
SO
IMAGE READING CHIP
415(415-1)
EN2
EN2
CLK
RES
SO
IMAGE READING CHIP
415(415-2)
EN3
ENm
CLK
RES
SO
IMAGE READING CHIP
415(415-m)
ENm+1
202b
202a
AFE
AFE
SO2
SO1
41(41b)
IMAGE SENSOR MODULE

FIG. 17

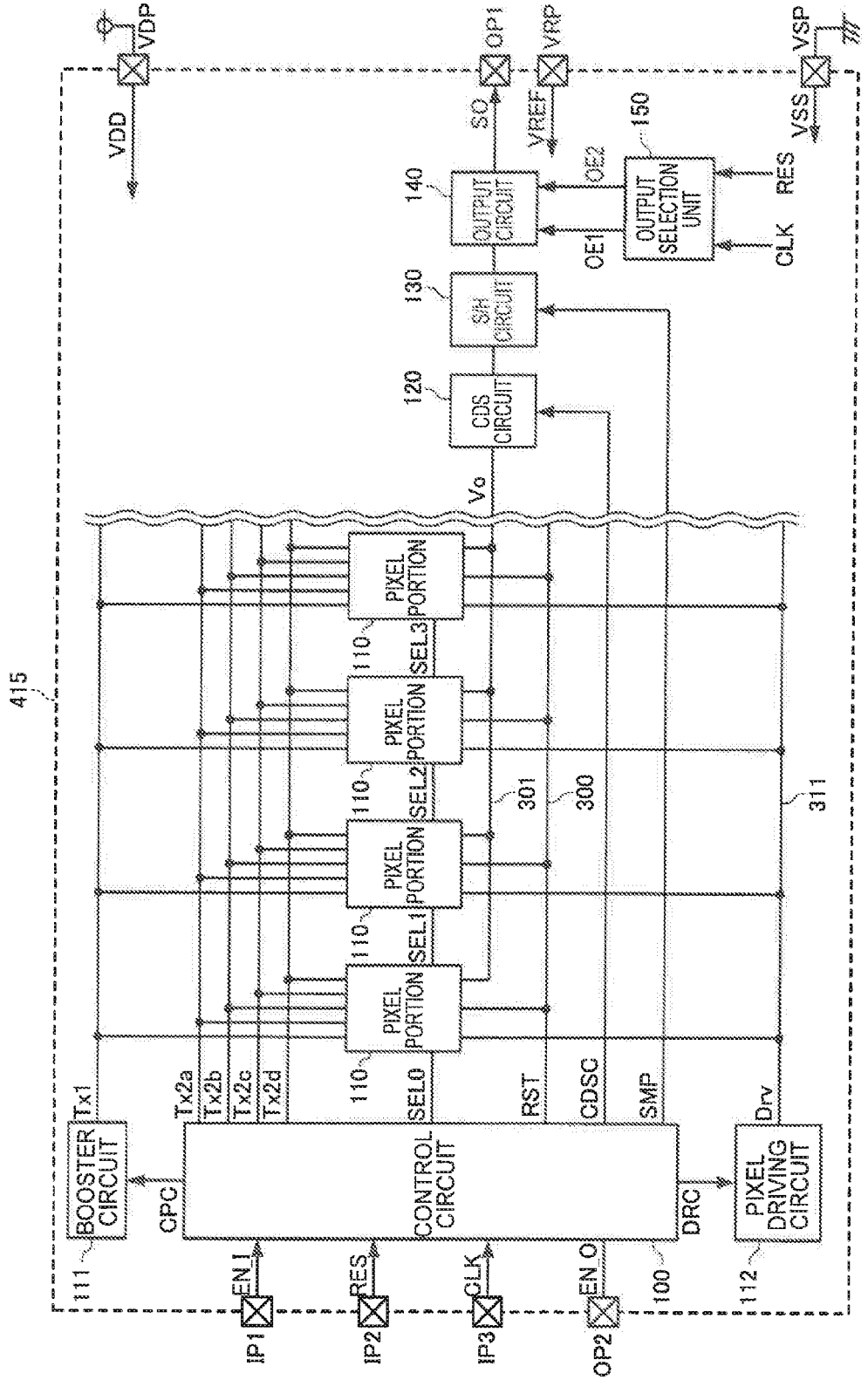

415
VDD
VDP
VSS
VSP
VRP
VREF
OP1
SO
140
OUTPUT CIRCUIT
150
OUTPUT SELECTION UNIT
OE1
OE2
CLK
RES
130
S/H CIRCUIT
120
CDS CIRCUIT
Vo
PIXEL PORTION
110
SEL3
SEL2
SEL1
SEL0
301
300
311
BOOSTER CIRCUIT
111
Tx1
Tx2a
Tx2b
Tx2c
Tx2d
CPC
CONTROL CIRCUIT
RST
CDSC
SMP
DRC
100
PIXEL DRIVING CIRCUIT
112
Drv
IP1
EN_I
IP2
RES
IP3
CLK
OP2
EN_O

FIG. 18

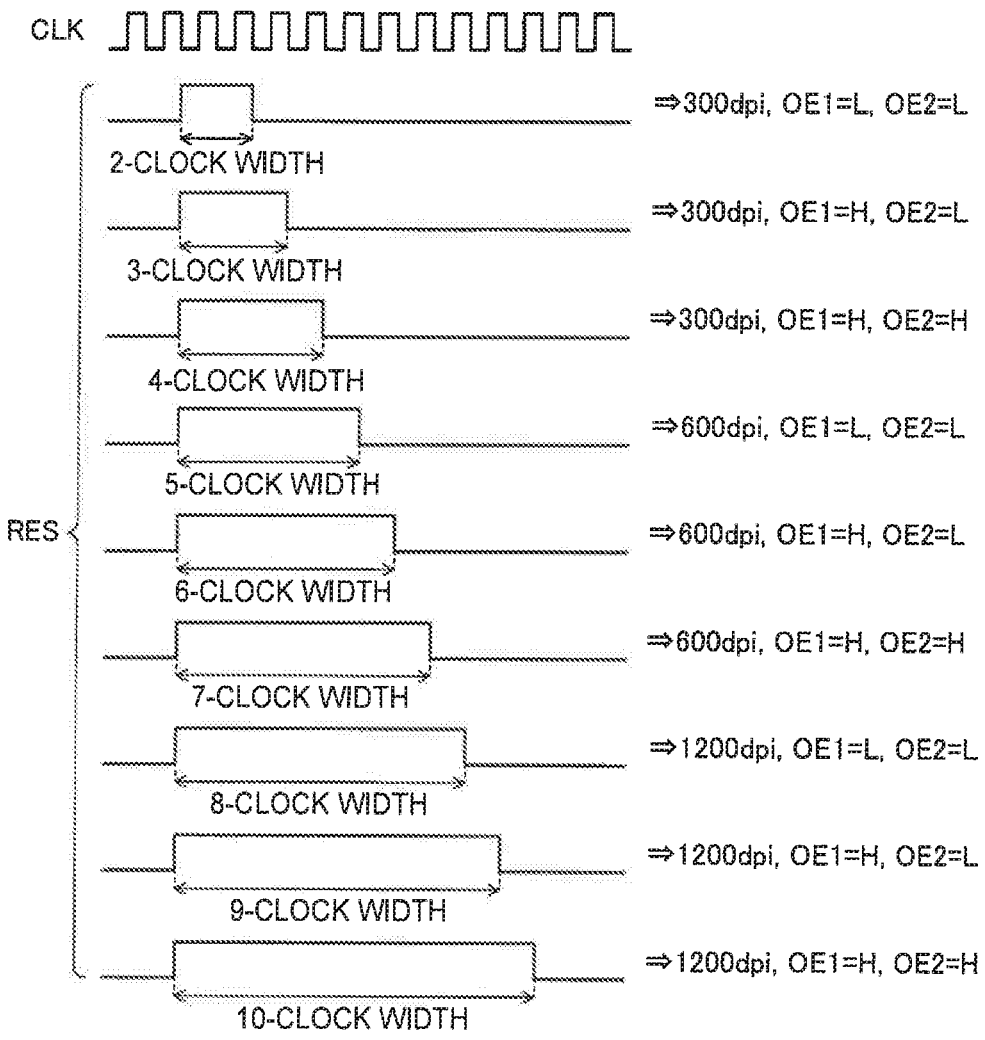

CLK
RES
2-CLOCK WIDTH
⇒300dpi, OE1=L, OE2=L
3-CLOCK WIDTH
⇒300dpi, OE1=H, OE2=L
4-CLOCK WIDTH
⇒300dpi, OE1=H, OE2=H
5-CLOCK WIDTH
⇒600dpi, OE1=L, OE2=L
6-CLOCK WIDTH
⇒600dpi, OE1=H, OE2=L
7-CLOCK WIDTH
⇒600dpi, OE1=H, OE2=H
8-CLOCK WIDTH
⇒1200dpi, OE1=L, OE2=L
9-CLOCK WIDTH
⇒1200dpi, OE1=H, OE2=L
10-CLOCK WIDTH
⇒1200dpi, OE1=H, OE2=H

FIG. 19

IMAGE READING APPARATUS

BACKGROUND

1. Technical Field

[0001] The present invention relates to an image reading apparatus.

2. Related Art

[0002] JP-A-2006-314039 discloses an image reading apparatus (scanner) that reads an original image using an image sensor, converts the image signal obtained by reading into digital image data using an analog front end (AFE), and outputs the converted digital image data to a digital processing unit or a data transfer unit.

[0003] JP-A-2006-314039 is an example of related art.

[0004] Since various types of scanners such as sheet-feeding and flat-feeding scanners exist and the arrangement of the image sensor and the analog front end (AFE) differs according to the type of the scanner, the length of a wire by which the image signal output from the image sensor is transferred (load capacity of image signal) differs for each scanner. For this reason, heretofore, a general-purpose image sensor that can be applied to various types of scanners has high drive capability, which is needed to drive an envisioned maximum load.

[0005] However, since the driving load of the image sensor is relatively small depending on the arrangement relationship of the image sensor and the analog front end (AFE), there are also cases where the drive capability of the image sensor is excessive, and thus there has been a risk that excessive power consumption will occur, and excessive noise accompanying signal transfer will occur.

SUMMARY

[0006] According to several aspects of the invention, it is possible to provide an image reading apparatus according to which it is possible to suppress the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

[0007] The invention was made to solve at least a portion of the foregoing problems, and can be realized as the following aspects or application examples.

APPLICATION EXAMPLE 1

[0008] An image reading apparatus according to the present application example includes: a first image reading chip for reading an image formed on a first surface of a medium; and a second image reading chip for reading an image formed on a second surface that is different from the first surface of the medium, wherein the first image reading chip includes: a first pixel portion that is configured to output a first pixel signal and includes a first light-receiving element that receives and photoelectrically converts light from the image formed on the first surface; a first output circuit that can output an image signal based on the first pixel signal with one of a plurality of drive capabilities including a first drive capability; and a first output selection unit configured to select the drive capability of the first output circuit from among the plurality of drive capabilities, the second image reading chip includes: a second pixel portion that is configured to output a second pixel signal and includes a second light-receiving element that receives and photoelectrically converts light from the image formed on the second surface; a second output circuit that can output a signal based on the second pixel signal with one of a plurality of drive capabilities including a second drive capability that is different from the first drive capability; and a second output selection unit configured to select the drive capability of the second output circuit from among the plurality of drive capabilities, the first output selection unit selects the first drive capability, and the second output selection unit selects the second drive capability.

[0009] With the image reading apparatus according to the present application example, in the first image reading chip that reads the image formed on the first surface of the medium, the drive capability of the first output circuit is set to the first drive capability such that the drive capability matches the size of the load of the transfer wire for the output signals and does not become excessive, and in the second image reading chip that reads the image formed on the second surface of the medium, the drive capability of the second output circuit is set to the second drive capability, which is different from the first drive capability, such that drive capability matches the load of the transfer wire for the output signals and does not become excessive. Accordingly, with the image reading apparatus according to the present application example, it is possible to read the images formed on both sides of the medium while suppressing the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

APPLICATION EXAMPLE 2

[0010] The image reading apparatus according to the above-described application example may include: a control substrate; a first wire that electrically connects the first image reading chip and the control substrate; and a second wire that electrically connects the second image reading chip and the control substrate and is longer than the first wire, a signal that is based on the first pixel signal output from the first output circuit may be transferred to the control substrate by being transmitted through the first wire, a signal that is based on the second pixel signal output from the second output circuit may be transferred to the control substrate by being transmitted through the second wire, and the second drive capability may be larger than the first drive capability.

[0011] With the image reading apparatus according to the present application example, the second wire, which electrically connects the second image reading chip and the control substrate, is longer than the first wire, which electrically connects the first image reading chip and the control substrate, and therefore the load of the second wire is larger than the load of the first wire. For this reason, with the image reading apparatus according to the present application example, in the first image reading chip, the drive capability of the first output circuit is set to the first drive capability such that the drive capability matches the size of the load (a relatively small load) of the transfer wire for the output signals and does not become excessive, and in the second image reading chip, the drive capability of the second output circuit is set to the second drive capability, which is greater than the first drive capability, such that the drive capability matches the size of the load (a relatively large load) of the transfer wire for the output signals and does not become excessive. Accordingly, with the image reading apparatus according to the present application example, it is possible

to suppress the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

APPLICATION EXAMPLE 3

[0012] With the image reading apparatus according to the above-described application example, the first image reading chip may include a first terminal, the first output selection unit selects the drive capability of the first output circuit based on a signal input to the first terminal, the second image reading chip may include a second terminal, and the second output selection unit may select the drive capability of the second output circuit based on a signal input to the second terminal.

[0013] With the image reading apparatus according to the present application example, in the first image reading chip, the drive capability of the first output circuit can be set appropriately based on the signal input to the first terminal, and in the second image reading chip, the drive capability of the second output circuit can be set appropriately based on the signal input to the second terminal, and therefore it is possible to suppress the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

APPLICATION EXAMPLE 4

[0014] The image reading apparatus according to the above-described application example may include a control unit configured to control operation of the first image reading chip and the second image reading chip, and at least one of the signal input to the first terminal and the signal input to the second terminal may be transferred from the control unit.

[0015] With the image reading apparatus according to the present application example, if the drive capability of the first output circuit of the first image reading chip is selected based on the signal transferred from the control unit, after the image reading apparatus is assembled, the drive capability of the first output circuit can be changed according to a change in the load of the output signal from the first image reading chip, and it is possible to effectively suppress the occurrence of excessive power consumption and excessive noise accompanying signal transfer. Also, with the image reading apparatus according to the present application example, if the drive capability of the second output circuit of the second image reading chip is selected based on the signal transferred from the control unit, after the image reading apparatus is assembled, the drive capability of the second output circuit can be changed according to a change in the load of the output signal from the second image reading chip, and it is possible to efficiently suppress the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

APPLICATION EXAMPLE 5

[0016] With the image reading apparatus according to the above-described application example, at least one of the signal input to the first terminal and the signal input to the second terminal may be a signal for setting the drive capability and for setting a resolution for reading the image.

[0017] With the image reading apparatus according to the present application example, for example, a signal for setting the drive capability of the first output circuit of the first image reading chip can be used as a signal for setting the resolution for image reading performed by the first image reading chip, and therefore a dedicated terminal to which the signal for setting the drive capability of the first output circuit is supplied is not needed in the first image reading chip. Also, with the image reading apparatus according to the present application example, for example, a signal for setting the drive capability of the second output circuit of the second image reading chip can also be used as a signal for setting the resolution for image reading performed by the second image reading chip, and therefore a dedicated terminal to which the signal for setting the drive capability of the second output circuit is supplied is not needed in the second image reading chip.

APPLICATION EXAMPLE 6

[0018] With the image reading apparatus according to the above-described application example, at least one of the first terminal and the second terminal may be electrically connected to a voltage source that outputs a fixed voltage.

[0019] With the image reading apparatus according to the present application example, during assembly, the drive capability of the first output circuit of the first image reading chip can be easily set by connecting the first terminal of the first image reading chip to a predetermined voltage source. Also, with the image reading apparatus according to the present application example, during assembly, the drive capability of the second output circuit of the second image reading chip can be easily set by connecting the second terminal of the second image reading chip to a predetermined voltage source.

APPLICATION EXAMPLE 7

[0020] With the image reading apparatus according to the above-described application example, the first drive capability may be the smallest among the plurality of drive capabilities of the first output circuit.

[0021] With the image reading apparatus according to the present application example, the first output circuit of the first image reading chip is set to the smallest drive capability, and therefore it is possible to reduce the power consumption and the noise that accompanies the transfer of output signals from the first image reading chip.

APPLICATION EXAMPLE 8

[0022] With the image reading apparatus according to the above-described application example, the first image reading chip and the second image reading chip may be chips of the same type.

[0023] With the image reading apparatus according to the above-described application example, the characteristics of the first image reading chip and the characteristics of the second image reading chip are similar, and therefore variation in the image reading precision (quality) can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The invention will be described with reference to the accompanying drawings, wherein like numbers reference like elements.

[0025] FIG. **1** is a perspective view illustrating an exterior of a scanner according to a first embodiment.

[0026] FIG. **2** is a diagram illustrating a cross-section of the scanner according to the first embodiment.

[0027] FIG. **3** is an exploded perspective view schematically showing a configuration of an image sensor module.
[0028] FIG. **4** is a plan view schematically showing an arrangement of image reading chips.
[0029] FIG. **5** is a diagram illustrating an example of a functional configuration of the scanner according to the first embodiment.
[0030] FIG. **6** is a diagram showing an example of a resolution setting signal.
[0031] FIG. **7** is a functional block diagram of an image reading chip.
[0032] FIG. **8** is a diagram showing a configuration of a pixel portion.
[0033] FIG. **9** is a diagram showing a timing chart for signals of an image reading chip.
[0034] FIG. **10** is a diagram showing an example of a configuration of an output circuit.
[0035] FIG. **11** is a diagram showing another example of a configuration of an output circuit.
[0036] FIG. **12** is a diagram showing an example of a truth-value table for decoding logic used by an output selection unit.
[0037] FIG. **13** is a diagram showing an example of a functional configuration of a scanner according to a second embodiment.
[0038] FIG. **14** is a diagram showing an example of a functional configuration of a scanner according to a third embodiment.
[0039] FIG. **15** is a functional block diagram of an image reading chip according to the third embodiment.
[0040] FIG. **16** is a diagram showing an example of a correspondence relationship between a pattern of an output control signal and a drive capability selection signal.
[0041] FIG. **17** is a diagram showing an example of a functional configuration of a scanner according to a fourth embodiment.
[0042] FIG. **18** is a functional block diagram of an image reading chip according to the fourth embodiment.
[0043] FIG. **19** is a diagram showing an example of a resolution setting signal according to the fourth embodiment.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0044] Hereinafter, preferred embodiments of the invention will be described in detail with reference to the drawings. The drawings are used for the sake of convenience in the description. Note that the embodiments described hereinafter are not to be unduly limited to the content of the present invention disclosed in the scope of the claims. Also, all configurations described hereinafter are not necessarily essential constituent components of the present invention.
[0045] Hereinafter, a scanner **1**, which is an example of an image reading apparatus of the invention, will be described with reference to the accompanying drawings.

1. First Embodiment

[0046] 1-1. Structure of Scanner
[0047] FIG. **1** is a perspective view illustrating an exterior of the scanner **1** (image reading apparatus) according to the first embodiment. The scanner **1** of the first embodiment is an image reading scanner that optically reads an object to be read and outputs image data.
[0048] As shown in FIG. **1**, the scanner **1** includes a case **10**, a front cover plate **20**, and a rear cover plate **30**.
[0049] The front cover plate **20** includes a plate-shaped portion **21** that is formed into an approximately rectangular shape, and leg portions **22**, and an original document (an example of a "medium") to be introduced into an introduction port is supported on the plate-shaped portion **21**.
[0050] The case **10** has an approximate box shape and stores various later-described apparatuses in its interior. The case **10** includes a sheet supply port **11**, a sheet discharge port **12**, a display panel **13**, and operation switches **14**. The sheet supply port **11** is arranged on the upper side of the case **10**, and an original document on the plate-shaped portion **21** of the front cover plate **20** is introduced into the sheet supply port **11** between the leg portions **22**. The sheet discharge port **12** discharges an original document that was introduced through the sheet supply port **11** and had an image thereof read by an internal apparatus. The display panel **13** is arranged on the upper side of the case **10** and displays the operation state of the scanner **1**, in addition to the reading precision, reading range, and the like. The operation switches **14** enable input of operations, reading precision, and the like of the scanner **1**.
[0051] The rear cover plate **30** is arranged on the rear side of the front cover plate **20** and is provided so as to cover the sheet supply port **11** when the front cover plate **20** is closed.
[0052] FIG. **2** is a diagram illustrating a cross section of the scanner **1**. The operation of the scanner **1** will be described with reference to FIG. **2**. Inside of the case **10**, the scanner **1** includes sheet supply rollers **51**, sheet discharge rollers **52**, two transparent sheets **53***a* and **53***b*, two image sensor modules **41** (**41***a* and **41***b*), and a main substrate **60**. The scanner **1** transports an original document mounted on the plate-shaped portion **21** through the sheet supply port **11** between the transparent plate **53***a* and the transparent plate **53***b* using the sheet supply rollers **51**. When the original document is transported between the transparent plate **53***a* and the transparent plate **53***b*, the image sensor module **41***a* emits light to a first surface (front surface or rear surface) of the original document via the transparent plate **53***a*, receives light (light from an image) reflected by the original document, generates image signals based on signals obtained through photoelectric conversion, and thereby reads the image formed on the first surface of the original document. Similarly, the image sensor module **41***b* emits light to a second surface (rear surface or front surface) that is different from the first surface of the original document via the transparent plate **53***b*, receives light (light from an image) reflected by the original document, and generates image signals based on signals obtained through photoelectric conversion, and thereby reads the image formed on the second surface of the original document. The image sensor modules **41** (**41***a* and **41***b*) are CMOS (Complementary metal-oxide-semiconductor) line sensors of a CIS (Contact Image Sensor) type, for example. The image signals generated by the image sensor modules **41***a* and **41***b* are transferred to the main substrate **60** and processed. Then, the original document is read one line at a time, and the document is transported in the direction of the sheet discharge port **12** by the rollers each time reading ends. The original document that was read is transported to the sheet discharge port **12** by the sheet discharge rollers **52**.
[0053] The sheet supply rollers **51** and the sheet discharge rollers **52** constitute transport portions that transport the

original document, and the scanner **1** of the first embodiment is a so-called double-side sheet-feeding scanner.

[0054] FIG. **3** is an exploded perspective view schematically showing a configuration of the image sensor module **41** (**41***a*, **41***b*). In the example shown in FIG. **3**, the image sensor module **41** is constituted by including a case **411**, a light source **412**, a lens **413**, a module substrate **414**, and image reading chips **415** (semiconductor devices) for reading an image. The light source **412**, the lens **413**, and the image reading chips **415** are accommodated between the case **411** and the module substrate **414**. The case **411** is provided with a slit. For example, the light source **412** has R, G, and B light-emitting diodes (LEDs), and sequentially causes the R, G, and B light-emitting diodes (red LED, green LED, and blue LED) to emit light while switching therebetween at a high speed. The light emitted by the light source **412** is emitted via the slit to a medium being read, and the light from the medium being read is input to the lens **413** via the slit. The lens **413** guides the input light to the image reading chips **415**.

[0055] FIG. **4** is a plan view schematically showing an arrangement of the image reading chips **415**. As shown in FIG. **4**, multiple (m) image reading chips **415** are arranged in alignment in a one-dimensional direction (in FIG. **4**, the X-axis direction) on the module substrate **414**. The image reading chips **415** have many light receiving elements (see FIGS. **7** and **8**) arranged in a line, and thus it is possible to realize a scanner **1** whose image reading resolution is higher the higher the density of the light receiving elements of the image reading chips **415** is. Also, it is possible to realize a scanner **1** that can read larger images the larger the number of image reading chips **415** is.

[0056] 1-2. Functional Configuration of Scanner

[0057] FIG. **5** is a functional block diagram showing an example of a functional configuration of the scanner **1** of the first embodiment. In the example shown in FIG. **5**, the scanner **1** is constituted by including a control unit **200**, two analog front ends (AFEs) **202***a* and **202***b* and two image sensor modules **41***a* and **41***b*. Since the configurations of the image sensor modules **41***a* and **41***b* are the same, in FIG. **5**, only the configuration of the image sensor module **41***a* is illustrated, and illustration of the configuration of the image sensor module **41***b* is not included.

[0058] The image sensor module **41** (**41***a*, **41***b*) is constituted by including a red LED **412**R, a green LED **412**G, a blue LED **412**B, and m image reading chips **415** (**415-1** to **415**-*m*).

[0059] The red LED **412**R, the green LED **412**G, and the blue LED **412**B are included in the light source **412**, and the multiple image reading chips **415** are arranged in alignment on the module substrate **414**. Multiple red LEDs **412**R, green LEDs **412**G, and blue LEDs **412**B may exist.

[0060] Also, the control unit **200** and the analog front ends (AFEs) **202***a* and **202***b* are included on the main substrate **60** (an example of a "control substrate") shown in FIG. **2**, which is different from the module substrate **414**. The control unit **200** and the analog front ends (AFEs) **202***a* and **202***b* are realized by integrated circuits (ICs).

[0061] The control unit **200** controls the operation of the image sensor module **41** (**41***a*, **41***b*). First, the control unit **200** controls the operation of the red LED **412**R, the green LED **412**G, and the blue LED **412**B, which are included in each of the image sensor modules **41***a* and **41***b*. Specifically, the control unit **200** supplies a driving signal DrvR with a fixed period T for a fixed exposure time Δt to the red LED **412**R and causes the red LED **412**R to emit light. Similarly, the control unit **200** supplies a driving signal DrvG with the period T for the exposure time Δt to the green LED **412**G to cause the green LED **412**G to emit light, and supplies a driving signal DrvB with the period T for an exposure time Δt to the blue LED **412**B to cause the blue LED **412**B to emit light. The control unit **200** causes the red LED **412**R, the green LED **412**G, and the blue LED **412**B to exclusively emit light one-by-one in sequence for the period T.

[0062] Also, the control unit **200** controls the operation of the m image reading chips **415** included in the image sensor modules **41***a* and **41***b*. Specifically, the control unit **200** supplies a clock signal CLK and a resolution setting signal RES to all of the m image reading chips **415**. The clock signal CLK is an operation clock signal for the m image reading chips **415**, and the m image reading chips **415** operate based on the clock signal CLK. Also, the resolution setting signal RES is a signal for setting the resolution for image reading performed by the scanner **1**. The resolution is set according to the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is active (in the present embodiment, at a high level).

[0063] As shown in FIG. **6**, in the present embodiment, the resolution 300 dpi is set in the case where the number of the rising edges of the clock signal CLK in the period for which the resolution setting signal RES is active (at a high level) is 2, the resolution 600 dpi is set in the case where the number of the rising edges of the clock signal CLK in the period for which the resolution setting signal RES is active (at a high level) is 4, and the resolution 1200 dpi is set in the case where the number of the rising edges of the clock signal CLK in the period for which the resolution setting signal RES is active (at a high level) is 8.

[0064] The light receiving elements of the image reading chip **415**-*j* (j=1 to m) receive light from the image formed on the medium to be read, and thereafter, upon receiving a chip enable signal ENj (in the present embodiment, a high-pulse signal), the image reading chip **415**-*j* generates and outputs an image signal SO having image information with the resolution set by the resolution setting signal RES based on the light received by the light receiving elements, in synchronization with the clock signal CLK.

[0065] In the present embodiment, the control unit **200** causes the red LED **411**R, the green LED **412**G, or the blue LED **412**B to emit light, and thereafter generates the chip enable signal EN**1**, which is active (at a high level) for a fixed amount of time (amount of time until the image reading chip **415-1** ends output of the image signal SO), and supplies the chip enable signal EN**1** to the image reading chip **415-1** (an example of a "first image reading chip") of the image sensor module **41***a* and the image reading chip **415-1** (an example of a "second image reading chip") of the image sensor module **41***b*. Also, in each of the image sensor modules **41***a* and **41***b*, the image sensor chip **415**-*j* (j=1 to m) generates the chip enable signal ENj+1 (high-pulse signal) slightly before the output of the image signal SO ends. Then, the chip enable signals EN**2** to ENm are supplied to the image reading chips **415-2** to **415**-*m* respectively.

[0066] Accordingly, in each of the image sensor modules **41***a* and **41***b*, the red LED **412**R, the green LED **412**G, or the blue LED **412**B emits light, and thereafter the m image reading chips **415** sequentially output the image signals SO.

Also, the image sensor module **41***a* outputs the image signals SO sequentially output by the m image reading chips **415** as image signals SO**1** from a terminal (not shown), and the image sensor module **41***b* outputs the image signals SO sequentially output by the m image reading chips **415** as the image signals SO**2** from a terminal (not shown).

[0067] The image signals SO**1** are transferred to the main substrate **60** by being transmitted through a wire (an example of a "first wire") (not shown) that electrically connects the image sensor module **41***a* (m image reading chips **415**) and the main substrate **60** on which the analog front ends (AFE) **202***a* and **202***b* and the control unit **200** are mounted. Also, the image signals SO**2** are transferred to the main substrate **60** by being transmitted through a wire (an example of a "second wire") (not shown) that electrically connects the image sensor module **41***b* (m image reading chips **415**) and the main substrate **60**.

[0068] Here, in each of the image sensor modules **41***a* and **41***b*, the output control signal OEA is supplied to the input terminals IP**4** (see FIG. **7**) of them image reading chips **415**, the output control signal OEB is supplied to the input terminals IP**5** (see FIG. **7**), and the image signals SO can be output with one of multiple drive capabilities selected based on the output control signals OEA and OEB. In particular, in the present embodiment, in the m image reading chips **415** of the image sensor module **41***a*, the input terminals IP**4** (see FIG. **7**) are electrically connected to a voltage source (not shown) that outputs a fixed voltage VA**1** via a bonding wire or the like, and the input terminals IP**5** (see FIG. **7**) are electrically connected to a voltage source (not shown) that outputs a fixed voltage VB**1** via a bonding wire or the like. Accordingly, the output control signal OEA**1** with the fixed voltage VA**1** is supplied as the output control signal OEA to the m image reading chips **415** of the image sensor module **41***a*, and the output control signal OEB**1** with the fixed voltage VB**1** is supplied as the output control signal OEB. Also, in the m image reading chips **415** of the image sensor module **41***b*, the input terminals IP**4** (see FIG. **7**) are electrically connected via the bonding wire or the like to the voltage source (not shown) that outputs the fixed voltage VA**2**, and the input terminals IP**5** (see FIG. **7**) are electrically connected to the voltage source (not shown) that outputs the fixed voltage VB**2** via the bonding wire or the like. Accordingly, the output control signal OEA**2** with the fixed voltage VA**2** is supplied as the output control signal OEA to the m image reading chips **415** of the image sensor module **41***b*, and the output control signal OEB**2** with the fixed voltage VB**2** is supplied as the output control signal OEB. These voltage sources may be provided inside of the scanner **1**, or may be provided outside thereof. In the present embodiment, in the image sensor modules **41***a* and **41***b*, the m image reading chips **415** are all the same type of chip (IC chips with the same configuration) and a detailed circuit configuration and operation of the image reading chips **415** will be described later.

[0069] The analog front end (AFE) **202***a* receives the image signals SO**1** (image signals SO sequentially output by them image reading chips **415**) output by the image sensor module **41***a*, performs amplification processing and A/D conversion processing on the image signals SO**1** (image signals SO), converts the resulting image signals SO**1** into digital signals including digital values corresponding to the light reception amounts of the light-receiving elements, and sequentially transmits the digital signals to the control unit **200**.

[0070] Similarly, the analog front end (AFE) **202***b* receives the image signals SO**2** (image signals SO sequentially output by the m image reading chips **415**) output by the image sensor module **41***b*, performs amplification processing and A/D conversion processing on the image signals SO**2** (image signals SO), converts the resulting image signals SO**2** into digital signals including digital values corresponding to the light reception amounts of the light-receiving elements, and sequentially transmits the digital signals to the control unit **200**.

[0071] The control unit **200** receives the digital signals transmitted sequentially from the analog front end (AFE) **202***a* and generates information on the image read by the image sensor module **41***a*. Also, the control unit **200** receives the digital signals sequentially transmitted from the analog front end (AFE) **202***b* and generates the image information received by the image sensor module **41***b*.

[0072] 1-3. Configuration and Operation of Image Reading Chip

[0073] FIG. **7** is a functional block diagram of an image reading chip **415**. The image reading chip **415** shown in FIG. **7** includes a control circuit **100**, a booster circuit **111**, a pixel driving circuit **112**, n pixel portions **110**, a CDS (Correlated Double Sampling) circuit **120**, a sampling/holding circuit **130**, an output circuit **140**, and an output selection unit **150**. The image reading chip **415** receives supply of a power source voltage VDD (e.g., 3.3 V) and a power source voltage VSS (e.g., 0 V) through two power source terminals VDP and VSP respectively, and operates based on a chip enable signal EN_I (one of the chip enable signals EN**1** to ENm shown in FIG. **5**), the resolution setting signal RES, and the clock signal CLK, which are input through three input terminals IP**1**, IP**2**, and IP**3** respectively, the output control signals OEA and OEB, which are input through the two input terminals IP**2** and IP**5** respectively, and the reference voltage VREF, which is supplied through a reference voltage supply terminal VRP.

[0074] The chip enable signal EN_I, the resolution setting signal RES, and the clock signal CLK are input to the control circuit **100**. The control circuit **100** controls operation of the booster circuit **111**, the pixel driving circuit **112**, the n pixel portions **110**, the CDS circuit **120**, and the sampling/holding circuit **130** based on the chip enable signal EN_I, the resolution setting signal RES, and the clock signal CLK. Specifically, the control circuit **100** generates a control signal CPC for controlling the booster circuit **111**, a control signal DRC for controlling the pixel driving circuit **112**, a control signal CDSC for controlling the CDS circuit **120**, a sampling signal SMP for controlling the sampling/holding circuit **130**, a pixel selection signal SEL**0**, reset signal RST, and second transfer control signals Tx**2** (Tx**2***a*, Tx**2***b*, Tx**2***c*, and Tx**2***d*) for controlling the pixel portion **110**, and a chip enable signal EN_O. The specific circuit configuration and operation of the control circuit **100** will be described later.

[0075] Based on the control signal CPC from the control circuit **100**, the booster circuit **111** boosts the power source voltage VDD and generates a first transfer control signal Tx**1** with the boosted power source voltage being a high level. The first transfer control signal Tx**1** is a control signal for transferring a charge (charge accumulated in a light-receiving element) generated based on photoelectric conversion

performed by the light-receiving element for an exposure time Δt, and the first transfer control signal Tx**1** is supplied to all of the n pixel portions **110**.

[0076] Based on the control signal DRC from the control circuit **100**, the pixel driving circuit **112** generates a driving signal Drv for driving the n pixel portions **110**. The n pixel portions **110** are provided in alignment in a one-dimensional direction, and the driving signal Drv is transferred to the n pixel portions **110** using a driving signal line **311**. Then, when the driving signal Drv is active (high level) and the pixel selection signal SELi−1 is active (high level), the i-th (i being one of 1 to n) pixel portion **110** sets the pixel selection signal SELi to active (high level) and outputs an output signal (pixel signal). The pixel selection signal SELi is output to the i+1-th pixel portion **110**.

[0077] The n pixel portions **110** (examples of "first pixel portions" or "second pixel portions") include light-receiving elements (examples of "first light-receiving elements" or "second light-receiving elements") that receive and photoelectrically convert light from an image formed on a first surface or a second surface of a medium to be read, and each outputs a pixel signal (an example of a "first pixel signal" or a "second pixel signal") with a voltage corresponding to light received by the light-receiving element during the exposure time Δt based on the first transfer control signal Tx**1**, the second transfer control signals Tx**2**, the pixel selection signal SEL (one of SEL**0** to SELn−1), the reset signal RST, and the driving signal Drv. The output signals (pixel signals) output from the n pixel portions **110** are sequentially transferred to the CDS circuit **120** using an output signal line **301**.

[0078] The n pixel portions **110** all have the same configuration, and FIG. **8** is a diagram showing the configuration of a pixel portion **110** (i-th pixel portion **110**). As shown in FIG. **8**, the pixel portion **110** includes four light-receiving elements PD**1**, PD**2**, PD**3**, and PD**4**. In other words, the pixel portion **110** includes four pixels.

[0079] The light-receiving elements PD**1**, PD**2**, PD**3**, and PD**4** receive light (in the present embodiment, light from an image formed on first surface or a second surface of a medium to be read) and convert it into an electrical signal (perform photoelectric conversion). In the present embodiment, the light-receiving elements PD**1**, PD**2**, PD**3**, and PD**4** are constituted by photodiodes with grounded anodes. The cathode of the light-receiving element PD**1** is connected to the source of an NMOS transistor M**11**, the cathode of the light-receiving element PD**2** is connected to the source of an NMOS transistor M**12**, the cathode of the light-receiving element PD**3** is connected to the source of an NMOS transistor M**13**, and the cathode of the light-receiving element PD**4** is connected to the source of an NMOS transistor M**14**.

[0080] The drain of the NMOS transistor M**11** is connected to the source of an NMOS transistor M**21**, the drain of the NMOS transistor M**12** is connected to the source of an NMOS transistor M**22**, the drain of the NMOS transistor M**13** is connected to the source of an NMOS transistor M**23**, and the drain of the NMOS transistor M**14** is connected to the source of an NMOS transistor M**24**. The first transfer control signal Tx**1** is supplied to the gates of the four NMOS transistors M**11**, M**12**, M**13**, and M**14**. Accordingly, the NMOS transistors M**11**, M**12**, M**13**, and M**14** function as switches that switch on and off based on the first transfer control signal Tx**1**.

[0081] The drains of the four NMOS transistors M**21**, M**22**, M**23**, and M**24** are connected in common to the source of an NMOS transistor M**3**, the gate of an NMOS transistor M**4**, and one end of a capacitor C**0**. The other end of the capacitor C**0** is grounded. A signal Tx**2***a* is supplied to the gate of the NMOS transistor M**21**, a signal Tx**2***b* is supplied to the gate of the NMOS transistor M**22**, a signal Tx**2***c* is supplied to the gate of the NMOS transistor M**23**, and a signal Tx**2***d* is supplied to the gate of the NMOS transistor M**24**.

[0082] For example, the power source voltage VDD is supplied to the drain of the NMOS transistor M**3**, and the reset signal RST is supplied to the gate of the NMOS transistor M**3**.

[0083] For example, the power source voltage VDD is supplied to the drain of the NMOS transistor M**4**, and the source of the NMOS transistor M**4** is connected to the drain of the NMOS transistor M**5**.

[0084] The source of the NMOS transistor M**5** is connected to the output signal line **301** and the output signal (pixel selection signal SELi) of a flip-flop (F/F) is supplied to the gate of the NMOS transistor M**5**.

[0085] The flip-flop (F/F) receives input of the pixel selection signal SELi−1 and the driving signal Drv and outputs the pixel selection signal SELi, which is generated by delaying the pixel selection signal SELi−1 taken in at the rising edge of the driving signal Drv. Note that the pixel selection signal SELi is a non-synchronous reset signal of the flip-flop (F/F) delayed by a delay circuit (not shown). For this reason, after the pixel selection signal SELi becomes active (high level), the pixel selection signal SELi returns to inactive (low level) upon the elapse of a desired amount of time.

[0086] The thus-configured i-th pixel portion **110** operates as follows. First, in exposure time Δt, the first transfer control signal Tx**1**, the second transfer control signals Tx**2** (Tx**2***a*, Tx**2***b*, Tx**2***c*, and Tx**2***d*), the pixel selection signal SELi−1, and the driving signal Drv are all inactive (low level), and the light-receiving elements PD**1**, PD**2**, PD**3**, and PD**4** accumulate charge (negative charge) corresponding to the received light.

[0087] Next, only the first transfer control signal Tx**1** becomes active (high level), and all four of the NMOS transistors M**11**, M**12**, M**13**, and M**14** are switched on. Accordingly, the charge generated based on the photoelectric conversion performed by the light-receiving element PD**1** (the charge (negative charge) accumulated in the light-receiving element PD**1**) is transferred via the NMOS transistor M**11** to an intermediate accumulation capacitor C**1** (not shown) formed at a connection node between the drain of the NMOS transistor M**11** and the source of the NMOS transistor M**21**, and the charge is accumulated therein. Also, the charge generated based on the photoelectric conversion performed by the light-receiving element PD**2** (the charge (negative charge) accumulated in the light-receiving element PD**2**) is transferred via the NMOS transistor M**12** to an intermediate accumulation capacitor C**2** (not shown) formed at a connection node between the drain of the NMOS transistor M**12** and the source of the NMOS transistor M**22**, and the charge is accumulated therein. Also, the charge generated based on the photoelectric conversion performed by the light-receiving element PD**3** (the charge (negative charge) accumulated in the light-receiving element PD**3**) is transferred via the NMOS transistor M**13** to an intermediate

accumulation capacitor C3 (not shown) formed at a connection node between the drain of the NMOS transistor M13 and the source of the NMOS transistor M23, and the charge is accumulated therein. Also, the charge generated based on the photoelectric conversion performed by the light-receiving element PD4 (the charge (negative charge) accumulated in the light-receiving element PD4) is transferred via the NMOS transistor M14 to an intermediate accumulation capacitor C4 (not shown) formed at a connection node between the drain of the NMOS transistor M14 and the source of the NMOS transistor M24, and the charge is accumulated therein.

[0088] Next, the first transfer control signal Tx1 becomes inactive (low level) and the driving signal Drv supplied to the pixel portion 110 repeatedly becomes active (high level) and inactive (low level) each half-cycle of the clock signal CLK.

[0089] Also, the reset signal RST becomes active (high level) for a fixed amount of time each cycle of the clock signal CLK. Accordingly, the NMOS transistor M3 switches on so as to reset the capacitor C0, and a fixed amount of charge (positive charge) is accumulated in the capacitor C0. Also, each cycle of the clock signal CLK, the reset signal RST returns to inactive (low level) and at least one of the four signals Tx2*a*, Tx2*b*, Tx2*c*, and Tx2*d* constituting the second transfer control signals Tx2 becomes active (high level) for a fixed amount of time.

[0090] Specifically, when the resolution is set to 1200 dpi, first, in one cycle of the clock signal CLK, only the signal Tx2*a* becomes active (high level) for a fixed amount of time. Next, in one cycle of the clock signal CLK, only the signal Tx2*b* becomes active (high level) for a fixed amount of time. Next, in one cycle of the clock signal CLK, only the signal Tx2*c* becomes active (high level) for a fixed amount of time. Next, in one cycle of the clock signal CLK, only the signal Tx2*d* becomes active (high level) for a fixed amount of time. This is repeated for the four signals Tx2*a*, Tx2*b*, Tx2*c*, and Tx2*d*.

[0091] Also, when the resolution is set to 600 dpi, first, in one cycle of the clock signal CLK, only the two signals Tx2*a* and Tx2*b* simultaneously become active (high level) for a fixed amount of time. Next, in one cycle of the clock signal CLK, only the two signals Tx2*c* and Tx2*d* simultaneously become active (high level) for a fixed amount of time, and this operation is repeated.

[0092] Also, when the resolution is set to 300 dpi, first, in one cycle of the clock signal CLK, the four signals Tx2*a*, Tx2*b*, Tx2*c*, and Tx2*d* simultaneously become active (high level) for a fixed amount of time, and this operation is repeated.

[0093] Then, when at least one of the four signals Tx2*a*, Tx2*b*, Tx2*c*, and Tx2*d* becomes active (high level) for a fixed amount of time, at least one of the four NMOS transistors M21, M22, M23, and M24 switches on, and the fixed amount of charge (positive charge) accumulated in the capacitor C0 decreases by an amount corresponding to the charge (negative charge) accumulated in at least one of the intermediate accumulation capacitors C1, C2, C3, and C4.

[0094] Also, in a pixel portion 110 from which a pixel signal is to be read out, the pixel selection signal SELi−1 becomes active (high level) for a fixed amount of time, the reset signal RST returns to being inactive (low level), and thereafter the pixel selection signal SELi becomes active (high level) for a fixed amount of time.

[0095] Accordingly, the NMOS transistor M5 switches on, and the current that flows in the NMOS transistor M4 changes according to the charge accumulated in the capacitor C0. Accordingly, the source potential of the NMOS transistor M4 changes and a pixel signal with a voltage corresponding to the source potential of the NMOS transistor M4 is output from the pixel portion 110 to the output signal line 301.

[0096] On the other hand, in a pixel portion 110 from which a pixel signal is not to be read out, the pixel selection signal SELi−1 remains inactive (low level), and therefore the pixel selection signal SELi is also at a low level. Accordingly, the NMOS transistor M5 is off, and the pixel signal is not output from the pixel unit 110.

[0097] Note that the output of the booster circuit 111 is used as the gate signals of the four NMOS transistors M11, M12, M13, and M14 to efficiently perform charge transfer in a short amount of time.

[0098] Returning to FIG. 7, via the output signal line 301, the CDS circuit 120 receives input of an image signal Vo that sequentially includes the pixel signals output from the n pixel portions 110, and the CDS circuit 120 operates based on the control signal CDSC from the control circuit 100. The CDS circuit 120 uses correlated double sampling using the reference voltage VREF as a reference to remove noise that is generated due to characteristic variation of amplification transistors included in then pixel portions 110 and is superimposed on the image signal Vo. In other words, the CDS circuit 120 is a noise reduction circuit that reduces noise included in output signals (pixel signals) output from the n pixel portions 110.

[0099] Based on the sampling signal SMP, the sampling/holding circuit 130 samples the image signal from which the noise was removed by the CDS circuit 120, holds the sampled signal, and outputs the signal to the output circuit 140.

[0100] The output circuit 140 amplifies the signals output by the sampling/holding circuit 130 and generates an image signal SO. As described above, the image signal SO is output from the image reading chip 415 via the output terminal OP1 and is supplied to the analog front end (AFE) 202*a* or the analog front end (AFE) 202*b* as the image signal SO1 or the image signal SO2 (see FIG. 5).

[0101] In particular, in the present embodiment, the output circuit 140 (an example of a "first output circuit" or a "second output circuit") can output the image signal SO, which is a signal based on pixel signals, using one of multiple drive capabilities including a first drive capability (alternatively, multiple drive capabilities including a second drive capability that is different from the first drive capability). Specifically, the output circuit 140 receives supply of the drive capability selection signals OE1 and OE2 and outputs the image signal SO with one of the multiple drive capabilities selected based on the drive capability selection signals OE1 and OE2.

[0102] The output selection unit 150 (an example of a "first output selection unit" or a "second output selection unit") selects a drive capability of the output circuit 140 from among the multiple drive capabilities based on the output control signals OEA and OEB input through the input terminals IP4 and IP5 (examples of a "first terminal" and a "second terminal") respectively. Specifically, the output selection unit 150 decodes the output control signals OEA and OEB input through the input terminals IP4 and IP5

respectively to generate the drive capability selection signals OE**1** and OE**2** and supplies the drive capability selection signals OE**1** and OE**2** to the output circuit **140**.

[0103] Slightly before the output of the image signal SO from the output circuit **140** ends, the control circuit **100** generates the chip enable signal EN_O (one of the chip enable signals EN**2** to ENm+1 shown in FIG. **5**), which is a high pulse signal, and outputs it from the output terminal OP**2** to the next image reading chip **415**. Thereafter, the control circuit **100** causes the output circuit **140** to stop the output of the image signal SO and sets the output terminal OP**1** to a high impedance.

[0104] FIG. **9** is a diagram showing a timing chart for signals of the image reading chip **415**. Note that FIG. **9** is a diagram showing a timing chart in the case where the resolution with which the scanner **1** reads an image is set to 300 dpi.

[0105] As shown in FIG. **9**, first, the resolution setting signal RES becomes high level for two cycles of the clock signal CLK. Then, when the exposure time Δt elapses, thereafter, various signals at 300 dpi are supplied to the pixel portions **110**.

[0106] First, the first transfer control signal Tx**1** becomes active (high level) for several cycles of the clock signal CLK.

[0107] Next, upon the chip enable signal EN_I (high pulse) being input, the pixel selection signal SEL**0** becomes active (high level) for one cycle of the clock signal CLK.

[0108] Next, the driving signal Drv becomes active (high level) for a half-cycle of the clock signal CLK, and both the first transfer control signal Tx**1** and the pixel selection signal SEL**0** become inactive (low level). Also, the reset signal RST becomes active (high level) with a slight delay for a short time.

[0109] Next, after the reset signal RST returns to being inactive (low level), all of the four signals Tx**2***a*, Tx**2***b*, Tx**2***c*, and Tx**2***d* constituting the second transfer control signals Tx**2** become active (high level) until the next falling edge of the clock signal CLK. Also, the pixel selection signal SEL**1** becomes active (high level), whereby the pixel signal from the first pixel portion **110** is output to the output signal line **301**, and the image signal Vo becomes a voltage corresponding to the pixel signal. The noise in the image signal Vo is removed by the CDS circuit **120**, and the image signal SO reaches a voltage that corresponds to the first pixel signal in synchronization with the falling edge of the sampling signal SMP.

[0110] Next, the driving signal Drv becomes active (high level) for a half-cycle of the clock signal CLK, and the pixel selection signal SEL**1** becomes inactive (low level). Also, the reset signal RST becomes active (high level) with a slight delay for a short time.

[0111] Next, after the reset signal RST returns to being inactive (low level), all of the four signals Tx**2***a*, Tx**2***b*, Tx**2***c*, and Tx**2***d* become active (high level) until the next falling edge of the clock signal CLK. Also, the pixel selection signal SEL**2** becomes active (high level), whereby the pixel signal from the second pixel portion **110** is output to the output signal line **301**, and the image signal Vo reaches a voltage corresponding to the pixel signal. The noise in the image signal Vo is removed by the CDS circuit **120**, and the image signal SO reaches a voltage that corresponds to the second pixel signal in synchronization with the falling edge of the sampling signal SMP.

[0112] Next, the driving signal Drv becomes active (high level) for a half-cycle of the clock signal CLK, and the pixel selection signal SEL**2** becomes inactive (low level). Also, the reset signal RST becomes active (high level) with a slight delay for a short time.

[0113] Hereinafter, similarly, the image signal SO reaches the voltages corresponding to the third to n-th pixel signals in synchronization with the falling edges of the sampling signal SMP.

[0114] Also, slightly before the output of the image signal SO (output of the voltage corresponding to the n-th pixel signal) ends, the chip enable signal EN_O (high pulse) is output, and when the output of the image signal SO ends, the output terminal OP**1** reaches a high impedance.

[0115] 1-4. Configuration of Output Circuit

[0116] FIG. **10** is a diagram showing an example of a configuration of the output circuit **140** according to the present embodiment. The output circuit **140** shown in FIG. **10** includes a resistor **141**, three NMOS transistors **142**, **143**, and **144**, and two switches **145** and **146**.

[0117] For example, the power source voltage VDD is supplied to one end of the resistor **141**, and the other end of the resistor **141** is connected to the drain terminal of the NMOS transistor **142**. The signal at the other end of the resistor **141** is an output signal OUT from the output circuit **140**, and the output signal OUT is the image signal SO (see FIG. **7**).

[0118] The drain terminal of the NMOS transistor **142** is connected to the other end of the resistor **141**, and the source terminal of the NMOS transistor **142** is grounded. Also, an input signal IN to the output circuit **140** is supplied to the gate terminal of the NMOS transistor **142**. This input signal IN is the output signal of the sampling/holding circuit **130** (see FIG. **7**).

[0119] A first terminal of the switch **145** is connected to the gate terminal of the NMOS transistor **142**, the power source voltage VSS is supplied to a second terminal of the switch **145**, and a third terminal of the switch **145** is connected to the gate terminal of the NMOS transistor **143**. Also, the drive capability selection signal OE**1** is supplied to the control terminal of the switch **145**, and when the drive capability selection signal OE**1** is active (in the present embodiment, at the high level), the first terminal and the third terminal of the switch **145** are connected, and the input signal IN is supplied to the gate terminal of the NMOS transistor **143**. Also, when the drive capability selection signal OE**1** is inactive (in the present embodiment, at the low level), the second terminal and the third terminal of the switch **145** are connected, and for example, the power source voltage VSS is supplied to the gate terminal of the NMOS transistor **143**.

[0120] The drain terminal of the NMOS transistor **143** is connected to the other end of the resistor **141**, the source terminal of the NMOS transistor **143** is grounded, and the gate terminal of the NMOS transistor **143** is connected to the third terminal of the switch **145**.

[0121] A first terminal of the switch **146** is connected to the gate terminal of the NMOS transistor **142**, the power source voltage VSS is supplied to a second terminal of the switch **146**, and a third terminal of the switch **146** is connected to the gate terminal of the NMOS transistor **144**. Also, the drive capability selection signal OE**2** is supplied to the control terminal of the switch **146**, and when the drive capability selection signal OE**2** is active (in the present

embodiment, at the high level), the first terminal and the third terminal of the switch **145** are connected, and the input signal IN is supplied to the gate terminal of the NMOS transistor **144**. Also, when the drive capability selection signal OE**2** is inactive (in the present embodiment, at the low level), the second terminal and the third terminal of the switch **146** are connected, and for example, the power source voltage VSS is supplied to the gate terminal of the NMOS transistor **144**.

[0122] The drain terminal of the NMOS transistor **144** is connected to the other end of the resistor **141**, the source terminal of the NMOS transistor **144** is grounded, and the gate terminal of the NMOS transistor **144** is connected to the third terminal of the switch **146**.

[0123] For example, the three NMOS transistors **142**, **143**, and **144** have the same threshold values and gate sizes (W/L) (manufacturing error is allowed).

[0124] The thus-configured output circuit **140** is a common source circuit, and when the voltage of the input signal IN falls within a predetermined range in which the NMOS transistors **142**, **143**, and **144** operate in a linear region, the higher the voltage of the input signal IN is, the larger the current that flows in the resistor **141** is (the larger the voltage drop at the resistor **141** is), and therefore the lower the voltage of the output signal OUT is. Accordingly, if the voltage of the output signal (input signal IN) of the sampling/holding circuit **130** changes only in the predetermined range, the image signal SO (output signal OUT) is a signal obtained by inverting and amplifying the output signal of the sampling/holding circuit **130** (input signal IN).

[0125] Also, in the output circuit **140**, when both the drive capability selection signal OE**1** and the drive capability selection signal OE**2** are inactive (low level), a current I_1 flows between the drain and source of the NMOS transistor **142**, but no current flows between the drains and sources of the NMOS transistors **143** and **144**. Accordingly, the current I_1 flows in the resistor **141**, and the drive capability (driving current) at that time is set to α_1.

[0126] Also, when the drive capability selection signal OE**1** is active (high level) and the drive capability selection signal OE**2** is inactive (low level), the current I_1 flows between the respective drains and sources of the NMOS transistors **142** and **143**, but no current flows between the drain and source of the NMOS transistor **144**. Accordingly, a current that is two times the current flows in the resistor **141** and the drive capability (driving current) α_2 at that time is two times α_1.

[0127] Also, when the drive capability selection signal OE**1** and the drive capability selection signal OE**2** are both active (high level), the current I_1 flows between the respective drains and sources of the NMOS transistors **142**, **143**, and **144**. Accordingly, a current that is three times the current I_1 flows in the resistor **141** and the drive capability (driving current) α_3 at that time is three times α_1.

[0128] Note that with the output circuit shown in FIG. **10**, if the amplification factors when the drive capabilities are α_1, α_2, and α_3 are set to β_1, β_2, and β_3 respectively, β_2 is two times β_1 and β_3 is three times β_1, but the output circuit **140** may be a circuit with a configuration in which it is possible to select multiple drive capabilities with the amplification factor remaining constant.

[0129] FIG. **11** is a diagram showing an example of another configuration of the output circuit **140** according to the present embodiment. The output circuit **140** shown in FIG. **11** includes five CMOS inverter elements **161**, **162**, **163**, **164**, and **165**, two PMOS transistors **166** and **167**, and two NMOS transistors **168** and **169**.

[0130] For example, the power source voltage VDD is supplied to a high-side power source terminal of the CMOS inverter element **161**, and for example, the power source voltage VSS is supplied to a low-side power source terminal of the CMOS inverter element **161**. The input signal IN to the output circuit **140** is supplied to the input terminal of the CMOS inverter terminal **161**. This input signal IN is the output signal of the sampling/holding circuit **130** (see FIG. **7**). Also, the signal output from the output terminal of the CMOS inverter element **161** is the output signal OUT from the output circuit **140**, and the output signal OUT is the image signal SO (see FIG. **7**).

[0131] The drive capability selection signal OE**1** is supplied to the input terminal of the CMOS inverter element **164**, and the output terminal of the CMOS inverter element **164** is connected to the gate terminal of the PMOS transistor **166**.

[0132] The gate terminal of the PMOS transistor **166** is connected to the output terminal of the CMOS inverter element **164**, the power source voltage VDD for example is supplied to the source terminal of the PMOS transistor **166**, and the drain terminal of the PMOS transistor **166** is connected to the high-side power source terminal of the CMOS inverter element **162**. Accordingly, when the drive capability selection signal OE**1** is active (high level), the source and drain of the PMOS transistor **166** are connected, and the power source voltage VDD for example is supplied to the high-side power source terminal of the CMOS inverter element **162**.

[0133] The drive capability selection signal OE**1** is supplied to the gate terminal of the NMOS transistor **168**, the power source voltage VSS for example is supplied to the source terminal of the NMOS transistor **168**, and the drain terminal of the NMOS transistor **168** is connected to the low-side power source terminal of the CMOS inverter element **162**. Accordingly, when the drive capability selection signal OE**1** is active (high level), the source and drain of the NMOS transistor **168** are connected, and the power source voltage VSS for example is supplied to the low-side power source terminal of the CMOS inverter element **162**.

[0134] The high-side power source terminal of the CMOS inverter element **162** is connected to the drain terminal of the PMOS transistor **166**, and the low-side power source terminal of the CMOS inverter element **162** is connected to the drain terminal of the NMOS transistor **168**. Accordingly, when the drive capability selection signal OE**1** is active (high level), the power source voltage VDD and the power source voltage VSS for example are supplied to the high-side power source terminal and the low-side power source terminal of the CMOS inverter element **162**, whereby the CMOS inverter element **162** operates. Also, the input terminal of the CMOS inverter element **162** is connected to the input terminal of the CMOS inverter element **161** and the input signal IN is supplied thereto. Also, the output terminal of the CMOS inverter element **162** is connected to the output terminal of the CMOS inverter element **161**.

[0135] The drive capability selection signal OE**2** is supplied to the input terminal of the CMOS inverter element **165**, and the output terminal of the CMOS inverter element **165** is connected to the gate terminal of the PMOS transistor **167**.

[0136] The gate terminal of the PMOS transistor **167** is connected to the output terminal of the CMOS inverter element **165**, the power source voltage VDD for example is supplied to the source terminal of the PMOS transistor **167**, and the drain terminal of the PMOS transistor **167** is connected to the high-side power source terminal of the CMOS inverter element **163**. Accordingly, when the drive capability selection signal OE**2** is active (high level), the source and drain of the PMOS transistor **167** are connected, and the power source voltage VDD for example is supplied to the high-side power source terminal of the CMOS inverter element **163**.

[0137] The drive capability selection signal OE**2** is supplied to the gate terminal of the NMOS transistor **169**, the power source voltage VSS for example is supplied to the source terminal of the NMOS transistor **169**, and the drain terminal of the NMOS transistor **169** is connected to the low-side power source terminal of the CMOS inverter element **163**. Accordingly, when the drive capability selection signal OE**2** is active (high level), the source and drain of the NMOS transistor **169** are connected, and the power source voltage VSS for example is supplied to the low-side power source terminal of the CMOS inverter element **163**.

[0138] The high-side power source terminal of the CMOS inverter element **163** is connected to the drain terminal of the PMOS transistor **167**, and the low-side power source terminal of the CMOS inverter element **163** is connected to the drain terminal of the NMOS transistor **169**. Accordingly, when the drive capability selection signal OE**2** is active (high level), the power source voltage VDD and the power source voltage VSS for example are respectively supplied to the high-side power source terminal and the low-side power source terminal of the CMOS inverter element **262**, whereby the CMOS inverter element **163** operates. Also, the input terminal of the CMOS inverter element **163** is connected to the input terminal of the CMOS inverter element **161** and the input signal IN is supplied thereto. Also, the output terminal of the CMOS inverter element **163** is connected to the output terminal of the CMOS inverter element **161**.

[0139] For example, the three CMOS inverter elements **161**, **162**, and **163** have the same threshold value and gate size (W/L) (manufacturing error is allowed).

[0140] With the thus-configured output circuit **140**, when the voltage of the input signal IN falls within a predetermined range in which the CMOS inverter elements **161**, **162**, and **163** operate in linear regions, the higher the voltage of the input signal IN is, the lower the voltage of the output signal OUT is. Accordingly, if the voltage of the output signal (input signal IN) of the sampling/holding circuit **130** changes only in the predetermined range, the image signal SO (output signal OUT) is a signal obtained by inverting and amplifying the output signal of the sampling/holding circuit **130** (input signal IN).

[0141] Also, in the output circuit **140**, when both the drive capability selection signal OE**1** and the drive capability selection signal OE**2** are inactive (low level), the CMOS inverter element **161** operates, but the CMOS inverter elements **162** and **163** do not operate. Accordingly, the current I_1 flows from the high-side power source terminal to the output terminal of the CMOS inverter element **161** and the drive capability (driving current) at this time is set to α_1.

[0142] Also, when the drive capability selection signal OE**1** is active (high level) and the drive capability selection signal OE**2** is inactive (low level), the CMOS inverter elements **161** and **162** operate, and the CMOS inverter element **163** does not operate. Accordingly, the current I_1 flows from the high-side power source terminals to the output terminals of the CMOS inverter elements **161** and **162** respectively, and the drive capability (driving current) α_2 at this time is two times α_1.

[0143] Also, when both the drive capability selection signal OE**1** and the drive capability selection signal OE**2** are active (high level), the CMOS inverter elements **161**, **162**, and **163** all operate. Accordingly, the current I_1 flows from the high-side power source terminals to the output terminals of the CMOS inverter elements **161**, **162**, and **163** respectively, and the drive capability (driving current) α_3 at this time is three times α_1.

[0144] Note that with the output circuit **140** shown in FIG. **11**, if the amplification factors when the drive capabilities are α_1, α_2, and α_3 are set to β_1, β_2, and β_3 respectively, $\beta_1=\beta_2=\beta_3$ is satisfied.

[0145] Thus, according to the voltage levels of the drive capability selection signals OE**1** and OE**2**, the output circuit **140** shown in FIG. **10** or **11** can output an image signal SO, which is a signal based on the pixel signals, at one of the drive capability α_1 (an example of a "first drive capability"), the drive capability α_2 (an example of a "second drive capability"), which is larger than the drive capability α_1, and the drive capability α_3 (and example of a "second drive capability"), which is larger than the drive capability α_1 and larger than the drive capability α_2. The drive capability α_1 is the smallest among the drive capabilities α_1, α_2, and α_3, and the drive capability α_3 is the largest among the drive capabilities α_1, α_2, and α_3.

[0146] As described above, the output selection unit **150** decodes the output control signals OEA and OEB input through the input terminals IP**4** and IP**5** respectively to generate the drive capability selection signals OE**1** and OE**2** and supplies the drive capability selection signals OE**1** and OE**2** to the output circuit **140**.

[0147] FIG. **12** shows an example of a truth value table for decoding logic used by the output selection unit **150**. In the example shown in FIG. **12**, if both the output control signal OEA and the output control signal OEB are at the low level, the drive capability selection signals OE**1** and OE**2** are both at the low level. Accordingly, if the fixed voltages VA**1** (or VA**2**) and VB**1** (or VB**2**) supplied to the input terminals IP**4** and IP**5** respectively are both the power source voltage VSS (0 V), the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_1. Also, if the output control signal OEA is at the high level and the output control signal OEB is at the low level, the drive capability selection signal OE**1** is at the high level and the drive capability selection signal OE**2** is at the low level. Accordingly, if the fixed voltage VA**1** (or VA**2**) supplied to the input terminal IP**4** is the power source voltage VDD (e.g., 3.3 V) and the fixed voltage VB**1** (or VB**2**) supplied to the input terminal IP**5** is the power source voltage VSS (0 V), the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_2. Also, if the output control signal OEA is at the low level and the output control signal OEB is at the high level, the drive capability selection signals OE**1** and OE**2** are both at the high level. Accordingly, if the fixed voltage VA**1** (or VA**2**) supplied to the input terminal IP**4** is the power source voltage VSS (0 V) and the fixed voltage VB**1** (or VB**2**) supplied to the input terminal

IP**5** is the power source voltage VDD (e.g., 3.3 V), the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_3.

[0148] Thus, the image reading chip **415** according to the present embodiment can output the image signal SO with a drive capability selected according to the fixed voltages VA**1** (or VA**2**) and VB**1** (or VB**2**) supplied to the input terminals IP**4** and IP**5**, and is a highly versatile IC chip.

[0149] As described above, the scanner **1** of the present embodiment is a sheet-feeding double-side scanner in which an original document is transported, and therefore the image sensor modules **41***a* and **41***b* do not need to move. Accordingly, for example, as shown in FIG. **2**, the image sensor module **41***a* is fixed at a location that is relatively close to the main substrate **60**, on which the analog front ends (AFEs) **202***a* and **202***b* and the control unit **200** are mounted, and the image sensor module **41***b* is fixed at location that is relatively far from the main substrate **60**.

[0150] Upon doing so, the wire electrically connecting the image sensor module **41***a* (m image reading chips **415**) and the main substrate **60**, or in other words, the wire (transfer wire for the image signals SO**1**) for transferring the image signals SO**1** from the m image reading chips **415** of the image sensor module **41***a* to the analog front end (AFE) **202***a* is relatively short. For this reason, the load of the transfer wire for the image signals SO**1** is relatively small, the drive capability of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***a* can be set to α_1 or α_2, and need not be set to the largest drive capability α_3. In other words, in each of the m image reading chips **415** of the image sensor module **41***a,* the output selection unit **150** may select the drive capability α_1 or α_2 as the drive capability of the output circuit **140**. In particular, if assembly is performed such that the distance between the image sensor module **41***a* and the main substrate **60** (the length of the transfer wire for the image signals SO**1**) is extremely short, the drive capability of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***a* can be set to the smallest drive capability α_1. In other words, in each of the m image reading chips **415** of the image sensor module **41***a,* the output selection unit **150** may select the smallest drive capability α_1 as the drive capability of the output circuit **140**.

[0151] In contrast to this, the wire that electrically connects the image sensor module **41***b* (m image reading chips **415**) and the main substrate **60**, or in other words, the wire (transfer wire for the image signals SO**2**) for transferring the image signals SO**2** from the m image reading chips **415** of the image sensor module **41***b* to the analog front end (AFE) **202***b* is longer than the transfer wire for the image signals SO**1**. For example, the transfer wire for the image signals SO**2** is realized by a flexible flat cable or the like in some cases. For this reason, the load of the transfer wire for the image signals SO**2** is larger than the load of the transfer wire for the image signals SO**1**, and the drive capability of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***b* may be set to the drive capability α_2 or α_3, which is larger than the drive capability α_1 or α_2 of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***a.* In other words, in each of the m image reading chips **415** of the image sensor module **41***b,* the output selection unit **150** may select the drive capability α_2 or α_3 as the drive capability of the output circuit **140**. In particular, if assembly is performed such that the transfer wire for the image signals SO**2** is extremely long, the drive capability of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***b* can be set to the largest drive capability α_3. In other words, in each of the m image reading chips **415** of the image sensor module **41***b,* the output selection unit **150** may select the largest drive capability α_3 as the drive capability of the output circuit **140**.

[0152] 1-5. Effect

[0153] As described above, with the scanner **1** of the first embodiment, in the m image reading chips **415** of the image sensor module **41***a* that reads the image formed on the first surface of the original document, based on the voltages VA**1** and VB**1** of the output control signals OEA and OEB (output control signals OEA**1** and OEB**1**) input to the input terminals IP**4** and IP**5**, the drive capability of the output circuits **140** can be set appropriately such that the drive capability matches the size of the load of the transfer wire for the image signals SO (image signals SO**1**) and does not become excessive. Also, in the m image reading chips **415** of the image sensor module **41***b* for reading the image formed on the second surface of the original document, based on the voltages VA**2** and VB**2** of the output control signals OEA and OEB (output control signals OEA**2** and OEB**2**) input to the input terminals IP**4** and IP**5**, the drive capability of the output circuits **140** can be set appropriately such that the drive capability matches the size of the load of the transfer wire for the image signals SO (image signals SO**2**) and does not become excessive. Accordingly, with the scanner **1** of the first embodiment, it is possible to read the images formed on both sides of the original document while suppressing the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

[0154] In particular, since the scanner **1** of the present embodiment is a sheet-feeding double-side scanner in which the image sensor modules **41***a* and **41***b* do not move, for example, the image sensor module **41***a* can be fixed at a location that is relatively close to the main substrate **60**. Accordingly, the transfer wire for the image signals SO**1** is short, and the wire load is relatively small. For this reason, in the image sensor module **41***a,* the drive capability of the output circuit **140** of the image reading chip **415** can be set to α_1 or α_2, which are relatively small, and as a result, power consumption and noise accompanying the transfer of the image signals SO can be reduced. In this case, the image sensor module **41***b* is fixed at a location that is relatively far from the main substrate **60** and has a relatively larger wire load, but the drive capability of the output circuits **140** of the image reading chips **415** of the image sensor module **41***b* can be set to α_2 or α_3, which are relatively large, and as a result, it is possible to reliably transfer the image signals SO while suppressing the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

[0155] Also, since the scanner **1** of the first embodiment uses highly-versatile image reading chips **415** that can output the image signals SO with a drive capability selected from multiple drive capabilities, it is not necessary to design an image reading chip specialized for the scanner **1**, and it is possible to reduce cost.

[0156] Also, with the scanner **1** of the present embodiment, during assembly, it is sufficient that the input terminals IP**4** and IP**5** of the image reading chips **415** are respectively connected to the voltage sources that output the fixed voltages VA**1** and VB**1** or the voltage sources that output the

fixed voltages VA**2** and VB**2**, and therefore the drive capabilities of the output circuits **140** of the image reading chips **415** can be set easily.

[0157] Note that in the present embodiment, with the image reading chip **415**, the drive capability of the output circuit **140** can be selected from among three types, namely α_1, α_2, and α_3, but it is also possible to select from two types, or from four or more types.

[0158] Also, the scanner **1** of the first embodiment may have a configuration in which the output control signals OEA and OEB with fixed voltages are supplied to only the m image reading chips **415** included in the image sensor module **41***a* or the m image reading chips **415** included in the image sensor module **41***b*.

2. Second Embodiment

[0159] Hereinafter, regarding a scanner **1** of a second embodiment, constituent elements similar to those of the first embodiment are denoted by the same reference numerals, description that is redundant with the first embodiment is not included, and mainly content that differs from that of the first embodiment will be described.

[0160] The structure of the scanner **1** of the second embodiment is similar to that of the first embodiment (FIGS. **1** to **4**), and therefore illustration and description thereof is not included here. Also, the functional block diagram of the image reading chip **415** according to the second embodiment is similar to that of the first embodiment (FIG. **7**), and therefore illustration and description thereof is not included here.

[0161] FIG. **13** is a functional block diagram showing an example of a functional configuration of the scanner **1** of the second embodiment. As shown in FIG. **13**, with the scanner **1** of the second embodiment, the output control signals OEA and OEB (OEA**1** and OEB**1**) input to the input terminals IP**4** and IP**5** of the m image reading chips **415** of the image sensor module **41***a* and the output control signals OEA and OEB (OEA**2** and OEB**2**) input to the input terminals IP**4** and IP**5** of the m image reading chips **415** of the image sensor module **41***b* are transferred from the control unit **200**. For example, the control unit **200** supplies the output control signal OEA**1** with the fixed voltage VA**1** as the output control signal OEA to the input terminals IP**4** of the m image reading chips **415** of the image sensor module **41***a* and supplies the output control signal OEB**1** with the fixed voltage VB**1** as the output control signal OEB to the input terminals IP**5**. Also, the control unit **200** supplies the output control signal OEA**2** with the fixed voltage VA**2** as the output control signal OEA to the input terminals IP**4** of them image reading chips **415** of the image sensor module **41***b* and supplies the output control signal OEB**2** with the fixed voltage VB**2** as the output control signal OEB to the input terminal IP**5**.

[0162] Similarly to the first embodiment, with the image reading chip **415**, the output selection unit **150** decodes the output control signals OEA and OEB input from the input terminals IP**4** and IP**5** in accordance with the decoding logic shown in FIG. **12** for example, generates the drive capability selection signals OE**1** and OE**2**, and supplies them to the output circuit **140**. Also, similarly to the first embodiment, the output circuit **140** is a circuit with the configuration shown in FIG. **10** or **11**, for example, and outputs the image signal SO with one of the drive capabilities α_1, α_2, and α_3 according to the voltage levels of the drive capability selection signals OE**1** and OE**2**.

[0163] According to the above-described scanner **1** of the second embodiment, an effect similar to that of the first embodiment is exhibited. Furthermore, with the scanner **1** of the second embodiment, the drive capability of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***a* is selected based on the output control signals OEA**1** and OEB**1** transferred from the control unit **200**, and the drive capability of the output circuits **140** of the m image reading chips **415** of the image sensor module **41***b* is selected based on the output control signals OEA**2** and OEB**2** transferred from the control unit **200**. Accordingly, with the scanner **1** of the second embodiment, after the scanner **1** is assembled, the drive capabilities of the output circuits **140** can be changed according to a change in the load of the transfer wire for the image signals SO**1** and a change in the load of the transfer wire for the image signals SO**2**, and it is possible to effectively suppress the occurrence of excessive power consumption and excessive noise accompanying signal transfer.

[0164] Note that the scanner **1** of the second embodiment may have a configuration in which the control unit **200** supplies the output control signals OEA and OEB only to the m image reading chips **415** of the image sensor module **41***a* or only to the m image reading chips **415** of the image sensor module **41***b*. For example, the scanner **1** of the second embodiment may have a configuration in which the control unit **200** supplies the output control signals OEA**2** and OEB**2** to the input terminals IP**4** and IP**5** of the m image reading chips **415** of the image sensor module **41***a* and the input terminals IP**4** and IP**5** of the m image reading chips **415** of the image sensor module **41***b* are electrically connected to respective voltage sources (not shown) that output fixed voltages. Also, the scanner **1** of the second embodiment may have a configuration in which the control unit **200** supplies the output control signals OEA**2** and OEB**2** to the input terminals IP**4** and IP**5** of the m image reading chips **415** of the image sensor module **41***b* and the input terminals IP**4** and IP**5** of the m image reading chips **415** of the image sensor module **41***b* are electrically connected to respective voltage sources (not shown) that output fixed voltages.

3. Third Embodiment

[0165] Hereinafter, regarding a scanner **1** of a third embodiment, constituent elements similar to those of the first embodiment or the second embodiment are denoted by the same reference numerals, description that is redundant with the first embodiment or the second embodiment is not included, and mainly content that differs from that of the first embodiment and the second embodiment will be described.

[0166] The structure of the scanner **1** of the third embodiment is similar to that of the first embodiment (FIGS. **1** to **4**), and therefore illustration and description thereof is not included.

[0167] FIG. **14** is a functional block diagram showing an example of a functional configuration of the scanner **1** of the third embodiment. Also, FIG. **15** is a functional block diagram of an image reading chip **415**. As shown in FIG. **14**, with the scanner **1** of the third embodiment, the control unit **200** supplies the output control signal OC**1** as the output control signal OC, which is a serial signal, to all of the m image reading chips **415** (**415**-**1** to **415**-*m*) of the image sensor module **41***a*. Also, the control unit **200** supplies the

output control signal OC**2** as the output control signal OC, which is a serial signal, to all of the m image reading chips **415** (**415-1** to **415-***m*) of the image sensor module **41***b*. The output control signal OC is a signal for setting the drive capability of the output circuit **140** that outputs the image signal SO in an image reading chip **415**.

[0168] Here, the output control signal OC, which is a serial signal, is supplied to the input terminals IP**4** of the m image reading chips **415** of the image sensor module **41***a* and the m image reading chips **415** of the image sensor module **41***b*, and it is possible to output the image signals SO with one of the multiple drive capabilities selected based on the output control signal OC. In the present embodiment, in the m image reading chips **415** of the image sensor module **41***a*, the output control signal OC (output control signal OC**1**) input to the input terminals IP**4** is transferred from the control unit **200**. Similarly, in them image reading chips **415** of the image sensor module **41***b*, the output control signal OC (output control signal OC**2**) input to the input terminals IP**4** is transferred from the control unit **200**.

[0169] Also, in the present embodiment, in the image reading chip **415**, the output selection unit **150** selects the drive capability of the output circuit **140** from among multiple drive capabilities based on the output control signal OC input through the input terminal IP**4**. Specifically, the output selection unit **150** samples the output control signal OC input through the input terminal IP**4** based on the clock signal CLK, and if one of multiple pre-determined patterns is detected, the output selection unit **150** generates the drive capability selection signals OE**1** and OE**2** that are associated with the detected pattern and supplies them to the output circuit **140**.

[0170] FIG. **16** shows an example of a correspondence relationship between the patterns of the output control signal OC and the drive capability selection signals OE**1** and OE**2**. In the example shown in FIG. **16**, if the number of rising edges of the clock signal CLK in the period during which the output control signal OC is at the high level is 2, the drive capability selection signals OE**1** and OE**2** are both at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_1. Also, if the number of rising edges of the clock signal CLK in the period during which the output control signal OC is at the high level is 3, the drive capability selection signal OE**1** is at the high level and the drive capability selection signal OE**2** is at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_2. Also, if the number of rising edges of the clock signal CLK in the period during which the output control signal OC is at the high level is 4, the drive capability selection signals OE**1** and OE**2** are both at the high level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_3.

[0171] As described above, according to the scanner **1** of the third embodiment, an effect similar to that of the first embodiment is exhibited. Furthermore, according to the scanner **1** of the third embodiment, the image reading chip **415** selects the drive capability of the output circuit **140** based on the output control signal OC, which is a serial signal, and therefore it is sufficient to provide one terminal (input terminal IP**4**) as the terminal to which the signal for setting the drive capability of the output circuit **140** is supplied, and there is no need to provide multiple terminals (the input terminals IP**4** and IP**5** of the first embodiment or the second embodiment). Accordingly, this is advantageous for reducing the size and lowering the cost of the image reading chip **415**.

[0172] Note that the scanner **1** of the third embodiment may have a configuration in which the control unit **200** supplies the output control signals OC only to the m image reading chips **415** of the image sensor module **41***a* or only to the m image reading chips **415** of the image sensor module **41***b*.

4. Fourth Embodiment

[0173] Hereinafter, regarding the scanner **1** of the fourth embodiment, constituent elements that are the same as those of the first embodiment, the second embodiment, and the third embodiment are denoted by the same reference numerals, description that is redundant with that of the first embodiment, second embodiment, and third embodiment is not included here, and mainly content that differs from that of the first embodiment, second embodiment, and third embodiment will be described.

[0174] The structure of the scanner **1** of the fourth embodiment is similar to that of the first embodiment (FIGS. **1** to **4**), and therefore illustration and description thereof is not included here.

[0175] FIG. **17** is a functional block diagram showing an example of a functional configuration of the scanner **1** of the fourth embodiment. Also, FIG. **18** is a functional block diagram of the image reading chip **415** of the fourth embodiment. As shown in FIGS. **17** and **18**, in the scanner **1** of the fourth embodiment, the resolution setting signal RES input to the input terminals IP**2** of the m image reading chips **415** of the image sensor module **41***a* and the m image reading chips **415** of the image sensor module **41***b* is also used as a signal for setting the drive capability of the output circuits **140**. In other words, in the fourth embodiment, the resolution setting signal RES is a signal for setting the drive capability of the output circuits **140** and for setting the resolution for image reading performed by the image reading chip **415**. Specifically, with the scanner **1** of the fourth embodiment, the control unit **200** supplies the resolution setting signal RES**1** as the resolution setting signal RES, which is a serial signal, to all of the m image reading chips **415** of the image sensor module **41***a*. Also, the control unit **200** supplies the resolution setting signal RES**2** as the resolution setting signal RES, which is a serial signal, to all of the m image reading chips **415** of the image sensor module **41***b*.

[0176] Then, in the image reading chip **415**, the output selection unit **150** selects the drive capability of the output circuit **140** from multiple drive capabilities based on the resolution setting signal RES. Specifically, if the resolution setting signal RES is sampled based on the clock signal CLK and one of multiple pre-determined patterns is detected, the output selection unit **150** generates the drive capability selection signals OE**1** and OE**2** associated with the detected pattern and supplies them to the output circuit **140**.

[0177] FIG. **19** is a diagram showing an example of a correspondence relationship between the pattern of the resolution setting signal RES of the fourth embodiment, the resolution, and the drive capability selection signals OE**1** and OE**2**. In the example shown in FIG. **19**, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 2, the resolution is set to 300 dpi and the drive capability

selection signals OE1 and OE2 are both at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_1. Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is **3**, the resolution is set to 300 dpi, the drive capability selection signal OE1 is at the high level, and the drive capability selection signal OE2 is at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_2. Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 4, the resolution is set to 300 dpi, the drive capability selection signals OE1 and OE2 are both at the high level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_3.

[0178] Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 5, the resolution is set to 600 dpi, and the drive capability selection signals OE1 and OE2 are both at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_1. Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 6, the resolution is set to 600 dpi, the drive capability selection signal OE1 is at the high level, and the drive capability selection signal OE2 is at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_2. Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 7, the resolution is set to 600 dpi, the drive capability selection signals OE1 and OE2 are both at the high level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_3.

[0179] Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 8, the resolution is set to 1200 dpi, and the drive capability selection signals OE1 and OE2 are both at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_1. Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 9, the resolution is set to 1200 dpi, the drive capability selection signal OE1 is at the high level, and the drive capability selection signal OE2 is at the low level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_2. Also, if the number of rising edges of the clock signal CLK in the period during which the resolution setting signal RES is at the high level is 10, the resolution is set to 1200 dpi, and the drive capability selection signals OE1 and OE2 are both at the high level. Accordingly, in this case, the drive capability of the output circuit **140** shown in FIG. **10** or **11** is α_3.

[0180] According to the above-described scanner **1** of the fourth embodiment, an effect similar to that of the first embodiment is exhibited. Furthermore, with the scanner **1** of the fourth embodiment, the signal for setting the drive capability of the output circuit **140** of the image reading chip **415** can also be used as a signal for setting the resolution of image reading performed by the image reading chip **415**, and therefore a dedicated terminal (the terminal IP**4** in the first embodiment) to which the signal for setting the drive capability of the output circuit is supplied is not needed in the image reading chip **415**. Accordingly, this is advantageous for reducing the size and lowering the cost of the image reading chip **415**.

[0181] Note that the scanner **1** of the fourth embodiment may have a configuration in which the control unit **200** transfers the resolution setting signal RES, which is also used as a signal for setting the drive capability of the output circuit **140**, only to the m image reading chips **415** of the image sensor module **41***a* or only to the m image reading chips **415** of the image sensor module **41***b*.

[0182] Although embodiments were described above, the invention is not limited to these embodiments, and can be carried out in various forms without departing from the gist of the invention. For example, the above-described embodiments can also be used in combination as appropriate.

[0183] The invention encompasses configurations that are substantially the same as the configurations described in the present embodiment (e.g., configurations with the same functions, methods, and results, or configurations with the same object and effect). Also, the invention encompasses a configuration obtained by replacing a non-essential portion of the configuration described in the embodiments. Also, the invention encompasses configurations that exhibit the same effect as the configuration described in the embodiment and configurations that can achieve the same object. Also, the invention encompasses a configuration obtained by adding a known technique to the configuration described in the embodiments.

[0184] This application claims priority from Japanese Patent Application No. 2016-190810 filed in the Japanese Patent Office on Sep. 29, 2016, the entire disclosure of which is hereby incorporated by reference in its entirely.

What is claimed is:

1. An image reading apparatus comprising:

a first image reading chip for reading an image of a first surface of a medium; and

a second image reading chip for reading an image of a second surface that is different from the first surface of the medium,

wherein the first image reading chip includes:

a first pixel portion that is configured to output a first pixel signal and includes a first light-receiving element that receives light from the first surface and photoelectrically converts the light to the first pixel signal;

a first output circuit that can perform driving with one of a plurality of drive capabilities including a first drive capability, and is configured to output a signal based on the first pixel signal; and

a first output selection unit configured to cause the first output circuit to perform driving with the first drive capability,

the second image reading chip includes:

a second pixel portion that is configured to output a second pixel signal and includes a second light-receiving element that receives and photoelectrically converts light from the second surface;

a second output circuit that can output a signal based on the second pixel signal with one of a plurality of drive capabilities including a second drive capability that is different from the first drive capability; and

a second output selection unit configured to cause the second output circuit to perform driving with the second drive capability.

2. The image reading apparatus according to claim 1, further comprising:
a control substrate;
a first wire that electrically connects the first image reading chip and the control substrate; and
a second wire that electrically connects the second image reading chip and the control substrate and is longer than the first wire,
wherein a signal that is based on the first pixel signal output from the first output circuit is transferred to the control substrate by being transmitted through the first wire,
a signal that is based on the second pixel signal output from the second output circuit is transferred to the control substrate by being transmitted through the second wire, and
the second drive capability is larger than the first drive capability.

3. The image reading apparatus according to claim 1, wherein
the first image reading chip includes a first terminal,
the first output selection unit selects the drive capability of the first output circuit based on a signal input to the first terminal,
the second image reading chip includes a second terminal, and
the second output selection unit selects the drive capability of the second output circuit based on a signal input to the second terminal.

4. The image reading apparatus according to claim 3, further comprising
a control unit configured to control operation of the first image reading chip and the second image reading chip,
wherein at least one of the signal input to the first terminal and the signal input to the second terminal is transferred from the control unit.

5. The image reading apparatus according to claim 3, wherein
at least one of the signal input to the first terminal and the signal input to the second terminal is a signal for setting the drive capability and for setting a resolution for reading the image.

6. The image reading apparatus according to claim 3, wherein
at least one of the first terminal and the second terminal is electrically connected to a voltage source that outputs a fixed voltage.

7. The image reading apparatus according to claim 1, wherein
the first drive capability is the smallest among the plurality of drive capabilities of the first output circuit.

8. The image reading apparatus according to claim 1, wherein
the first image reading chip and the second image reading chip are chips of the same type.

9. An image reading apparatus comprising:
a first module substrate;
a first image reading chip for reading an image of a first surface of a medium and is disposed on the first module substrate;
a second module substrate;
a second image reading chip for reading an image of a second surface that is different from the first surface of the medium and is disposed on the second module substrate;
a control substrate;
a processor that is disposed on the control substrate,
a first wire that electrically connects the first module substrate and the control substrate; and
a second wire that electrically connects the second module substrate and the control substrate and is longer than the first wire,
wherein the first image reading chip includes:
a first pixel circuit that is configured to output a first pixel signal and includes a first light-receiving element that receives light from the first surface and photoelectrically converts the light to the first pixel signal;
a first output circuit that can perform driving with one of a plurality of drive capabilities including a first drive capability, and is configured to output a first signal based on the first pixel signal; and
a first output selection unit configured to cause the first output circuit to perform driving with the first drive capability,
the second image reading chip includes:
a second pixel circuit that is configured to output a second pixel signal and includes a second light-receiving element that receives and photoelectrically converts light from the second surface;
a second output circuit that can output a second signal based on the second pixel signal with one of a plurality of drive capabilities including a second drive capability that is greater than the first drive capability; and
a second output selection circuit configured to cause the second output circuit to perform driving with the second drive capability.

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