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(54) **SEMICONDUCTOR DEVICE WITH LOW RESISTIVITY CONTACT STRUCTURE AND METHOD FOR FORMING THE SAME**

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(52) **U.S. Cl.**
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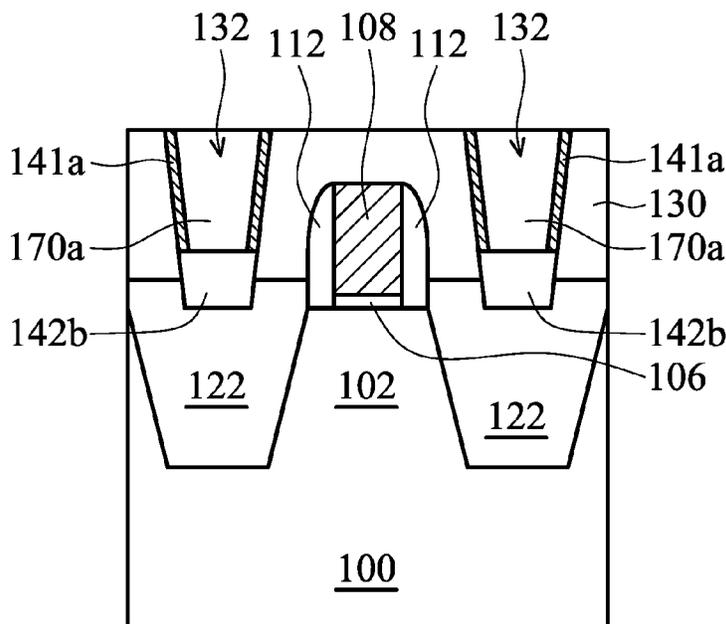
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(51) **Int. Cl.**
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H01L 21/768 (2006.01)
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(57) **ABSTRACT**

A method for forming a semiconductor device structure is provided. The method includes providing a semiconductor substrate including a conductive region made of silicon, germanium or a combination thereof. The method also includes forming an insulating layer over the semiconductor substrate and forming an opening in the insulating layer to expose the conductive region. The method also includes performing a deposition process to form a metal layer over a sidewall and a bottom of the opening, so that a metal silicide or germanide layer is formed on the exposed conductive region by the deposition process. The method also includes performing a first in-situ etching process to etch at least a portion of the metal layer and forming a fill metal material layer in the opening.



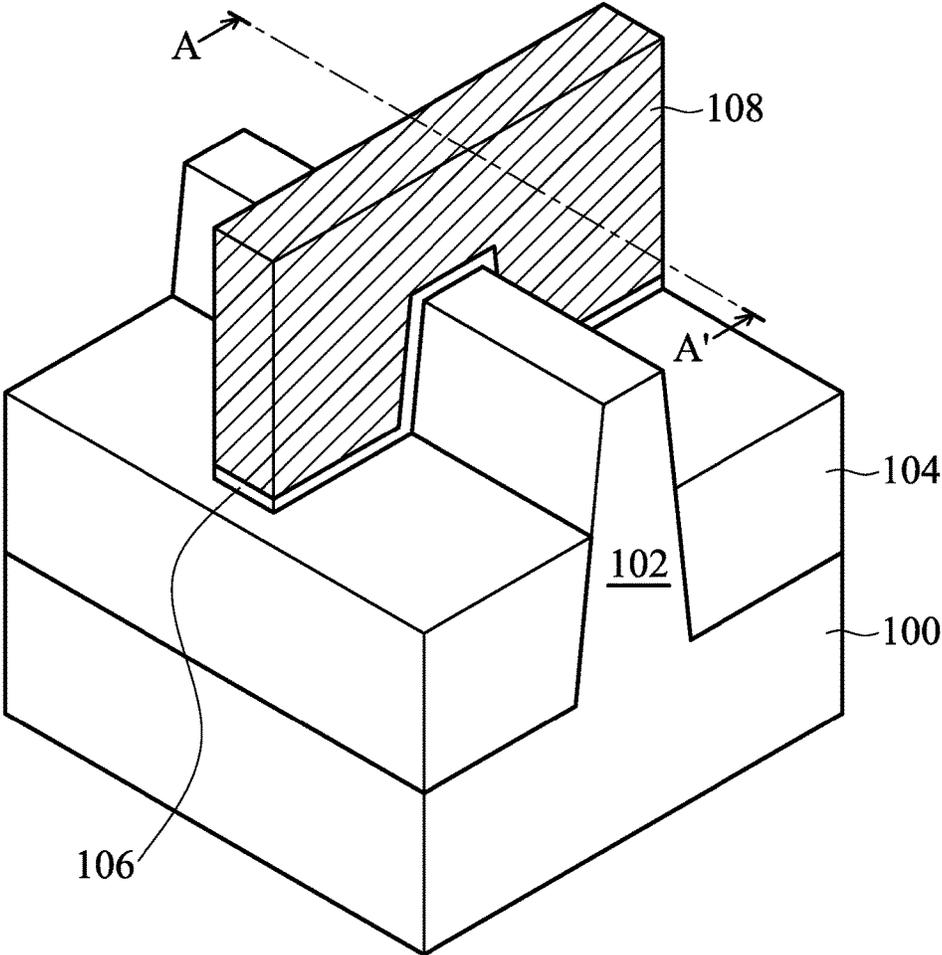


FIG. 1

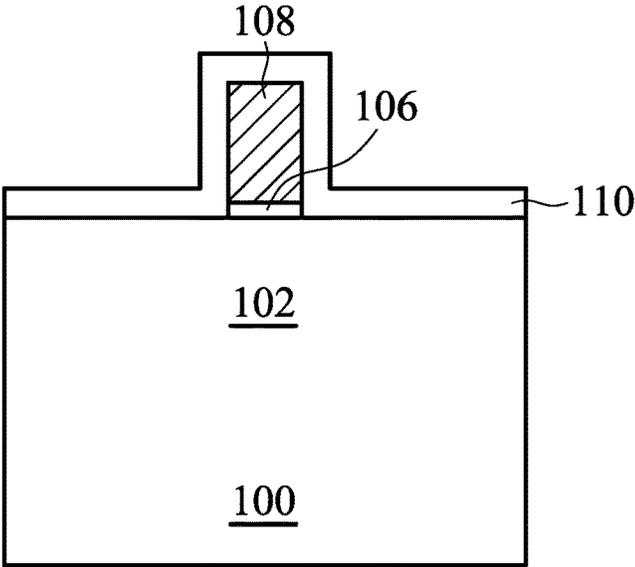


FIG. 2

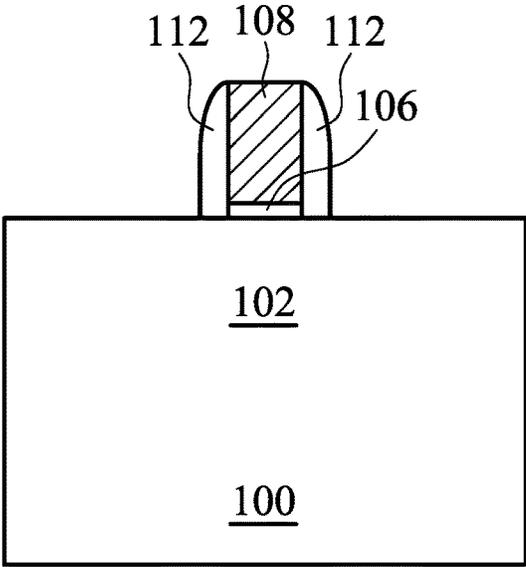


FIG. 3

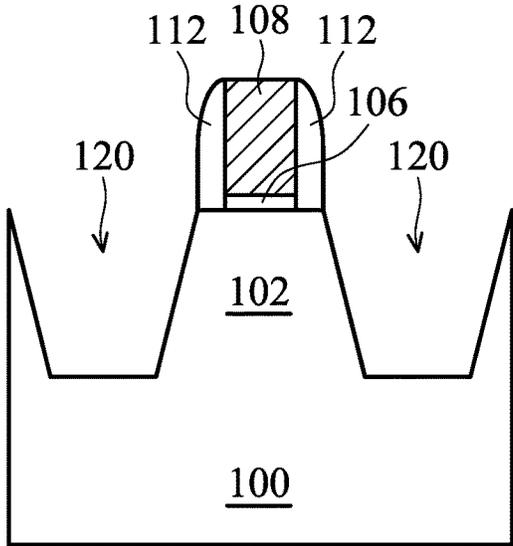


FIG. 4

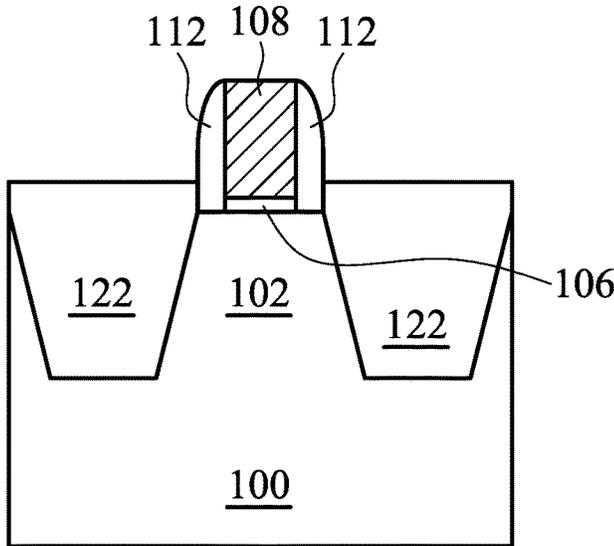


FIG. 5

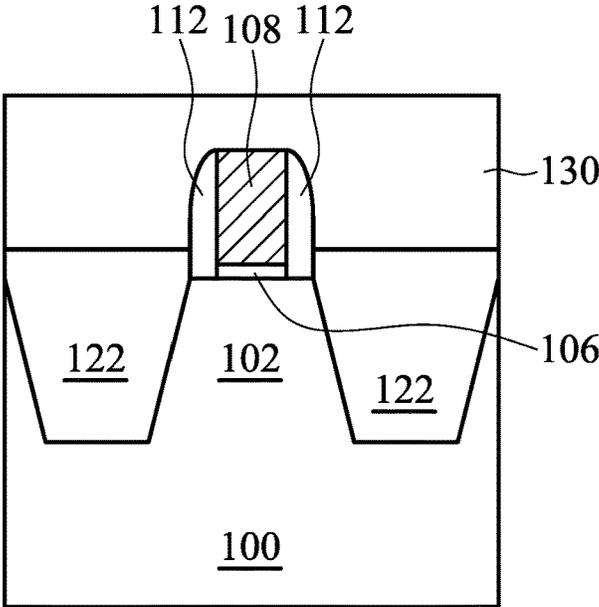


FIG. 6

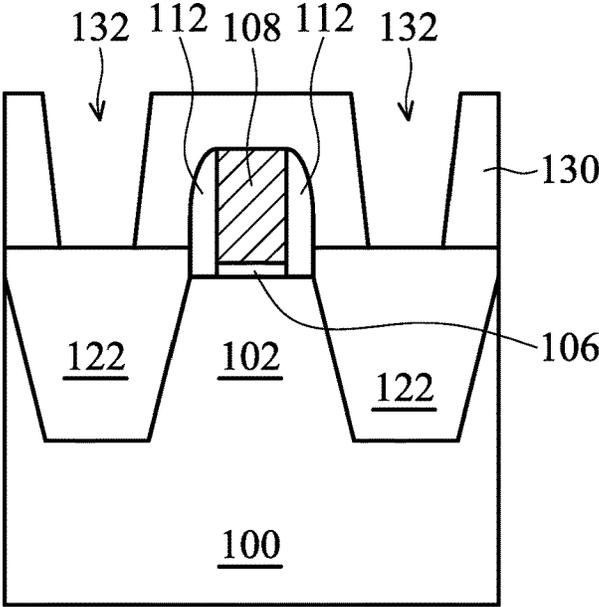


FIG. 7

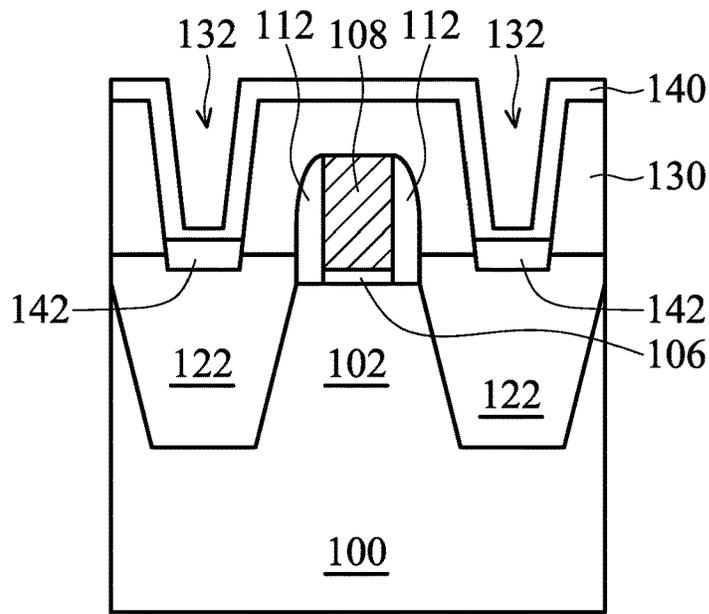


FIG. 8

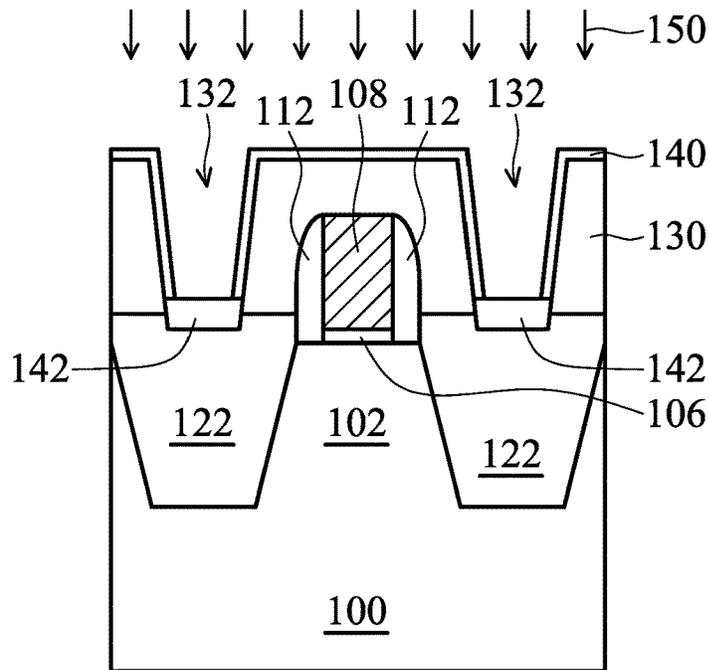


FIG. 9

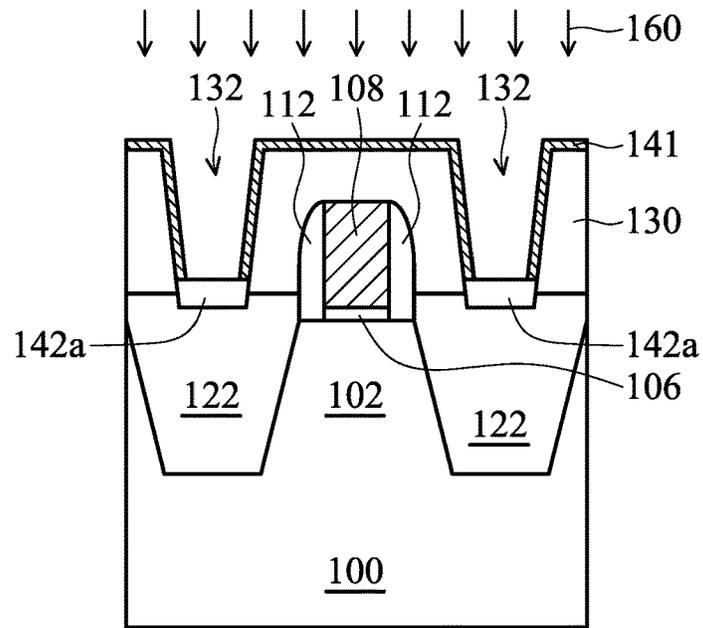


FIG. 10

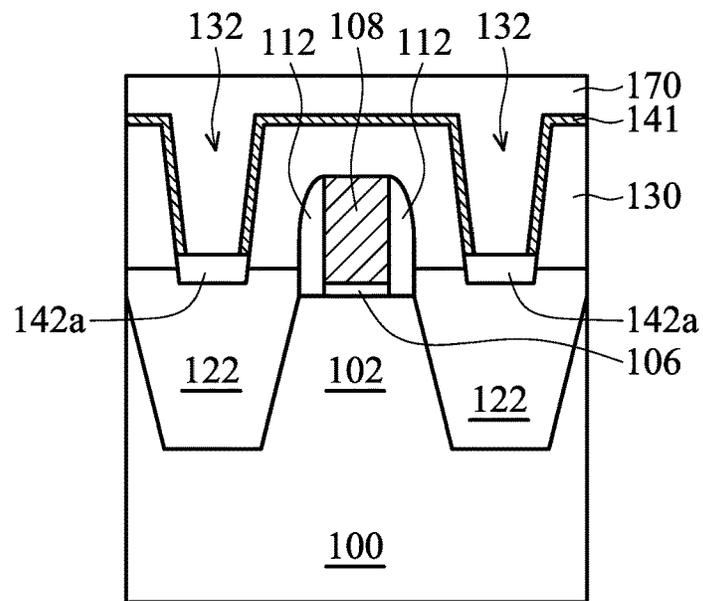


FIG. 11

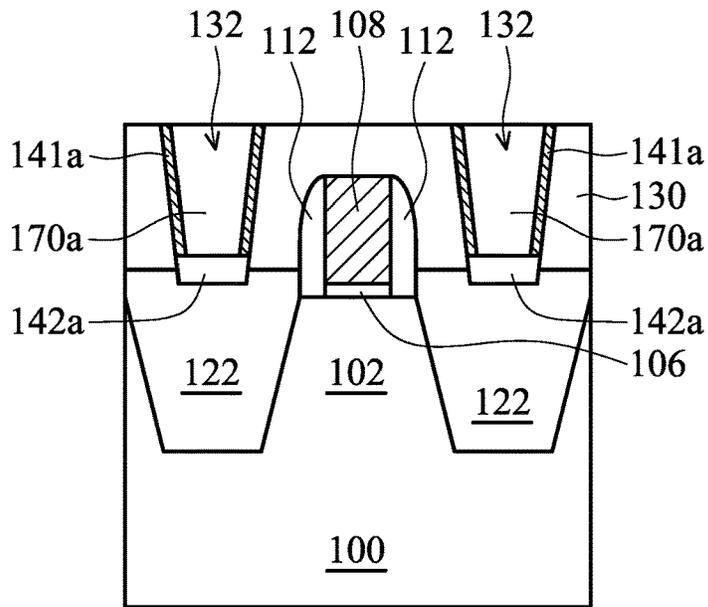


FIG. 12

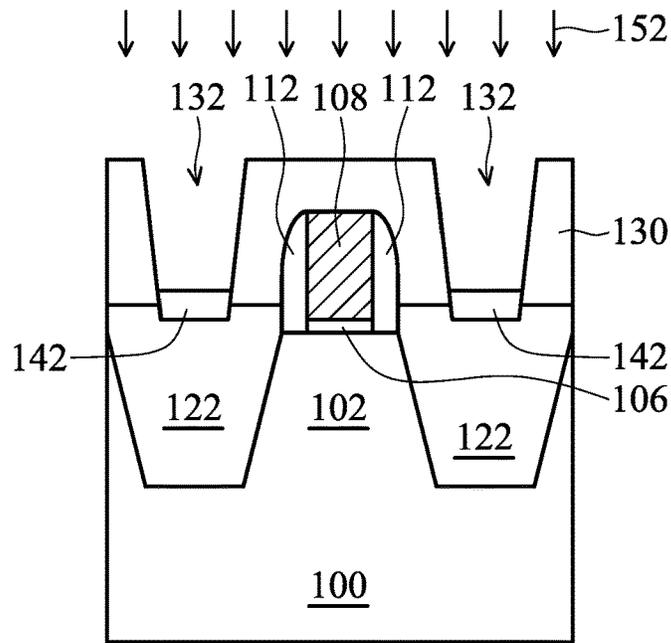


FIG. 13

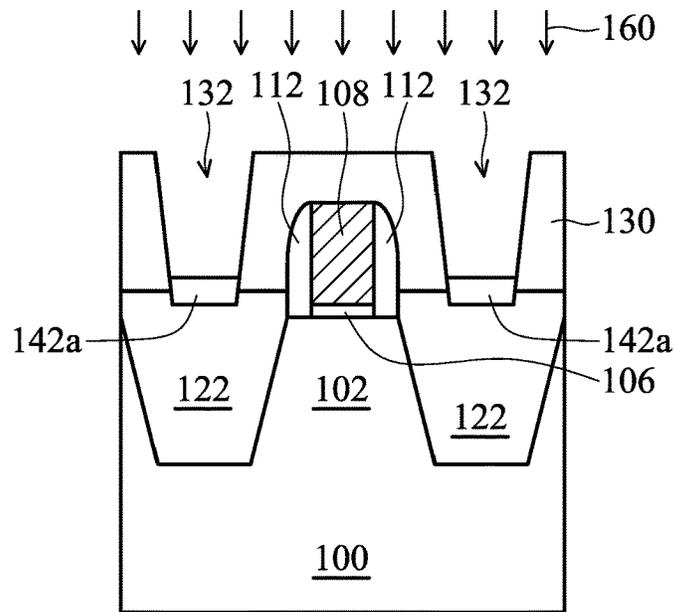


FIG. 14

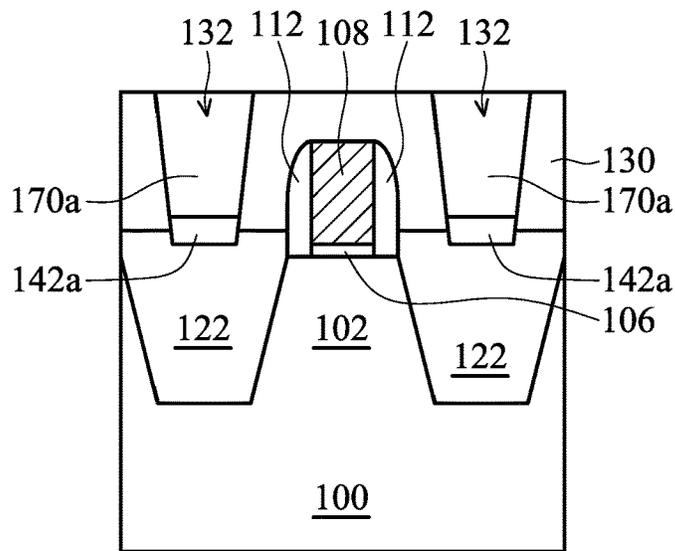


FIG. 15

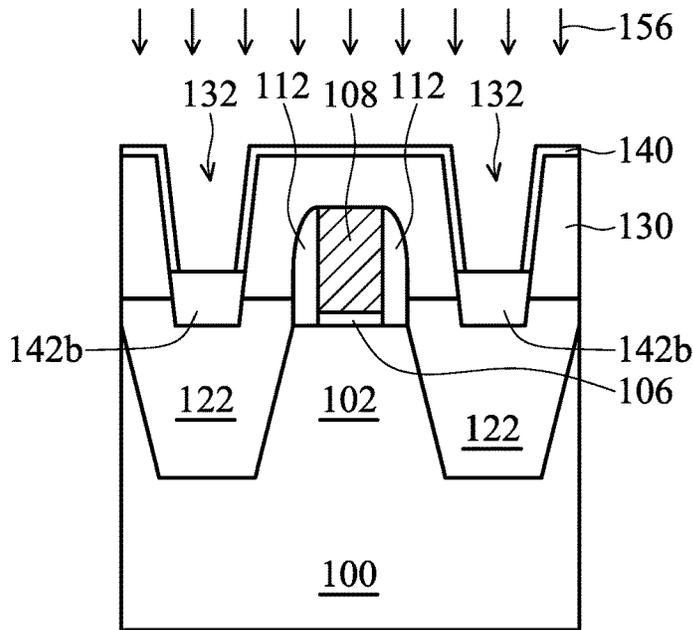


FIG. 16

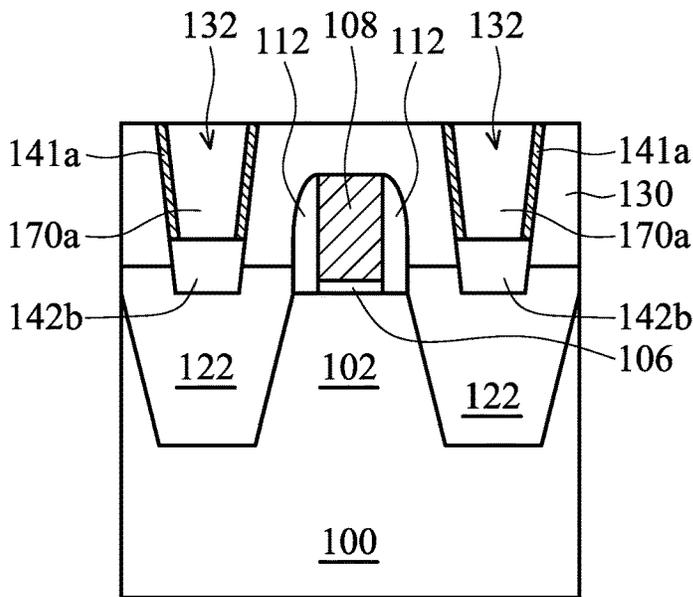


FIG. 17

SEMICONDUCTOR DEVICE WITH LOW RESISTIVITY CONTACT STRUCTURE AND METHOD FOR FORMING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 62/563,795 filed on Sep. 27, 2017, the entirety of which is incorporated by reference herein.

BACKGROUND

[0002] The semiconductor integrated circuit (IC) industry has experienced rapid growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. As the semiconductor industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design issues have resulted in the development of three-dimensional designs, such as the fin field effect transistor (FinFET). FinFETs are fabricated with a thin vertical “fin” (or fin structure) extending from a substrate. The channel of the FinFET is formed in this vertical fin. A gate is provided over three sides (e.g., wrapping) the fin. Advantages of the FinFET may include reducing the short channel effect and raising the current flow.

[0003] Although existing FinFETs and methods of fabricating FinFETs have been generally adequate for their intended purposes, they have not been entirely satisfactory in all respects. For example, as the size of FinFET device structure has been reduced, problems (e.g., poor step coverage, opening overhang, void formation, and increased contact resistance) may occur when contact metal materials are filled into contact openings (e.g., vias or trenches) with small critical dimension (CD). Therefore, it is a challenge to form reliable contact structures at smaller and smaller sizes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It should be noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. 1 is schematic an intermediate semiconductor device structure with a fin in a three-dimensional view in accordance with some embodiments;

[0006] FIGS. 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12 are cross-sectional views of various intermediate stages showing a method of forming the semiconductor device structure with a fin taken along line A-A' in FIG. 1 in accordance with some embodiments;

[0007] FIGS. 13, 14, and 15 are cross-sectional views of various intermediate stages showing a method of forming the semiconductor device structure with a fin in accordance with some embodiments; and

[0008] FIGS. 16 and 17 are cross-sectional views of various intermediate stages showing a method of forming the semiconductor device structure with a fin in accordance with some embodiments.

DETAILED DESCRIPTION

[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows includes embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. The present disclosure may repeat reference numerals and/or letters in some various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between some various embodiments and/or configurations discussed.

[0010] Furthermore, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0011] Some embodiments of the disclosure are described. Additional operations can be provided before, during, and/or after the stages described in these embodiments. Some of the stages that are described can be replaced or eliminated for different embodiments. Additional features can be added to the semiconductor device structure. Some of the features described below can be replaced or eliminated for different embodiments. Although some embodiments are discussed with operations performed in a particular order, these operations may be performed in another logical order.

[0012] The fins may be patterned using any suitable method. For example, the fins may be patterned using one or more photolithography processes, including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process. For example, in one embodiment, a sacrificial layer is formed over a substrate and patterned using a photolithography process. Spacers are formed alongside the patterned sacrificial layer using a self-alignment process. The sacrificial layer is then removed, and the remaining spacers may then be used to pattern the fins.

[0013] Embodiments of a semiconductor device structure and a method for forming a semiconductor device structure are provided. FIG. 1 is a schematic three-dimensional view showing a semiconductor device structure with a fin in accordance with some embodiments. As shown in FIG. 1, the semiconductor device structure, such as a FinFET structure includes a semiconductor substrate 100, which may be, for example, a part of a wafer. In some embodiments, the semiconductor substrate 100 includes a semiconductor material (e.g., silicon). In some other embodiments, the semiconductor substrate 100 may include another elemen-

tary semiconductor, such as germanium; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP, or a combination thereof. Alternatively, the semiconductor substrate **100** is a semiconductor on insulator (SOI).

[0014] In some embodiments, the semiconductor substrate **100** includes at least a fin **102** formed therein. The fin **102** may be formed in the semiconductor substrate **100** by etching trenches in the semiconductor substrate **100**. The etching may be a reactive ion etching (RIE), neutral beam etching (NBE), the like, or a combination thereof. In some embodiments, the fin **102** may include silicon, silicon germanium, silicon carbide, pure or substantially pure germanium, a III-V compound semiconductor, a II-VI compound semiconductor, or the like. For example, the available materials for forming III-V compound semiconductor include, but are not limited to, InAs, AlAs, GaAs, InP, GaN, InGaAs, InAlAs, GaSb, AlSb, AlP, GaP, and the like. A person of ordinary skill in the art will readily understand other methods of forming the fin, which are contemplated within the scope of some embodiments.

[0015] In some embodiments, the semiconductor device structure further includes isolation regions may be positioned on opposite sides of the fin **102**. In some embodiments, each of the isolation regions includes an isolation feature **104** and a liner structure (not shown) covering the sidewall and the bottom of the isolation feature **104**, so that the semiconductor substrate **100** and the lower portion of the fin **102** are spaced apart from the isolation features **104** by the liner structures.

[0016] In some embodiments, the isolation feature **104** is made of a dielectric material, such as silicon oxide, fluoride-doped silicate glass (FSG), a low-k dielectric material, and/or another suitable insulating material. The isolation features **104** may be shallow trench isolation (STI) features. In some embodiments, the liner structure may include a single layer or a multiple structure and may be made of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide (SiC), or a combination thereof.

[0017] In some embodiments, the semiconductor device structure further includes a gate structure positioned over the semiconductor substrate **100**. The gate structure may be across the fin **102**. In some embodiments, the gate structure may include a gate dielectric layer, a gate electrode layer, and/or one or more additional layers (not shown). For example, the gate structure may include an interfacial layer (not shown), a gate dielectric layer **106** and a gate electrode layer **108** including work function layer(s) and a fill metal layer. In some embodiments, the interfacial layer may include a dielectric material such as silicon oxide layer (SiO₂) or silicon oxynitride (SiON). The gate dielectric layer **106** may include silicon dioxide or another suitable dielectric material. Alternatively, the gate dielectric layer **106** may include a high-k dielectric layer such as HfO₂, TiO₂, HfZrO, Ta₂O₃, HfSiO₄, ZrO₂, ZrSiO₂, or a combination thereof. An exemplary p-type work function metal may include TiN, TaN, Ru, Mo, Al, WN, ZrSi₂, MoSi₂, TaSi₂, NiSi₂, WN, or a combination thereof. An exemplary n-type work function metal may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, or a combination thereof. The fill metal layer

may be made of a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof, or multi-layers thereof.

[0018] Although not depicted, a P well or an N well may be formed in various regions of the semiconductor substrate **100** by, for example, an ion implantation process followed by an annealing process. In some embodiments, a p-type impurity implantation may be performed in the NFET region. The p-type impurities may be boron, BF₂, implanted in the NFET region to a concentration between about 10¹⁵ cm⁻³ and about 7×10¹⁸ cm⁻³. An n-type impurity implant may be performed in the PFET region. The n-type impurities may be phosphorus or arsenic, implanted in the PFET region to a concentration between about 10¹⁵ cm⁻³ and about 7×10¹⁸ cm⁻³. The implantations may form a p-well in the NFET region or an n-well in the PFET region.

[0019] FIGS. **2, 3, 4, 5, 6, 7, 8, 9, 10, 11,** and **12** are cross-sectional views of various intermediate stages showing a method of forming the semiconductor device structure with a fin taken along line A-A' in FIG. **1** in accordance with some embodiments. As shown in FIG. **2**, a spacer layer **110** is conformally formed over the intermediate semiconductor device structure in FIG. **1** in accordance with some embodiments. The spacer layer **110** is illustrated as being conformally over the surface of the fin **102** and along sidewalls and a top surface of the gate structure including the gate electrode **108**. In some embodiments, the spacer layer **110** may be silicon nitride (SiN), silicon carbon-nitride (SiCN), silicon carbon-oxynitride (SiCON), the like, or a combination thereof, formed by a deposition process, such as a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, the like, or a combination thereof.

[0020] As shown in FIG. **3**, an anisotropic etching process is performed on the spacer layer **110** shown in FIG. **2** in accordance with some embodiments. As a result, spacers **112** are formed on opposite sidewalls of the gate structure, e.g., at least adjacent to the gate electrode **108**. In some embodiments, the etching process may be a reactive ion etching (RIE) process, an inductively coupled plasma (ICP) etching process, a transformer coupled plasma (TCP) etching process, a high density plasma (HDP) etching process, an electron cyclotron resonance (ECR) etching process, the like, or a combination thereof.

[0021] As shown in FIG. **4**, portions of the fin **102** uncovered by the spacers **112** and the gate structure including the gate dielectric layer **106** and the gate electrode layer **108** are etched in accordance with some embodiments. For example, the portions of the fin **102** are etched using an isotropic etching process, such as a wet etching process. In some embodiments, the wet etching process may use hydrofluoric (HF) acid, buffered oxide etch (BOE), or the like as an etchant. In other embodiments, multiple etch process steps comprising different etchants may be used. After the isotropic etching process is performed, recesses **120** are formed in the fin **102** on opposite sides of the gate structure. The depth of the recess **120** may be between about 5 nm and about 150 nm from the original top surface of the fin **102** to an upper surface of a remaining portion of the fin **102**.

[0022] As shown in FIG. **5**, a conductive region **122** is formed in each of the recesses **120** shown in FIG. **4** in accordance with some embodiments. For example, an epitaxial growth process is performed to form the conductive regions **122** in the recesses **120**. In some embodiments, the conductive regions **122** serve as source/drain regions and

sometimes are referred to as raised epitaxial source/drain regions. The conductive regions **122** (i.e., raised epitaxial source/drain regions) are grown from the upper surfaces of the remaining portions of the fin **102** in the recesses **120** and above the recesses **102**.

[0023] In some embodiments, the raised epitaxial source/drain regions (i.e., the conductive region **122**) may be made of silicon, germanium, silicon germanium, silicon carbide, indium phosphide (InP), gallium arsenide (GaAs), the like, or a combination thereof. In some embodiments, the raised epitaxial source/drain regions (i.e., the conductive region **122**) may be formed using metal-organic CVD (MOCVD), molecular beam epitaxy (MBE), liquid phase epitaxy (LPE), vapor phase epitaxy (VPE), selective epitaxial growth (SEG), the like, or a combination thereof. In some embodiments, the raised epitaxial source/drain regions (i.e., the conductive region **122**) may be doped by in-situ doping during growth and/or subsequent implantation. In those cases, the raised epitaxial source/drain regions may have a doping concentration of greater than or equal to $5 \times 10^{19} \text{ cm}^{-3}$. The dopants for a p-type transistor may include boron, indium, or the like, and those for an n-type transistor may include phosphorus, arsenic, or the like.

[0024] As shown in FIG. 6, an insulating layer **130** is formed over the structure illustrated in FIG. 5 in accordance with some embodiments. In some embodiments, the insulating layer **130** is an inter-layer dielectric (ILD) layer that may be formed of a dielectric material such as silicon oxide, tetraethyl orthosilicate (TEOS), phosphosilicate glass (PSG), borosilicate glass (BSG), boron-doped phosphosilicate Glass (BPSG), fluorinated silicate glass (FSG), undoped silicate glass (USG), or the like, and may be deposited by any suitable method, such as CVD, plasma enhanced CVD (PECVD), flowable CVD (FCVD), the like, or a combination thereof. In some embodiments, ILD layer may be a single layer or include multiple dielectric layers with the same or different dielectric materials. Moreover, the ILD layer has a thickness in a range from about 4000 Å to about 8000 Å.

[0025] As shown in FIG. 7, contact openings **132** (such as via holes or trenches) are formed in the insulating layer **130** to expose the corresponding conductive regions **122** (i.e., the raised epitaxial source/drain regions) in accordance with some embodiments. As one example, the formation of the contact openings **132** includes forming a photoresist layer (not shown) over the insulating layer **130** (i.e., the ILD layer) by a suitable process, such as spin-on coating, patterning the layer of photoresist to form a patterned photoresist feature by a proper photolithography method, etching the exposed insulating layer **130** (for example, by a dry etching, wet etching, and/or plasma etching process) to remove portions of the insulating layer **130** to expose a portion of the raised epitaxial source/drain regions (i.e., the conductive regions **122**). In some embodiments, the etching is a wet etching that uses a dilute HF (DHF) acid, BOE, phosphoric acid (H_3PO_4), or the like as an etchant. As a result, the contact openings **132** are over the raised epitaxial source/drain regions. The etching may remove at least a portion of the raised epitaxial source/drain regions (i.e., the conductive regions **122**), and hence, more surface area of the raised epitaxial source/drain regions may be exposed. The patterned photoresist layer may be stripped thereafter.

[0026] As shown in FIG. 8, after formation of the contact openings **132** in the insulating layer **130** (i.e., the ILD layer),

the structure in FIG. 8 is produced by performing a deposition process to form a conformal metal layer **140** over a sidewall and a bottom of each of the contact openings **132** in accordance with some embodiments. In some embodiments, the metal layer **140** may be formed of Ti, Al, Zr, Hf, Ta, Co, Ni, Y, and may be formed by, for example, a CVD, ALD or electrochemical plating (ECP) process. In some embodiments, the deposition process is performed at a temperature lower than 600° C. in order to form silicide or germanide. For example, the deposition process is performed at a temperature of about 350° C. to about 500° C. If the process temperature less than 350° C., precursor or by-product will be the residual on wafer. Moreover, the used power for the deposition process may be in a range from about 150 W to about 1500 W. While the deposition process is being performed, the metal layer **140** reacts with the semiconductor material of the exposed the conductive regions **122** (i.e., the raised epitaxial source/drain regions), so as to form a metal silicide or germanide layer **142** on each of the exposed the conductive regions **122**. That is, the metal silicide or germanide layer **142** is formed due to the deposition process. Therefore, after performing the deposition process, no annealing process is needed for formation of the metal silicide or germanide on the exposed epitaxial source/drain regions. Due to the formation of the metal silicide or germanide layer **142**, the thickness of the metal layer **140** over the sidewall of the opening **132** is greater than that of the metal layer **140** over the bottom of the contact opening **132**, as shown in FIG. 8. The deposition including CVD, ALD or ECP provides excellent step coverage in the contact opening **132**, so as to increase the contact area between the metal layer **140** and the exposed conductive region **122**. As a result, the contact resistance between the conductive region **122** and the subsequently formed fill metal material layer is reduced.

[0027] As shown in FIG. 9, after the metal layer **140** is formed, an in-situ etching process **150** is performed to etch back at least a portion of the metal layer **140** in accordance with some embodiments. In some embodiments, the in-situ etching process **150** is a dry etching process using a metal halide as a process gas. For example, the metal layer **140** is made of titanium (Ti), and the process gas includes titanium tetrachloride (TiCl_4), titanium tetrafluoride (TiF_4), titanium tetrabromide (TiBr_4) or titanium tetraiodide (TiI_4). In this case, the flow rate of metal halide is in a range from about 2 sccm to about 50 sccm depending on the deposition rate. Moreover, plasma power is sometimes applied when the in-situ etching process **150** is performed. For an example, the plasma power is substantially equal to or less than 300 W. In some embodiments, the process gas for the in-situ etching process **150** may further include hydrogen (H_2) and the flow rate of hydrogen is substantially equal to or less than 50 sccm.

[0028] After the in-situ etching process **150** is performed, the metal layer **140** on the sidewall of the contact opening **132** is thinned, so that the critical dimension (CD) loss of the contact opening **132** due to the formation of the metal layer **140** is mitigated. That is, the opening overhang or the void formation during the subsequent metal filling process can be eliminated or mitigated. Since the thickness of the metal layer **140** on the sidewall of the contact opening **132** is greater than that of the metal layer **140** on the bottom of the contact opening **132**, the portion of the metal layer **140** on the bottom of the contact opening **132** may be entirely

removed after the in-situ etching process 150 is performed, such that the metal silicide or germanide layer 142 is exposed, as shown in FIG. 9.

[0029] In some other embodiments, after the in-situ etching process 150 is performed, an optional second in-situ etching process (not shown) is performed, so that the etched metal layer 140 is thinned further. In those cases, the second in-situ etching process is similar to the previous in-situ etching process 150. For example, the second in-situ etching process is also performed using metal halide and hydrogen as a process gas, in which the flow rate of metal halide may be in a range from about 10 sccm to 50 sccm and the flow rate of hydrogen may be in a range from about 10 sccm to 500 sccm. Unlike the previous in-situ etching process 150, the second in-situ etching process is performed without applying plasma power. After the second in-situ etching process is performed, the etched metal layer 140 shown in FIG. 9 may be entirely etched or removed.

[0030] As shown in FIG. 10, after the in-situ etching process 150 is performed, an in-situ nitridation treatment 160 is performed on the sidewall and the bottom of the contact opening 132 in accordance with some embodiments. As a result, a nitrogen-containing metal silicide or germanide layer 142a is formed over the bottom of each of the contact openings 132 by performing the in-situ nitridation treatment 160 on the metal silicide or germanide layer 142 shown in FIG. 9. At the same time, a liner 141 including a metal nitride region is formed over the sidewall of each of the contact openings 132 by performing the in-situ nitridation treatment 160 on the etched metal layer 140 shown in FIG. 9.

[0031] In some embodiments, the metal nitride region is formed on the surface of the etched metal layer 140 shown in FIG. 9, so that the liner 141 includes a metal (e.g., Ti) portion in direct contact with the sidewall of the contact openings 132. In some embodiments, the etched metal layer 140 shown in FIG. 9 is entirely nitrided, such that the entire liner 141 forms a metal nitride (e.g., TiN) region, as shown in FIG. 10. The formed liner 141 may serve as an adhesion layer, a diffusion barrier layer, and an oxygen blocking layer for subsequent metal filling process.

[0032] In some embodiments, the in-situ nitridation treatment 160 is performed at a temperature of about 350° C. to about 500° C. for 30 sec to 300 sec. Moreover, the in-situ nitridation treatment 160 is performed using ammonia (NH₃) and nitrogen (N₂) as a process gas.

[0033] As shown in FIG. 11, following formation of the liner 141, a fill metal material layer 170 covers the liner 141 above the insulating layer 130 and fills the contact openings 132 to cover the liner 141 and the nitrogen-containing metal silicide or germanide layer 142a in each of the contact openings 132 in accordance with some embodiments. As a result, the liner 141 is interposed between the insulating layer 130 and the sidewall of the fill metal material layer 170. Moreover, the nitrogen-containing metal silicide or germanide layer 142a is interposed between the bottom of the fill metal material layer 170 and the top of the conductive regions 122 (i.e., the raised epitaxial source/drain regions). In some embodiments, the fill metal material layer 170 is made of cobalt (Co), tungsten (W), copper (Cu), nickel (Ni), or aluminum (Al). In some embodiments, the fill metal material layer 170 is formed by a deposition process, such as CVD, ECP, ALD, or other suitable deposition. The fill

metal material layer 170 is thus deposited until each of the contact openings 132 is substantially filled or over-filled.

[0034] As shown in FIG. 12, a planarization process is performed on the fill metal material layer 170 shown in FIG. 11 in accordance with some embodiments. In some embodiments, the fill metal material layer 170 is planarized by a chemical-mechanical planarization (CMP) process, but any other suitable polishing or etching back process may be used. The planarization process removes a portion of the fill metal material layer 170 and a portion of the liner 141 outside of the contact opening 132 and stops when reaching the insulating layer 130, so as to provide a substantially planar surface. After the planarization process is performed, the remaining liner 141a and the remaining fill metal material layer 170a in each of the contact openings 132 form a contact structure over the conductive region 122 (i.e., raised epitaxial source/drain region).

[0035] Following the formation of the contact structures in the contact openings 132, dielectric layers, such as inter-metal dielectric (IMD) layers, which may include metallization patterns, and any corresponding etch stop layers, may be formed over the insulating layer (i.e., the ILD layer) 130. A person of ordinary skill in the art will understand the additional processing that the structures in the figures may undergo, and hence, explicit discussion thereof is omitted herein for brevity.

[0036] FIGS. 13, 14, and 15 are cross-sectional views of various intermediate stages showing a method of forming the semiconductor device structure with a fin in accordance with some embodiments. Elements in FIGS. 13, 14, and 15 that are the same as those in FIGS. 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12 are labeled with the same reference numbers as in FIGS. 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12 and may not be described again for brevity. As shown in FIG. 13, a structure as shown in FIG. 8 is provided and an in-situ etching process 152 is then performed to entirely remove the metal layer 140 in accordance with some embodiments. In some embodiments, the in-situ etching process 152 is similar to the in-situ etching process 150 shown in FIG. 9. For example, the in-situ etching process 152 is also performed using metal halide and hydrogen as a process gas, in which the flow rate of metal halide may be in a range from about 10 sccm to about 50 sccm and the flow rate of hydrogen may be in a range from about 10 sccm to about 500 sccm. Unlike the in-situ etching process 150, the in-situ etching process 152 is performed without applying plasma power.

[0037] After the in-situ etching process 152 is performed, the metal layer 140 in the structure as shown in FIG. 8 may be entirely etched or removed, as shown in FIG. 13. For an example, the metal layer 140 is made of titanium (Ti), and the metal halide in the process gas for the in-situ etching process 152 includes TiCl₄, TiF₄, TiBr₄ or TiI₄. In those cases, since the metal layer 140 is entirely removed after the in-situ etching process 152 is performed, the CD loss of the contact opening 132 due to the formation of the metal layer 140 may be mitigated.

[0038] As shown in FIG. 14, after the in-situ etching process 152 is performed, an optional in-situ nitridation treatment 160 is performed on the sidewall and the bottom of the contact opening 132 in accordance with some embodiments. As a result, a nitrogen-containing metal silicide or germanide layer 142a is formed over the bottom of each of the contact openings 132. In some embodiments, the in-situ nitridation treatment 160 is performed at a temperature of

about 350° C. to about 500° C. for 30 sec to 300 sec. Moreover, the in-situ nitridation treatment **160** is performed using ammonia (NH₃) and nitrogen (N₂) as a process gas.

[0039] As shown in FIG. **15**, after the in-situ nitridation treatment **160** is performed, a contact structure is formed in each of the contact openings **132** in accordance with some embodiments. For example, a fill metal material layer (not shown) that may be similar to or the same as the fill metal material layer **170** shown in FIG. **11** is formed to cover the insulating layer **130** and to fill the contact openings **132** in accordance with some embodiments. In those cases, the material and the formation of the fill metal material layer may be the same as or similar to those of the fill metal material layer **170** shown in FIG. **11**.

[0040] Following the formation of the fill metal material layer, the fill metal material layer is planarized by a CMP process, but any other suitable polishing or etching back process may be used. As a result, a substantially planar surface is provided. The remaining fill metal material layer **170a** in each of the contact openings **132** forms the contact structure that is in direct contact with the insulating layer **130** and the nitrogen-containing metal silicide or germanide layer **142a** over the conductive region **122** (i.e., the raised epitaxial source/drain region).

[0041] Similarly, IMD layers may be formed over the insulating layer (i.e., the ILD layer) **130**. A person of ordinary skill in the art will understand the additional processing that the structures in the figures may undergo, and hence, explicit discussion thereof is omitted herein for brevity.

[0042] FIGS. **16** and **17** are cross-sectional views of various intermediate stages showing a method of forming the semiconductor device structure with a fin in accordance with some embodiments. Elements in FIGS. **16** and **17** that are the same as those in FIGS. **2**, **3**, **4**, **5**, **6**, **7**, **8**, **9**, **10**, **11**, and **12** are labeled with the same reference numbers as in FIGS. **2**, **3**, **4**, **5**, **6**, **7**, **8**, **9**, **10**, **11**, and **12** and may not be described again for brevity. As shown in FIG. **16**, a structure as shown in FIG. **9** is provided and one or more cycle processes **156** that includes a deposition process for formation of the metal layer **140** (as shown in FIG. **8**) and an in-situ etching process **150** (as shown in FIG. **9**) is then performed to etch the metal layer **140** and increase the thickness of the metal silicide or germanide layer **142** in accordance with some embodiments.

[0043] In some embodiments, the cycle process **156** further includes an optional second in-situ etching process after the in-situ etching process **150** is performed, so that the metal layer **140** etched by the in-situ etching process **150** is thinned further. In those cases, the second in-situ etching process is similar to the in-situ etching process **150**. For example, the second in-situ etching process is also performed using metal halide and hydrogen as a process gas, in which the flow rate of metal halide may be in a range from about 10 sccm to about 50 sccm and the flow rate of hydrogen may be in a range from about 10 sccm to about 500 sccm. Unlike the previous in-situ etching process **150**, the second in-situ etching process is performed without applying plasma power.

[0044] In some embodiments, the number of the cycle process **156** is based on the desired thickness of the formed metal silicide or germanide layer **142**. Namely, the cycle process **156** may be repeated until the thickness of the metal silicide or germanide layer **142** reach to a target thickness.

[0045] As shown in FIG. **17**, after the cycle process **156** is performed, an in-situ nitridation treatment (not shown) is performed on the sidewall and the bottom of the contact opening **132** in accordance with some embodiments. As a result, a nitrogen-containing metal silicide or germanide layer **142a** is formed over the bottom of each of the contact openings **132**. At the same time, a liner (not shown) including a metal nitride region is also formed over the sidewall of each of the contact openings **132**. In some embodiments, the metal nitride region is formed on the surface of the liner, so that the liner includes a metal (e.g., Ti) portion in direct contact with the sidewall of the contact openings **132**. In some embodiments, the metal layer **140** formed after performing the cycle process **156** is entirely nitrided, such that the entire liner **141** forms a metal nitride (e.g., TiN) region. The formed liner may serve as an adhesion layer and a diffusion barrier layer for subsequent metal filling process. In some embodiments, the in-situ nitridation treatment may be similar to or the same as the in-situ nitridation treatment **160** (shown in FIG. **10**). For example, the in-situ nitridation treatment is performed at a temperature of about 350° C. to about 500° C. for 30 sec to 300 sec. Moreover, the in-situ nitridation treatment **160** is performed using ammonia (NH₃) and nitrogen (N₂) as a process gas.

[0046] After the in-situ nitridation treatment is performed, a contact structure is formed in each of the contact openings **132** in accordance with some embodiments. For example, a fill metal material layer (not shown) that may be similar to or the same as the fill metal material layer **170** shown in FIG. **11** is formed to cover the insulating layer **130** and to fill the contact openings **132** in accordance with some embodiments. In those cases, the material and the formation of the fill metal material layer may be the same as or similar to those of the fill metal material layer **170** shown in FIG. **11**.

[0047] Following the formation of the fill metal material layer, the fill metal material layer is planarized by a CMP process, but any other suitable polishing or etching back process may be used. As a result, a substantially planar surface is provided. The remaining liner **141a** and the remaining fill metal material layer **170a** in each of the contact openings **132** form the contact structure that is in direct contact with the insulating layer **130** and the nitrogen-containing metal silicide or germanide layer **142a** over the conductive region **122** (i.e., the raised epitaxial source/drain region).

[0048] Similarly, IMD layers may be formed over the insulating layer (i.e., the ILD layer) **130**. A person of ordinary skill in the art will understand the additional processing that the structures in the figures may undergo, and hence, explicit discussion thereof is omitted herein for brevity.

[0049] Embodiments of a semiconductor device structure and a method for forming the same are provided. The method for forming the semiconductor device structure includes providing a semiconductor substrate that includes a conductive region made of silicon, germanium or a combination thereof. In some embodiments, the semiconductor substrate has a fin and the conductive region is an epitaxial source/drain region in the fin. An insulating layer is formed over the semiconductor substrate and has an opening exposing the conductive region. A deposition process is performed to form a metal layer over a sidewall and the bottom of the opening, so that a metal silicide or germanide layer is formed on the exposed conductive region by the deposition

process. In some embodiments, the deposition process includes CVD. An in-situ etching process is performed to thin the metal layer over the sidewall of the opening. In some embodiments, the metal layer in the opening is entirely removed by the in-situ etching process. Before a fill metal material layer is formed in the opening, an in-situ nitridation treatment is performed on the sidewall and the bottom of the opening, so as to form a liner including a metal nitride region over the sidewall of the opening and a nitrogen-containing metal silicide or germanide layer over the bottom of the opening.

[0050] According to the foregoing embodiments, since the metal layer in the opening is thinned by the in-situ etching process before the fill metal material layer is filled into the opening, the CD loss of the opening can be mitigated and thus a relatively larger volume of the fill metal material layer can be filled into the opening. As a result, the resistance of a contact structure formed of the metal material layer can be reduced and therefore the resistivity of source-drain contact (R_{csd}) is reduced.

[0051] According to the foregoing embodiments, since the metal deposition process including CVD provides excellent step coverage in the opening, the contact area between the metal layer and the exposed conductive region can be increased. As a result, the contact resistance between the conductive region and the fill metal material layer is reduced, so as to reduce the resistivity of source-drain contact (R_{csd}) further.

[0052] According to the foregoing embodiments, a self-aligned and nitrided liner and a nitrogen-containing metal silicide or germanide layer can be formed in the opening by the deposition process and the subsequent in-situ nitridation process, in which the liner may serve as an adhesion layer, a diffusion barrier layer, and an oxygen blocking layer and the silicide or germanide layer may be employed to reduce the contact resistance. Therefore, the process steps can be simplified. For example, there is no need to perform additional deposition processes for formation of the diffusion barrier layer. Moreover, there is no need to perform additional self-aligned silicide (salicide) process for formation of the silicide layer. As a result, the manufacture cost can be reduced.

[0053] In some embodiments, a method for forming a semiconductor device structure is provided. The method includes providing a semiconductor substrate that includes a conductive region made of silicon, germanium or a combination thereof. An insulating layer is formed over the semiconductor substrate. An opening is formed in the insulating layer to expose the conductive region. A deposition process is performed to form a metal layer over a sidewall and a bottom of the opening, so that a metal silicide or germanide layer is formed on the exposed conductive region by the deposition process. A first in-situ etching process is performed to etch at least a portion of the metal layer. A fill metal material layer is formed in the opening.

[0054] In some embodiments, a method for forming a semiconductor device structure is provided. The method includes providing a semiconductor substrate having a fin with an epitaxial source/drain region. The epitaxial source/drain region includes silicon, germanium or a combination thereof. An insulating layer is formed over the fin. A contact opening is formed in the insulating layer to expose the epitaxial source/drain region. A deposition process is performed to form a metal layer over a sidewall and a bottom

of the opening, so that a metal silicide or germanide layer is formed on the exposed epitaxial source/drain region by the deposition process. A first in-situ etching process is performed using a metal halide as a process gas, so as to etch at least a portion of the metal layer. An in-situ nitridation treatment is performed on the sidewall and the bottom of the opening, so as to form a nitrogen-containing metal silicide or germanide layer over the bottom of the opening. A fill metal material layer is formed over the nitrogen-containing metal silicide or germanide layer and in the opening.

[0055] In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes a semiconductor substrate having a conductive region made of silicon, germanium or a combination thereof. An insulating layer overlies the semiconductor substrate. A fill metal material layer is in the insulating layer. A nitrogen-containing metal silicide or germanide layer is formed between the conductive region and the fill metal material layer.

[0056] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method for forming a semiconductor device structure, comprising:
 - providing a semiconductor substrate that comprises a conductive region made of silicon, germanium or a combination thereof;
 - forming an insulating layer over the semiconductor substrate;
 - forming an opening in the insulating layer to expose the conductive region;
 - performing a deposition process to form a metal layer over a sidewall and a bottom of the opening, so that a metal silicide or germanide layer is formed on the exposed conductive region by the deposition process;
 - performing a first in-situ etching process to etch at least a portion of the metal layer; and
 - forming a fill metal material layer in the opening.
2. The method as claimed in claim 1, further comprising performing an in-situ nitridation treatment on the sidewall and the bottom of the opening before forming the metal material and after performing the first in-situ etching process, so as to form a nitrogen-containing metal silicide or germanide layer over the bottom of the opening.
3. The method as claimed in claim 2, wherein a liner comprising a metal nitride region is formed over the sidewall of the opening by performing the in-situ nitridation treatment.
4. The method as claimed in claim 1, wherein plasma power is applied when the first in-situ etching process is performed.

5. The method as claimed in claim 4, further comprising performing a second in-situ etching process without applying plasma power after performing the first in-situ etching process.

6. The method as claimed in claim 5, wherein the metal layer is entirely etched by performing the second in-situ etching process.

7. The method as claimed in claim 1, wherein the first in-situ etching process is performed without applying plasma power.

8. The method as claimed in claim 7, wherein the metal layer is entirely etched by performing the first in-situ etching process.

9. The method as claimed in claim 1, further comprising performing at least one cycle process that comprises the deposition process and the first in-situ etching process prior to formation of the metal material.

10. A method for forming a semiconductor device structure, comprising:

providing a semiconductor substrate having a fin with an epitaxial source/drain region, wherein the epitaxial source/drain region comprises silicon, germanium or a combination thereof;

forming an insulating layer over the fin;

forming a contact opening in the insulating layer to expose the epitaxial source/drain region;

performing a deposition process to form a metal layer over a sidewall and the bottom of the opening, so that a metal silicide or germanide layer is formed on the exposed epitaxial source/drain region by the deposition process;

performing a first in-situ etching process using a metal halide as a process gas, so as to etch at least a portion of the metal layer;

performing an in-situ nitridation treatment on the sidewall and the bottom of the opening, so as to form a nitrogen-containing metal silicide or germanide layer over the bottom of the opening; and

forming a fill metal material layer over the nitrogen-containing metal silicide or germanide layer and in the opening.

11. The method as claimed in claim 10, wherein a metal nitride region is formed over the sidewall of the opening after performing the in-situ nitridation treatment.

12. The method as claimed in claim 10, wherein plasma power is applied when the first in-situ etching process is performed.

13. The method as claimed in claim 12, further comprising performing a second in-situ etching process without applying plasma power after performing the first in-situ etching process, wherein the second in-situ etching process is performed using a metal halide as a process gas.

14. The method as claimed in claim 10, wherein the first in-situ etching process is performed without applying plasma power, wherein the metal layer is entirely etched by performing the first in-situ etching process.

15. The method as claimed in claim 10, further comprising performing at least one cycle process that comprises the deposition process and the first in-situ etching process before performing the in-situ nitridation treatment.

16. A semiconductor device structure, comprising:

a semiconductor substrate having a conductive region made of silicon, germanium or a combination thereof;

an insulating layer over the semiconductor substrate;

a fill metal material layer in the insulating layer; and

a nitrogen-containing metal silicide or germanide layer between the conductive region and the fill metal material layer.

17. The semiconductor device structure as claimed in claim 16, further comprising a liner having a metal nitride region that is in the insulating layer and between the insulating layer and a sidewall of the fill metal material layer.

18. The semiconductor device structure as claimed in claim 17, wherein the liner has a metal region between the insulating layer and the metal nitride region.

19. The semiconductor device structure as claimed in claim 16, wherein the semiconductor substrate has a fin and the conductive region is an epitaxial source/drain region in the fin.

20. The semiconductor device structure as claimed in claim 16, wherein the fill metal material layer is in direct contact with the insulating layer and the nitrogen-containing metal silicide or germanide layer.

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