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(54) **METHOD FOR PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE**

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(73) Assignee: **Unisantis Electronics Singapore Pte. Ltd.**

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Related U.S. Application Data

(63) Continuation of application No. 14/743,266, filed on Jun. 18, 2015, now Pat. No. 9,299,701, which is a continuation of application No. 14/083,060, filed on Nov. 18, 2013, now Pat. No. 9,117,690, which is a continuation-in-part of application No. 13/679,225, filed on Nov. 16, 2012, now Pat. No. 8,735,971.

(60) Provisional application No. 61/566,244, filed on Dec. 2, 2011.

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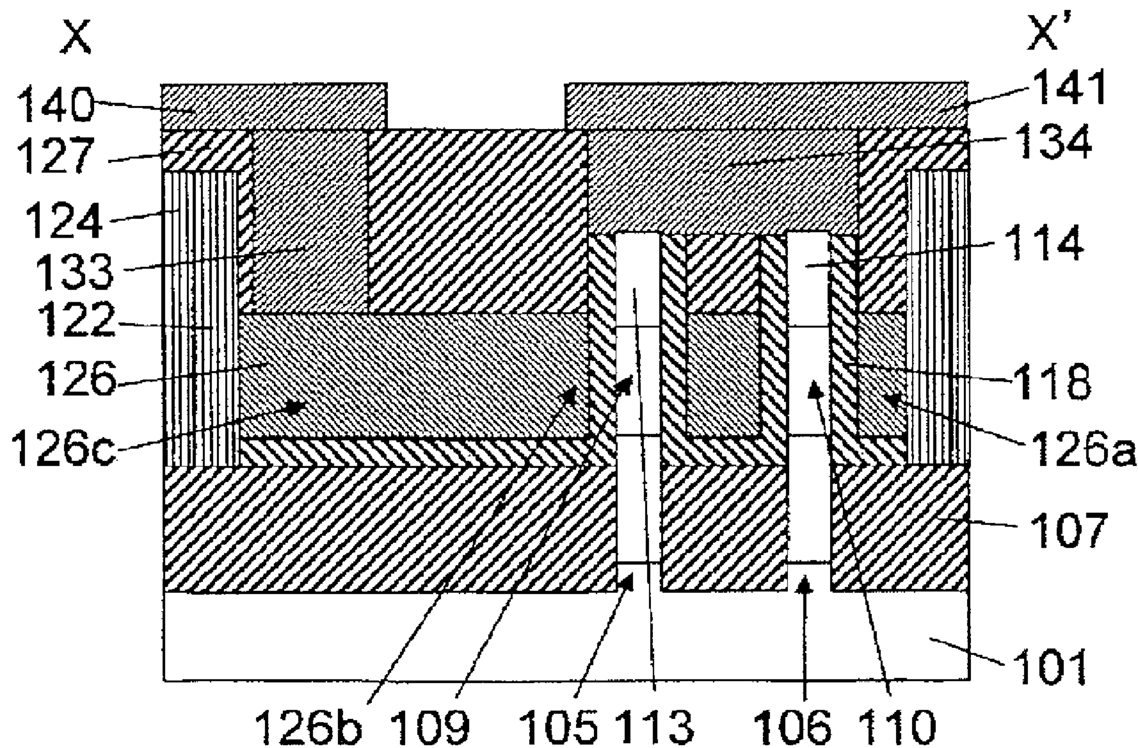
H01L 27/088 (2006.01)
H01L 29/423 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/78642*** (2013.01); ***H01L 29/42392*** (2013.01); ***H01L 29/78654*** (2013.01); ***H01L 29/78618*** (2013.01); ***H01L 29/78696*** (2013.01); ***H01L 27/088*** (2013.01)

(57) **ABSTRACT**

A semiconductor device includes first and second fin-shaped semiconductor layers on a substrate. First and second pillar-shaped semiconductor layers reside on the first and second fin-shaped semiconductor layers, respectively, where a width of the bottom of the first and second pillar-shaped semiconductors is equal to a width of the top of the first and second fin-shaped semiconductor layers, respectively. A gate insulating film and metal gate electrode are around underlying gate insulating layers on each fin-shaped semiconductor layer. A metal gate line is connected to the metal gate electrodes and extends in a direction perpendicular to the first and second fin-shaped semiconductor layers. Contacts reside on the upper portion of diffusion layers in upper portions of the first and second pillar-shaped semiconductor layers and are directly connected to the diffusion layers.



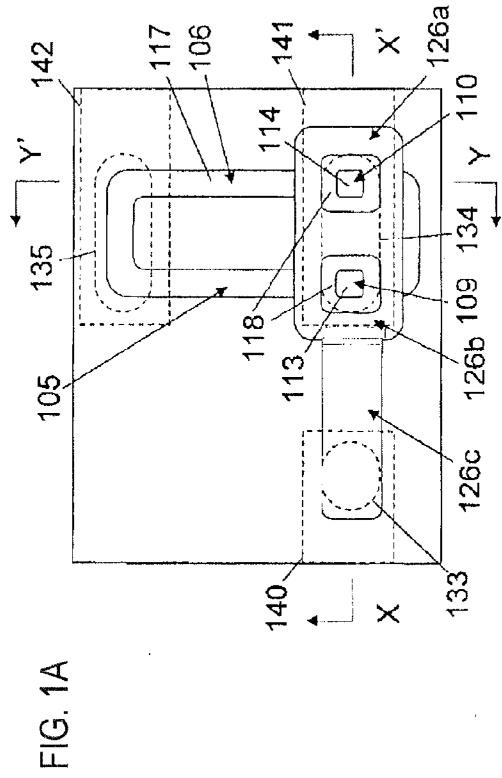


FIG. 1A

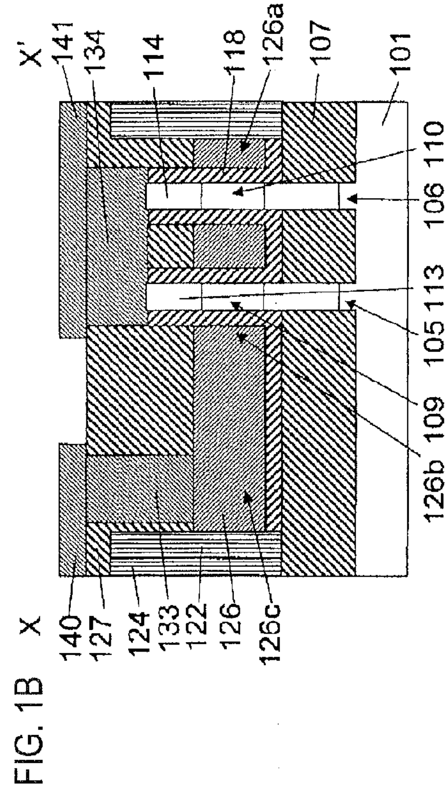


FIG. 1B

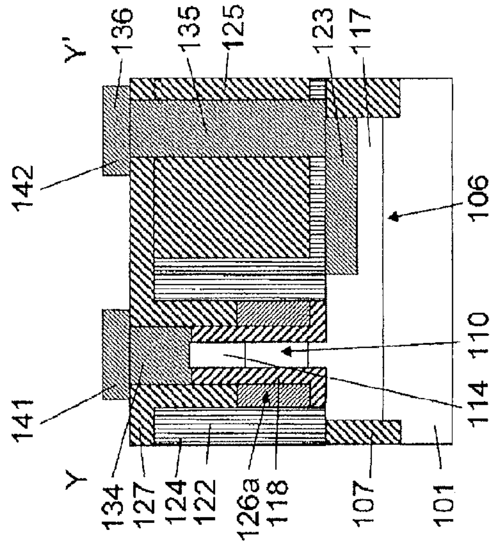


FIG. 1C

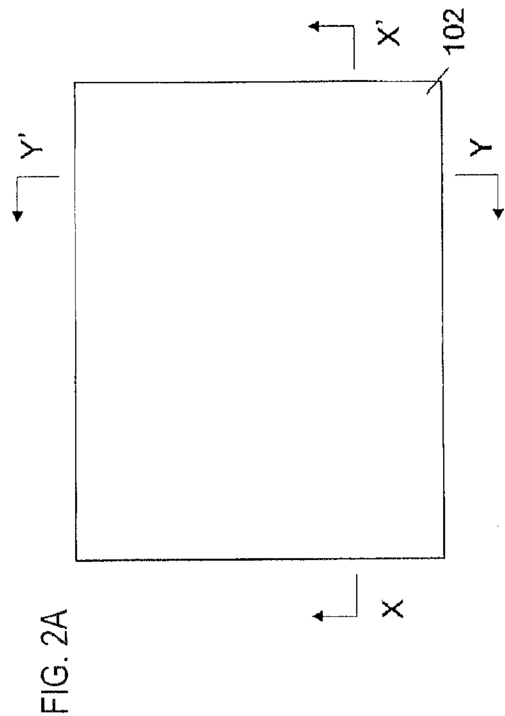


FIG. 2A
Y'
Y
X
X'
102

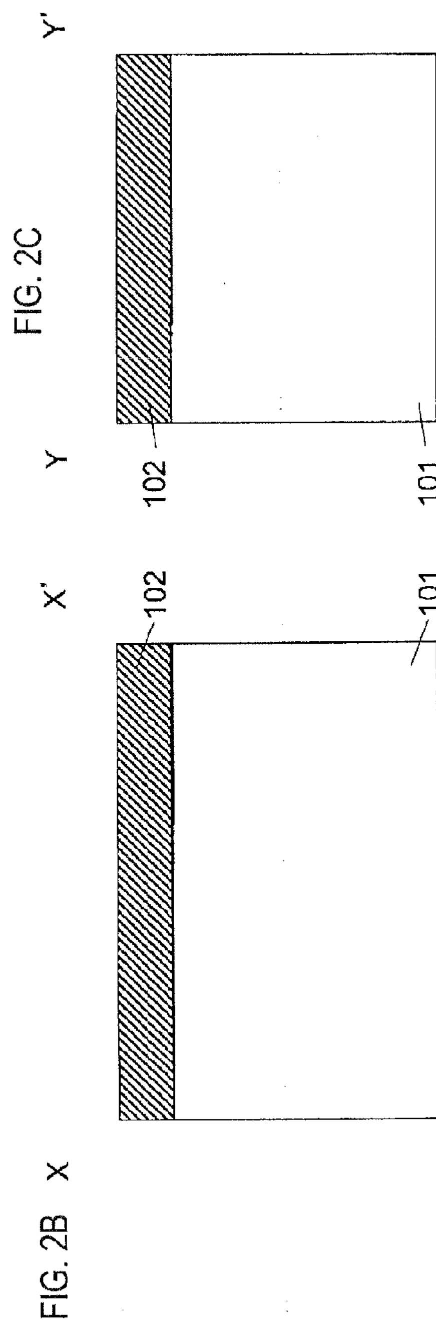


FIG. 2B
X
X'
102
101
FIG. 2C
Y
Y'
102
101

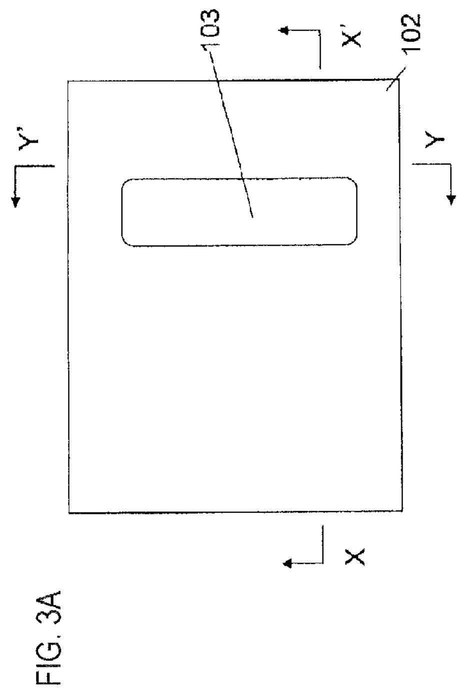


FIG. 3A

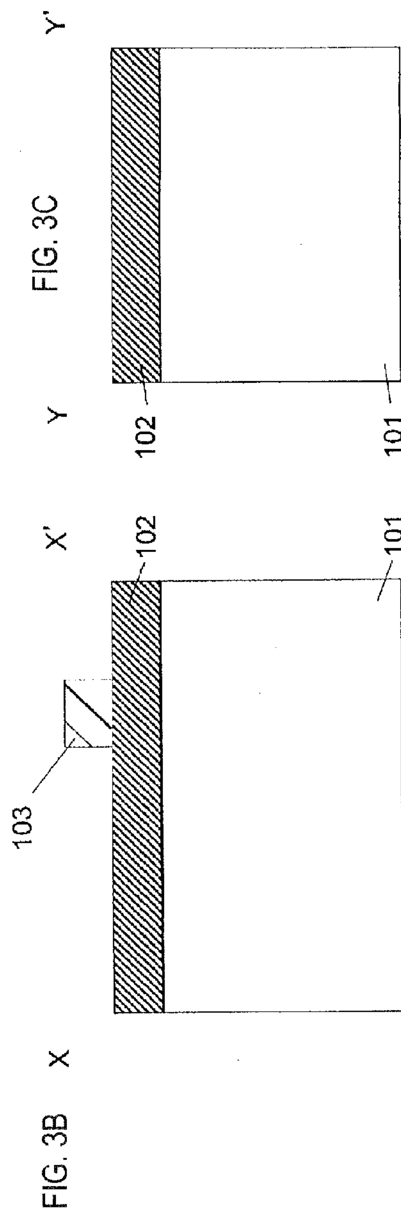


FIG. 3B

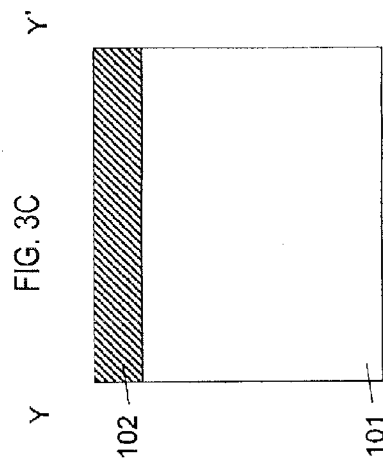


FIG. 3C

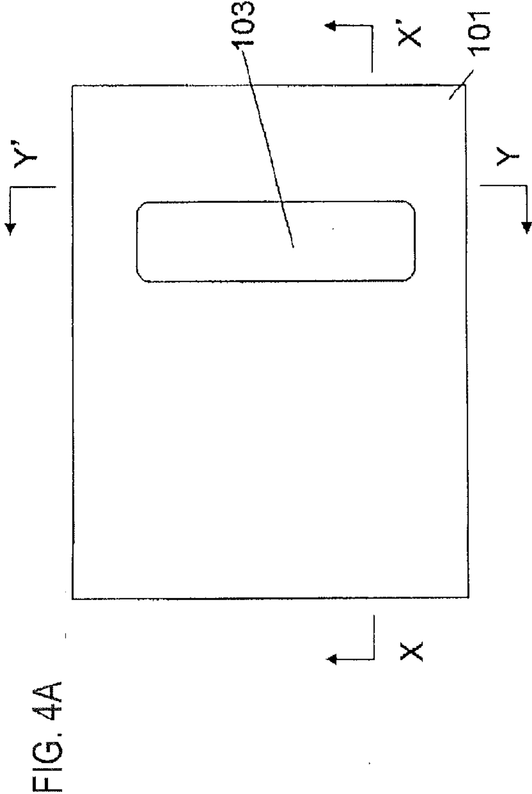


FIG. 4A

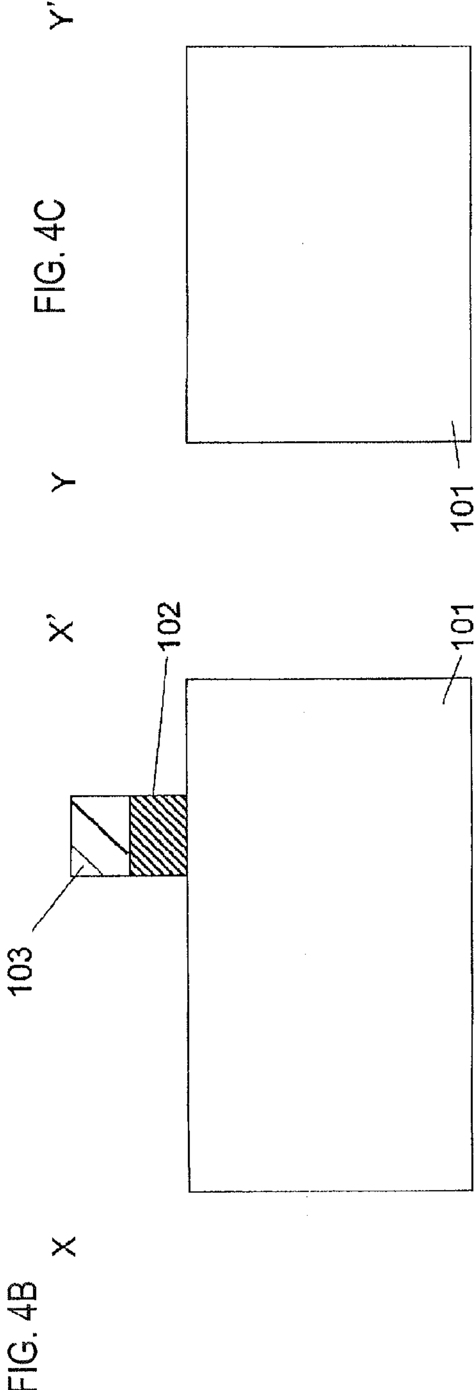


FIG. 4B

FIG. 4C

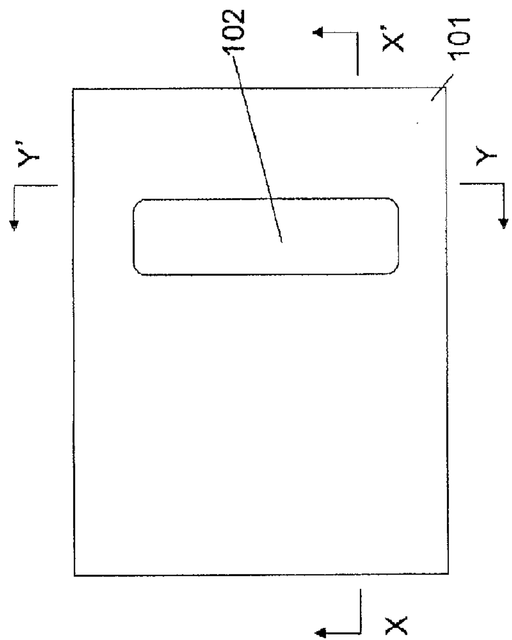


FIG. 5A

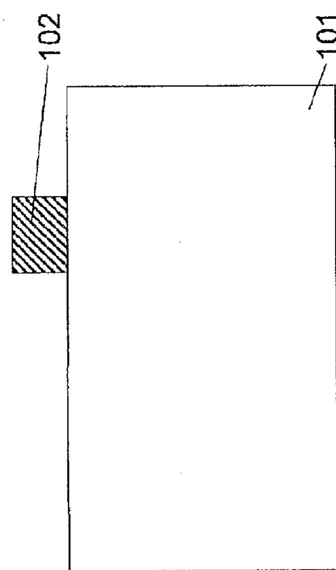


FIG. 5B

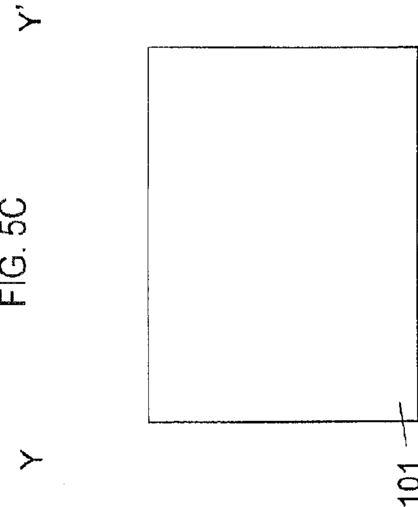


FIG. 5C

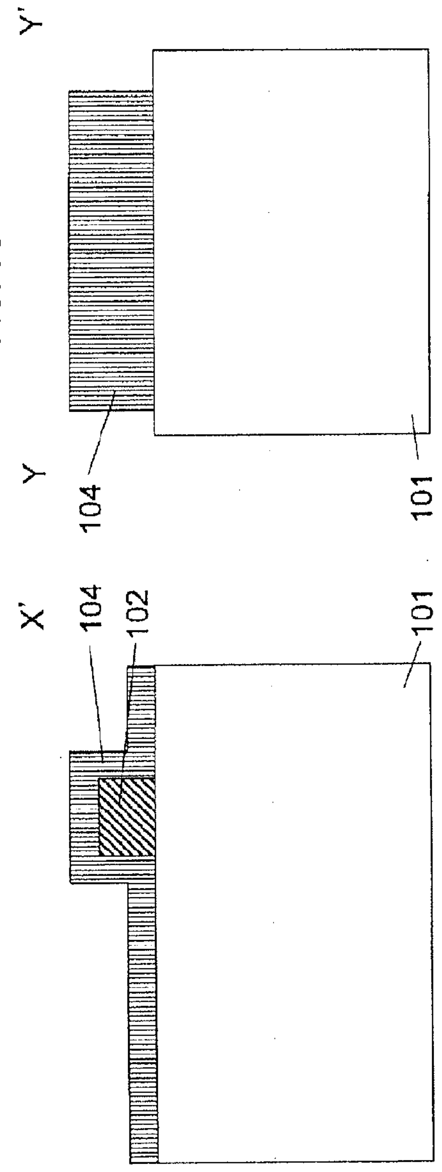


FIG. 6C

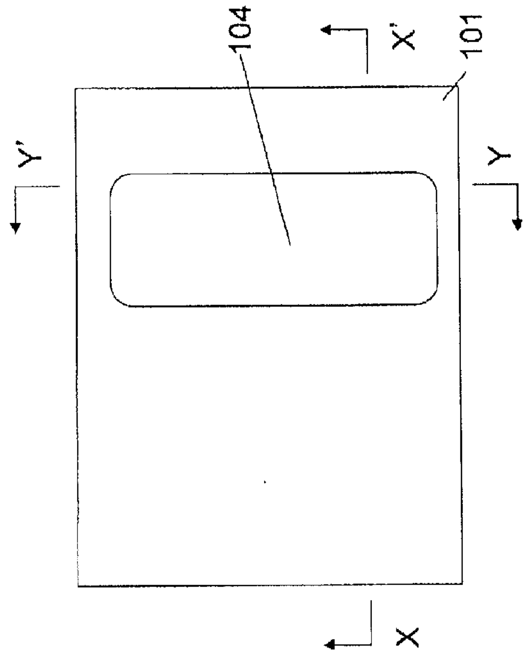


FIG. 6A

FIG. 6B

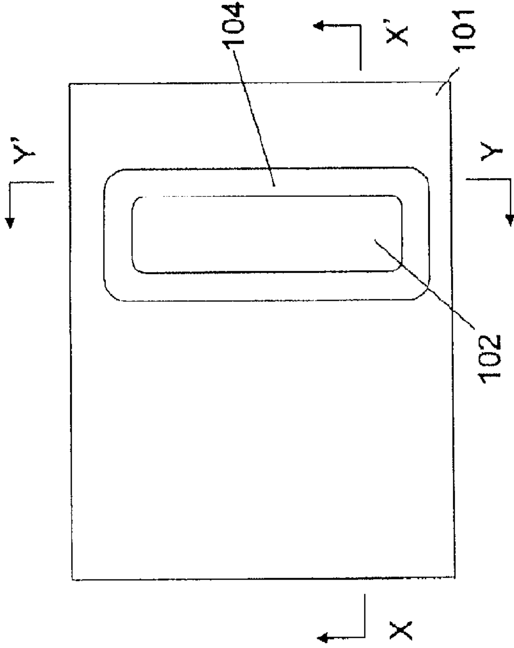


FIG. 7A

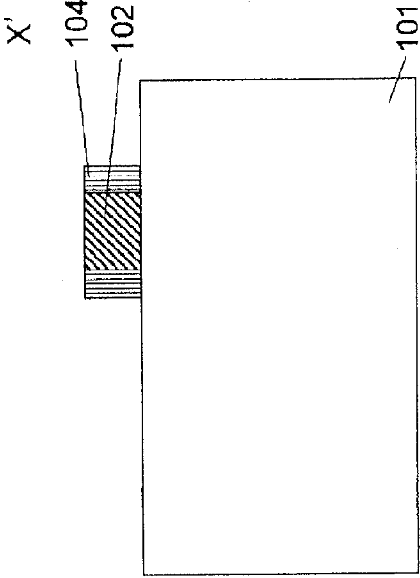


FIG. 7B

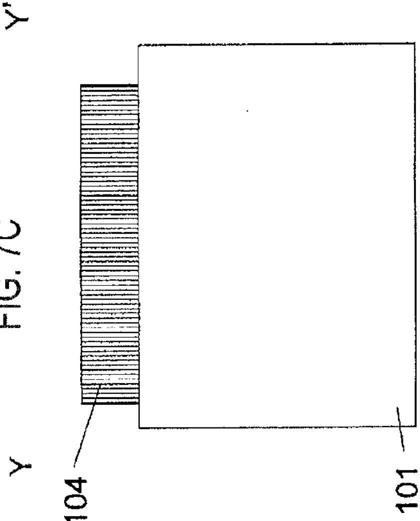


FIG. 7C

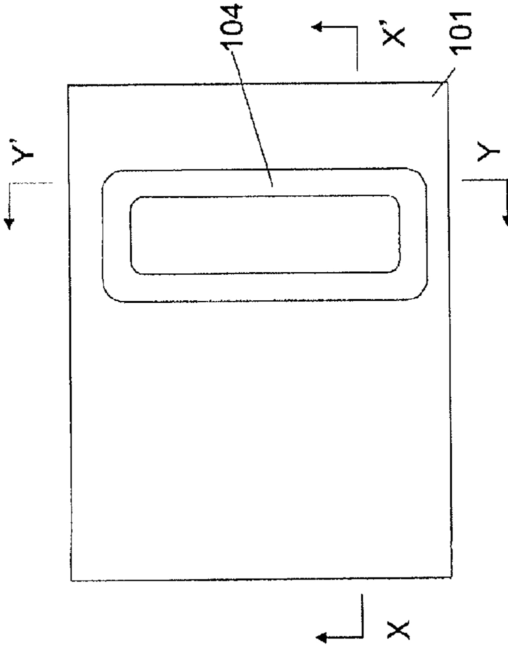


FIG. 8A

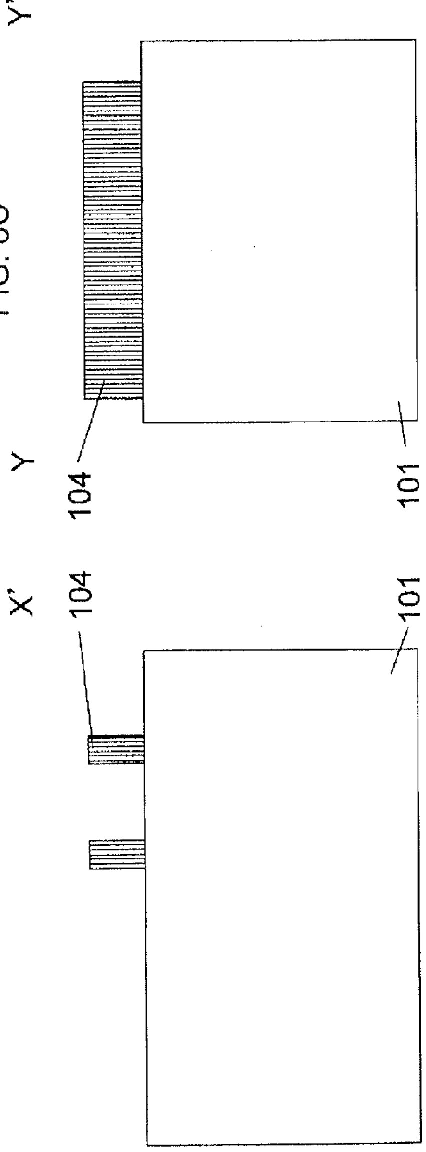


FIG. 8C

FIG. 8B

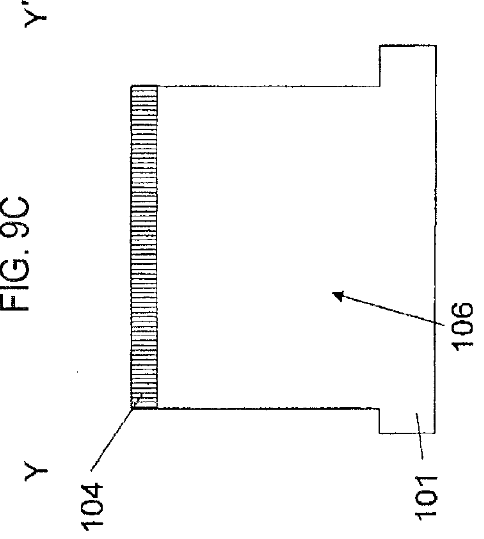


FIG. 9C

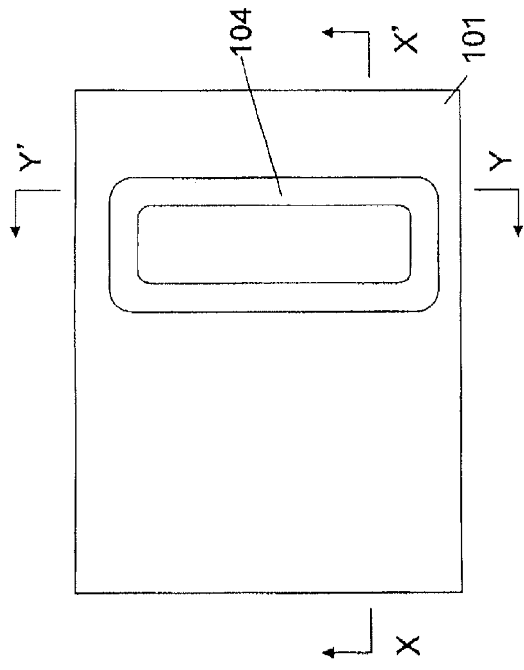


FIG. 9A

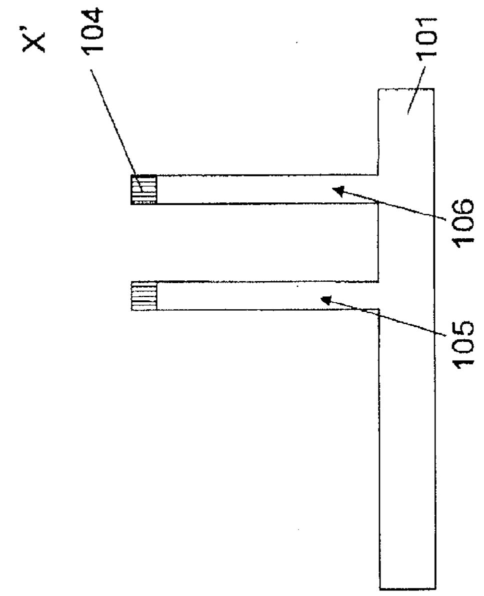


FIG. 9B

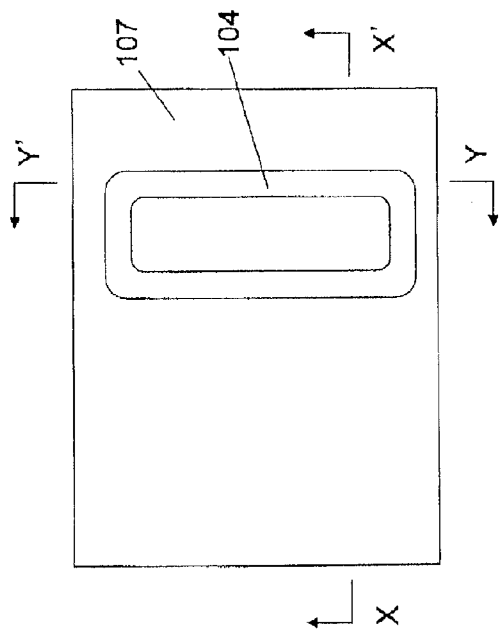


FIG. 10A

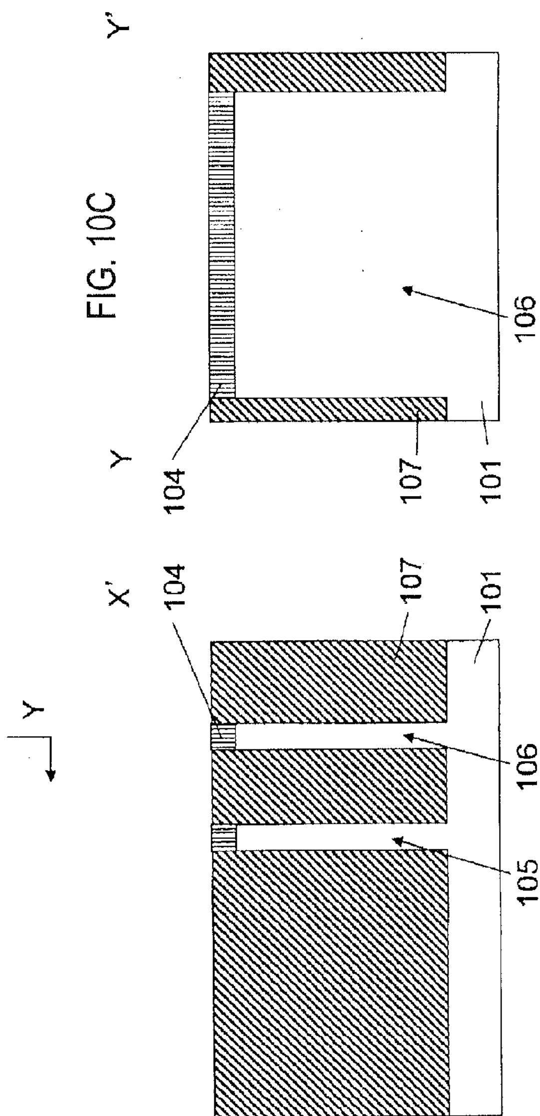


FIG. 10B

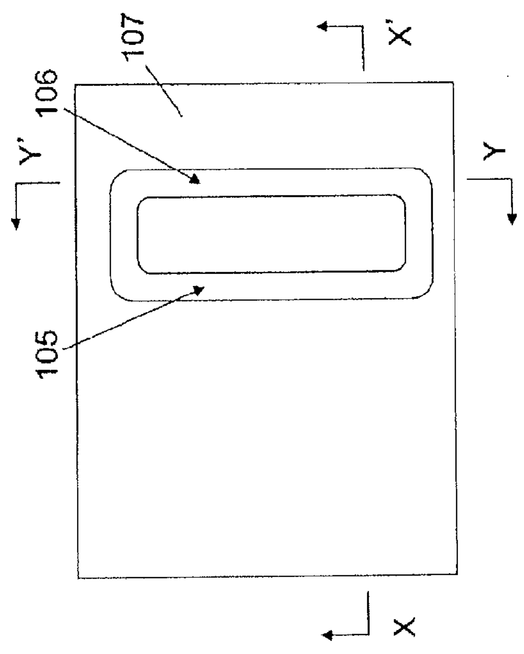


FIG. 11A

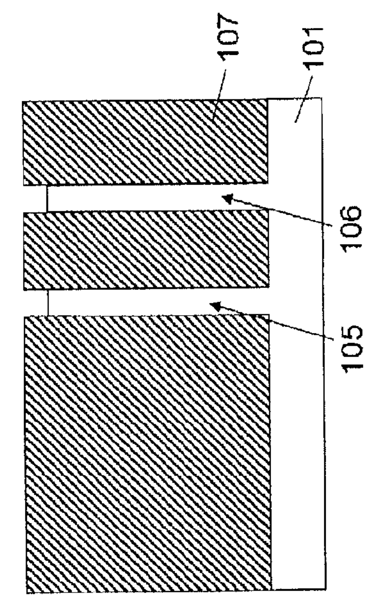


FIG. 11B

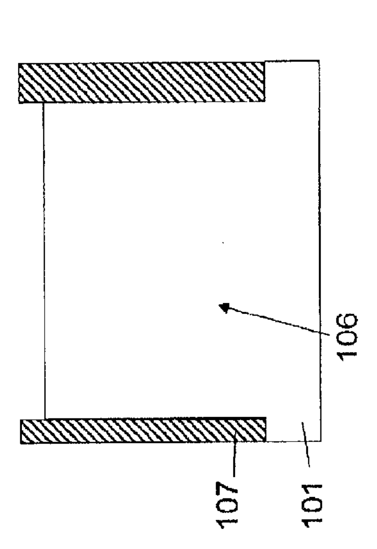


FIG. 11C

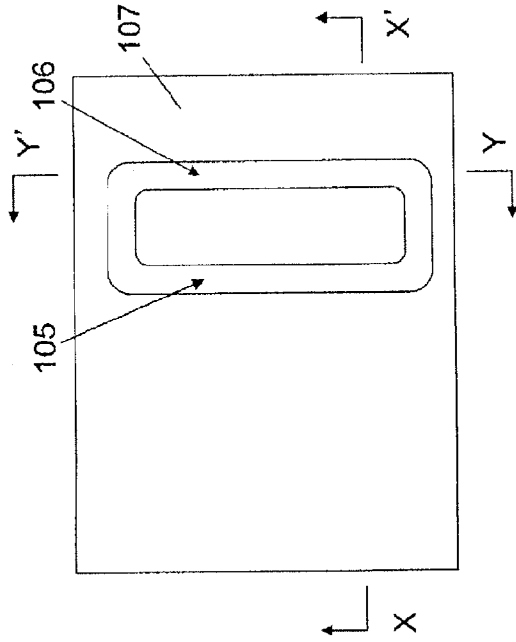
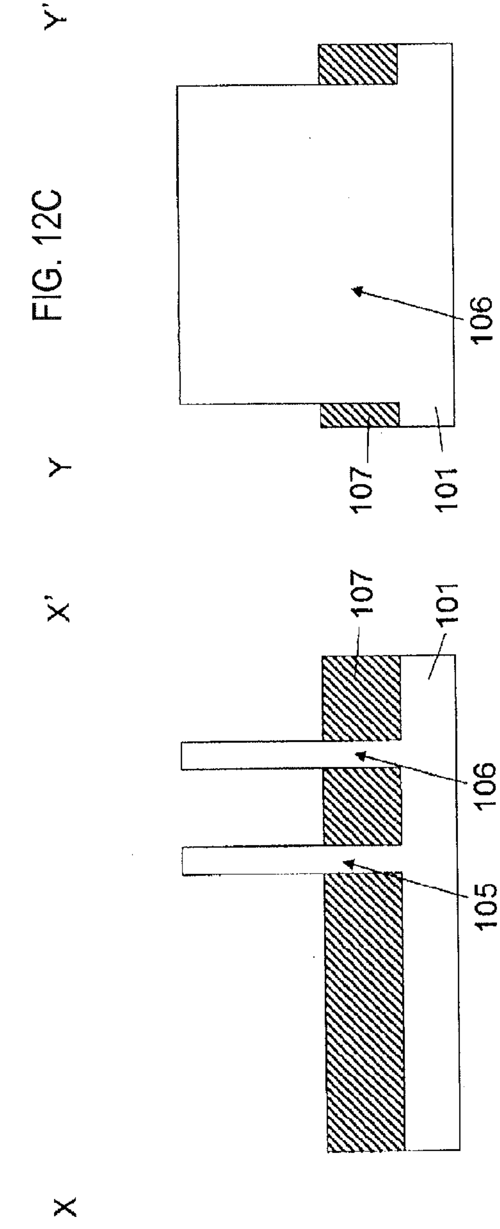


FIG. 12A



X

FIG. 12B

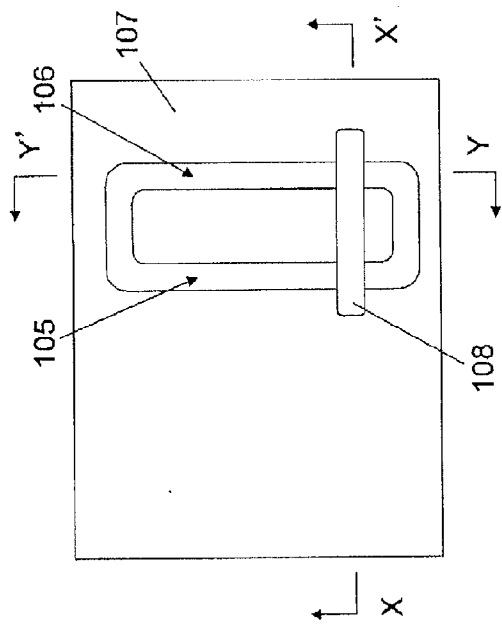


FIG. 13A

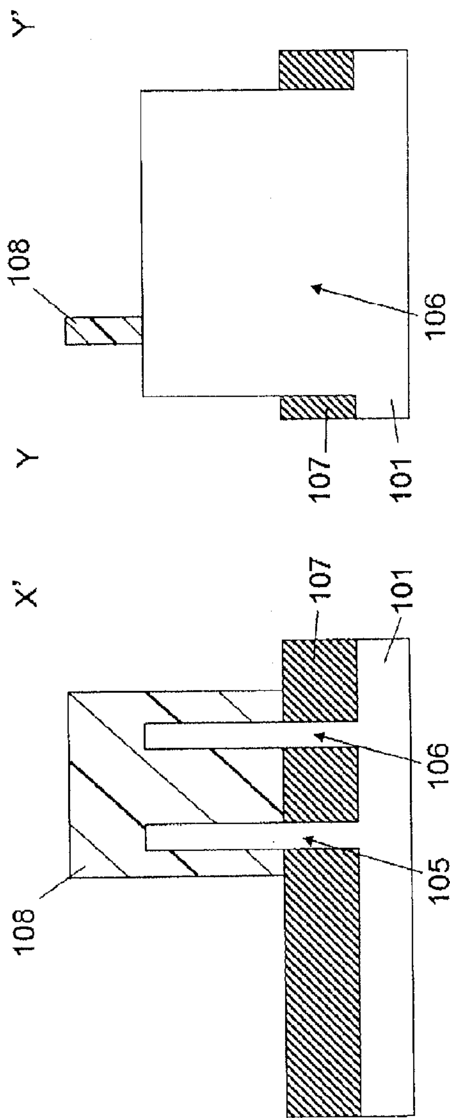


FIG. 13B

FIG. 13C

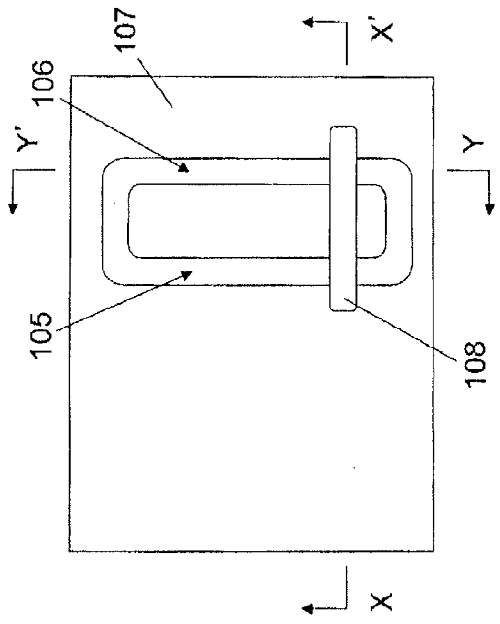


FIG. 14A

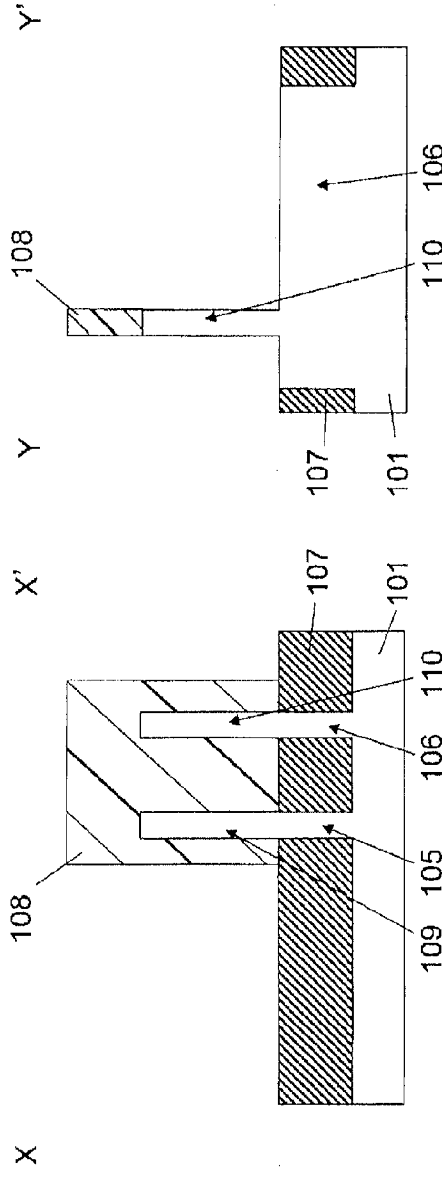


FIG. 14B

FIG. 14C

FIG. 15A

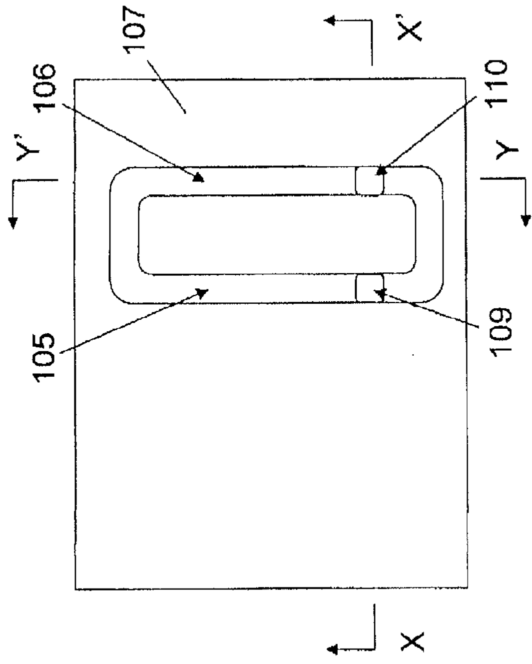


FIG. 15B

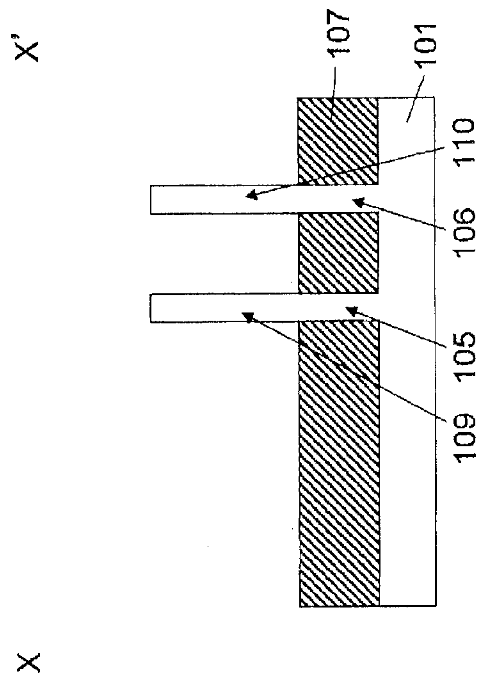


FIG. 15C

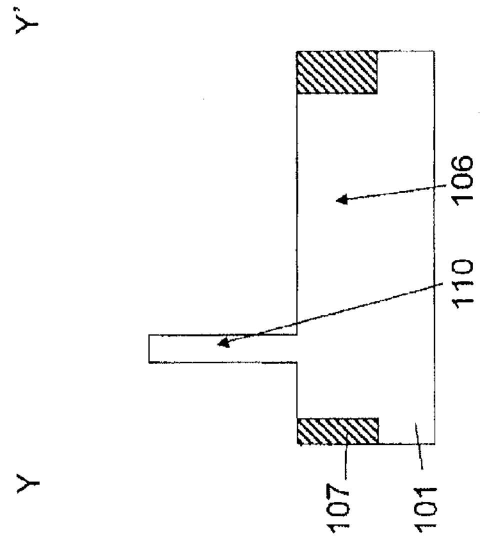


FIG. 16A

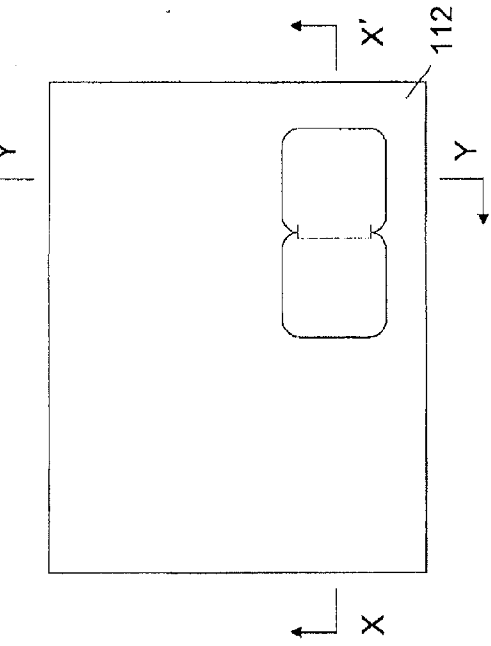


FIG. 16B

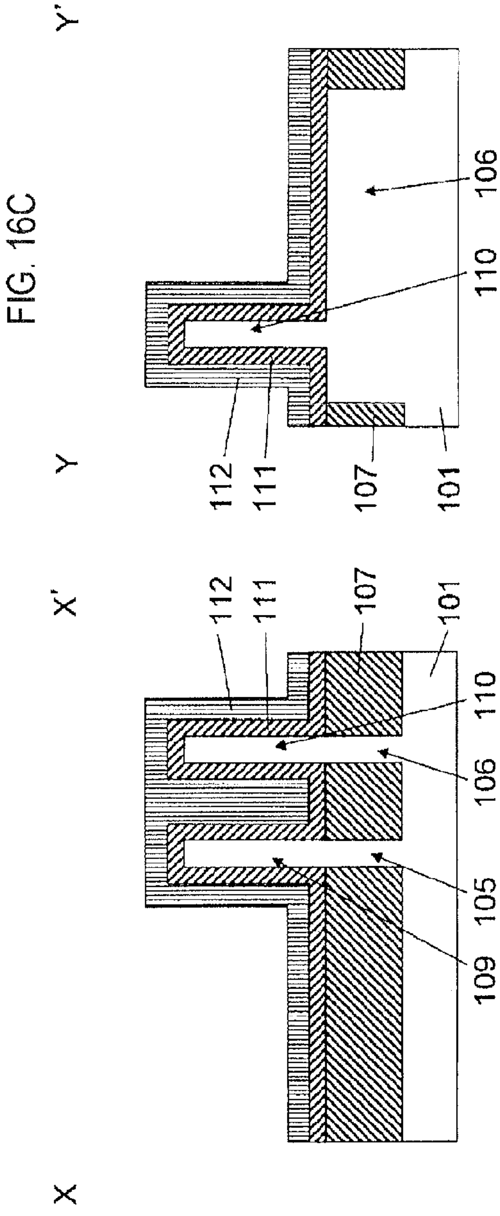
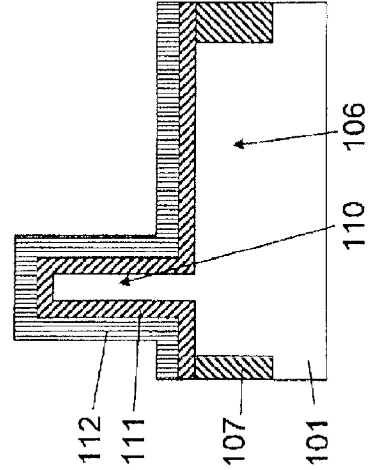


FIG. 16C



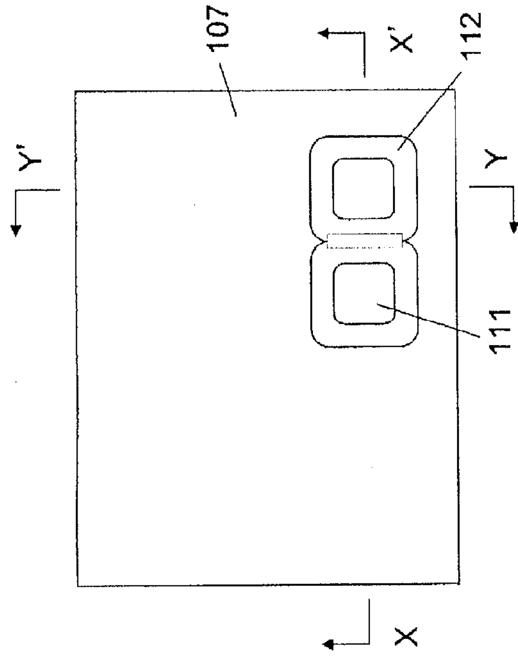


FIG. 17A

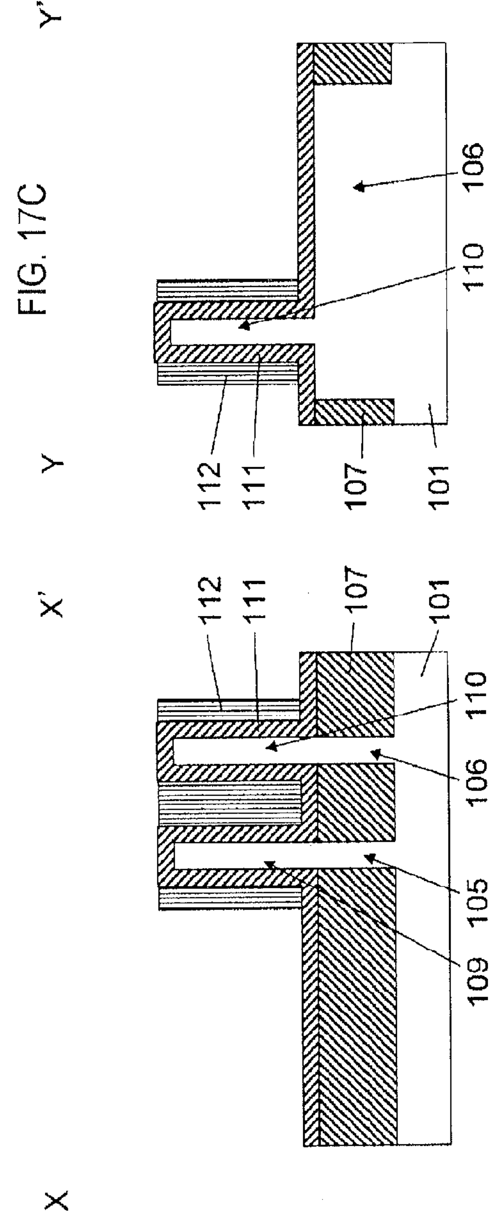


FIG. 17B

FIG. 17C

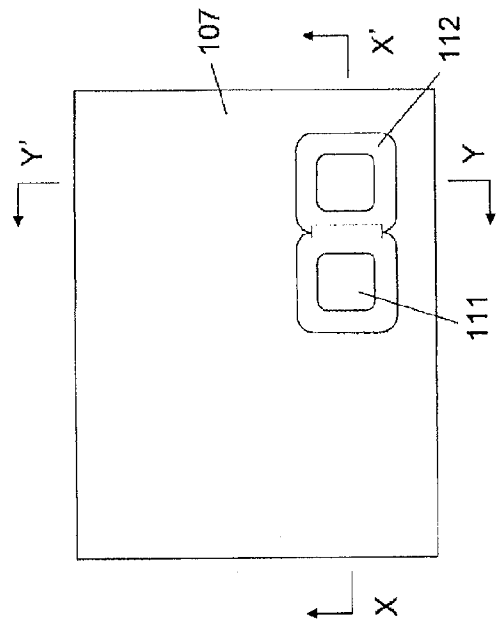


FIG. 18A

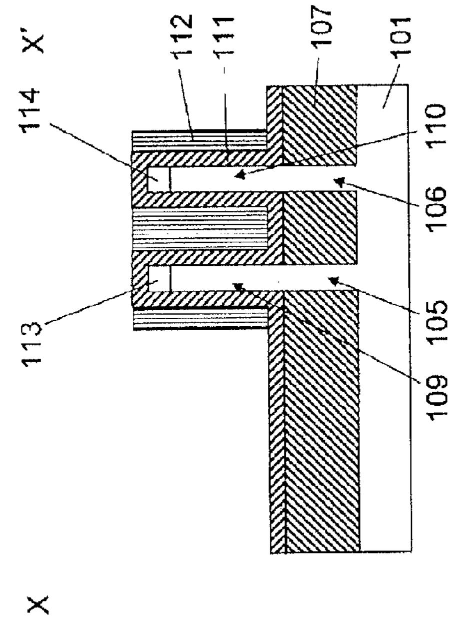


FIG. 18B

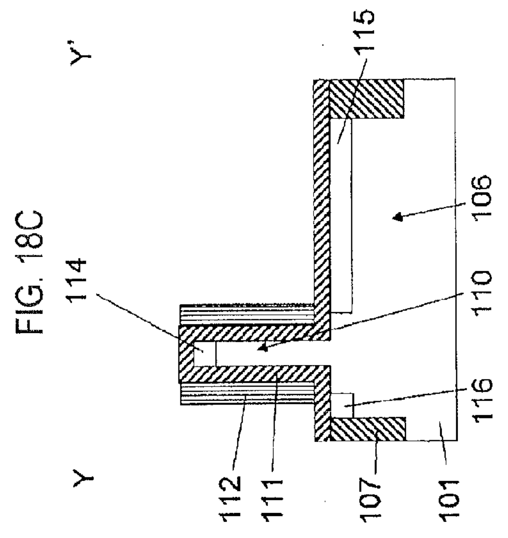


FIG. 18C

FIG. 19A

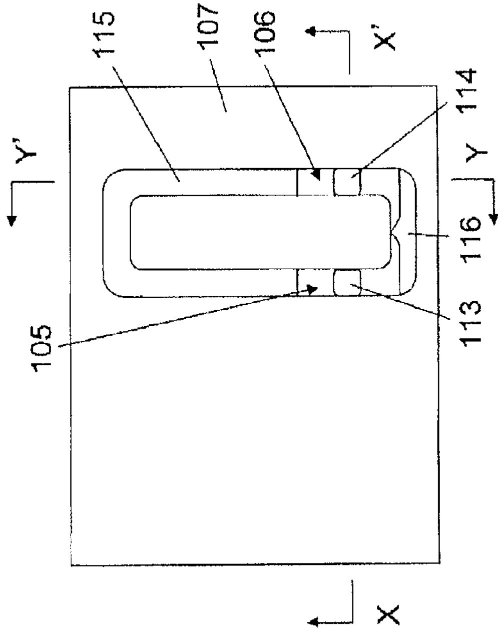
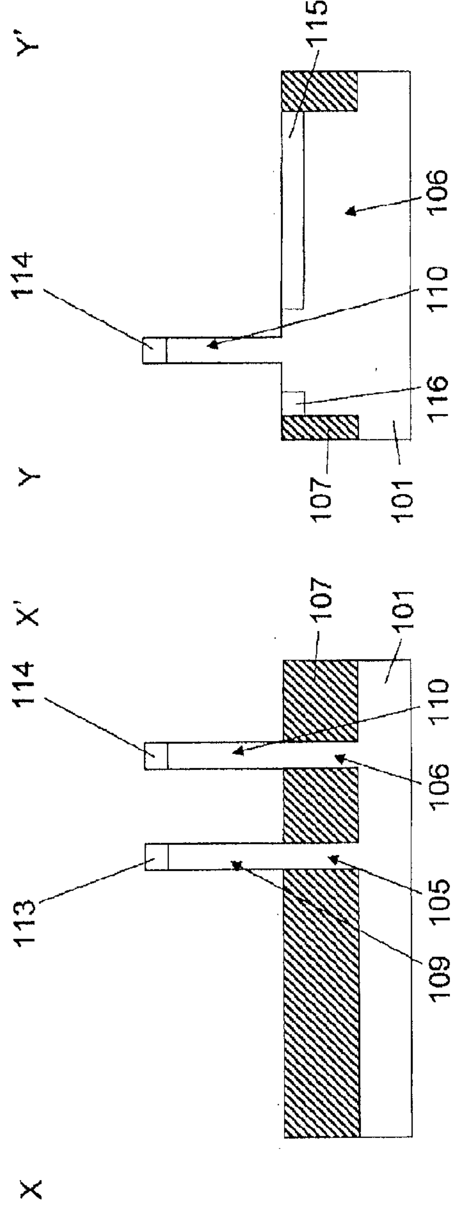


FIG. 19B

FIG. 19C



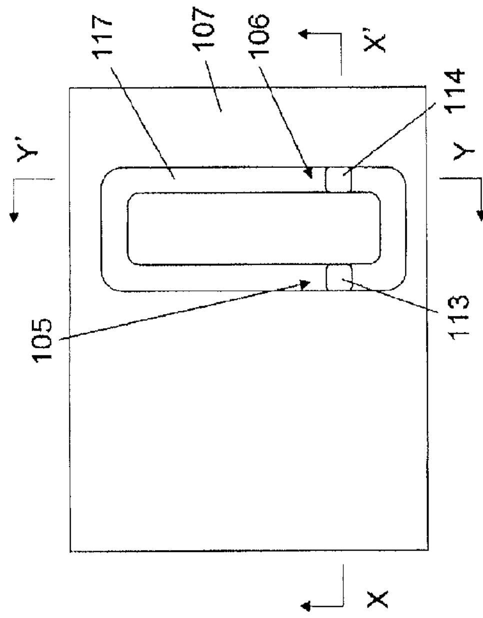


FIG. 20A

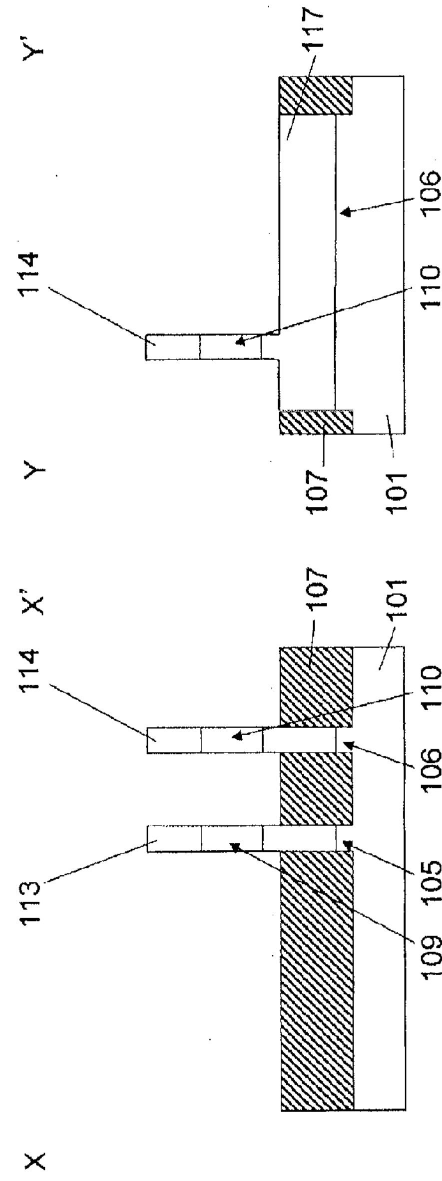


FIG. 20B

FIG. 20C

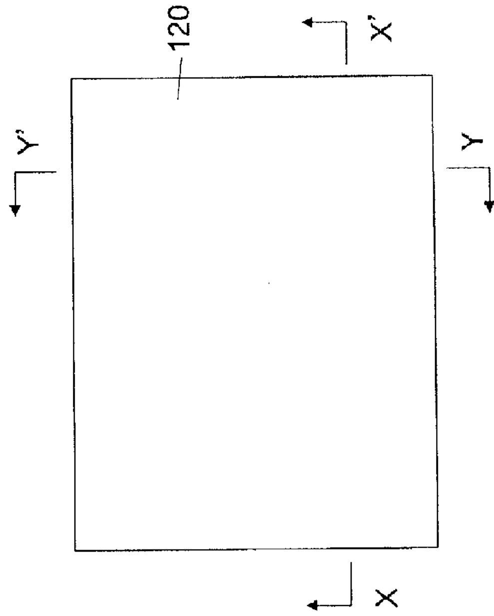


FIG. 21A

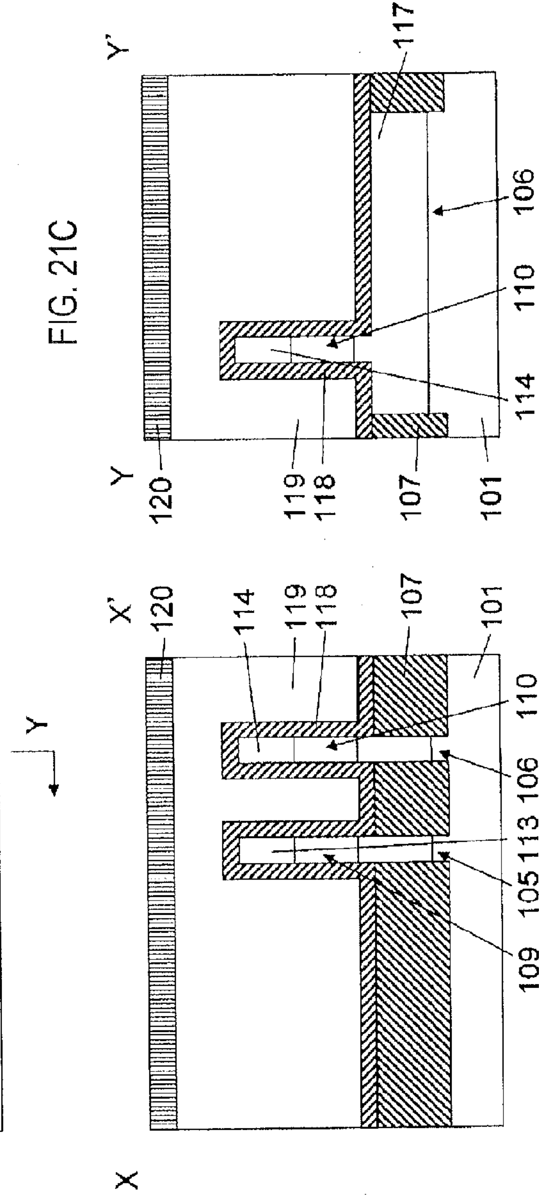


FIG. 21B

FIG. 21C

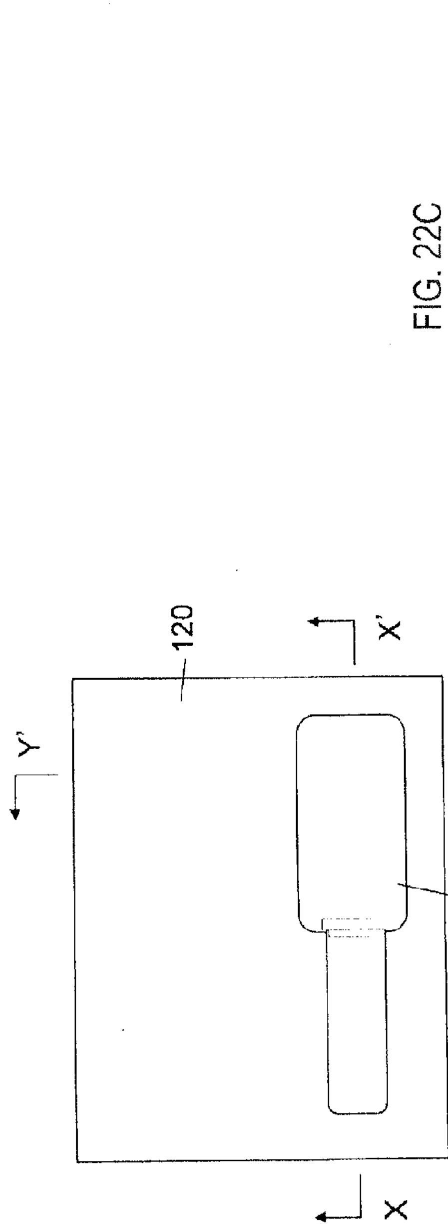


FIG. 22A

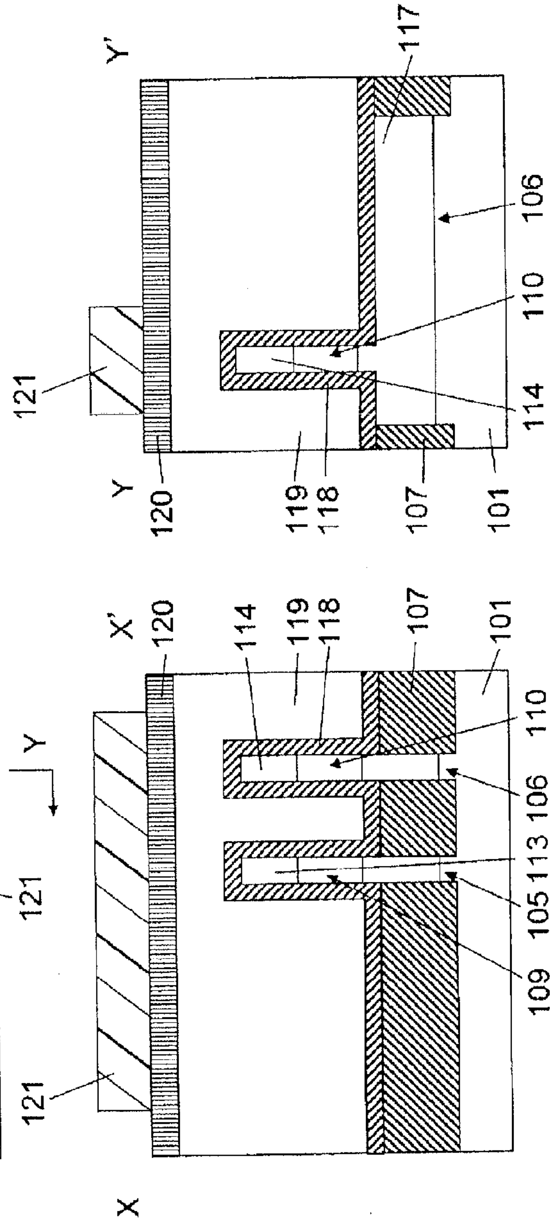


FIG. 22B

FIG. 22C

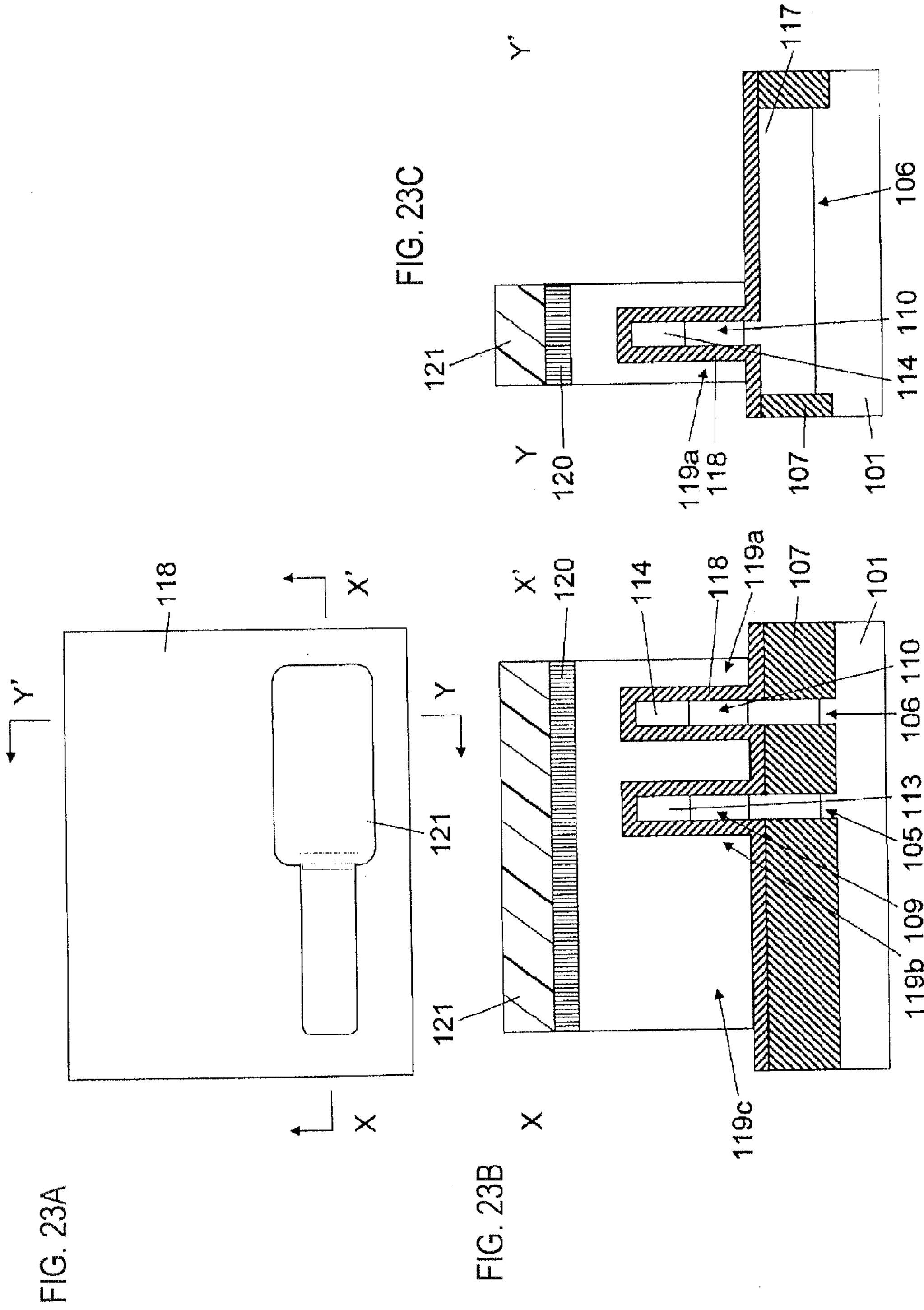


FIG. 23A
FIG. 23B
FIG. 23C
X
X'
Y
Y'
101
105
106
107
109
110
113
114
117
118
119a
119b
119c
120
121

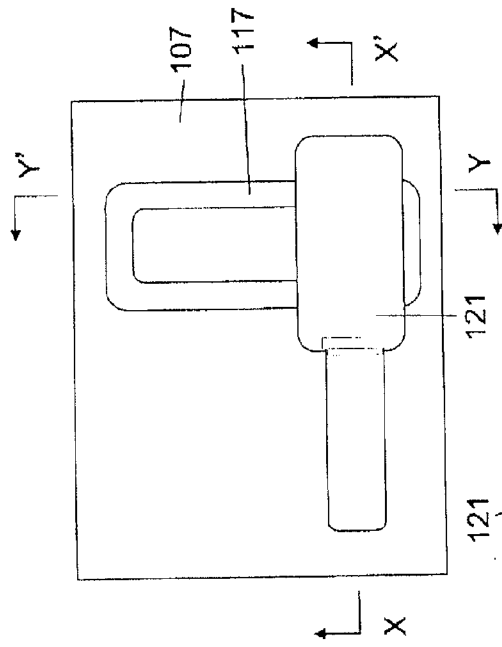


FIG. 24A

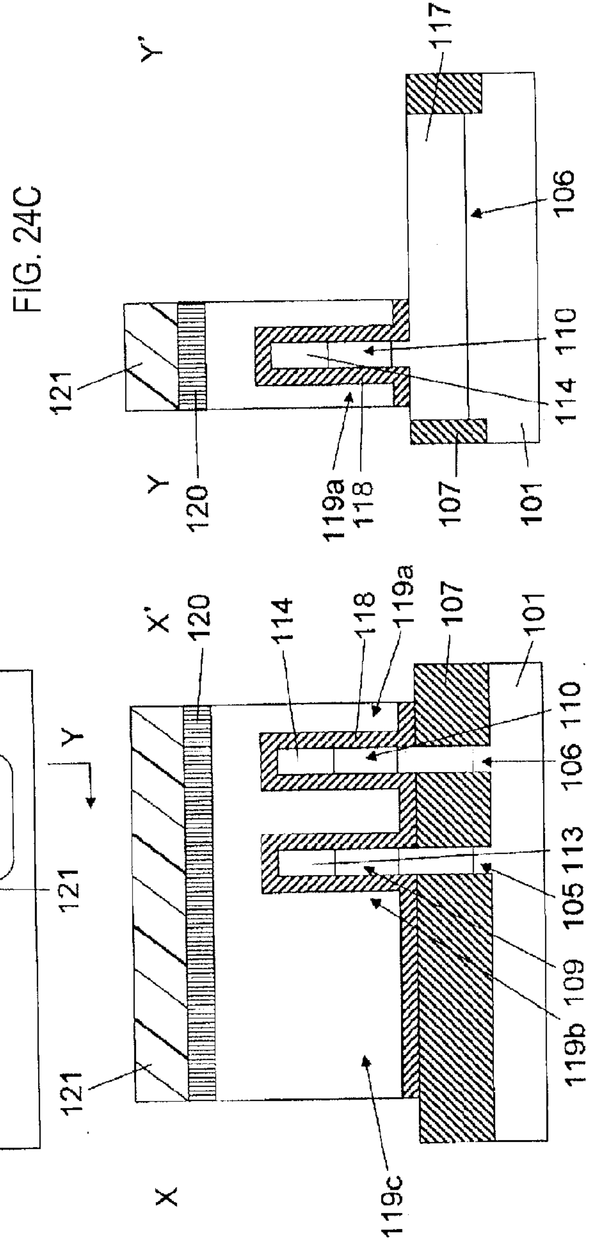


FIG. 24B

FIG. 24C

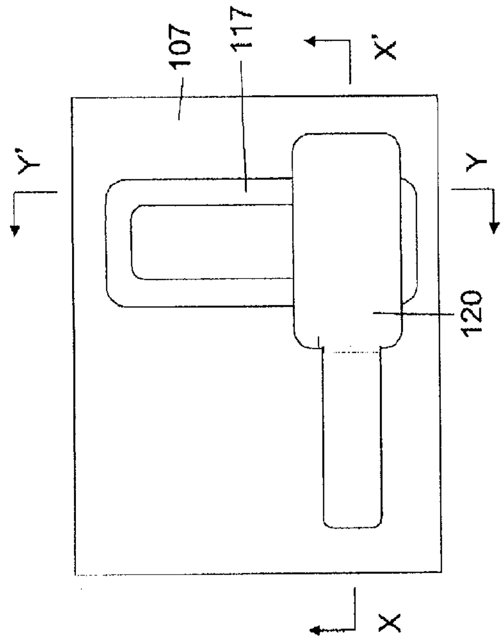


FIG. 25A

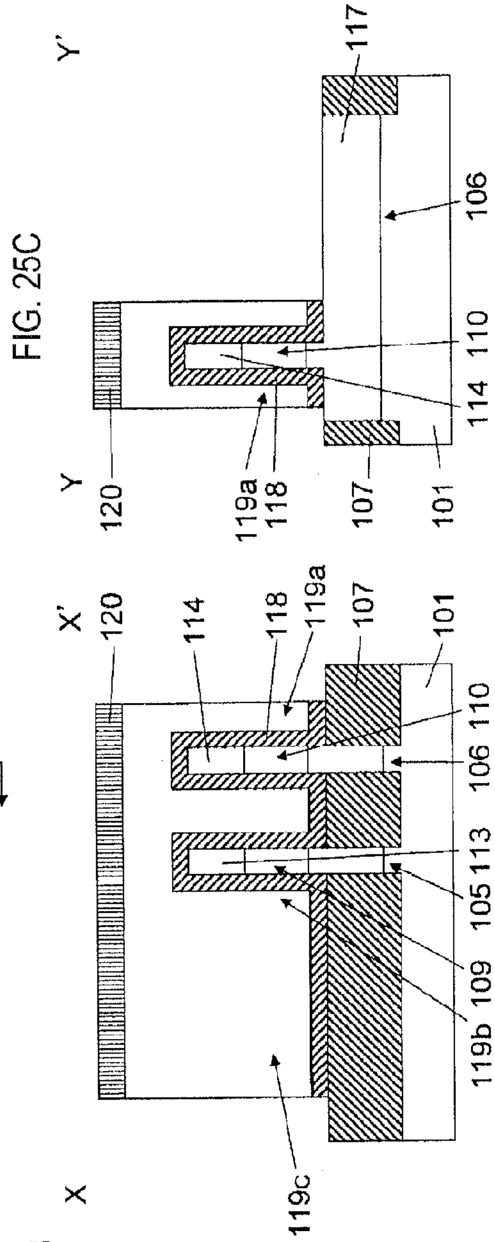


FIG. 25B

FIG. 25C

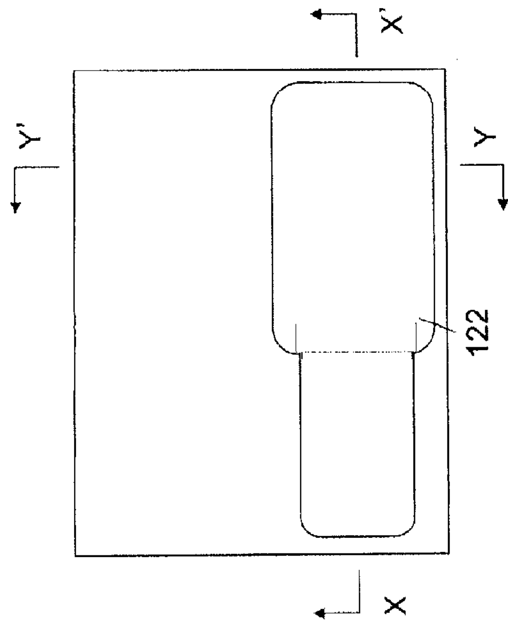


FIG. 26A

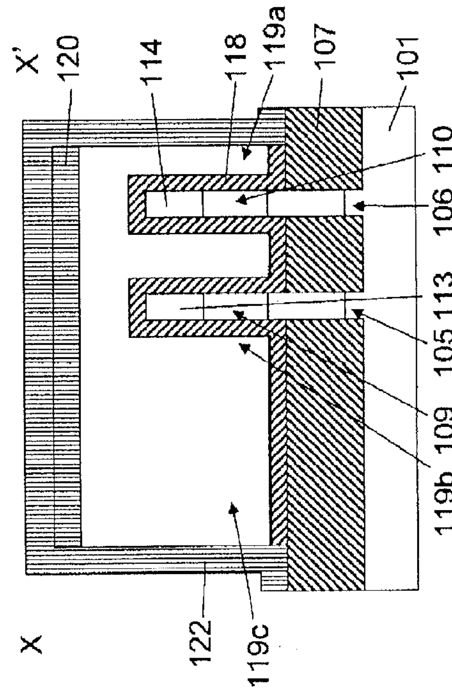


FIG. 26B

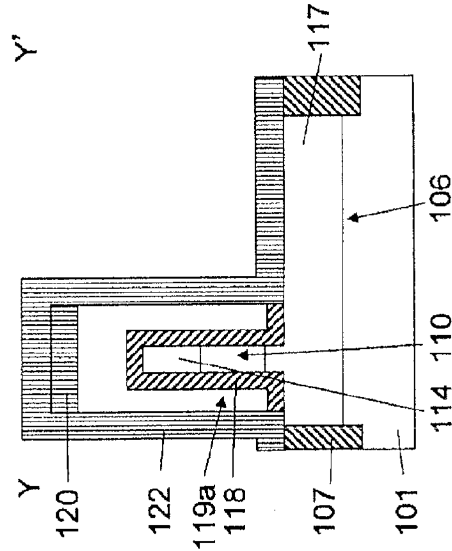


FIG. 26C

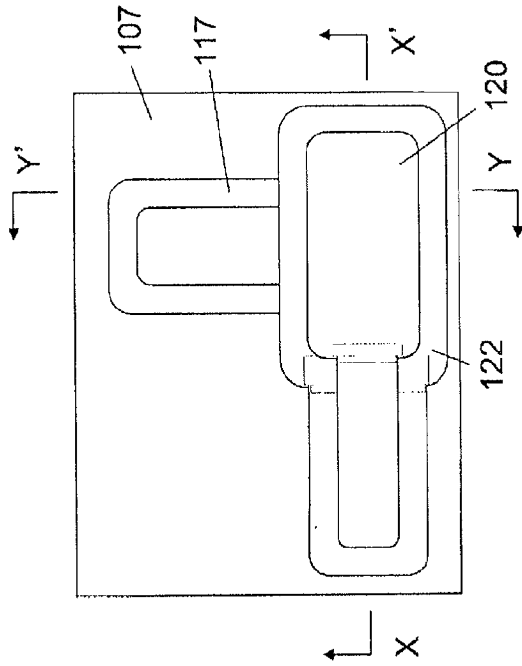


FIG. 27A

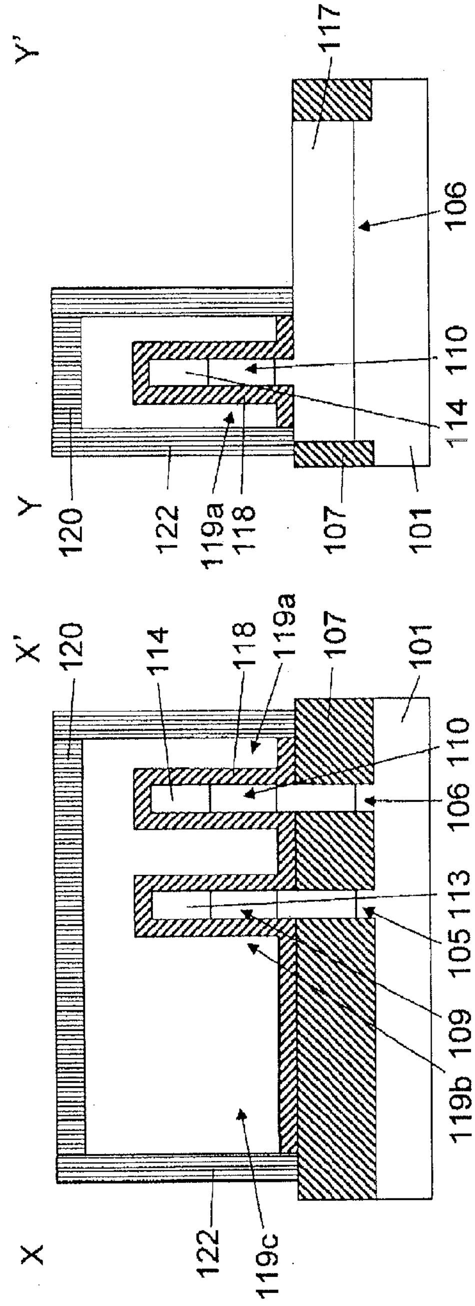


FIG. 27B

FIG. 27C

FIG. 28A

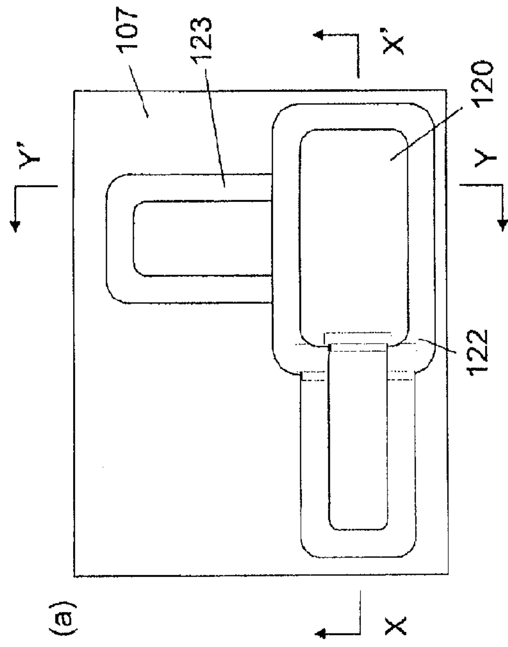


FIG. 28B

FIG. 28C

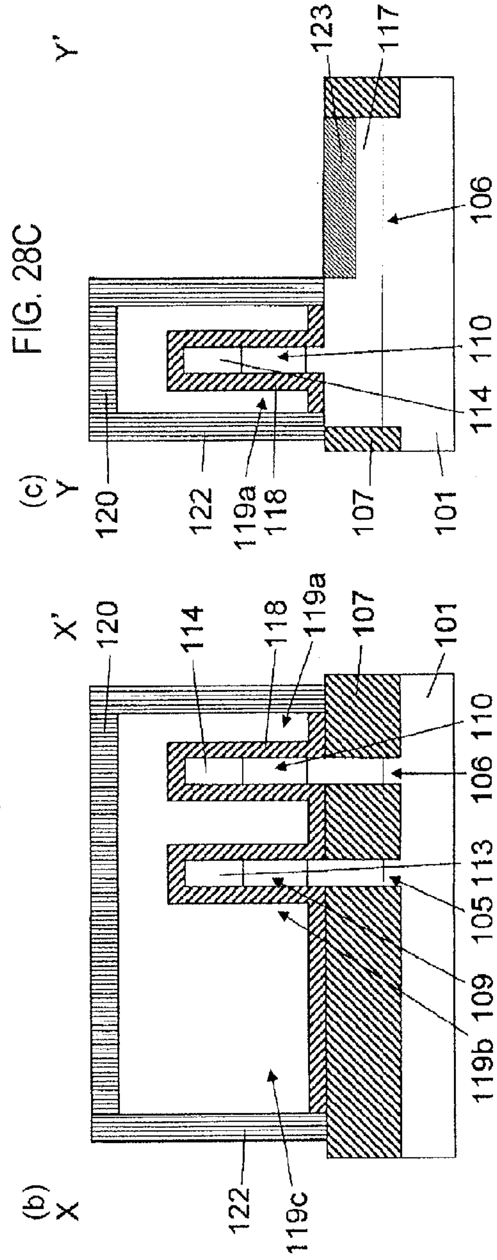


FIG. 29A

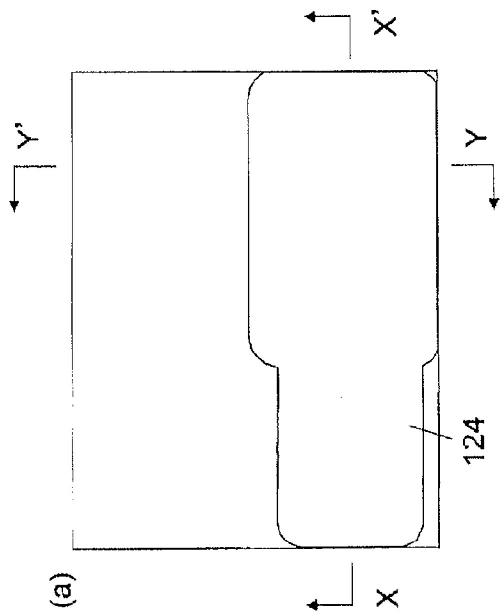


FIG. 29B

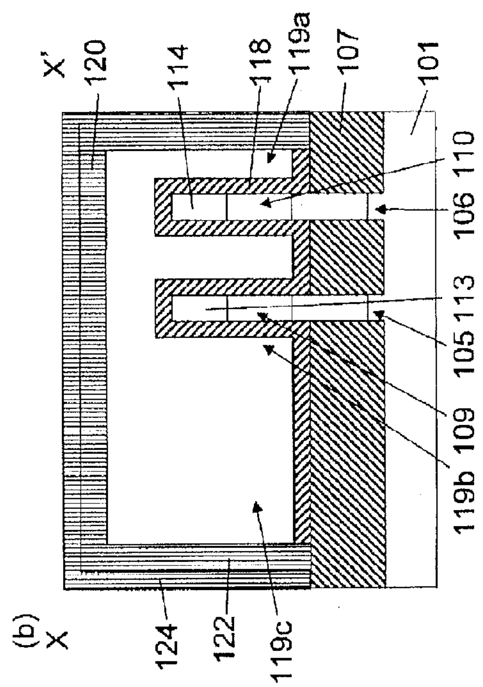
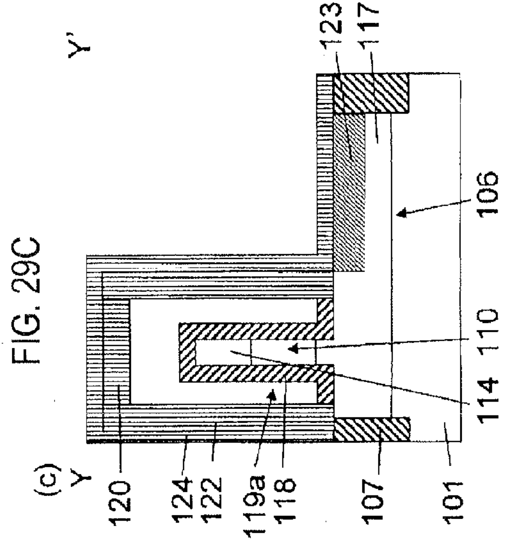


FIG. 29C



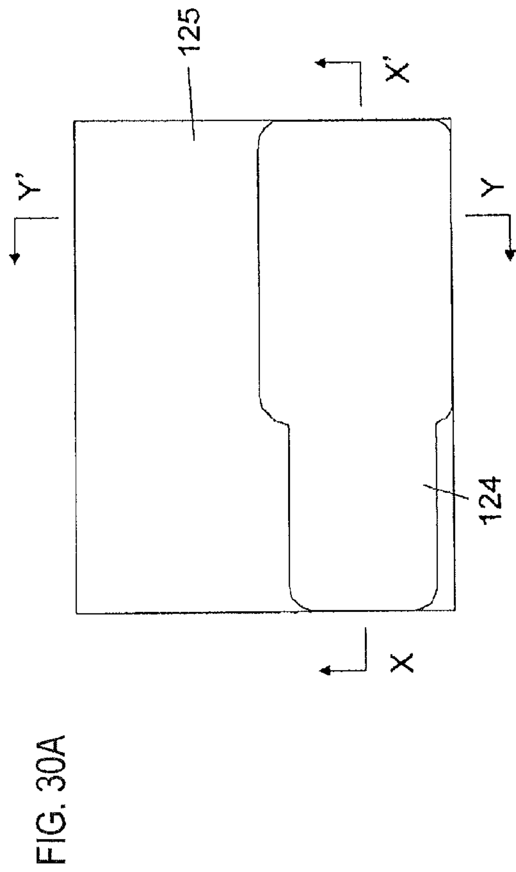


FIG. 30A

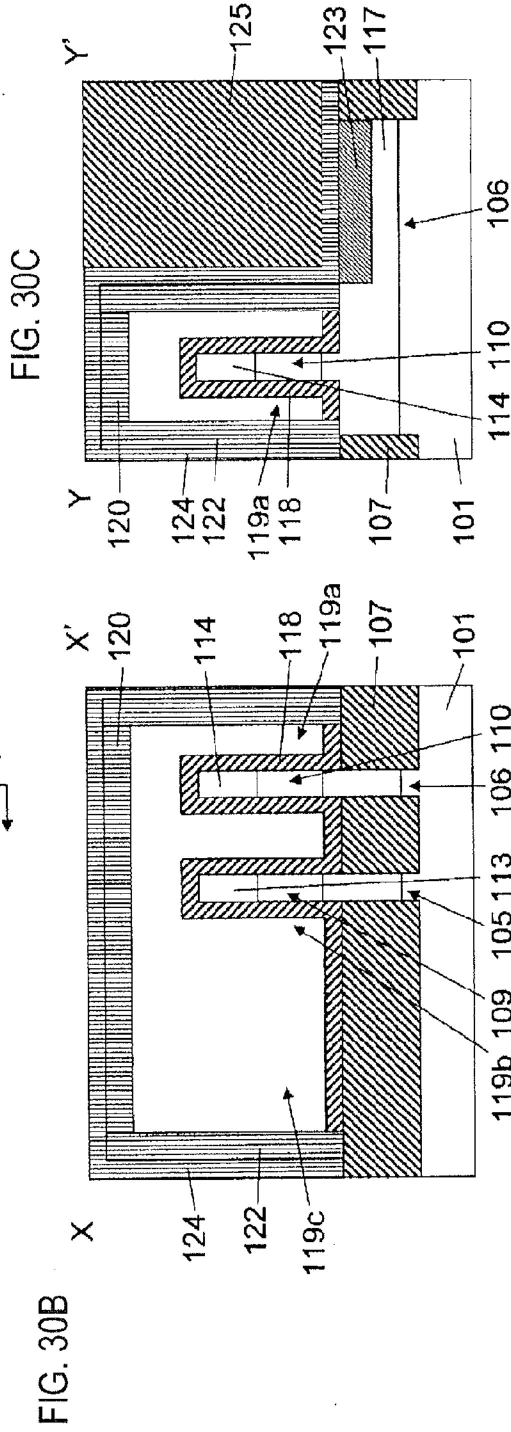


FIG. 30B

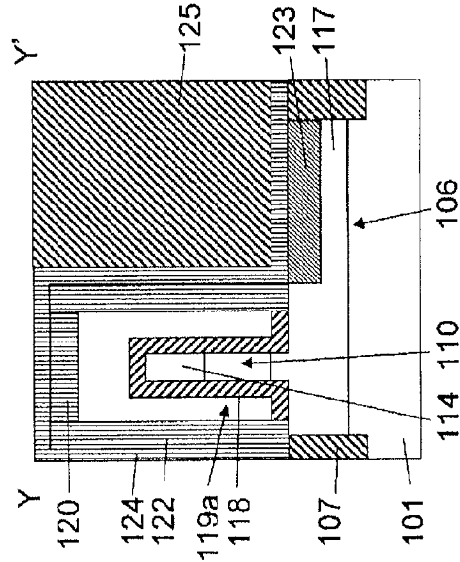


FIG. 30C

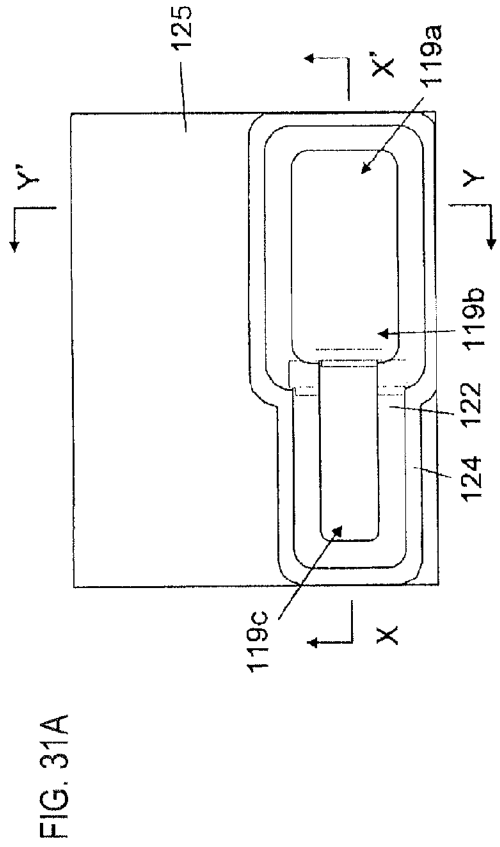


FIG. 31A

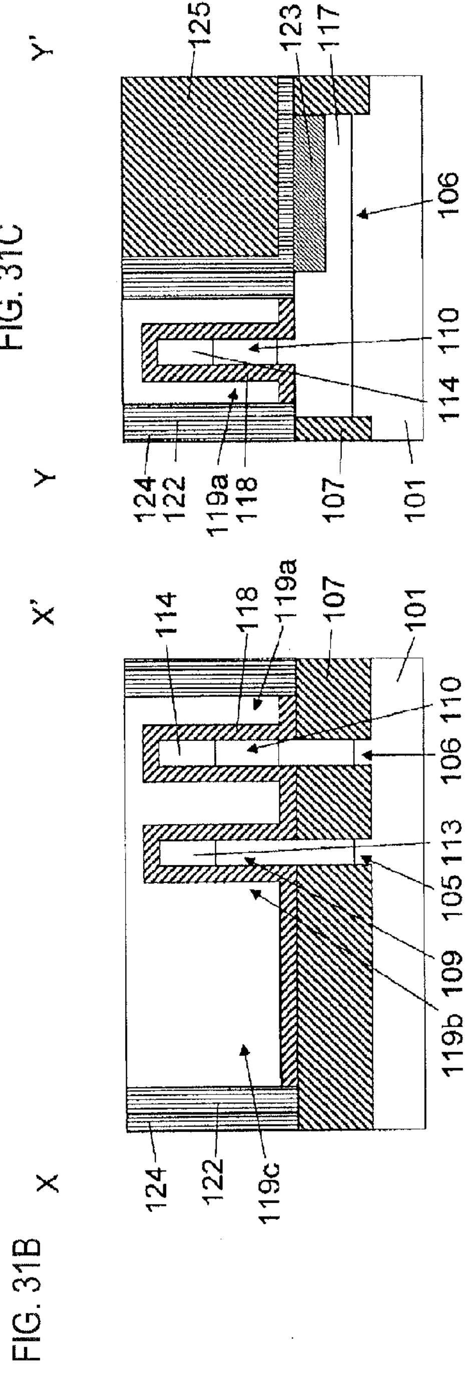


FIG. 31B

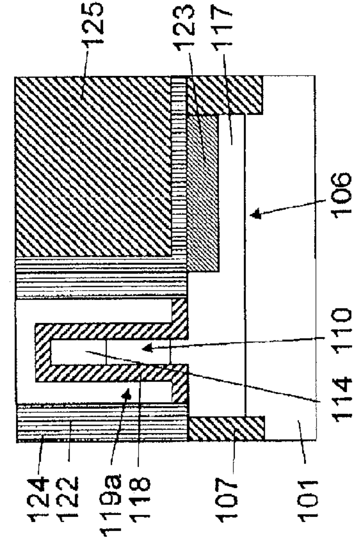


FIG. 31C

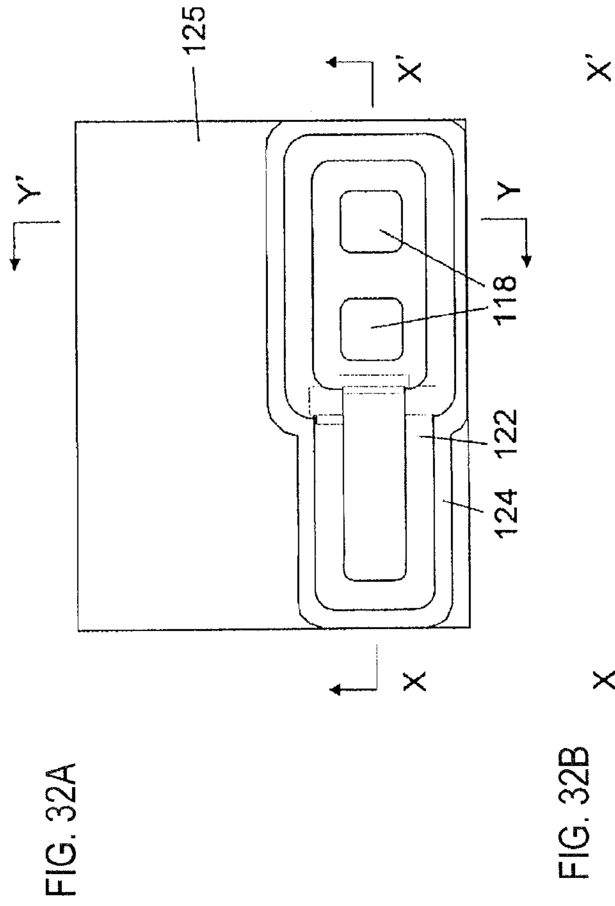


FIG. 32A

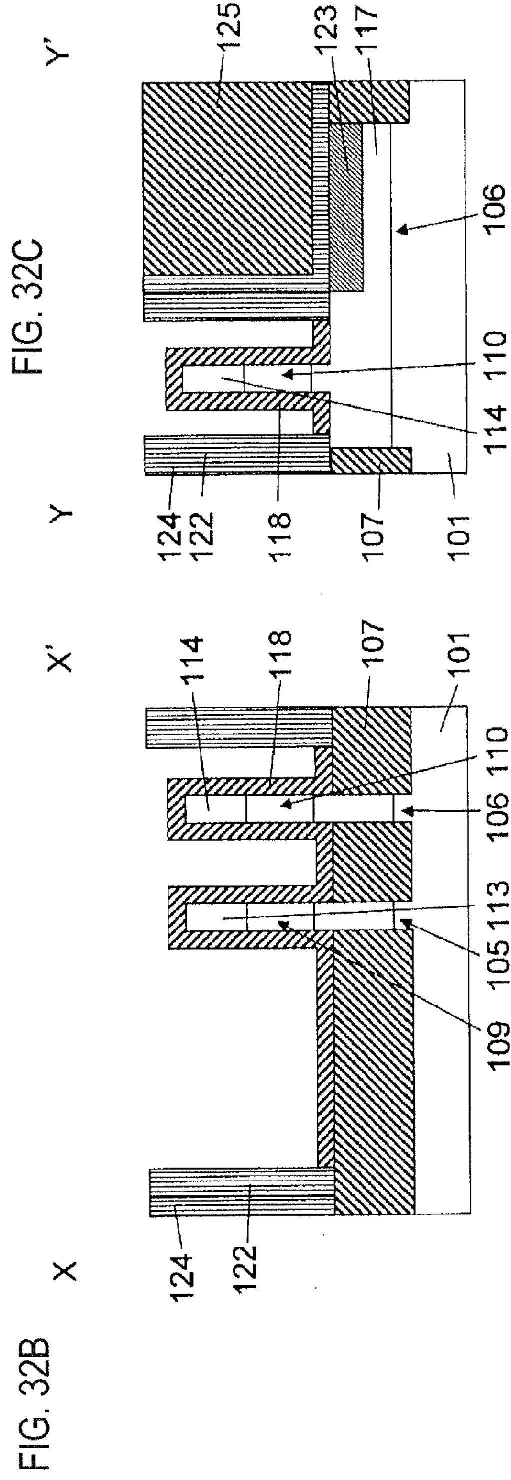


FIG. 32B

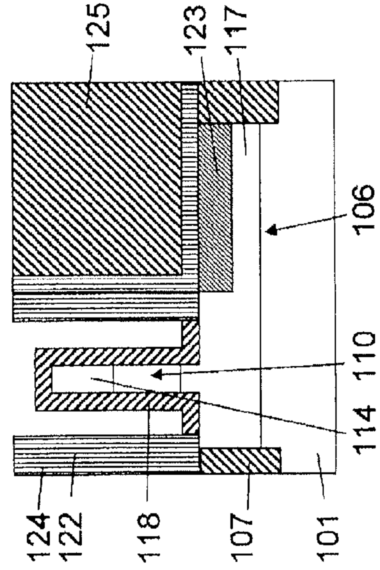


FIG. 32C

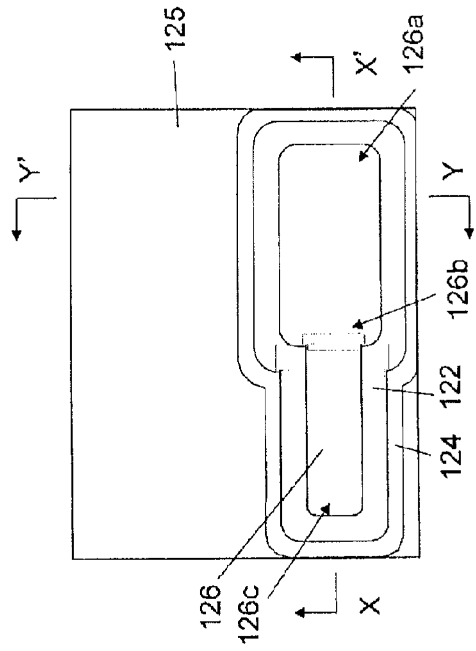


FIG. 33A

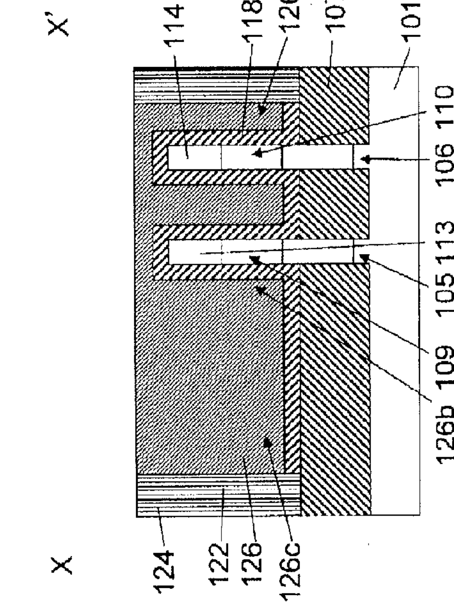


FIG. 33B

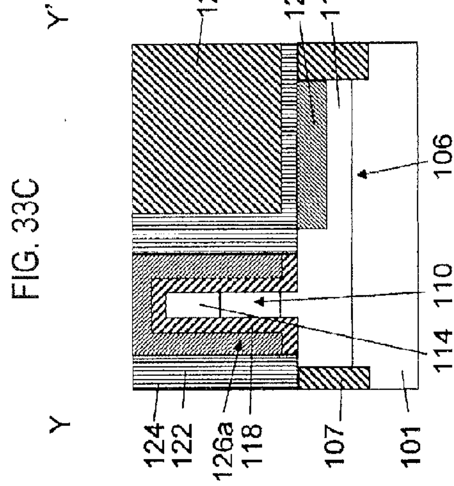


FIG. 33C

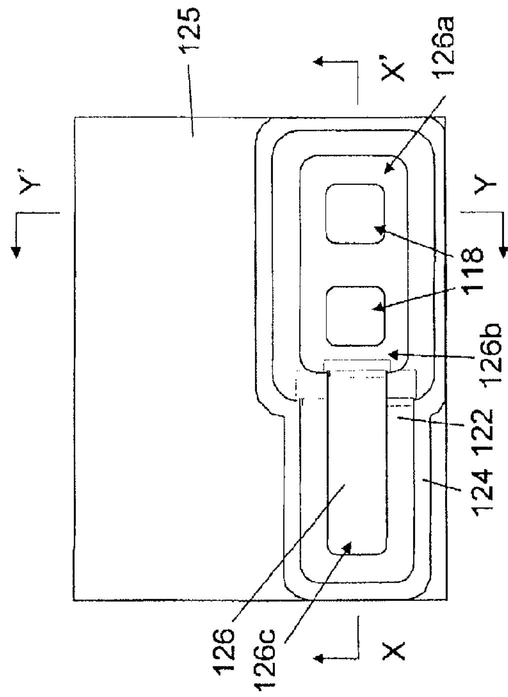


FIG. 34A

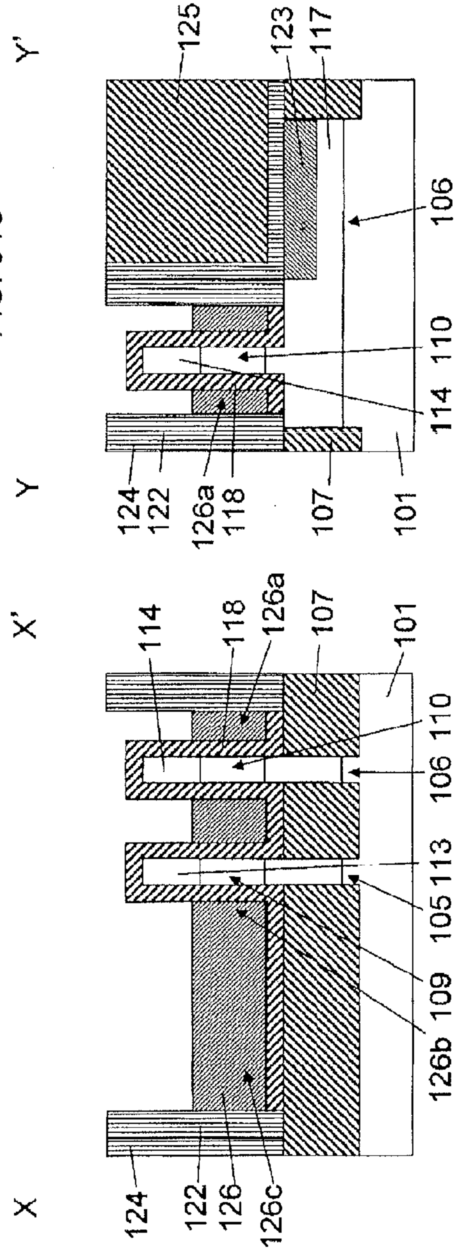


FIG. 34B

FIG. 34C

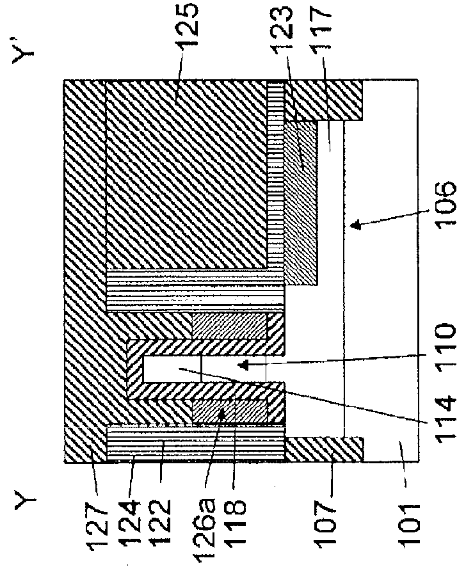


FIG. 35C

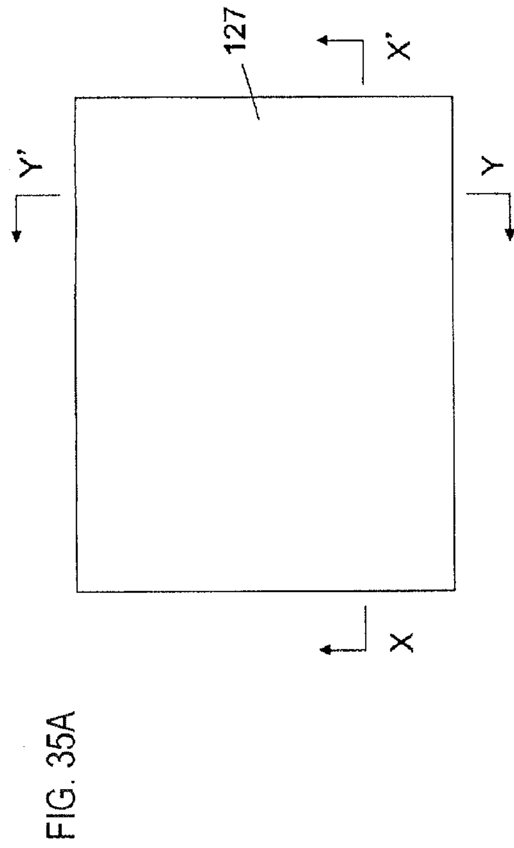


FIG. 35A

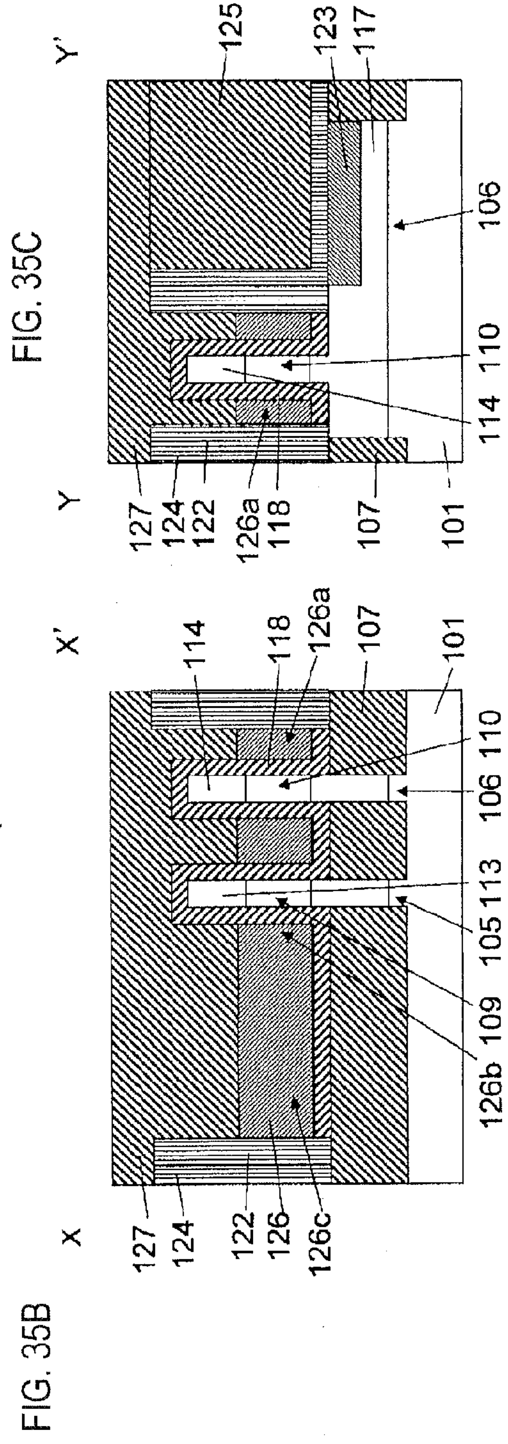


FIG. 35B

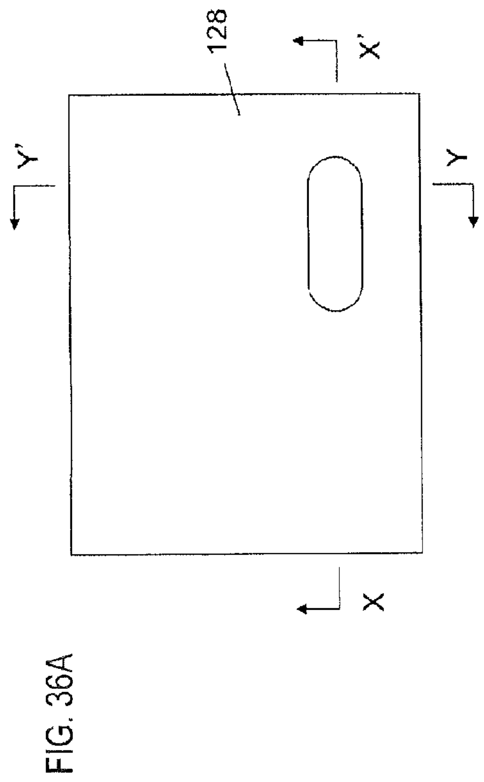


FIG. 36A

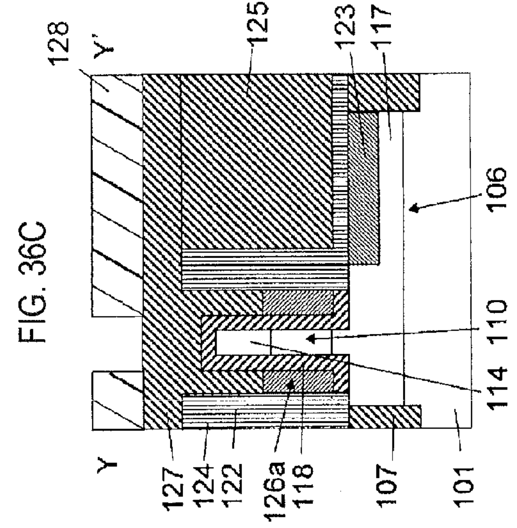


FIG. 36C

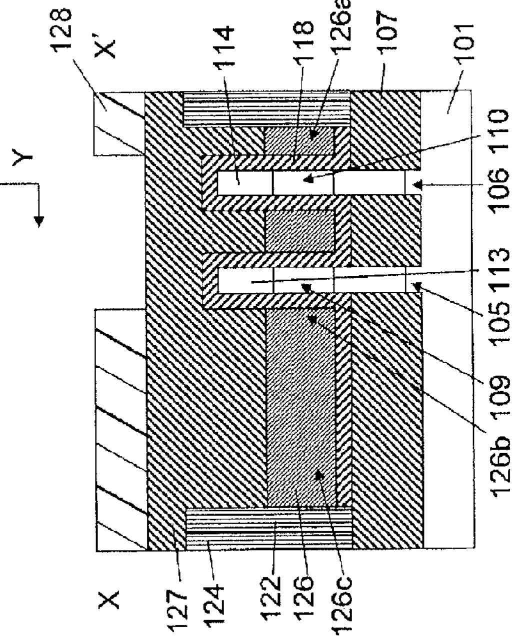


FIG. 36B

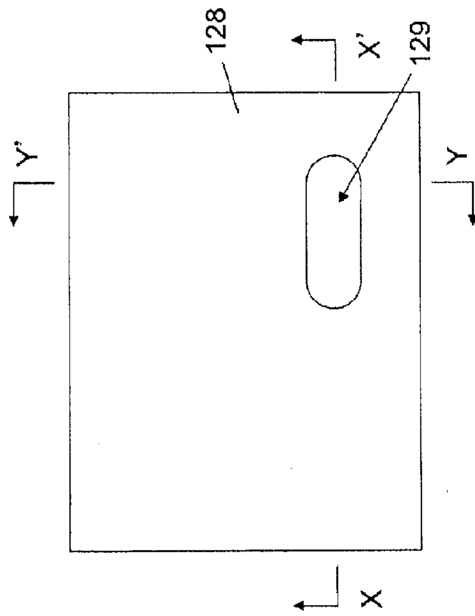


FIG. 37A

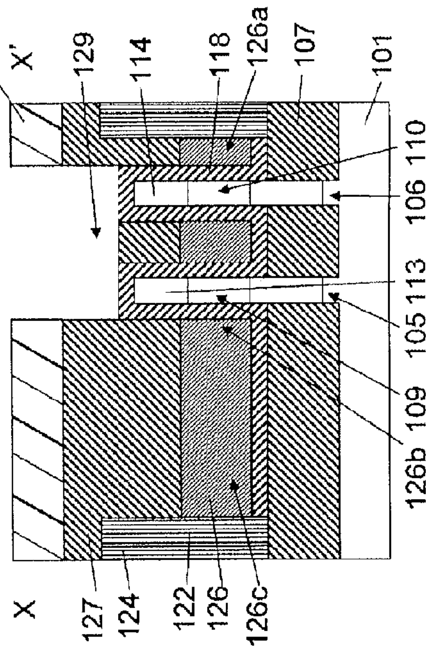


FIG. 37B

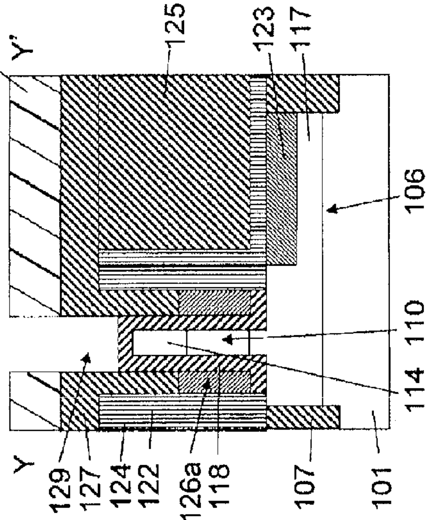


FIG. 37C

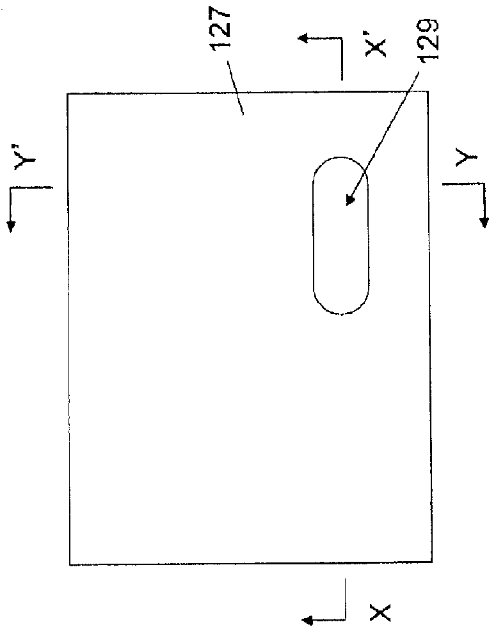


FIG. 38A

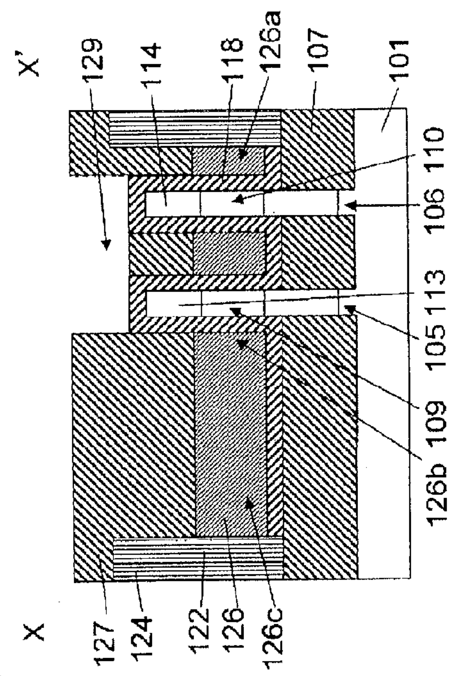


FIG. 38B

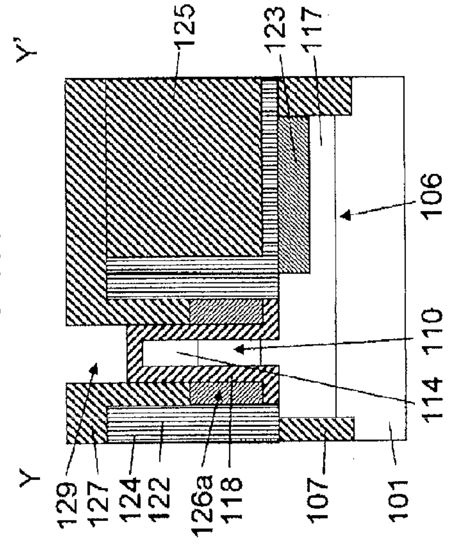


FIG. 38C

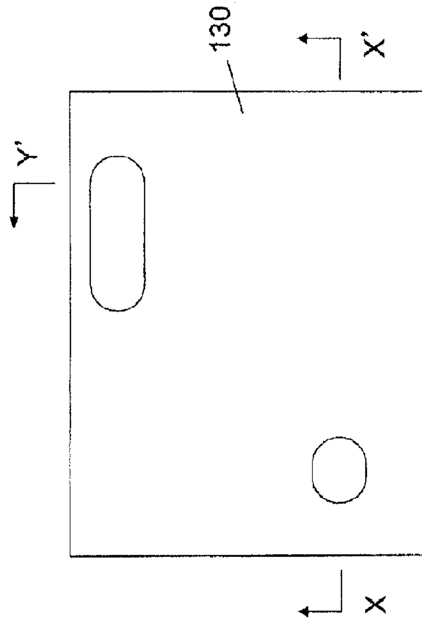


FIG. 39A

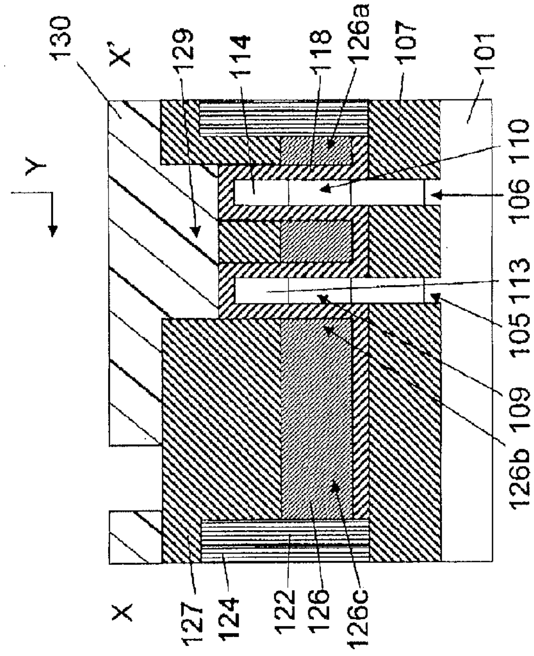


FIG. 39B

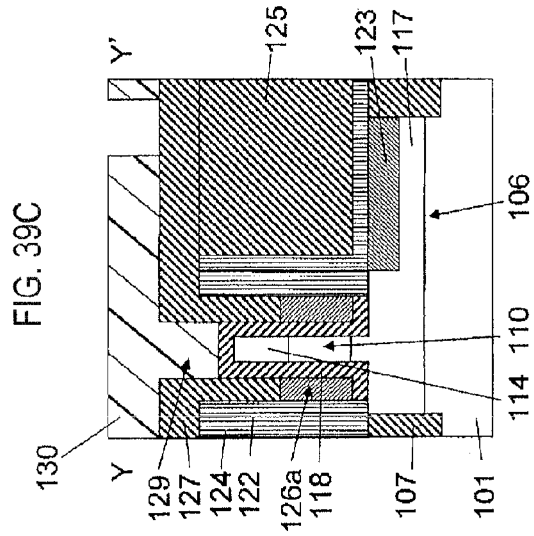


FIG. 39C

FIG. 40A

132 130 Y' Y X X' 131

FIG. 40B

X X' 130 129 114 118 126a 107 101 110 106 113 105 109 126b 127 124 131 122 126 126c

FIG. 40C

Y Y' 132 125 123 117 106 110 114 130 129 127 124 122 126a 118 107 101

FIG. 41A

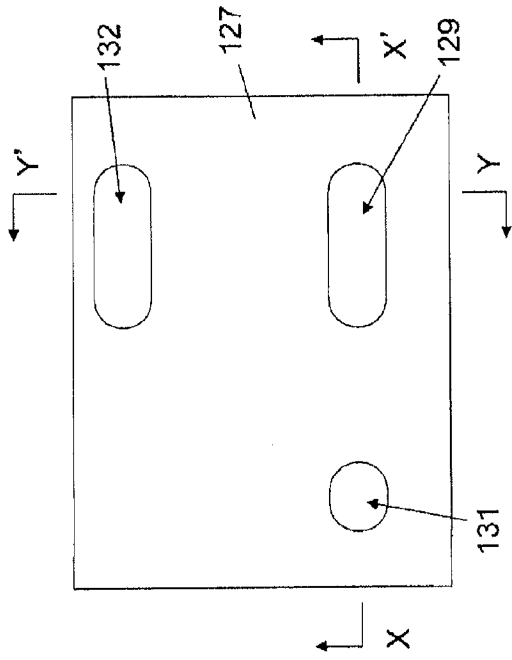


FIG. 41B

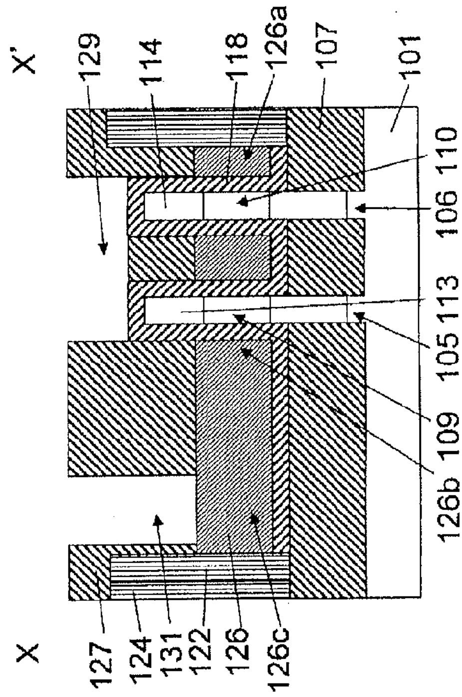
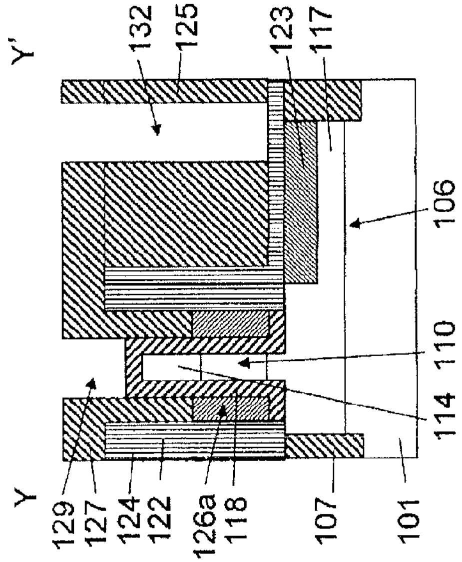


FIG. 41C



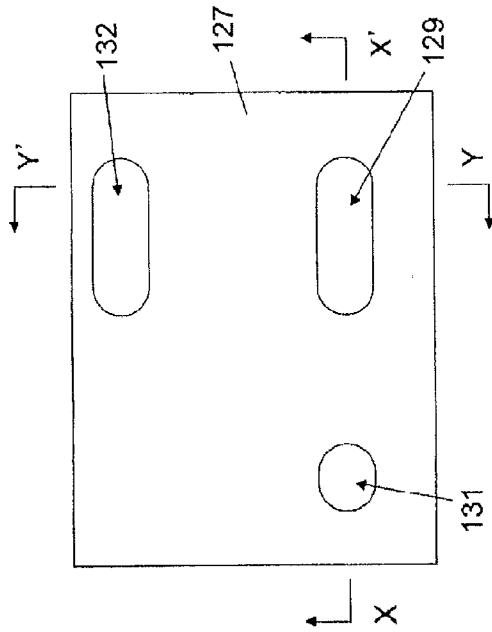


FIG. 42A

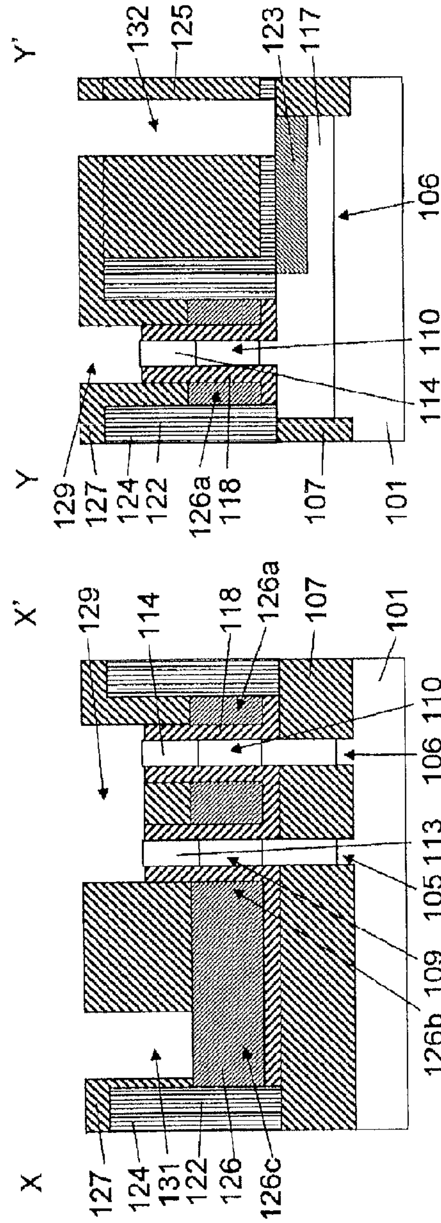


FIG. 42B

FIG. 42C

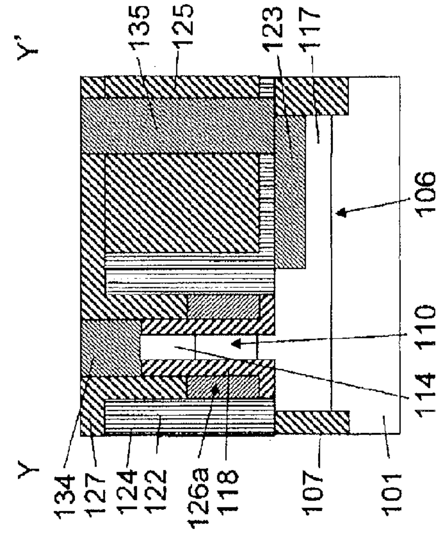


FIG. 43C

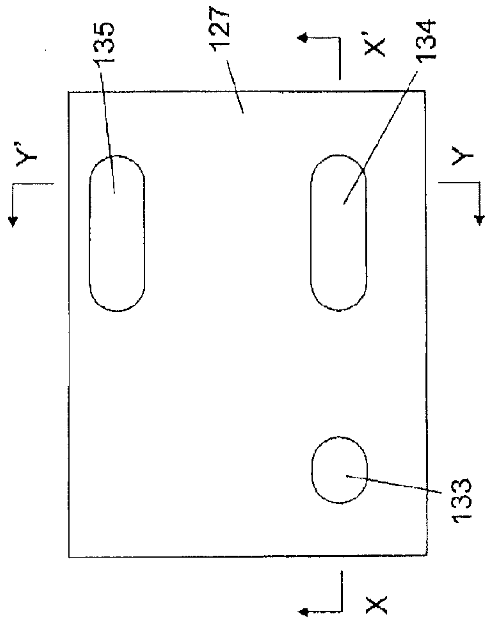


FIG. 43A

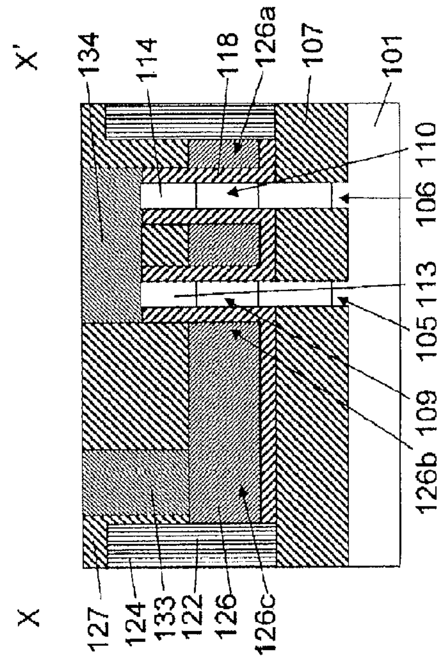


FIG. 43B

FIG. 44A

Y' 136 X X' Y

FIG. 44B

X X'
136 127 134 124 133 114 122 126 118 126c 126a 107 101
126b 109 105 113 106 110

FIG. 44C

Y Y'
134 136 127 124 135 122 125 126a 118 123 107 117 101
114 110 106

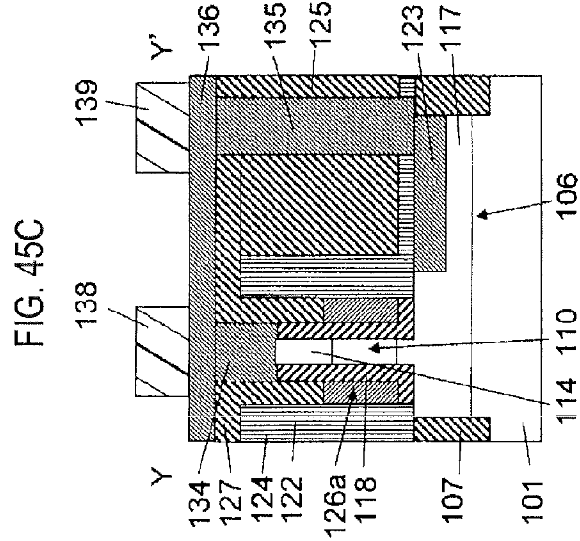


FIG. 45C

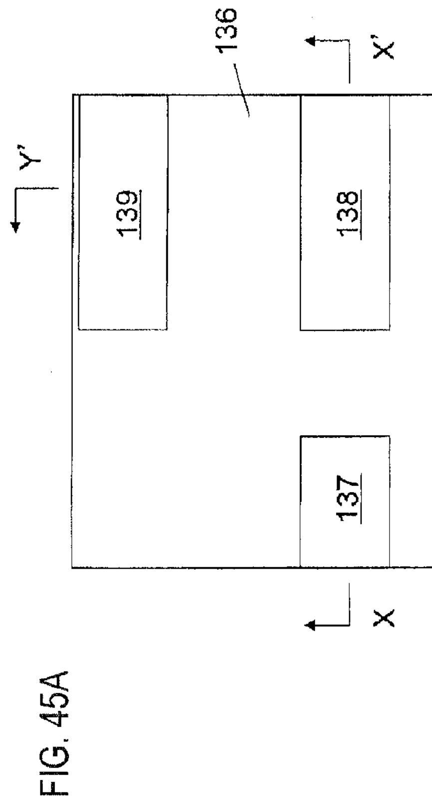


FIG. 45A

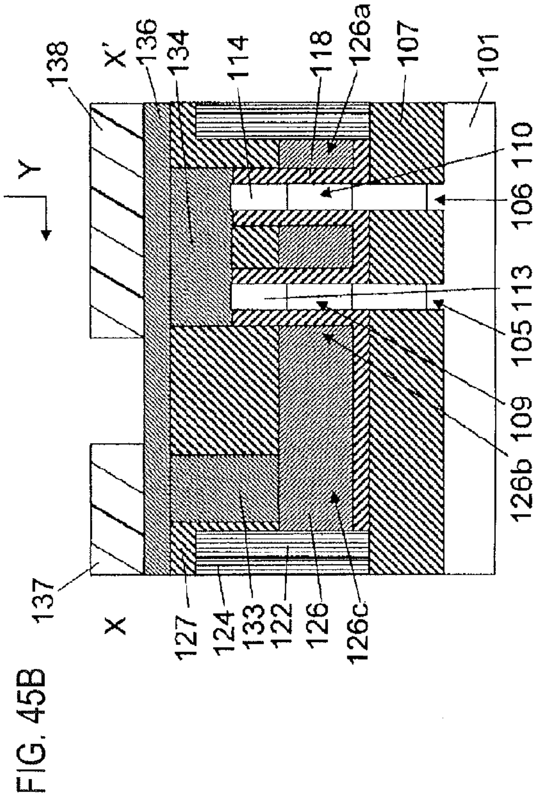


FIG. 45B

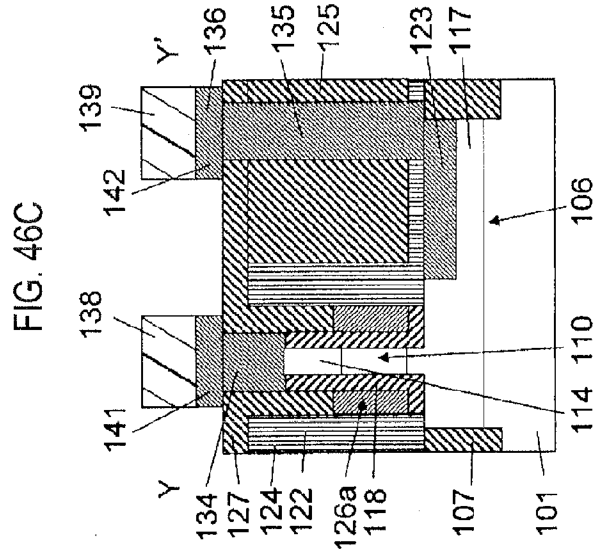


FIG. 46C

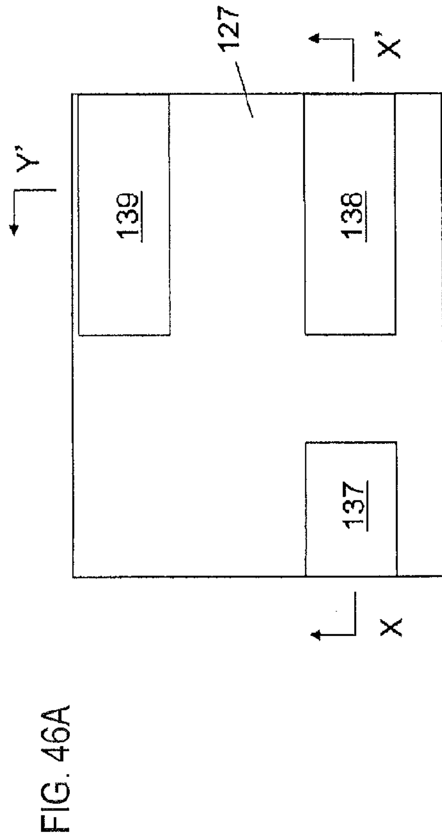


FIG. 46A

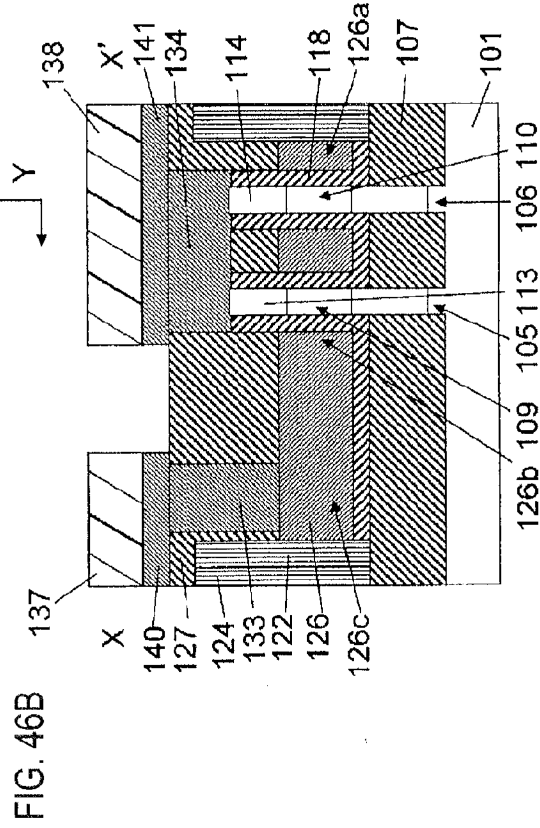


FIG. 46B

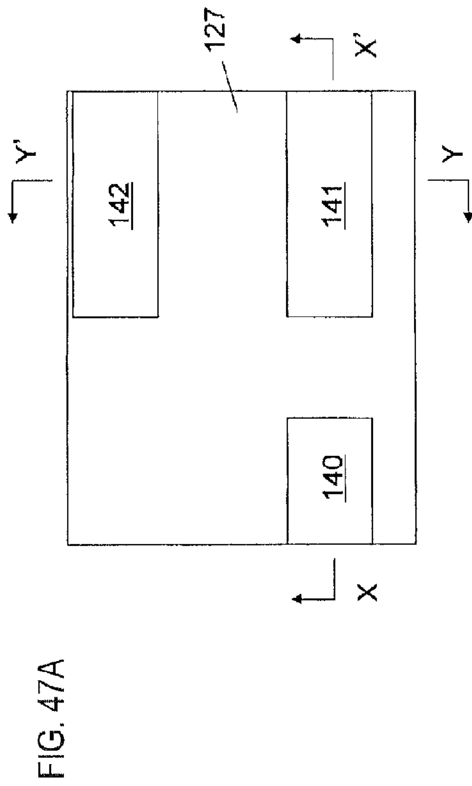


FIG. 47A

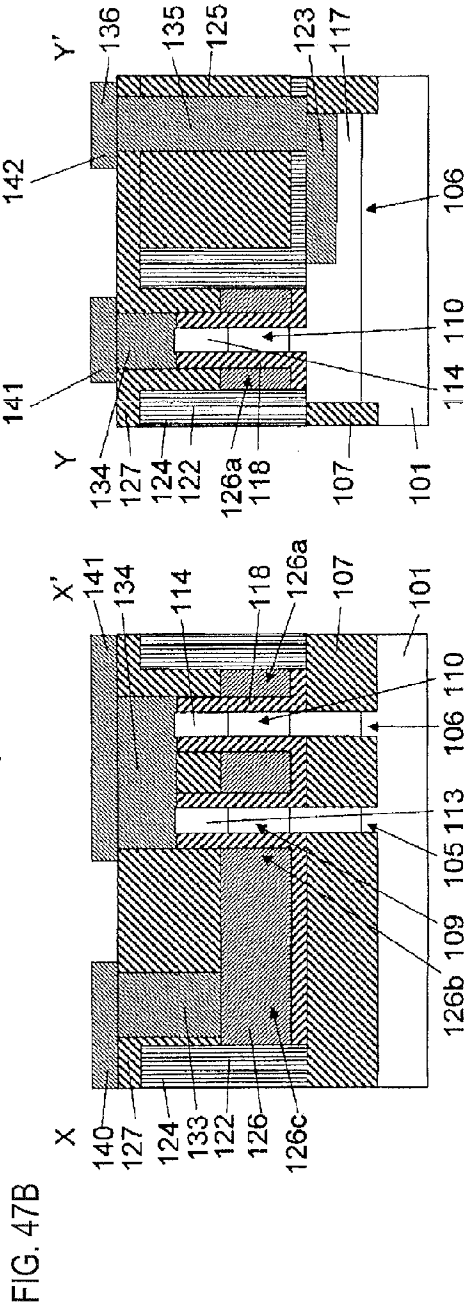


FIG. 47B

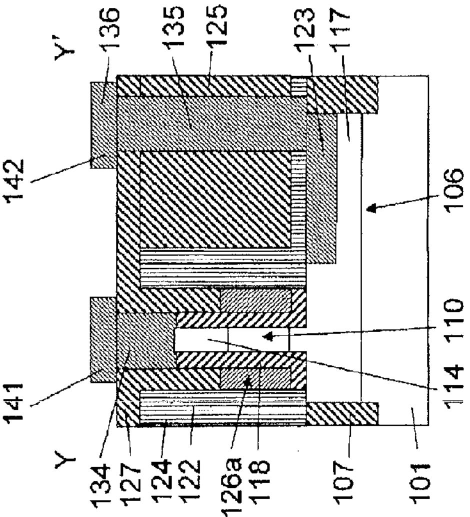


FIG. 47C

METHOD FOR PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 14/743,266, filed Jun. 18, 2015, which is a continuation of U.S. patent application Ser. No. 14/083,060, now U.S. Pat. No. 9,117,690, filed Nov. 18, 2013, which is Continuation In Part (CIP) application of U.S. patent application Ser. No. 13/679,225, now U.S. Pat. No. 8,735,971, filed Nov. 16, 2013, which pursuant to 35 U.S.C. §119(e), claims the benefit of the filing date of Provisional U.S. Patent Application Ser. No. 61/566,244 filed on Dec. 2, 2011. The entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device.

[0004] 2. Description of the Related Art

[0005] The degree of integration of semiconductor integrated circuits, in particular, integrated circuits using MOS transistors, has been increasing. With the increasing degree of integration, the size of MOS transistors used in integrated circuits has been decreased to nano-scale dimensions. Such a decrease in the size of MOS transistors causes difficulty in suppressing leak currents, which poses a problem in that it is hard to reduce the area occupied by the circuits because of the requirements of the secure retention of necessary currents. To address the problem, a surrounding gate transistor (SGT) having a structure in which a source, a gate, and a drain are arranged vertically with respect to a substrate and the gate surrounds a pillar-shaped semiconductor layer has been proposed (e.g., Japanese Unexamined Patent Application Publication Nos. 2-71556, 2-188966, and 3-145761).

[0006] By using a metal for gate electrodes instead of a polysilicon, the depletion can be suppressed and the resistance of the gate electrodes can be decreased. However, the production process after a metal gate is formed needs to be conducted always in consideration of metal contamination due to the metal gate.

[0007] In existing MOS transistors, in order to perform both a metal gate process and a high-temperature process, a metal gate last process in which a metal gate is formed after a high-temperature process has been employed in production of actual products (IEDM 2007 K. Mistry et al., pp. 247 to 250). The metal gate last process includes forming a gate using a polysilicon, then depositing an interlayer insulating film, exposing the polysilicon gate by chemical mechanical polishing, etching the polysilicon gate, and depositing a metal. Therefore, a metal gate last process in which a metal gate is formed after a high-temperature process also needs to be employed in SGTs in order to perform both a metal gate process and a high-temperature process. In SGTs, since a pillar-shaped silicon layer is located at a higher position than a gate, a scheme for employing the metal gate last process is required.

[0008] To decrease the parasitic capacitance between a gate line and a substrate, a first insulating film is used in existing MOS transistors. For example, in the FINFET (IEDM 2010 CC. Wu et al., 27.1.1 to 27.1.4), the parasitic capacitance between a gate line and a substrate is decreased by forming a first insulating film around a single fin-shaped semiconductor layer and etching back the first insulating film to expose the fin-shaped semiconductor layer. Therefore, such a first insulating film also needs to be used in SGTs to decrease the parasitic capacitance between a gate line and a substrate. In SGTs, since a pillar-shaped semiconductor layer is formed in addition to the fin-shaped semiconductor layer, a scheme for forming a pillar-shaped semiconductor layer is required.

[0009] Furthermore, FINFETs in which two transistors are formed from a single dummy pattern has been known (e.g., Japanese Unexamined Patent Application Publication No. 2011-71235). A sidewall is formed around a dummy pattern and a substrate is etched using the sidewall as a mask to form a fin, and thus two transistors are formed from a single dummy pattern.

SUMMARY

[0010] It is an object to provide a SGT production method in which the parasitic capacitance between a gate line and a substrate is decreased, a gate last process is employed, and two transistors are produced from a single dummy pattern and a SGT structure formed by the production method.

[0011] A method for producing a semiconductor device according to an aspect of the present invention includes:

[0012] a first step of forming, on a substrate, a first fin-shaped silicon layer and a second fin-shaped silicon layer that are connected to each other at their ends to form a closed loop, forming a first insulating film around the first fin-shaped silicon layer and second fin-shaped silicon layer, forming a first pillar-shaped silicon layer in an upper portion of the first fin-shaped silicon layer, and forming a second pillar-shaped silicon layer in an upper portion of the second fin-shaped silicon layer, the first pillar-shaped silicon layer having a width equal to a width of the first fin-shaped silicon layer and the second pillar-shaped silicon layer having a width equal to a width of the second fin-shaped silicon layer; after the first step, a second step of forming diffusion layers by implanting an impurity into an upper portion of the first pillar-shaped silicon layer, an upper portion of the first fin-shaped silicon layer, and a lower portion of the first pillar-shaped silicon layer and forming diffusion layers by implanting an impurity into an upper portion of the second pillar-shaped silicon layer, an upper portion of the second fin-shaped silicon layer, and a lower portion of the second pillar-shaped silicon layer; after the second step, a third step of forming a gate insulating film on and around the first pillar-shaped silicon layer and second pillar-shaped silicon layer, forming a first polysilicon gate electrode and a second polysilicon gate electrode so as to cover the gate insulating film, and forming a polysilicon gate line, where an upper surface of a polysilicon after the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line are formed is located at a higher position than the gate insulating film on the diffusion layer in the upper portion of the first pillar-shaped silicon layer and the gate insulating film on the diffusion layer in the upper portion of the second pillar-shaped silicon layer; after the third step, a fourth step of forming a silicide in an upper portion of the diffusion layer formed in the upper portion of the first fin-shaped silicon layer and in an upper portion of the diffusion layer formed in the second fin-shaped silicon layer; after the fourth step, a fifth step of depositing an interlayer insulating film, exposing the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate

line, etching the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line, then depositing a metal, and forming a first metal gate electrode, a second metal gate electrode, and a metal gate line, the metal gate line being connected to the first metal gate electrode and second metal gate electrode and extending in a direction perpendicular to a direction in which the first fin-shaped silicon layer and second fin-shaped silicon layer extend; and, after the fifth step, a sixth step of forming a contact that is directly connected to the diffusion layer in the upper portion of the first pillar-shaped silicon layer and the diffusion layer in the upper portion of the second pillar-shaped silicon layer.

[0013] Preferably, the first step includes depositing a second oxide film on a substrate in order to form a dummy pattern; forming a first resist for forming the dummy pattern; etching the second oxide film to form the dummy pattern; removing the first resist; depositing a first nitride film; forming a first nitride film sidewall around the dummy pattern by etching the first nitride film in such a manner that the first nitride film is made to remain in a sidewall shape; removing the dummy pattern; etching the substrate using the first nitride film sidewall as a mask to form the first fin-shaped silicon layer and the second fin-shaped silicon layer that are connected to each other at their ends to form a closed loop; forming the first insulating film around the first fin-shaped silicon layer and second fin-shaped silicon layer; removing the first nitride film sidewall; etching back the first insulating film to expose an upper portion of the first fin-shaped silicon layer and an upper portion of the second fin-shaped silicon layer; forming a second resist so as to be perpendicular to the first fin-shaped silicon layer and second fin-shaped silicon layer; etching the first fin-shaped silicon layer and the second fin-shaped silicon layer; and removing the second resist to form the first pillar-shaped silicon layer such that a portion in which the first fin-shaped silicon layer is perpendicular to the second resist is the first pillar-shaped silicon layer and to form the second pillar-shaped silicon layer such that a portion in which the second fin-shaped silicon layer is perpendicular to the second resist is the second pillar-shaped silicon layer.

[0014] Preferably, the second step performed after the first step includes depositing a third oxide film on the entire structure formed in the first step; forming a second nitride film; etching the second nitride film in such a manner that the second nitride film is made to remain in a sidewall shape; forming the diffusion layers by implanting an impurity into the upper portion of the first pillar-shaped silicon layer, the upper portion of the first fin-shaped silicon layer, the upper portion of the second pillar-shaped silicon layer, and the upper portion of the second fin-shaped silicon layer; removing the second nitride film and the third oxide film; and performing a heat treatment.

[0015] Preferably, the third step performed after the second step includes forming the gate insulating film so as to surround silicon pillars; depositing and planarizing a polysilicon such that an upper surface of the planarized polysilicon is located at a higher position than the gate insulating film on the diffusion layer formed in the upper portion of the first pillar-shaped silicon layer and the gate insulating film on the diffusion layer formed in the upper portion of the second pillar-shaped silicon layer; depositing a third nitride film; forming a third resist for forming the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line; etching the third nitride film and the polysilicon to form the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line; etching the gate insulating film; and removing the third resist.

[0016] Preferably, a fourth nitride film is deposited on the entire structure formed in the third step, the fourth nitride film is etched in such a manner that the fourth nitride film is made to remain in a sidewall shape, and a metal is deposited to form the silicide in the upper portions of the diffusion layers formed in the upper portions of the first fin-shaped silicon layer and second fin-shaped silicon layer.

[0017] Preferably, a fifth nitride film is deposited on the entire structure formed in the fourth step; an interlayer insulating film is deposited and planarized by chemical mechanical polishing; the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line are exposed by chemical mechanical polishing; the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line are etched; a metal is deposited to fill, with the metal, portions in which the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line have been present; and the metal is etched to expose the gate insulating film on the diffusion layer in the upper portion of the first pillar-shaped silicon layer and the gate insulating film on the diffusion layer in the upper portion of the second pillar-shaped silicon layer and to form the first metal gate electrode, the second metal gate electrode, and the metal gate line.

[0018] A semiconductor device according to an aspect of the invention includes a first fin-shaped semiconductor layer on a substrate, a second fin-shaped semiconductor layer on the substrate, a first insulating film around the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer; a first pillar-shaped semiconductor layer on the first fin-shaped semiconductor layer; a second pillar-shaped semiconductor layer on the second fin-shaped semiconductor layer, where a width of the bottom of the first and second pillar-shaped semiconductors is equal to a width of the top of the first and second fin-shaped semiconductor layers, respectively; a first diffusion layer in an upper portion of the first fin-shaped semiconductor layer and a lower portion of the first pillar-shaped semiconductor layer; a second diffusion layer in an upper portion of the first pillar-shaped semiconductor layer; a third diffusion layer in an upper portion of the second fin-shaped semiconductor layer and a lower portion of the second pillar-shaped semiconductor layer; a fourth diffusion layer in an upper portion of the second pillar-shaped semiconductor layer; a first gate insulating film around the first pillar-shaped semiconductor layer; a first metal gate electrode around the first gate insulating film; a second gate insulating film around the second pillar-shaped semiconductor layer; a second metal gate electrode around the second gate insulating film; a metal gate line connected to the first metal gate electrode and the second metal gate electrode and extending in a direction perpendicular to a direction in which the first fin-shaped semiconductor layer and second fin-shaped semiconductor layer extend; a contact on the upper portion of the second diffusion layer and directly connected to the second diffusion layer; and a contact on the upper portion of the fourth diffusion layer and directly connected to the fourth diffusion layer.

[0019] A semiconductor device according to another aspect of the present invention includes a first fin-shaped semiconductor layer formed on a substrate, a second fin-shaped semiconductor layer formed on the substrate, the first fin-shaped semiconductor layer and the second fin-shaped semiconduc-

tor layer being connected to each other at their ends to form a closed loop, a first insulating film formed around the first fin-shaped semiconductor layer and second fin-shaped semiconductor layer, a first pillar-shaped semiconductor layer formed on the first fin-shaped semiconductor layer and having a width equal to a width of the first fin-shaped semiconductor layer, a second pillar-shaped semiconductor layer formed on the second fin-shaped semiconductor layer and having a width equal to a width of the second fin-shaped semiconductor layer, a diffusion layer formed in an upper portion of the first fin-shaped semiconductor layer and a lower portion of the first pillar-shaped semiconductor layer, a diffusion layer formed in an upper portion of the first pillar-shaped semiconductor layer, a diffusion layer formed in an upper portion of the second fin-shaped semiconductor layer and a lower portion of the second pillar-shaped semiconductor layer, a diffusion layer formed in an upper portion of the second pillar-shaped semiconductor layer, a silicide formed in upper portions of the diffusion layers formed in the upper portion of the first fin-shaped semiconductor layer and in the upper portion of the second fin-shaped semiconductor layer, a gate insulating film formed around the first pillar-shaped semiconductor layer, a first metal gate electrode formed around the gate insulating film, a gate insulating film formed around the second pillar-shaped semiconductor layer, a second metal gate electrode formed around the gate insulating film, a metal gate line that is connected to the first metal gate electrode and the second metal gate electrode and that extends in a direction perpendicular to a direction in which the first fin-shaped semiconductor layer and second fin-shaped semiconductor layer extend, a contact formed on the diffusion layer formed in the upper portion of the first pillar-shaped semiconductor layer so as to be directly connected to the diffusion layer, and a contact formed on the diffusion layer formed in the upper portion of the second pillar-shaped semiconductor layer so as to be directly connected to the diffusion layer.

[0020] The present invention can provide a SGT production method in which the parasitic capacitance between a gate line and a substrate is decreased, a gate last process is employed, and two transistors are produced from a single dummy pattern and a SGT structure formed by the production method.

[0021] Two SGTs can be easily produced from a single dummy pattern by employing a method for producing an existing FINFET. In the method, a sidewall is formed around a dummy pattern and a substrate is etched using the sidewall as a mask to form a fin, and thus two transistors are formed from a single dummy pattern.

[0022] In addition, a metal gate SGT can be easily produced because a production method that employs an existing metal gate last process can be used. A silicide has been conventionally formed in an upper portion of a pillar-shaped silicon layer, but the temperature at which a polysilicon is deposited is higher than the temperature at which a silicide is formed and thus a silicide needs to be formed after the formation of a polysilicon gate. If a silicide is formed in an upper portion of a silicon pillar, a polysilicon gate is formed, a hole is made above a polysilicon gate electrode, an insulating film is formed on the sidewall of the hole, a silicide is formed, and the hole is filled with an insulating film. This increases the number of production steps. Therefore, the existing metal gate last process below can be employed. A diffusion layer is formed before the formation of a polysilicon gate electrode and a polysilicon gate line. By covering a pillar-shaped silicon layer with the polysilicon gate electrode and by forming a silicide only in an upper portion of a fin-shaped silicon layer, a polysilicon gate is formed. Subsequently, an interlayer insulating film is deposited and then the polysilicon gate is exposed by chemical mechanical polishing. The polysilicon gate is etched and then a metal is deposited.

BRIEF DESCRIPTION OF THE DRAWING

[0023] FIG. **1**A is a plan view of a semiconductor device according to an embodiment of the present invention, FIG. **1**B is a sectional view taken along line X-X' of FIG. **1**A, and FIG. **1**C is a sectional view taken along line Y-Y' of FIG. **1**A;

[0024] FIG. **2**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **2**B is a sectional view taken along line X-X' of FIG. **2**A, and FIG. **2**C is a sectional view taken along line Y-Y' of FIG. **2**A;

[0025] FIG. **3**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **3**B is a sectional view taken along line X-X' of FIG. **3**A, and FIG. **3**C is a sectional view taken along line Y-Y' of FIG. **3**A;

[0026] FIG. **4**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **4**B is a sectional view taken along line X-X' of FIG. **4**A, and FIG. **4**C is a sectional view taken along line Y-Y' of FIG. **4**A;

[0027] FIG. **5**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **5**B is a sectional view taken along line X-X' of FIG. **5**A, and FIG. **5**C is a sectional view taken along line Y-Y' of FIG. **5**A;

[0028] FIG. **6**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **6**B is a sectional view taken along line X-X' of FIG. **6**A, and FIG. **6**C is a sectional view taken along line Y-Y' of FIG. **6**A;

[0029] FIG. **7**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **7**B is a sectional view taken along line X-X' of FIG. **7**A, and FIG. **7**C is a sectional view taken along line Y-Y' of FIG. **7**A;

[0030] FIG. **8**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **8**B is a sectional view taken along line X-X' of FIG. **8**A, and FIG. **8**C is a sectional view taken along line Y-Y' of FIG. **8**A;

[0031] FIG. **9**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **9**B is a sectional view taken along line X-X' of FIG. **9**A, and FIG. **9**C is a sectional view taken along line Y-Y' of FIG. **9**A;

[0032] FIG. **10**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **10**B is a sectional view taken along line X-X' of FIG. **10**A, and FIG. **10**C is a sectional view taken along line Y-Y' of FIG. **10**A;

[0033] FIG. **11**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **11**B is a sectional view taken along line X-X' of FIG. **11**A, and FIG. **11**C is a sectional view taken along line Y-Y' of FIG. **11**A;

[0034] FIG. **12**A is a plan view showing a method for producing a semiconductor device according to an embodi-

ment of the present invention, FIG. **12**B is a sectional view taken along line X-X' of FIG. **12**A, and FIG. **12**C is a sectional view taken along line Y-Y' of FIG. **12**A;

[0035] FIG. **13**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **13**B is a sectional view taken along line X-X' of FIG. **13**A, and FIG. **13**C is a sectional view taken along line Y-Y' of FIG. **13**A;

[0036] FIG. **14**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **14**B is a sectional view taken along line X-X' of FIG. **14**A, and FIG. **14**C is a sectional view taken along line Y-Y' of FIG. **14**A;

[0037] FIG. **15**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **15**B is a sectional view taken along line X-X' of FIG. **15**A, and FIG. **15**C is a sectional view taken along line Y-Y' of FIG. **15**A;

[0038] FIG. **16**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **16**B is a sectional view taken along line X-X' of FIG. **16**A, and FIG. **16**C is a sectional view taken along line Y-Y' of FIG. **16**A;

[0039] FIG. **17**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **17**B is a sectional view taken along line X-X' of FIG. **17**A, and FIG. **17**C is a sectional view taken along line Y-Y' of FIG. **17**A;

[0040] FIG. **18**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **18**B is a sectional view taken along line X-X' of FIG. **18**A, and FIG. **18**C is a sectional view taken along line Y-Y' of FIG. **18**A;

[0041] FIG. **19**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **19**B is a sectional view taken along line X-X' of FIG. **19**A, and FIG. **19**C is a sectional view taken along line Y-Y' of FIG. **19**A;

[0042] FIG. **20**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **20**B is a sectional view taken along line X-X' of FIG. **20**A, and FIG. **20**C is a sectional view taken along line Y-Y' of FIG. **20**A;

[0043] FIG. **21**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **21**B is a sectional view taken along line X-X' of FIG. **21**A, and FIG. **21**C is a sectional view taken along line Y-Y' of FIG. **21**A;

[0044] FIG. **22**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **22**B is a sectional view taken along line X-X' of FIG. **22**A, and FIG. **22**C is a sectional view taken along line Y-Y' of FIG. **22**A;

[0045] FIG. **23**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **23**B is a sectional view taken along line X-X' of FIG. **23**A, and FIG. **23**C is a sectional view taken along line Y-Y' of FIG. **23**A;

[0046] FIG. **24**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **24**B is a sectional view taken along line X-X' of FIG. **24**A, and FIG. **24**C is a sectional view taken along line Y-Y' of FIG. **24**A;

[0047] FIG. **25**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **25**B is a sectional view taken along line X-X' of FIG. **25**A, and FIG. **25**C is a sectional view taken along line Y-Y' of FIG. **25**A;

[0048] FIG. **26**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **26**B is a sectional view taken along line X-X' of FIG. **26**A, and FIG. **26**C is a sectional view taken along line Y-Y' of FIG. **26**A;

[0049] FIG. **27**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **27**B is a sectional view taken along line X-X' of FIG. **27**A, and FIG. **27**C is a sectional view taken along line Y-Y' of FIG. **27**A;

[0050] FIG. **28**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **28**B is a sectional view taken along line X-X' of FIG. **28**A, and FIG. **28**C is a sectional view taken along line Y-Y' of FIG. **28**A;

[0051] FIG. **29**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **29**B is a sectional view taken along line X-X' of FIG. **29**A, and FIG. **29**C is a sectional view taken along line Y-Y' of FIG. **29**A;

[0052] FIG. **30**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **30**B is a sectional view taken along line X-X' of FIG. **30**A, and FIG. **30**C is a sectional view taken along line Y-Y' of FIG. **30**A;

[0053] FIG. **31**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **31**B is a sectional view taken along line X-X' of FIG. **31**A, and FIG. **31**C is a sectional view taken along line Y-Y' of FIG. **31**A;

[0054] FIG. **32**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **32**B is a sectional view taken along line X-X' of FIG. **32**A, and FIG. **32**C is a sectional view taken along line Y-Y' of FIG. **32**A;

[0055] FIG. **33**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **33**B is a sectional view taken along line X-X' of FIG. **33**A, and FIG. **33**C is a sectional view taken along line Y-Y' of FIG. **33**A;

[0056] FIG. **34**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **34**B is a sectional view taken along line X-X' of FIG. **34**A, and FIG. **34**C is a sectional view taken along line Y-Y' of FIG. **34**A;

[0057] FIG. **35**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **35**B is a sectional view taken along line X-X' of FIG. **35**A, and FIG. **35**C is a sectional view taken along line Y-Y' of FIG. **35**A;

[0058] FIG. **36**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **36**B is a sectional view taken along line X-X' of FIG. **36**A, and FIG. **36**C is a sectional view taken along line Y-Y' of FIG. **36**A;

[0059] FIG. **37**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **37**B is a sectional view

taken along line X-X' of FIG. **37**A, and FIG. **37**C is a sectional view taken along line Y-Y' of FIG. **37**A;

[0060] FIG. **38**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **38**B is a sectional view taken along line X-X' of FIG. **38**A, and FIG. **38**C is a sectional view taken along line Y-Y' of FIG. **38**A;

[0061] FIG. **39**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **39**B is a sectional view taken along line X-X' of FIG. **39**A, and FIG. **39**C is a sectional view taken along line Y-Y' of FIG. **39**A;

[0062] FIG. **40**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **40**B is a sectional view taken along line X-X' of FIG. **40**A, and FIG. **40**C is a sectional view taken along line Y-Y' of FIG. **40**A;

[0063] FIG. **41**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **41**B is a sectional view taken along line X-X' of FIG. **41**A, and FIG. **41**C is a sectional view taken along line Y-Y' of FIG. **41**A;

[0064] FIG. **42**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **42**B is a sectional view taken along line X-X' of FIG. **42**A, and FIG. **42**C is a sectional view taken along line Y-Y' of FIG. **42**A;

[0065] FIG. **43**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **43**B is a sectional view taken along line X-X' of FIG. **43**A, and FIG. **43**C is a sectional view taken along line Y-Y' of FIG. **43**A;

[0066] FIG. **44**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **44**B is a sectional view taken along line X-X' of FIG. **44**A, and FIG. **44**C is a sectional view taken along line Y-Y' of FIG. **44**A;

[0067] FIG. **45**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **45**B is a sectional view taken along line X-X' of FIG. **45**A, and FIG. **45**C is a sectional view taken along line Y-Y' of FIG. **45**A;

[0068] FIG. **46**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **46**B is a sectional view taken along line X-X' of FIG. **46**A, and FIG. **46**C is a sectional view taken along line Y-Y' of FIG. **46**A; and

[0069] FIG. **47**A is a plan view showing a method for producing a semiconductor device according to an embodiment of the present invention, FIG. **47**B is a sectional view taken along line X-X' of FIG. **47**A, and FIG. **47**C is a sectional view taken along line Y-Y' of FIG. **47**A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0070] A production process for forming a SGT structure according to an embodiment of the present invention will now be described with reference to FIGS. **2** to **47**.

[0071] A production method is described that includes forming a first fin-shaped silicon layer and a second fin-shaped silicon layer on a substrate, forming a first insulating film around the first fin-shaped silicon layer and second fin-shaped silicon layer, forming a first pillar-shaped silicon layer in an upper portion of the first fin-shaped silicon layer, and forming a second pillar-shaped silicon layer in an upper portion of the second fin-shaped silicon layer. As shown in FIG. **2**, a second oxide film **102** is deposited on a silicon substrate **101** in order to form a dummy pattern. A nitride film or a laminated film of an oxide film and a polysilicon may be used.

[0072] As shown in FIGS. **3**A-**3**C, a first resist **103** for forming the dummy pattern is formed.

[0073] As shown in FIGS. **4**A-**4**C, the second oxide film **102** is etched to form the dummy pattern **102**.

[0074] As shown in FIGS. **5**A-**5**C, the first resist **103** is removed.

[0075] As shown in FIGS. **6**A-**6**C, a first nitride film **104** is deposited.

[0076] As shown in FIGS. **7**A-**7**C, by etching the first nitride film **104**, the first nitride film **104** is made to remain in a sidewall shape. Thus, a first nitride film sidewall **104** is formed around the dummy pattern **102**. By etching silicon using the formed first nitride film sidewall **104**, a first fin-shaped silicon layer **105** and a second fin-shaped silicon layer **106** that are connected to each other at their ends to form a closed loop will be formed.

[0077] As shown in FIGS. **8**A-**8**C, the dummy pattern **102** is removed.

[0078] As shown in FIGS. **9**A-**9**C, by etching the silicon substrate **101** using the first nitride film sidewall **104** as a mask, a first fin-shaped silicon layer **105** and a second fin-shaped silicon layer **106** that are connected to each other at their ends to form a loop are formed.

[0079] As shown in FIGS. **10**A-**10**C, a first insulating film **107** is formed around the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106**.

[0080] An oxide film formed using high-density plasma or an oxide film formed by low-pressure chemical vapor deposition may be used as the first insulating film.

[0081] As shown in FIGS. **11**A-**11**C, the first nitride film sidewall **104** is removed. In the case where the first nitride film sidewall **104** is removed during the silicon etching or the oxide film deposition, this step is skipped.

[0082] As shown in FIGS. **12**A-**12**C, the first insulating film **107** is etched back to expose an upper portion of the first fin-shaped silicon layer **105** and an upper portion of the second fin-shaped silicon layer **106**.

[0083] As shown in FIGS. **13**A-**13**C, a second resist **108** is formed so as to be perpendicular to the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106**. The portions in which the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106** are perpendicular to the resist **108** are portions to be formed into pillar-shaped silicon layers. Since the resist can be formed linearly, there is a low probability of the resist falling over after the patterning. Consequently, the process can be stably performed.

[0084] As shown in FIGS. **14**A-**14**C, the first fin-shaped silicon layer **105** and the second fin-shaped silicon layer **106** are etched. The portion in which the first fin-shaped silicon layer **105** is perpendicular to the second resist **108** becomes a first pillar-shaped silicon layer **109**. The portion in which the second fin-shaped silicon layer **106** is perpendicular to the second resist **108** becomes a second pillar-shaped silicon layer **110**. Therefore, the first pillar-shaped silicon layer **109** has a width equal to the width of the first fin-shaped silicon layer **105**. The second pillar-shaped silicon layer **110** has a width equal to the width of the second fin-shaped silicon layer **106**.

[0085] As a result, a structure is formed in which the first pillar-shaped silicon layer **109** is formed in the upper portion of the first fin-shaped silicon layer **105**, the second pillar-shaped silicon layer **110** is formed in the upper portion of the second fin-shaped silicon layer **106**, and the first insulating film **107** is formed around the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106**.

[0086] As shown in FIGS. **15**A-**15**C, the second resist **108** is removed.

[0087] Next, there is described a production method that includes, in order to achieve gate last, forming diffusion layers by implanting an impurity into an upper portion of the first pillar-shaped silicon layer **109**, an upper portion of the first fin-shaped silicon layer **105**, and a lower portion of the first pillar-shaped silicon layer **109** and forming diffusion layers by implanting an impurity into an upper portion of the second pillar-shaped silicon layer **110**, an upper portion of the second fin-shaped silicon layer **106**, and a lower portion of the second pillar-shaped silicon layer **110**.

[0088] As shown in FIGS. **16**A-**16**C, a third oxide film **111** is deposited and a second nitride film **112** is formed. Since the upper portions of the pillar-shaped silicon layers will be covered with a gate insulating film and a polysilicon gate electrode later, diffusion layers are formed in the upper portions of the pillar-shaped silicon layers before covered with the gate insulating film and polysilicon gate electrode.

[0089] As shown in FIGS. **17**A-**17**C, by etching the second nitride film **112**, the second nitride film **112** is made to remain in a sidewall shape.

[0090] As shown in FIGS. **18**A-**18**C, an impurity such as arsenic, phosphorus, or boron is implanted to form a diffusion layer **113** in the upper portion of the first pillar-shaped silicon layer **109**, diffusion layers **115** and **116** in the upper portions of the first fin-shaped silicon layer **105**, a diffusion layer **114** in the upper portion of the second pillar-shaped silicon layer **110**, and diffusion layers **115** and **116** in the upper portions of the second fin-shaped silicon layer **106**.

[0091] As shown in FIGS. **19**A-**19**C, the second nitride film **112** and the third oxide film **111** are removed.

[0092] As shown in FIGS. **20**A-**20**C, a heat treatment is performed. The diffusion layers **115** and **116** in the upper portions of the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106** are brought into contact with each other and thus a diffusion layer **117** is formed. In order to achieve gate last, the diffusion layers **113** and **117** are formed by implanting an impurity into the upper portion of the first pillar-shaped silicon layer **109**, the upper portion of the first fin-shaped silicon layer **105**, and the lower portion of the first pillar-shaped silicon layer **109**; and the diffusion layers **114** and **117** are formed by implanting an impurity into the upper portion of the second pillar-shaped silicon layer **110**, the upper portion of the second fin-shaped silicon layer **106**, and the lower portion of the second pillar-shaped silicon layer **110**.

[0093] Next, there is described a production method that includes, in order to achieve gate last, forming a first polysilicon gate electrode **119***b*, a second polysilicon gate electrode **119***a*, and a polysilicon gate line **119***c* using a polysilicon. To achieve gate last, an interlayer insulating film is deposited and then polysilicon gate electrodes and a polysilicon gate line are exposed by chemical mechanical polishing. Therefore, the upper portions of the pillar-shaped silicon layers need to be prevented from being exposed by the chemical mechanical polishing.

[0094] As shown in FIGS. **21**A-**21**C, a gate insulating film **118** is formed and a polysilicon **119** is deposited and planarized. The upper surface of the planarized polysilicon **119** is located at a higher position than the gate insulating film **118** on the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the gate insulating film **118** on the diffusion layer **114** formed in the upper portion of the second pillar-shaped silicon layer **110**. Thus, when the interlayer insulating film is deposited and then the polysilicon gate electrodes and polysilicon gate line are exposed by chemical mechanical polishing in order to achieve gate last, the upper portions of the pillar-shaped silicon layers can be prevented from being exposed by chemical mechanical polishing.

[0095] A third nitride film **120** is deposited. The third nitride film **120** is a film that, when a silicide is formed in the upper portions of the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106**, prevents the formation of the silicide in upper portions of a first polysilicon gate electrode **119***b*, a second polysilicon gate electrode **119***a*, and a polysilicon gate line **119***c*.

[0096] As shown in FIGS. **22**A-**22**C, a third resist **121** for forming a first polysilicon gate electrode **119***b*, a second polysilicon gate electrode **119***a*, and a polysilicon gate line **119***c* is formed. A portion to be the gate line is desirably perpendicular to the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106** to decrease the parasitic capacitance between the gate line and the substrate.

[0097] As shown in FIGS. **23**A-**23**C, the third nitride film **120** is etched and the polysilicon **119** is etched to form a first polysilicon gate electrode **119***b*, a second polysilicon gate electrode **119***a*, and a polysilicon gate line **119***c*.

[0098] As shown in FIGS. **24**A-**24**C, the gate insulating film **118** is etched.

[0099] As shown in FIGS. **25**A-**25**C, the third resist **121** is removed.

[0100] The production method that includes, in order to achieve gate last, forming a first polysilicon gate electrode **119***b*, a second polysilicon gate electrode **119***a*, and a polysilicon gate line **119***c* using a polysilicon has been described. The upper surface of the polysilicon after the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* are formed is located at a higher position than the gate insulating film **118** on the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the gate insulating film **118** on the diffusion layer **114** formed in the upper portion of the second pillar-shaped silicon layer **110**.

[0101] Next, there is described a production method that includes forming a silicide in the upper portion of the diffusion layer **117** formed in the upper portion of the first fin-shaped silicon layer **105** and in the upper portion of the diffusion layer **117** formed in the upper portion of the second fin-shaped silicon layer **106**.

[0102] This production method is characterized in that a silicide is not formed in upper portions of the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* and in upper portions of the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the diffusion layer **114** formed in the upper portion of the second pillar-shaped silicon layer **110**. If a silicide is formed in the upper portions of the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the diffusion layer **114**

formed in the upper portion of the second pillar-shaped silicon layer **110**, the number of production steps is increased.

[0103] As shown in FIGS. **26**A-**26**C, a fourth nitride film **122** is deposited.

[0104] As shown in FIGS. **27**A-**27**C, by etching the fourth nitride film **122**, the fourth nitride film **122** is made to remain in a sidewall shape.

[0105] As shown in FIGS. **28**A-**28**C, a metal such as nickel or cobalt is deposited to form a silicide **123** in upper portions of the diffusion layers **117** formed in the upper portions of the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106**. Herein, a silicide is not formed in upper portions of the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* because the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* are covered with the fourth nitride film **122** and the third nitride film **120**. A silicide is also not formed in upper portions of the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the diffusion layer **114** formed in the upper portion of the second pillar-shaped silicon layer **110** because the diffusion layer **113** and the diffusion layer **114** are covered with the gate insulating film **118**, the first polysilicon gate electrode **119***b*, the second polysilicon gate electrode **119***a*, and the polysilicon gate line **119***c*.

[0106] The production method that includes forming a silicide in the upper portion of the diffusion layer **117** formed in the upper portion of the first fin-shaped silicon layer **105** and forming a silicide in the upper portion of the diffusion layer **117** formed in the upper portion of the second fin-shaped silicon layer **106** has been described.

[0107] Next, there is described a production method of gate last that includes depositing an interlayer insulating film **125**, exposing the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c*, etching the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c*, depositing a metal **126**, and forming a first metal gate electrode **126***b*, a second metal gate electrode **126***a*, and a metal gate line **126***c*.

[0108] As shown in FIGS. **29**A-**29**C, a fifth nitride film **124** is deposited in order to protect the silicide **123**.

[0109] As shown in FIGS. **30**A-**30**C, an interlayer insulating film **125** is deposited and planarized by chemical mechanical polishing.

[0110] As shown in FIGS. **31**A-**31**C, the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* are exposed by chemical mechanical polishing.

[0111] As shown in FIGS. **32**A-**32**C, the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* are etched. This etching is desirably performed by wet etching.

[0112] As shown in FIGS. **33**A-**33**C, a metal **126** is deposited and planarized to fill, with the metal **126**, the portions in which the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c* have been present. Atomic layer deposition is preferably used.

[0113] As shown in FIGS. **34**A-**34**C, the metal **126** is etched to expose the gate insulating film **118** on the diffusion layer **113** in the upper portion of the first pillar-shaped silicon layer **109** and the gate insulating film **118** on the diffusion layer **114** in the upper portion of the second pillar-shaped silicon layer **110**. As a result, a first metal gate electrode **126***b*, a second metal gate electrode **126***a*, and a metal gate line **126***c* are formed.

[0114] The production method of gate last that includes depositing the interlayer insulating film **125**, exposing the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c*, etching the first polysilicon gate electrode **119***b*, second polysilicon gate electrode **119***a*, and polysilicon gate line **119***c*, depositing the metal **126**, and forming the first metal gate electrode **126***b*, the second metal gate electrode **126***a*, and the metal gate line **126***c* has been described.

[0115] Next, there is described a production method for forming contacts. Since the silicide is not formed in the upper portions of the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the diffusion layer **114** formed in the upper portion of the second pillar-shaped silicon layer **110**, a contact is directly connected to the diffusion layer **113** in the upper portion of the first pillar-shaped silicon layer **109** and another contact is directly connected to the diffusion layer **114** in the upper portion of the second pillar-shaped silicon layer **110**.

[0116] As shown in FIGS. **35**A-**35**C, an interlayer insulating film **127** is deposited and planarized.

[0117] As shown in FIGS. **36**A-**36**C, a fourth resist **128** for making a contact hole above the first pillar-shaped silicon layer **109** and second pillar-shaped silicon layer **110** is formed.

[0118] As shown in FIGS. **37**A-**37**C, a contact hole **129** is made by etching the interlayer insulating film **127**.

[0119] As shown in FIGS. **38**A-**38**C, the fourth resist **128** is removed.

[0120] As shown in FIGS. **39**A-**39**C, a fifth resist **130** for making contact holes above the metal gate line **126***c* and above the first fin-shaped silicon layer **105** and second fin-shaped silicon layer **106** is formed.

[0121] As shown in FIGS. **40**A-**40**C, contact holes **131** and **132** are made by etching the interlayer insulating films **127** and **125**, respectively.

[0122] As shown in FIGS. **41**A-**41**C, the fifth resist **130** is removed.

[0123] As shown in FIGS. **42**A-**42**C, the fifth nitride film **124** and the gate insulating film **118** are etched to expose the silicide **123** and the diffusion layers **113** and **114**, respectively.

[0124] As shown in FIG. **43**, a metal is deposited to form contacts **133**, **134**, and **135**. The production method for forming contacts has been described. Since the silicide is not formed in the upper portions of the diffusion layer **113** formed in the upper portion of the first pillar-shaped silicon layer **109** and the diffusion layer **114** in the upper portion of the second pillar-shaped silicon layer **110**, the contact **134** is directly connected to the diffusion layer **113** in the upper portion of the first pillar-shaped silicon layer **109** and the other contact **134** is directly connected to the diffusion layer **114** in the upper portion of the second pillar-shaped silicon layer **110**.

[0125] Next, there is described a production method for forming metal wire layers.

[0126] As shown in FIGS. **44**A-**44**C, a metal **136** is deposited.

[0127] As shown in FIGS. **45**A-**45**C, sixth resists **137**, **138**, and **139** for forming metal wires are formed.

[0128] As shown in FIGS. **46**A-**46**C, the metal **136** is etched to form metal wires **140**, **141**, and **142**.

[0129] As shown in FIGS. **47**A-**47**C, the sixth resists **137**, **138**, and **139** are removed.

[0130] The production method for forming metal wire layers has been described.

[0131] FIG. **1** shows a SGT structure formed by the above-described production method.

[0132] The SGT structure includes a first fin-shaped semiconductor layer **105** formed on a substrate **101** and a second fin-shaped semiconductor layer **106** formed on the substrate **101**, the first fin-shaped semiconductor layer **105** and the second fin-shaped semiconductor layer **106** being connected to each other at their ends to form a closed loop; a first insulating film **107** formed around the first fin-shaped semiconductor layer **105** and second fin-shaped semiconductor layer **106**; a first pillar-shaped semiconductor layer **109** formed in an upper portion of the fin-shaped semiconductor layer **105** and a second pillar-shaped semiconductor layer **110** formed in an upper portion of the second fin-shaped semiconductor layer **106**, the first pillar-shaped semiconductor layer **109** having a width equal to the width of the first fin-shaped semiconductor layer **105** and the second pillar-shaped semiconductor layer **110** having a width equal to the width of the second fin-shaped semiconductor layer **106**; a diffusion layer **117** formed in an upper portion of the first fin-shaped semiconductor layer **105** and a lower portion of the first pillar-shaped semiconductor layer **109**, a diffusion layer **113** formed in an upper portion of the first pillar-shaped semiconductor layer **109**, a diffusion layer **117** formed in an upper portion of the second fin-shaped semiconductor layer **106** and a lower portion of the second pillar-shaped semiconductor layer **110**, and a diffusion layer **114** formed in an upper portion of the second pillar-shaped semiconductor layer **110**; a silicide **123** formed in upper portions of the diffusion layers **117** formed in the upper portion of the first fin-shaped semiconductor layer **105** and in the upper portion of the second fin-shaped semiconductor layer **106**; a gate insulating film **118** formed around the first pillar-shaped semiconductor layer **109**, a first metal gate electrode **126***b* formed around the gate insulating film **118**, a gate insulating film **118** formed around the second pillar-shaped semiconductor layer **110**, a second metal gate electrode **126***a* formed around the gate insulating film **118**, and a metal gate line **126***c* that is connected to the first metal gate electrode **126***b* and the second metal gate electrode **126***a* and that extends in a direction perpendicular to the direction in which the first fin-shaped semiconductor layer **105** and second fin-shaped semiconductor layer **106** extend; and a contact **134** formed on the diffusion layer **113** formed in the upper portion of the first pillar-shaped semiconductor layer **109** so as to be directly connected to the diffusion layer **113** and a contact **134** formed on the diffusion layer **114** formed in the upper portion of the second pillar-shaped semiconductor layer **110** so as to be directly connected to the diffusion layer **114**.

[0133] Accordingly, there are provided a SGT production method in which the parasitic capacitance between a gate line and a substrate is decreased, a gate last process is employed, and two transistors are produced from a single dummy pattern and a SGT structure formed by the production method.

1. A semiconductor device comprising:

a first fin-shaped semiconductor layer on a substrate;

a second fin-shaped semiconductor layer on the substrate;

a first insulating film around the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer;

a first pillar-shaped semiconductor layer on the first fin-shaped semiconductor layer, wherein a width of the bottom of the first pillar-shaped semiconductor is equal to a width of the top of the first fin-shaped semiconductor layer;

a second pillar-shaped semiconductor layer on the second fin-shaped semiconductor layer, wherein a width of the bottom of the second pillar-shaped semiconductor is equal to a width of the top of the second fin-shaped semiconductor layer;

a first diffusion layer in an upper portion of the first fin-shaped semiconductor layer and a lower portion of the first pillar-shaped semiconductor layer;

a second diffusion layer in an upper portion of the first pillar-shaped semiconductor layer;

a third diffusion layer in an upper portion of the second fin-shaped semiconductor layer and a lower portion of the second pillar-shaped semiconductor layer;

a fourth diffusion layer in an upper portion of the second pillar-shaped semiconductor layer;

a first gate insulating film around the first pillar-shaped semiconductor layer;

a first metal gate electrode around the first gate insulating film;

a second gate insulating film around the second pillar-shaped semiconductor layer;

a second metal gate electrode around the second gate insulating film;

a metal gate line connected to the first metal gate electrode and the second metal gate electrode and extending in a direction perpendicular to a direction in which the first fin-shaped semiconductor layer and second fin-shaped semiconductor layer extend;

a contact on the upper portion of the second diffusion layer and directly connected to the second diffusion layer; and

a contact on the upper portion of the fourth diffusion layer and directly connected to the fourth diffusion layer.

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