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(54) Title: SELF-ALIGNED BORDERLESS CONTACTS FOR HIGH DENSITY ELECTRONIC AND MEMORY DEVICE INTEGRATION

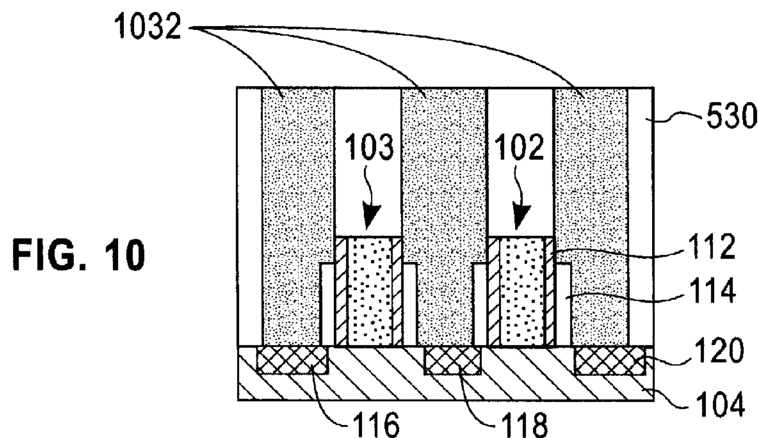

FIG. 10

(57) Abstract: A method for fabricating a transistor having self-aligned borderless electrical contacts is disclosed. A gate stack (102, 103) is formed on a silicon region (104). An off-set spacer (112, 114) is formed surrounding the gate stack. A sacrificial layer (222) that includes a carbon-based film is deposited overlying the silicon region, the gate stack, and the off-set spacer. A pattern (326) is defined in the sacrificial layer to define a contact area for the electrical contact. The pattern exposes at least a portion of the gate stack and source/drain. A dielectric layer (530) is deposited overlying the sacrificial layer that has been patterned and the portion of the gate stack that has been exposed. The sacrificial layer that has been patterned is selectively removed to define the contact area at the height that has been defined. The contact area for the height that has been defined is metalized to form the electrical contact.

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SELF-ALIGNED BORDERLESS CONTACTS FOR HIGH DENSITY ELECTRONIC AND MEMORY DEVICE INTEGRATION

Field of the Invention

The present invention generally relates to the field of semiconductors, and more particularly relates to high density electronic and memory device integration on semiconductor substrates.

Background of the Invention

The formation of electrical contacts to electronic and memory devices is a considerable challenge as the integration density of these devices is increased as a consequence of technology scaling. For example, the projected contact pitch for the 32nm, 22nm, and 15nm nodes are 130nm, 100nm, and 80nm respectively. Alignment of the contact to the source, drain, and gate of the device is critical. In particular, misalignment of the source and drain contacts with respect to the gate can cause electrical shorts, rendering the device inoperable.

Therefore a need exists to overcome the problems with the prior art as discussed above.

Summary of the Invention

The present invention accordingly provides, in a first aspect, a method for fabricating a transistor having self-aligned borderless electrical contacts, the method comprising the steps of: forming a gate stack on a silicon region; forming an off-set spacer surrounding the gate stack; depositing a sacrificial layer comprised of a carbon-based film overlying the silicon region, the gate stack, and the off-set spacer, wherein a thickness of the sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a source/drain of a transistor; defining a pattern in the sacrificial layer to define a contact area for the electrical contact, wherein defining the pattern exposes at least a portion of the gate stack and source/drain; depositing a dielectric layer overlying the sacrificial layer that has been patterned and the portion of the gate stack that has been exposed; selectively removing

the sacrificial layer that has been patterned to define the contact area at the height that has been defined; and metalizing the contact area for the height that has been defined to form the electrical contact.

5 Preferably, the sacrificial material extends over a portion of the off-set spacer. Preferably, defining a pattern in the sacrificial layer to define a contact area for the electrical contact further comprises: depositing a masking material over the sacrificial layer; lithographically patterning the masking material; and etching away a portion of the sacrificial layer that has not been patterned. The method may further comprise trimming the masking material that
10 has been patterned. The method may further comprise forming the silicided region on the silicon region, and wherein the contact area is metalized for the height that has been defined above the silicided region to form the electrical contact that contacts the silicided region.

Preferably, the sacrificial layer that has been patterned is wider than the silicided region.

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Preferably, the forming of the gate stack comprises forming a gate oxide layer on the silicon region and a gate electrode layer on the gate oxide layer. The method may further comprise: planarizing the dielectric layer to expose the sacrificial layer that has been patterned. The method may further comprise: trimming sacrificial layer that has been patterned. The
20 method may further comprise: depositing a liner over the silicon region, the sacrificial layer that has been patterned and the portion of the gate stack that has been exposed.

Preferably, depositing a dielectric further comprises: depositing dielectric layer over the liner.

25

Preferably, selectively removing the sacrificial layer further comprises: planarizing the dielectric layer; and etching the liner to expose the sacrificial layer that has been patterned.

In a second aspect, there is provided a transistor comprising: a silicon region; a gate stack on
30 the silicon region, the gate stack including a gate oxide layer on the silicon region and a gate electrode on the gate oxide layer, and an off-set spacer surrounding the gate stack; and a patterned sacrificial layer adjacent to the gate stack that defines a contact area for an

electrical contact, wherein a thickness of the patterned sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a collector/emitter of a transistor.

5 Preferably, the gate stack also includes a silicon nitride hard mask layer over the gate electrode layer. The transistor may further comprise a dielectric layer overlying a top portion of the gate stack. The transistor may further comprise a metalized contact in an area corresponding to the patterned sacrificial layer that has been subsequently removed, wherein the metalized contact is adjacent to the gate stack and the off-set spacer.

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In a third aspect, there is provided a integrated circuit comprising: a circuit supporting substrate including a transistor, wherein transistor includes: a silicon region a gate stack on the silicon region, the gate stack including a gate oxide layer on the silicon region and a gate electrode on the gate oxide layer, and an off-set spacer surrounding the gate stack; and a 15 patterned sacrificial layer adjacent to the gate stack that defines a contact area for an electrical contact, wherein a thickness of the sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a collector/emitter of a transistor.

Preferably, the gate stack also includes a silicon nitride hard mask layer over the gate 20 electrode layer. Preferably, the transistor further comprises: a dielectric layer overlying a top portion of the gate stack. Preferably, the transistor further comprises: a metalized contact in an area corresponding to the sacrificial layer that has been pattern and subsequently removed, wherein the metalized contact is adjacent to the gate stack and the off-set spacer.

25 In one embodiment, a method for fabricating a transistor having self-aligned borderless electrical contacts is disclosed. The method includes forming a gate stack on a silicon region. The gate stack includes a gate oxide layer on the silicon region and a gate electrode layer on the gate oxide layer. An off-set spacer is formed surrounding the gate stack. Ion implantation is performed as necessary to dope the device. An activation anneal is 30 performed to activate the dopant and recrystallize the Si in the source/drain regions of the devices. A silicide is formed on the source/drain regions and a portion of the gate stack of the device by depositing a metal layer, reacting the metal with the Si by a rapid thermal

annealing process, and then removing the unreacted metal through a selective chemical etch. A sacrificial layer is deposited comprised of a carbon-based film overlying the silicon region, the gate stack, and the off-set spacer. A thickness of the sacrificial layer defines a height of an electrical contact above and extending to the silicided region of the source/drain and the gate stack of the transistor. A pattern is defined in the sacrificial layer to define a contact area for the electrical contacts to the device. Defining the pattern exposes at least a portion of the gate stack and the source/drain (i.e. the regions outside of the patterned areas). A dielectric layer is deposited overlying the sacrificial layer that has been patterned and the portion of the gate stack and source/drain that has been exposed. The sacrificial layer that has been patterned is selectively removed exposing the contact areas. The contact areas are metalized forming electrical contacts to the source, drain and gate of the device.

In another embodiment, a transistor is disclosed. The transistor includes a gate stack. This gate stack is formed on a silicon region and includes a gate oxide layer on the silicon region and a gate electrode on the gate oxide layer. An off-set spacer surrounds the gate stack. A patterned sacrificial layer is adjacent to the gate stack that defines a contact area for an electrical contact. A thickness of the sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a source/drain of a transistor.

In yet another embodiment, an integrated circuit is disclosed. The integrated circuit includes a circuit supporting substrate. The circuit supporting substrate comprises a transistor. The transistor includes a gate stack. The gate stack is formed on the silicon region and includes a gate oxide layer on the silicon region and a gate electrode on the gate oxide layer. An off-set spacer surrounds the gate stack. A patterned sacrificial layer is adjacent to the gate stack that defines a contact area for an electrical contact. A thickness of the sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a source/drain of a transistor.

One advantage of the various embodiments of the present invention is that borderless contacts are created that meet the demands of electronic and memory device scaling. Conventional lithographic techniques can be used to define a masking material that defines a pattern in a sacrificial material. The patterned sacrificial material ultimately defines the

electrical contact to the device. The sacrificial material is chosen such that it can be patterned with high selectivity to the electronic device allowing aspects of the device geometry to self-align the bottom of the contact, forming a borderless contact.

5 Brief Description of the Drawings

A preferred embodiment of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

10 FIGs. 1-10 are cross-sectional views of various layers of a circuit supporting substrate illustrating a process for forming self-aligned borderless contacts for high integration density electronic and memory device according to one embodiment of the present invention.

FIG. 11 is a cross-sectional view of a circuit supporting substrate illustrating a process for
15 trimming a sacrificial layer deposited for forming self-aligned borderless contacts according to one embodiment of the present invention;

FIG. 12 is a cross-sectional view of a circuit supporting substrate illustrating a process for trimming a masking material according to an embodiment of the present invention; and

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FIGs. 13-17 are cross-sectional views of a circuit supporting substrate illustrating a process for depositing a liner during the formation of self-aligned borderless contacts according to one embodiment of the present invention.

25 DETAILED DESCRIPTION

FIGs. 1 to 17 illustrate one or more processes for forming a transistor device with self-aligned borderless contacts according to one embodiment of the present invention. In these figures although only two transistors are shown arranged in a side-by-side manner, an
30 infinite array of transistor can exist. In other words, the environment of FIGs. 1-17 is a high density environment. Also, it should be noted that although a planar transistor device 100 is

shown in FIG. 1, the various embodiments of the present invention are also applicable non-planar transistor or memory devices as well.

It should be noted that the overall fabrication scheme discussed below may be standard until after the formation of silicide regions. For example, as in a normal process flow the various silicide areas are formed within a silicon region. At this step, in accordance with the various embodiments of the present invention, self-aligned borderless contacts are then created.

The transistor device 100 of FIG. 1 comprises one or more gate stacks 102, 103 formed using any conventional gate patterning process. The gate stack 102 is formed over a region 104. In one embodiment, the region 104 is a silicon region 104 comprising at least a portion of a silicon layer and/or a silicon substrate. Such a region 104 can, in one embodiment, comprise a surface area of the silicon layer and/or silicon substrate. It should be noted that the region 104 comprises the entire layer or substrate or a portion (less than the whole) of the layer/substrate.

A Silicone dioxide layer, in one embodiment, may be present beneath the Si region (not shown). In this embodiment, a silicon substrate is present under the oxide layer (not shown). The gate stack 102, in one embodiment, includes a gate oxide 106 and a gate electrode 108. The gate oxide 106 can be (but not limited to) SiO2, SiOxNy, or a metal oxide such as (but not limited to) HfO2, HfSiOx, HfSiOxNy Ta2O5, TiO2, Al203, Y2O3 and La2O5. In some embodiments, the metal oxide creates a high-k layer. The material comprising the gate electrode 108 is determined by the choice of the gate oxide 106. For example, in the case of Si-based oxides, polysilicon can be used. In the case of metal oxides, a metal can be used such as (but not limited to) TiN, Ta, TaN, TaCN, TaSiN, TaSi, AlN, W and Mo. The gate oxide 106 and gate electrode 108 can be deposited using any conventional deposition process such as metal-organic chemical vapor deposition ("MOCVD") or atomic-layer deposition ("ALD") and physical vapor deposition ("PVD"), MOCVD, or ALD, respectively.

The gate stack 102 can also include an optional deposition of an amorphous Si or a poly Si layer 110 which is deposited using conventional processes such as LPCVD, RT CVD or

silicon sputtering. FIG. 1 also shows that one ore more offset spacers 112, 114 have been deposited and etched. In particular, FIG. 1 shows an oxide spacer 112 has been deposited around the gate stack 102 ad that another spacer such as a nitride spacer 114 has been deposited and formed around the oxide spacer 112. These spacers 112, 114 can be
5 deposited, for example, by PECVD, LPCVD, ALD or RTCVD. It should be noted that the transistor device 100 can include both spacers 112, 114; only the oxide spacer 112; or only the nitride spacer 114. FIG. 1 also shows that silicide regions 116, 118, 120 (typically with Ni or Co) have been formed within the Si region 104 and on the gate stack 103 and 102. For example, silicide areas 116, 118, 120 are formed for contacts using the spacer structure 112,
10 114. This is achieved by removing any native oxide present on the Si layer 104 or Si gate material 102, 103 (e.g., through a wet etch using HF), depositing a metal, performing an anneal to form silicide, and then selectively removing the metal but leaving the silicide untouched (e.g., through an aqua regia wet etch). The silicided regions 116, 118, 120 can be formed from (but are not limited to) metals such as nickel, cobalt, titanium, or platinum.

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After the transistor device 100 has been formed as shown in FIG. 1, a sacrificial material is deposited onto the transistor device 100, thereby forming a sacrificial layer 222, as shown in FIG. 2. It should be noted that from hereon in "sacrificial material" and "sacrificial layer" are referred as one in the same. The sacrificial material 222, in one embodiment, is a
20 carbon-based film that has the following properties: the material can be deposited or coated onto the substrate in a manner that covers the substrate topography such as (but not limited to) spin casting, plasma deposition, physical vapor deposition, chemical vapor deposition; the material can be patterned using a directional dry etch plasma chemistry that does not damage the materials present on the substrate (e.g. O2, N2, H2 or CO2 plasma); the material
25 can survive temperatures compatible with microelectronic middle of the line ("MOL") processing (e.g., 25 to 450 °C); and the material is a dielectric. Examples of a suitable sacrificial material 222 include ODL, NFC, ACL, plasma deposited amorphous carbon, or sputtered carbon. It should be noted that the present invention is not limited to using only these materials.

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In one embodiment, the thickness of the sacrificial material 222 is chosen to define the height of the contact to be formed above and extending to a silicided region 116, 118, 120

defining a source/drain of a transistor. A lithographic process is then used to define a masking material 224 for defining a pattern in the sacrificial material 222. For example, lithography techniques such as (but not limited to) electron beam lithography and optical lithography using single exposure, double exposure and double exposure/double etch techniques can be used to define the masking material. The masking material 224 can be any material that can be deposited onto the sacrificial material 222 and patterned selectively to the sacrificial material 222.

FIG. 2 shows the patterned mask material 224. The masking material 224 can include (but is not limited to) silicon oxide, silicon nitride, or antireflective coatings. Also, the masking material 224 can be a resist so long as it can be used as a mask for defining patterns in the sacrificial material 222. An example of such a material includes (but is not limited to) hydrogen silsesquioxanes, which is a silicon-oxide like electron beam lithography resist. Following lithographic definition of the masking material 224 and subsequent patterning steps, the sacrificial material 222 is patterned using pattern transfer techniques that do not compromise or degrade the operation of the electronic or memory device 100. FIG. 3 and FIG. 4, which is a three-dimensional view of FIG. 3, show this dry pattern transfer of the masking pattern 224 into the sacrificial layer 222.

As can be seen from FIG. 3 and FIG. 4, columns 326 of the sacrificial layer 222 are created under each of the pattern mask material sections 224. In other words, the pattern transfer techniques etched away all but the sacrificial material 222 under the patterning material 224 creating columns 326 of sacrificial material with canyons 328 there between. The sacrificial material 222 has been removed from the spacer 112, 114 without damaging the spacer 112, 114 in any way and stopped on the silicided regions 116, 118, 120 without damaging the silicide 116, 118. 120. Silimilarly, contacts to the gate electrode can be made though are not shown in these drawings. Also, as shown in FIG. 3 and FIG. 4, the width of the sacrificial material 222 after patterning expands over the spacer 112, 114. This is advantageous because the contacts can be defined larger than the region (e.g., the silicide regions) that is to be contacted. Furthermore, the contacts need not be perfectly aligned to the silicide regions. This enables the contact patterning to be performed with looser process tolerances. Therefore, in one embodiment, the patterning material 224 is defined with a larger

dimension than the silicide 116 to which the contact is to terminate on. These cylinders/columns 326 of sacrificial material 222 define where the contacts are going to be. The type of sacrificial material 222 that has been used and the patterning techniques that have been selected do not affect the regions where the contacts will ultimately land on the
5 device 100. In the embodiments of FIGs. 3-17 the contacts are to terminate on the silicide regions 116.

The self-aligned and borderless aspects of the various embodiments are illustrated by the fact that selectivity of the etch (e.g., the patterning techniques discussed above) that defines the
10 sacrificial material 222, as shown in FIG. 3 and FIG. 4, completely defines where the contacts will land on the device 100. Stated differently, when the patterning technique/etch is performed, the sacrificial material 222 defines the contact area because of the selectivity of the materials within the transistor device 100 once the sacrificial material 222 is etched between the two gates 102, 103. This is a self-aligning feature of the various embodiments
15 because the bottom of the contact is itself aligned and is borderless because the contact is being defined by the geometry of the device 100. The general region of the contact is lithographically defined and the footprint of the contact is self-aligned.

Once the sacrificial material 222 has been patterned/etched as shown in FIG. 3 and FIG. 4, a
20 suitable dielectric 530 such as (but not limited to) plasma deposited or spin on $SiO2$ is deposited onto the substrate, as shown in FIG. 5. This dielectric 530 encapsulates the devices and the sacrificial material 222. It is important that this dielectric 530, in one embodiment, completely fill the features of the substrate without forming voids or "keyholes". This dielectric is typically referred to as the MOL dielectric 430. The MOL
25 dielectric 530 is then polished back to reveal the sacrificial material 222 using chemical mechanical polishing, as shown in FIG. 6 and FIG. 7. The sacrificial material 222 can be used as a "polish stop" to help define the thickness of the planarized MOL dielectric 430. As can be seen in FIG. 6 and FIG. 7 the polishing process stops once it reaches the sacrificial material 222.

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The sacrificial material 222 is then removed using either wet or dry isotropic removal techniques as shown in FIG. 8 and FIG. 9. This process is chosen such that it is selective to

the MOL dielectric 530 and the materials present in the device 100. This enables the formation of a self-aligned borderless contact. Once the sacrificial material 222 has been removed, a metalized contact 1032 can formed using conventional CVD, PVD, ALD or plating-based techniques or some combination of these techniques, as shown in FIG. 10.

As can be seen from the above discussion the various embodiments of the present invention are advantageous because contacts are self aligned to the source and drain. The self-aligned contact(s) is a borderless contact that is defined using a carbon-based film sacrificial layer. The borderless contact can be defined with relaxed dimensional and alignment specifications. The bottom of the contact, where these parameters are critical is defined by aspects of the device geometry. This is done in such a way as to avoid compromising the functionality of the device or degrading its performance.

FIGs. 11-17 show additional embodiments for forming a transistor device with self-aligned borderless contacts. For example, FIG. 11 shows that after the sacrificial material 222 patterning/etching process of FIG. 3 and FIG. 4, the sacrificial material 222 can be trimmed. In one embodiment, the trimming process is performed using a suitable etching technique such as an isotropic etch process to form sub-lithographic features. In another embodiment, as shown in FIG. 12, the masking material 224 can be trimmed using a suitable etching technique to produce contacts at sub-lithographic dimensions. When the sacrificial material 222 is removed using either wet or dry isotropic removal techniques, as shown in FIGs. 8 and 9, the width of the canyons 228 created are smaller than if the material 222 had not been trimmed. Trimming is advantageous because the sacrificial material 222 can be dimensioned after a lithographic process and not use the lithographic process for dimensioning, reducing the tolerances of the lithographic process.

FIGs. 13-17 illustrate another embodiment implementing a liner 1334. In particular, the liner material 1334 can be coated onto the substrate following pattern transfer into the sacrificial material, as shown in FIGs. 13-14. The liner material 1334 is deposited over the Si layer 104 and encapsulates the masking material 24,the sacrificial material 222, the spacer 112, 114, and the gate stack 102.

This liner 1334 may be used to improve the electrical performance of the device 100, and in one embodiment, is a stressed nitride liner. The liner 1334 may be used to improve the reliability of the contact metallization 1032. Also, the liner 1334 may improve integration of subsequent wiring levels by providing an etch stop on top of the gate 102 to prevent gate to
5 wring shorts. In one more embodiment, the process can be integrated with a dual damascene wire level patterning to enable metallization of the contact and wiring level simultaneously.

Once the liner 1334 is deposited, the MOL dielectric 530 is deposited onto the substrate similar to FIG. 5. However, in the embodiment of FIG. 15, the MOL dielectric 530 is also
10 deposited over liner 1334. The polishing process of FIGs. 6 and 7 is then performed and stops once it reaches the liner 1334, as shown in FIG. 16. A liner etch back process can then be performed as shown in FIG. 16, thereby exposing the sacrificial material 222. The sacrificial material 222 is then removed, as shown in FIG. 17, using either wet or dry isotropic removal techniques similar to the process shown in FIGs. 8 and 9. Once the
15 sacrificial material 222 the metalized contact 1032 can be formed as discussed above with respect to FIG. 10.

It should be noted that some of the features of the examples of this invention may be used to advantage without the corresponding use of other features. As such, the foregoing
20 description should be considered as merely illustrative of the principles, teachings, examples and exemplary embodiments of this invention, and not in limitation thereof.

It should be understood that these embodiments are only examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the
25 specification of the present application do not necessarily limit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others. In general, unless otherwise indicated, singular elements may be in the plural and vice versa with no loss of generality.

30 The circuit as described above is part of the design for an integrated circuit chip. The chip design is created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a

storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer transmits the resulting design by physical means (e.g., by providing a copy of the storage medium storing the design) or electronically (e.g., through the Internet) to such entities, directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which typically include multiple copies of the chip design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

The method as described above is used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare chip, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard, or other input device, and a central processor.

Although specific embodiments of the invention have been disclosed, those having ordinary skill in the art will understand that changes can be made to the specific embodiments without departing from the scope of the invention.

CLAIMS

1. A method for fabricating a transistor having self-aligned borderless electrical contacts, the method comprising the steps of:

5 forming a gate stack on a silicon region;

forming an off-set spacer surrounding the gate stack;

depositing a sacrificial layer comprised of a carbon-based film overlying the silicon region, the gate stack, and the off-set spacer, wherein a thickness of the sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a

10 source/drain of a transistor;

defining a pattern in the sacrificial layer to define a contact area for the electrical contact, wherein defining the pattern exposes at least a portion of the gate stack and source/drain;

depositing a dielectric layer overlying the sacrificial layer that has been patterned and

15 the portion of the gate stack that has been exposed;

selectively removing the sacrificial layer that has been patterned to define the contact area at the height that has been defined; and

metalizing the contact area for the height that has been defined to form the electrical contact.

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2. The method of claim 1, wherein the sacrificial material extends over a portion of the off-set spacer.

3. The method of claim 1, wherein defining a pattern in the sacrificial layer to define a

25 contact area for the electrical contact further comprises:

depositing a masking material over the sacrificial layer;

lithographically patterning the masking material; and

etching away a portion of the sacrificial layer that has not been patterned.

30 4. The method of claim 3, further comprising:

trimming the masking material that has been patterned.

5. The method of claim 1, further comprising:

forming the silicided region on the silicon region, and wherein the contact area is metalized for the height that has been defined above the silicided region to form the electrical contact that contacts the silicided region.

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6. The method of claim 1, wherein the sacrificial layer that has been patterned is wider than the silicided region.

7. The method of claim 1, wherein the forming of the gate stack comprises forming a

10 gate oxide layer on the silicon region and a gate electrode layer on the gate oxide layer.

8. The method of claim 1, further comprising:

planarizing the dielectric layer to expose the sacrificial layer that has been patterned.

15 9. The method of claim 1, further comprising:

trimming sacrificial layer that has been patterned.

10. The method of claim 1, further comprising:

depositing a liner over the silicon region, the sacrificial layer that has been patterned

20 and the portion of the gate stack that has been exposed.

11. The method of claim 10, wherein depositing a dielectric further comprises:

depositing dielectric layer over the liner.

25 12. The method of claim 11, wherein selectively removing the sacrificial layer further comprises:

planarizing the dielectric layer; and

etching the liner to expose the sacrificial layer that has been patterned.

30 13. A transistor comprising:

a silicon region;

a gate stack on the silicon region, the gate stack including a gate oxide layer on the silicon region and a gate electrode on the gate oxide layer, and

an off-set spacer surrounding the gate stack; and

a patterned sacrificial layer adjacent to the gate stack that defines a contact area for
5 an electrical contact, wherein a thickness of the patterned sacrificial layer defines a height of an electrical contact above and extending to a silicided region defining a collector/emitter of a transistor.

14. The transistor of claim 13, wherein the gate stack also includes a silicon nitride hard
10 mask layer over the gate electrode layer.

15. The transistor of claim 13, further comprising:

a dielectric layer overlying a top portion of the gate stack; and

a metalized contact in an area corresponding to the patterned sacrificial layer that has
15 been subsequently removed, wherein the metalized contact is adjacent to the gate stack and the off-set spacer.

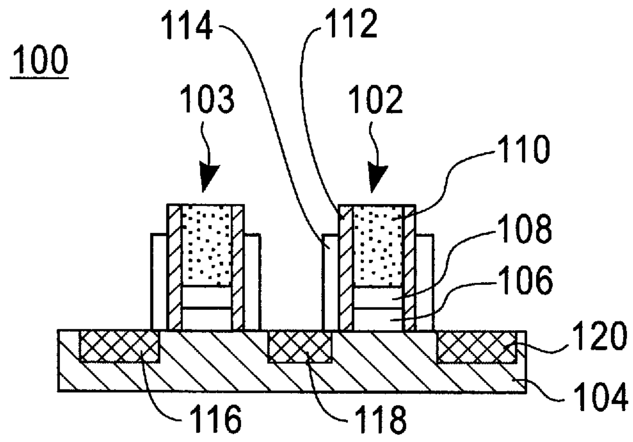


FIG. 1

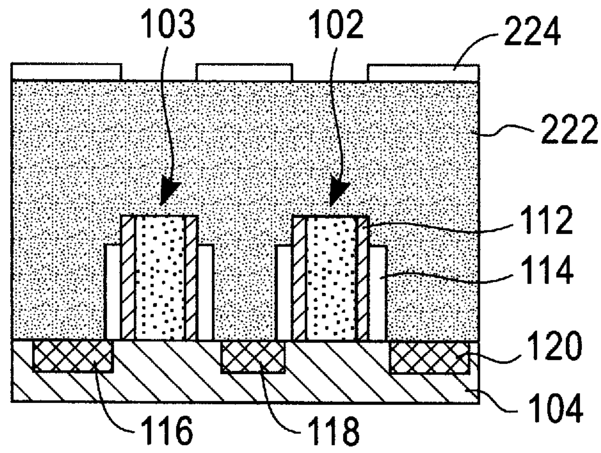


FIG. 2

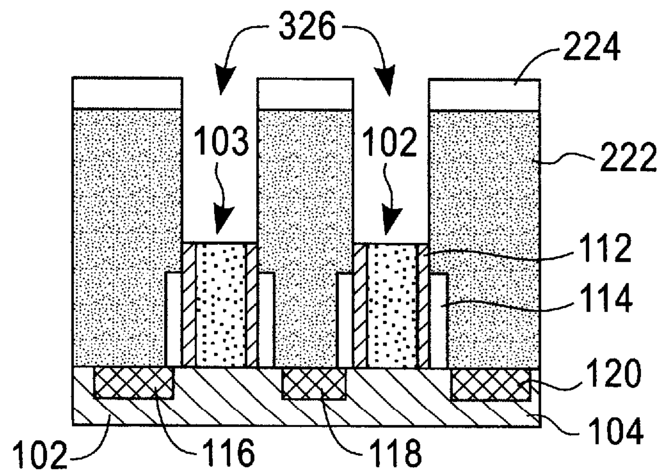


FIG. 3

FIG. 4

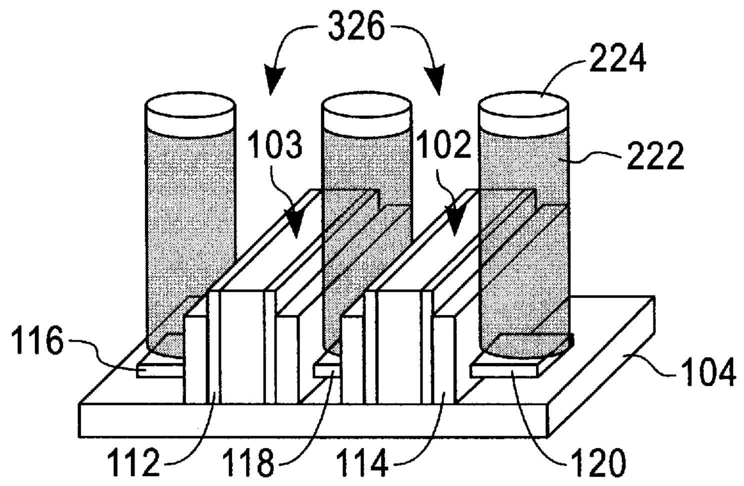


FIG. 5

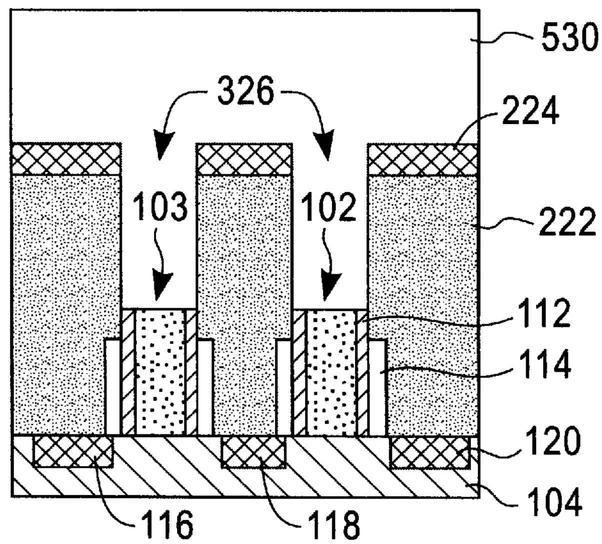
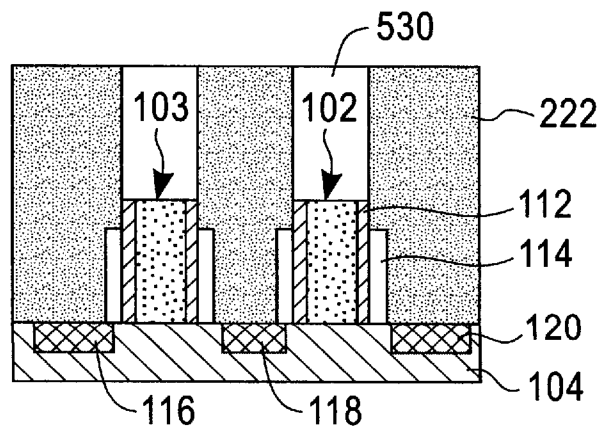
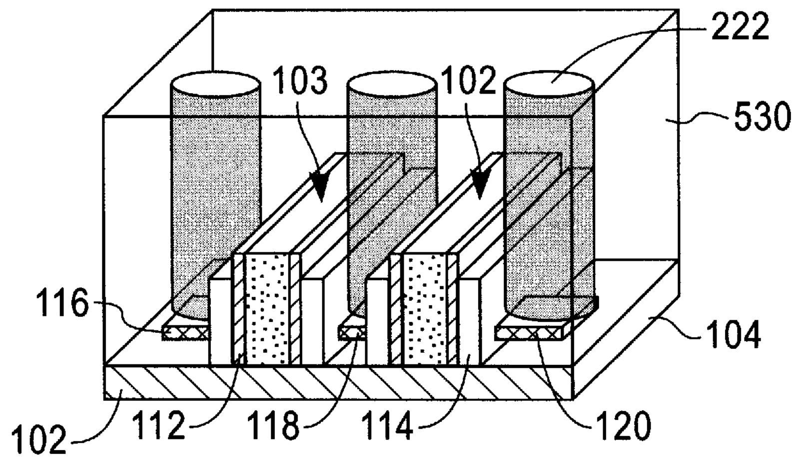
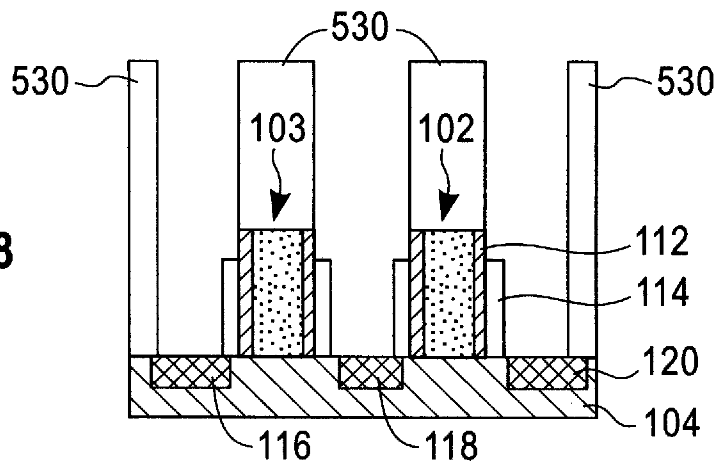


FIG. 6




222
103
102
530
FIG. 7
116
104
102
112
118
114
120


530
530
530
103
102
FIG. 8
112
114
120
104
116
118

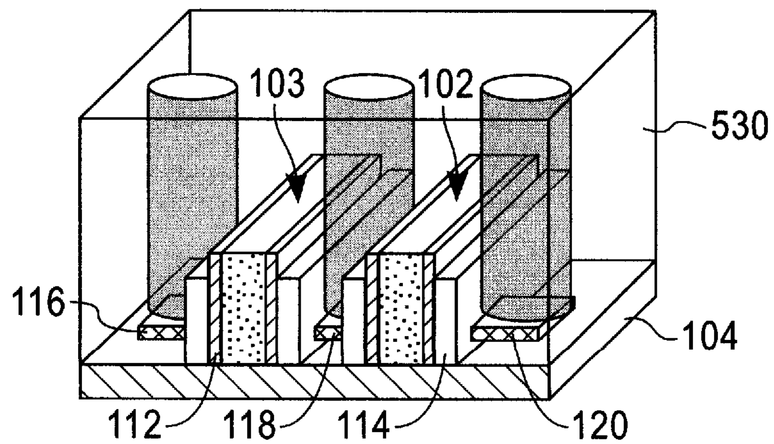

103
102
530
FIG. 9
116
104
112
118
114
120

FIG. 10

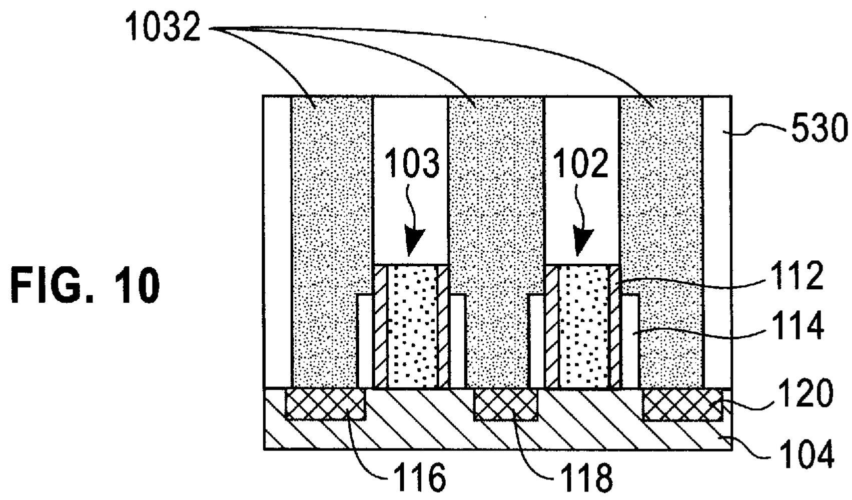


FIG. 11

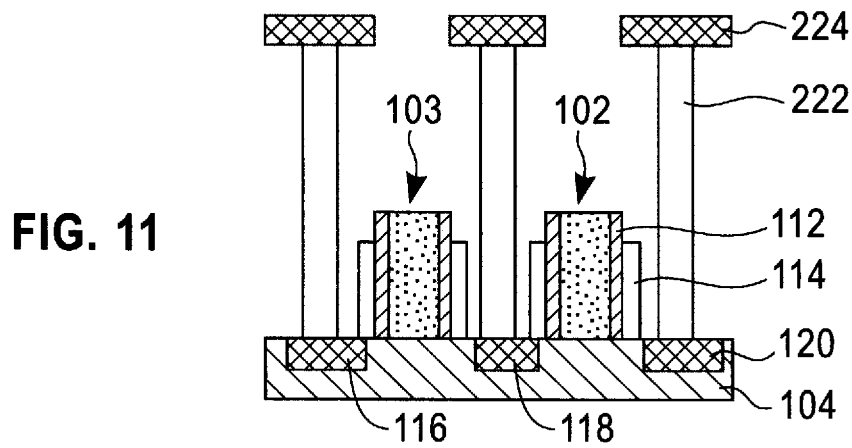


FIG. 12

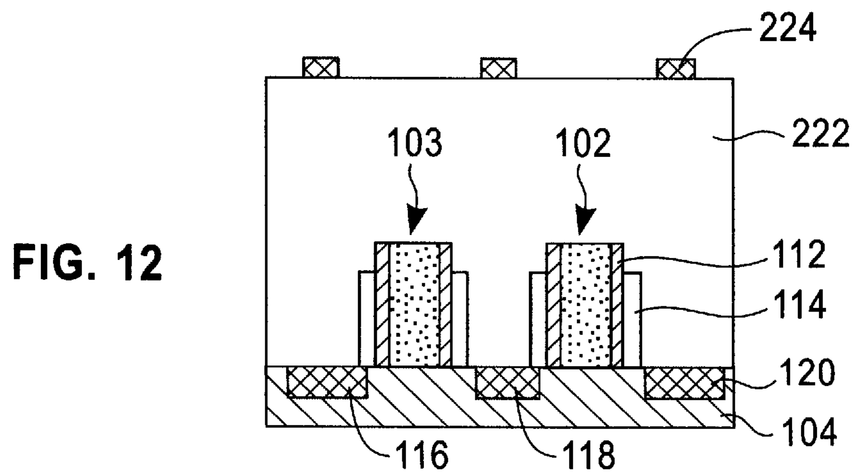


FIG. 13

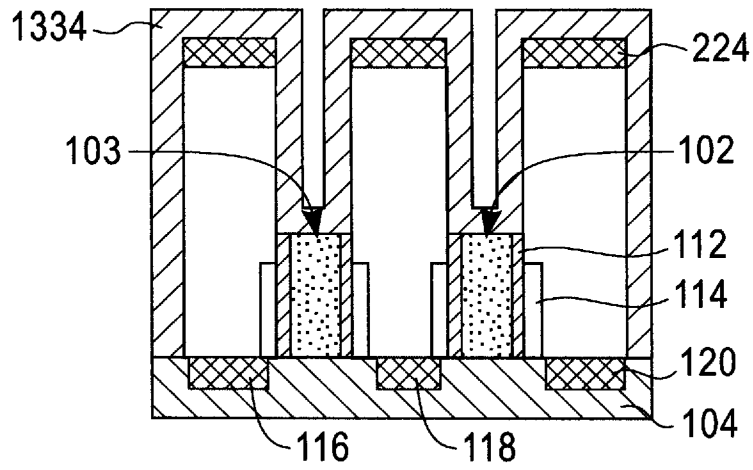


FIG. 14

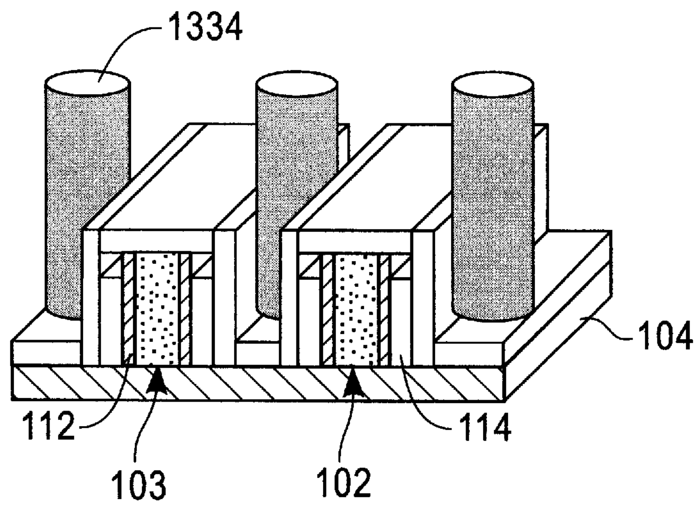
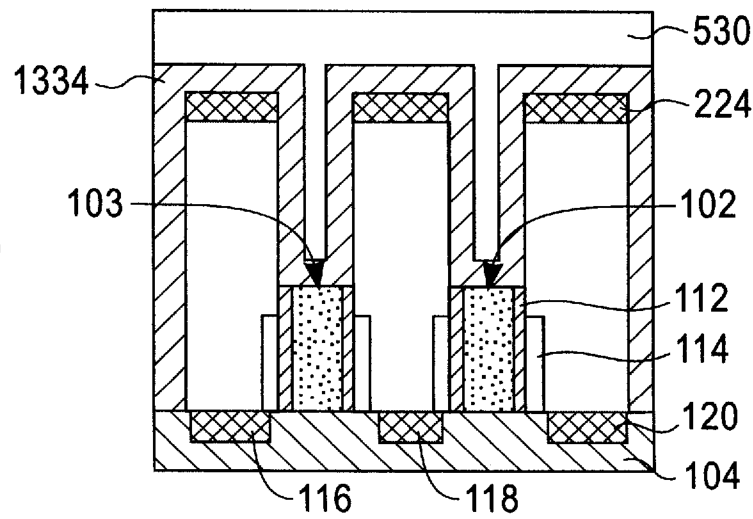


FIG. 15



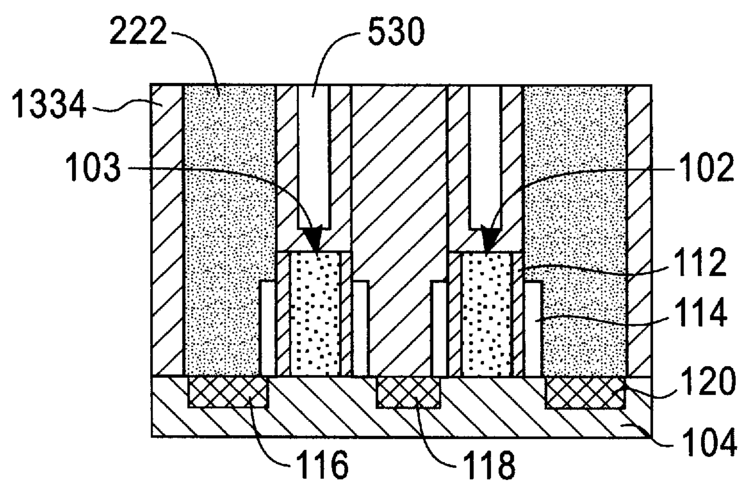


FIG. 16

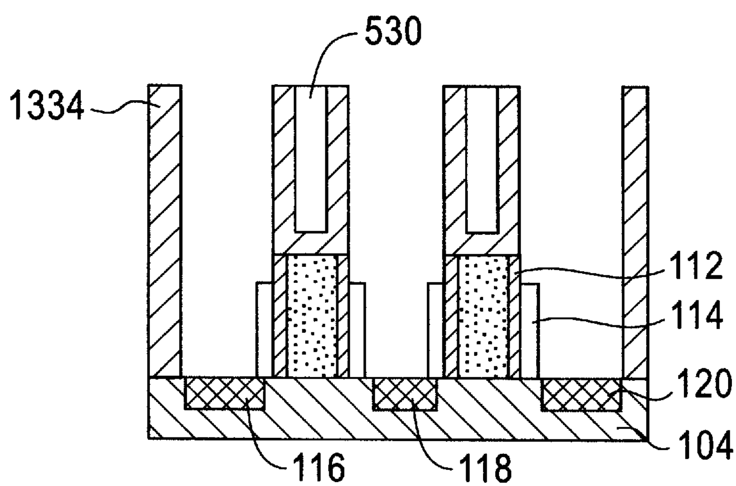


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/060484

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/60 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/026513 A1 (COSTRINI GREGORY [US] ET AL) 31 January 2008 (2008-01-31) page 1, paragraph 2 - paragraph 4 page 2, paragraph 27 - page 5, paragraph 46; figures 2-12 -----	1-3,5-7, 13-15
X	CLEEVES M ET AL: "A novel disposable post technology for self-aligned sub-micron contacts" VLSI TECHNOLOGY, 1994. DIGEST OF TECHNICAL PAPERS. 1994 SYMPOSIUM ON HONOLULU, HI, USA 7-9 JUNE 1994, NEW YORK, NY, USA,IEEE, 7 June 1994 (1994-06-07), pages 61-62, XP010123004 ISBN: 978-0-7803-1921-9 the whole document ----- -/--	1,2,5,7, 8,13-15

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2009	18/01/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Micke, Kornelia

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 710 061 A (CLEEVES JAMES M [US]) 20 January 1998 (1998-01-20) column 4, line 16 - column 7, line 42; figures 1,2	1,2,5,7, 8,13,15
A	US 2002/001931 A1 (KIM HYOUNG-JOON [KR] ET AL) 3 January 2002 (2002-01-03) the whole document	1-3,6-8, 13-15
A	US 2007/049010 A1 (BURGESS BYRON N [US] ET AL BURGESS BYRON NEVILLE [US] ET AL) 1 March 2007 (2007-03-01) page 1, paragraph 11 - paragraph 12 page 2, paragraph 14 - paragraph 15 page 3, paragraph 34 - page 6, paragraph 74; figures 1-14	1-3,7, 13-15
A	US 2007/134909 A1 (KLEE VEIT [US] ET AL) 14 June 2007 (2007-06-14) page 1, paragraph 14 - page 4, paragraph 42; figures 1-13	1,4,7
A	US 6 010 935 A (DOAN TRUNG T [US]) 4 January 2000 (2000-01-04) column 1, line 1 - column 3, line 11 column 4, line 66 - column 8, line 38; figures 2,3	1-3,5-8, 13,15
P,A	US 2008/233738 A1 (BEYER SVEN [DE] ET AL) 25 September 2008 (2008-09-25) the whole document	1,3,4,7, 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2009/060484

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-8, 13-15

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-8,13-15

A method for fabricating a transistor having self-aligned borderless electrical contacts, comprising the steps of:
- forming a gate stack surrounded by an off-set spacer on a silicon region;
- depositing a sacrificial material comprised of a carbon-based film overlying the silicon region, the gate stack, and the off-set spacer, the thickness of the sacrificial layer defining the height of an electrical contact to be formed;
- defining a pattern in the sacrificial layer to define a contact area for the electrical contact, exposing at least a portion of the gate stack and source/drain;
- depositing a dielectric layer overlying the patterned sacrificial layer and the portion of the exposed gate stack;
- selectively removing the sacrificial layer;
- metallizing the contact area in the height defined;
characterised in that the masking material used to pattern the sacrificial layer is trimmed before etching away the sacrificial layer not covered by the masking material.

---

2. claim: 9

A method for fabricating a transistor having self-aligned borderless electrical contacts, comprising the steps of:
- forming a gate stack surrounded by an off-set spacer on a silicon region;
- depositing a sacrificial material comprised of a carbon-based film overlying the silicon region, the gate stack, and the off-set spacer, the thickness of the sacrificial layer defining the height of an electrical contact to be formed;
- defining a pattern in the sacrificial layer to define a contact area for the electrical contact, exposing at least a portion of the gate stack and source/drain;
- depositing a dielectric layer overlying the patterned sacrificial layer and the portion of the exposed gate stack;
- selectively removing the sacrificial layer;
- metallizing the contact area in the height defined,
characterised in that the patterned sacrificial material is trimmed.

---

3. claims: 10-12

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

A method for fabricating a transistor having self-aligned borderless electrical contacts, comprising the steps of:
- forming a gate stack surrounded by an off-set spacer on a silicon region;
- depositing a sacrificial material comprised of a carbon-based film overlying the silicon region, the gate stack, and the off-set spacer, the thickness of the sacrificial layer defining the height of an electrical contact to be formed;
- defining a pattern in the sacrificial layer to define a contact area for the electrical contact, exposing at least a portion of the gate stack and source/drain;
- depositing a dielectric layer overlying the patterned sacrificial layer and the portion of the exposed gate stack;
- selectively removing the sacrificial layer;
- metallizing the contact area in the height defined, characterised in that a liner is deposited over the silicon region, the patterned sacrificial layer and the exposed portion of the gate stack.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2009/060484

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