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MIN et al.

(54) **METHOD OF FABRICATING MONOS SEMICONDUCTOR DEVICE**

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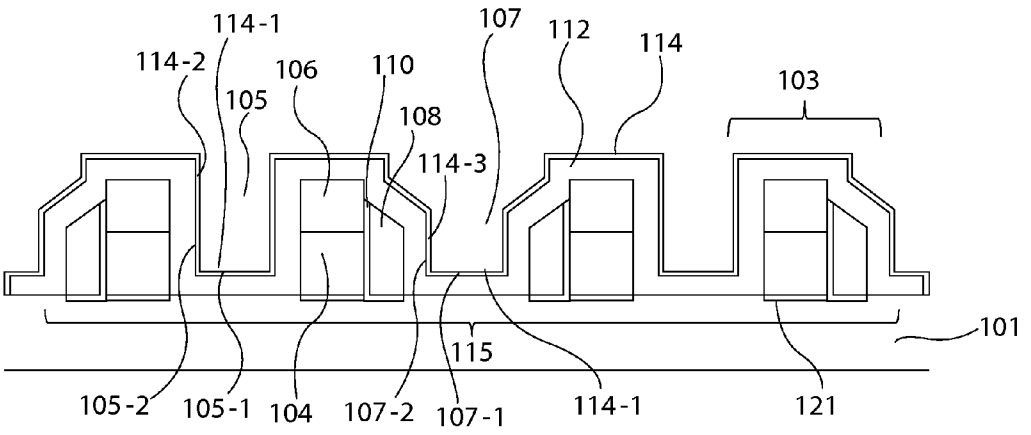
USPC **257/326**; 438/587

(57) **ABSTRACT**

A method for fabricating a semiconductor device is provided. The method includes forming a plurality of gate structures having asymmetric sidewalls including a tall side and a short side. Adjacent ones of the plurality of gate structures are separated by a tall side-tall side region and a short side-short side region. The method further comprises forming a spacer layer over the plurality of gate structures and a bottom surface of the tall side-tall side region and the short side-short side region, depositing an oxide layer over the spacer layer, etching the bottom surface portions of the oxide layer, and selectively etching the sidewall portions of the oxide layer in the tall side-tall side region.



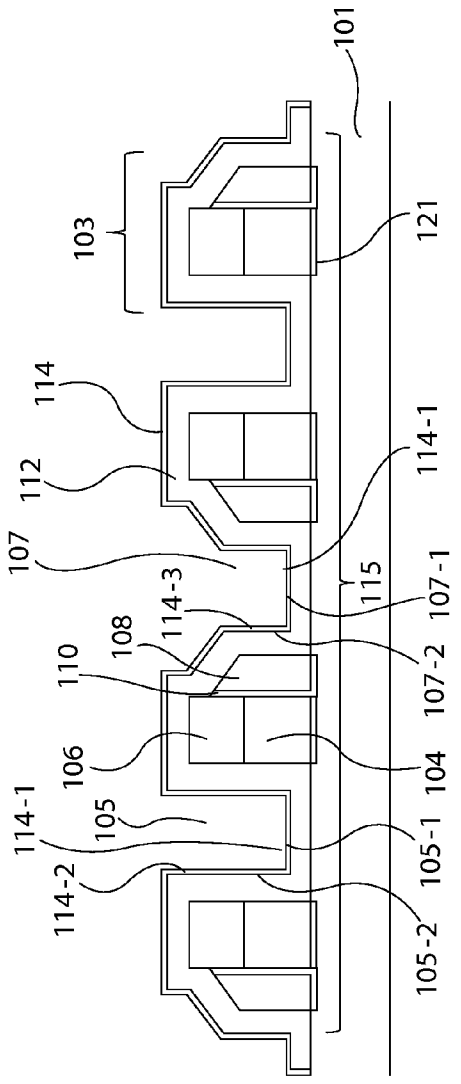

101
103
121
114
112
107
114-1
115
107-1
114-3
108
110
107-2
106
104
114-1
105
105-1
114-2
105-2

FIG. 1A

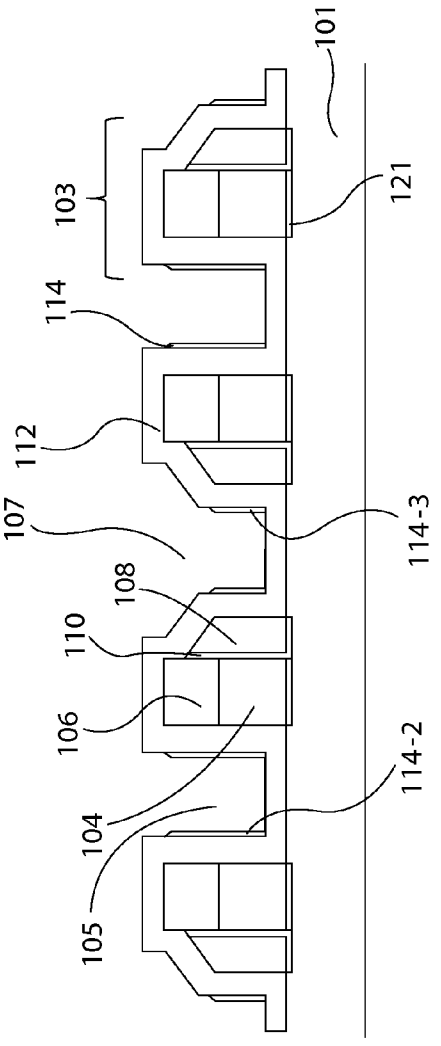

101
103
121
114
112
107
114-3
108
110
106
104
114-2
105

FIG. 1B

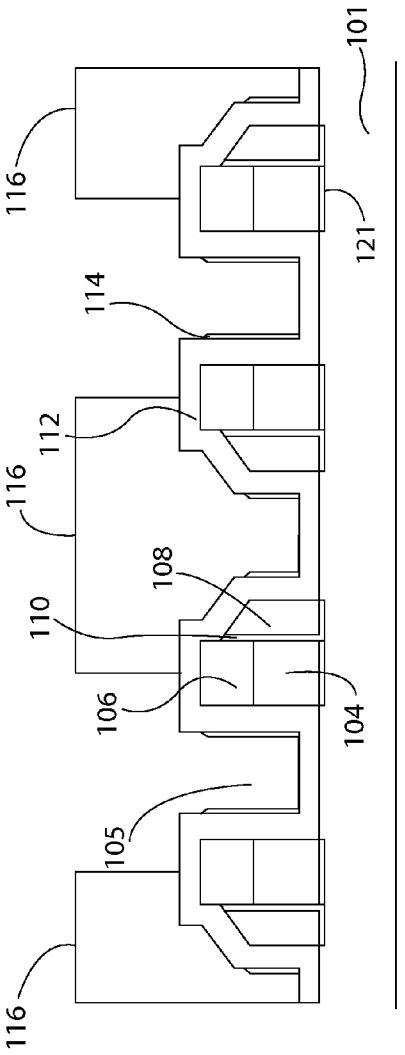

101
116
121
114
112
116
108
110
106
104
105
116

FIG. 1C

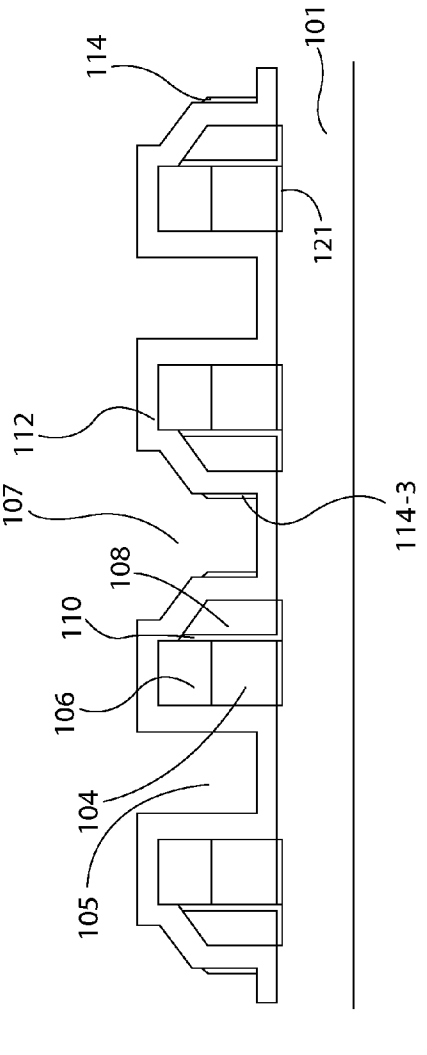

114
101
121
112
107
114-3
108
110
106
104
105

FIG. 1D

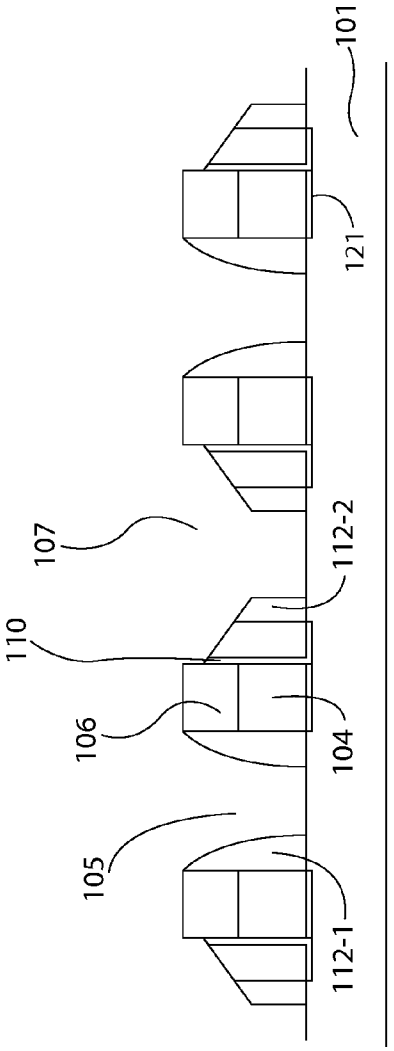

101
121
107
112-2
110
106
104
105
112-1

FIG. 1E

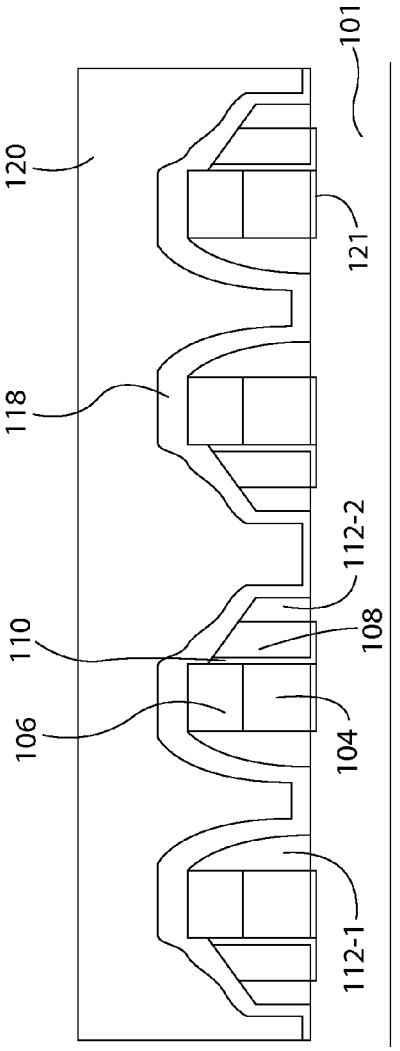

101
120
121
118
112-2
110
108
106
104
112-1

FIG. 1F

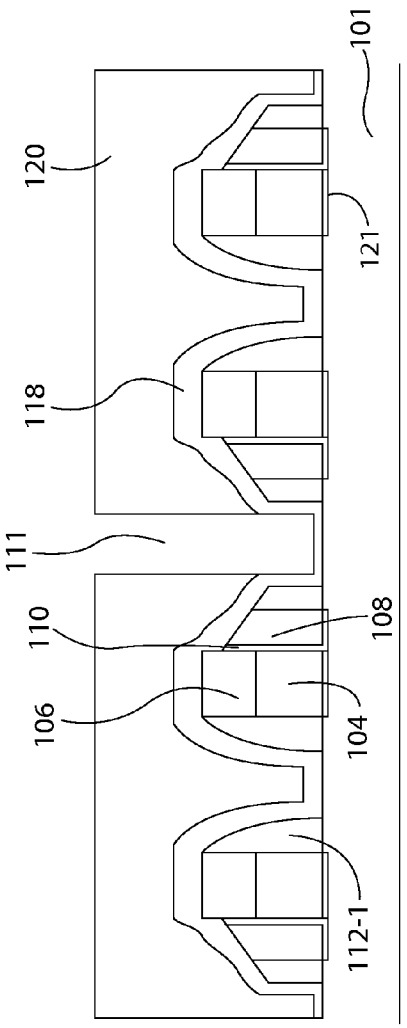


FIG. 1G

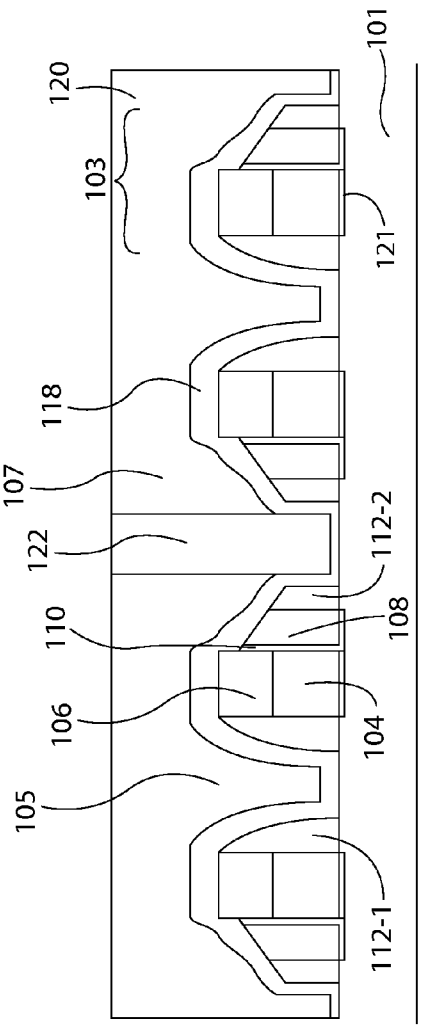


FIG. 1H

100

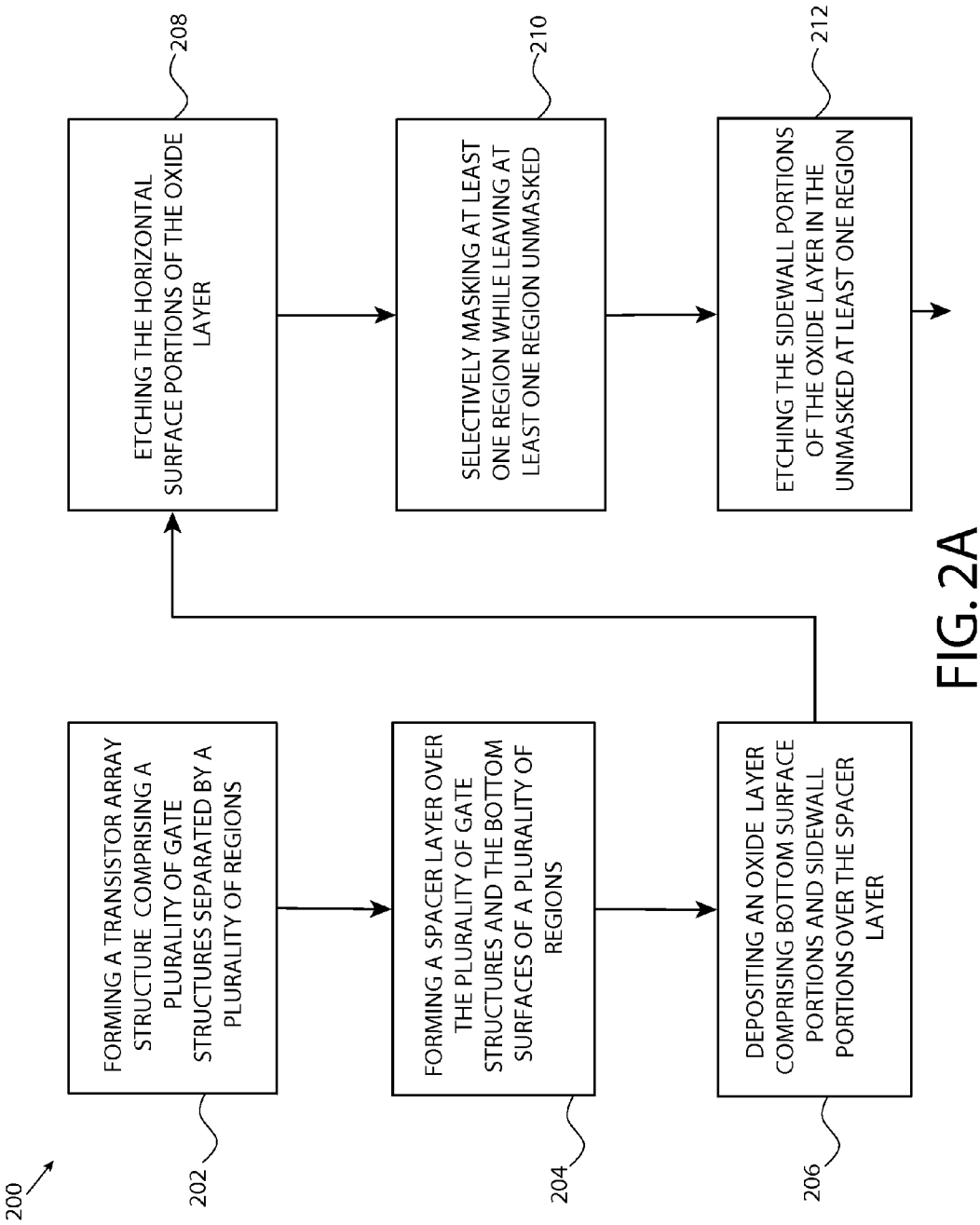

200
FORMING A TRANSISTOR ARRAY STRUCTURE COMPRISING A PLURALITY OF GATE STRUCTURES SEPARATED BY A PLURALITY OF REGIONS
202
FORMING A SPACER LAYER OVER THE PLURALITY OF GATE STRUCTURES AND THE BOTTOM SURFACES OF A PLURALITY OF REGIONS
204
DEPOSITING AN OXIDE LAYER COMPRISING BOTTOM SURFACE PORTIONS AND SIDEWALL PORTIONS OVER THE SPACER LAYER
206
ETCHING THE HORIZONTAL SURFACE PORTIONS OF THE OXIDE LAYER
208
SELECTIVELY MASKING AT LEAST ONE REGION WHILE LEAVING AT LEAST ONE REGION UNMASKED
210
ETCHING THE SIDEWALL PORTIONS OF THE OXIDE LAYER IN THE UNMASKED AT LEAST ONE REGION
212

FIG. 2A

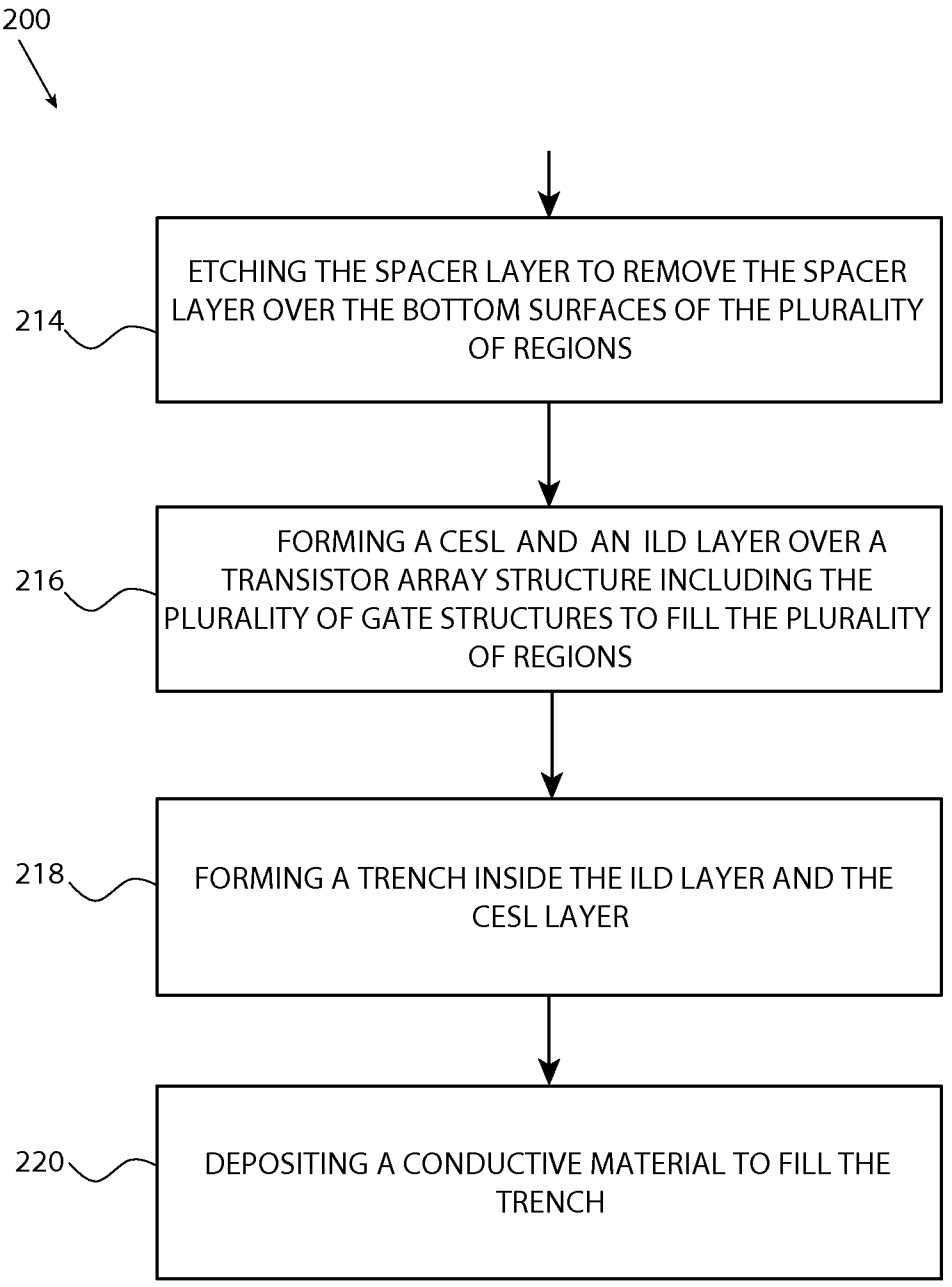

200
214
ETCHING THE SPACER LAYER TO REMOVE THE SPACER LAYER OVER THE BOTTOM SURFACES OF THE PLURALITY OF REGIONS
216
FORMING A CESL AND AN ILD LAYER OVER A TRANSISTOR ARRAY STRUCTURE INCLUDING THE PLURALITY OF GATE STRUCTURES TO FILL THE PLURALITY OF REGIONS
218
FORMING A TRENCH INSIDE THE ILD LAYER AND THE CESL LAYER
220
DEPOSITING A CONDUCTIVE MATERIAL TO FILL THE TRENCH

FIG. 2B

METHOD OF FABRICATING MONOS SEMICONDUCTOR DEVICE

FIELD

[0001] This disclosure relates to a method of forming a semiconductor device and the resulting semiconductor device. More particularly, the disclosed subject matter relates to a process for fabrication of a MONOS cell structure of a semiconductor device, and the resulting MONOS device.

BACKGROUND

[0002] A metal-oxide-nitride-oxide-semiconductor (MONOS) memory cell is a type of nonvolatile memory device structure. A MONOS cell generally comprises a semiconductor substrate, a channel layer above the semiconductor substrate, source and drain diffusion regions in the surface of the semiconductor substrate, and a gate conductor above the channel layer. An oxide-nitride-oxide (ONO) layer is disposed between the channel layer and the gate conductor. In the ONO layer, a layer of nitride is sandwiched between two insulative layers of oxide.

[0003] In a MONOS memory cell, electric charge is stored in traps in the nitride layer, and this stored charge is utilized to store data. MONOS memory devices provide high stability and reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present disclosure is best understood from the following detailed description when read in conjunction with the accompanying drawings. It is emphasized that, according to common practice, the various features of the drawings are not necessarily to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Like reference numerals denote like features throughout specification and drawings.

[0005] FIGS. **1**A-**1**H illustrate an exemplary method of forming a metal oxide nitride oxide semiconductor (MONOS) device in accordance with some embodiments.

[0006] FIGS. **2**A-**2**B are flow diagrams illustrating an exemplary method of forming a semiconductor device in accordance with some embodiments.

DETAILED DESCRIPTION

[0007] This description of the exemplary embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical,", "above," "below," "up," "down," "top" and "bottom" as well as derivative thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation.

[0008] Semiconductor devices such as MONOS devices and static random access memory (SRAM) semiconductor devices continue to be scaled to smaller size to meet advanced performance targets. Fabrication of devices with such small dimensions involves precise control. For example, semiconductor processing often involves filling a material into a region, a trench or a gap having a high aspect ratio defined by the ratio of a longest dimension such as height to a shortest dimension such as width of the region. Because of such a high aspect ratio, voids may exist inside such a region after the filling step. The voids may be filled with unwanted materials such as conductive material during subsequent fabrication processes. It is desirable to prevent or eliminate such voids during fabrication and provide a good region having a high aspect ratio in a semiconductor device.

[0009] The present disclosure provides a method for fabricating a semiconductor device such as a MONOS device or an SRAM device. In some embodiments, the method comprises forming a transistor array structure comprising a plurality of gate structures separated by a plurality of regions. The regions between adjacent gate structures can have a high aspect ratio. The method comprises a step of selectively masking at least one region between adjacent gate structures while leaving at least one region unmasked. The unmasked region is etched before filling the region with a material.

[0010] Unless expressly indicated otherwise, references to a "region" separating a plurality of gate structures made in this disclosure will be understood to encompass a space, a trench or a gap between adjacent gate structures. At least one of these regions can have a high aspect ratio, for example, more than 5 in some embodiments. Such aspect ratio is higher than 10 in some embodiments.

[0011] In FIGS. **1**A-**1**H, like items are indicated by like reference numerals, and for brevity, descriptions of the structure, provided above with reference to the previous figures, are not repeated. The method described in FIGS. **2**A-**2**B is described with reference to the exemplary structures described in FIGS. **1**A-**1**H. FIGS. **1**A-**1**H illustrate an exemplary method of forming a MONOS device in accordance with some embodiments.

[0012] FIGS. **2**A-**2**B are flow diagrams illustrating an exemplary method **200** of forming a semiconductor device such a MONOS device in accordance with some embodiments.

[0013] Steps **202**-**206** form the structure shown in FIG. **1**A. For brevity, separate drawings are not provided to show the intermediate structures in steps **202** and **204**. At step **202**, a transistor array structure **115** comprising a plurality of gate structures **103** is formed over a semiconductor substrate **101**. The plurality of gate structures **103** are separated by a plurality of regions **105** and **107**.

[0014] Substrate **101** can be a wafer comprising a semiconductor material. Examples of suitable materials for substrate **101** include but are not limited to silicon, germanium, a compound semiconductor, and a semiconductor-on-insulator (SOI) substrate. A compound semiconductor can be an III-V semiconductor compound such as gallium arsenide (GaAs). An SOI substrate can comprise a semiconductor on an insulator such as glass.

[0015] Two adjacent gate structures **103** are separated by a region **105** or **107**. Region **105** or **107** has a bottom surface (**105**-**1** or **107**-**1**) over semiconductor substrate **101** and a side wall (**105**-**2** or **107**-**2**) shared with the at least one gate structure **103**. At least one region **105** or **107** has an aspect ratio equal to or higher than 5 or 10, for example, 40 in some embodiments.

[0016] In some embodiments, the plurality of gate structures **103** have asymmetric sidewalls including a tall side and a short side as shown in FIG. **1**A. Adjacent ones of the plurality of gate structures **103** are separated by a tall side-tall side region **105** and a short side-short side region **107** as shown in FIG. **1**A.

[0017] The semiconductor device is not limited to any specific type. For example, the plurality of gate structures **103** are included in a metal oxide nitride oxide semiconductor (MONOS) device in some embodiments, or in a static random access memory (SRAM) semiconductor device in some other embodiments.

[0018] In some embodiments, the method is used for fabricating a MONOS device. Referring to FIG. **1**A, at step **202** of FIG. **2**, each respective gate structure **103** in the transistor array structure comprises a control gate **104**, a memory gate **108**, and an oxide-nitride-oxide (ONO) layer **110** between control gate **104** and memory gate **108**. Control gate **104** and memory gate **108** are disposed side-by-side over semiconductor substrate **101**. Each gate structure **103** can further comprise a hard mask layer **106** above control gate **104**.

[0019] Referring to FIG. **1**A, control gate **104** comprises any suitable material in any suitable configuration. Examples of suitable materials for control gate **104** include but are not limited to amorphous silicon, polysilicon, polysilicon/germanium. aluminum, copper, titanium, tantalum, tungsten, molybdenum, platinum, tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), titanium aluminum (TiAl), titanium aluminum nitride (TiAlN), TaCN, TaC, TaSiN, other conductive material, or combinations thereof. The conductive material of the control gate **104** can be doped or undoped. In some embodiments, control gate **104** comprises polysilicon.

[0020] Memory gate **108** can also comprise any suitable material in any suitable configuration. Examples of suitable materials for memory gate **108** include but are not limited to amorphous silicon, polysilicon, polysilicon/germanium, aluminum, copper, titanium, tantalum, tungsten, molybdenum, platinum, tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), titanium aluminum (TiAl), titanium aluminum nitride (TiAlN), TaCN, TaC, TaSiN, other conductive material, or combinations thereof. The conductive material of memory gate **108** can be doped or undoped. In some embodiments, memory gate **108** comprises polysilicon.

[0021] Oxide-nitride-oxide (ONO) layer **110** comprises a three-layer structure including a nitride layer sandwiched between two oxide layers. The nitride layer comprises silicon nitride while the oxide layer comprises silicon oxide in some embodiments. The ONO layer **110** is disposed between control gate **104** and memory gate **108**. The ONO layer **110** is also disposed underneath memory gate **108** in some embodiments, as shown in FIG. **1**A.

[0022] As shown in FIG. **1**A, hard mask **106** is disposed over control gate **104** in some embodiments. Examples of a suitable material for hard mask **106** include but are not limited to silicon oxide, silicon nitride (e.g., Si_3N_4), SiON, SiC, SiOC, or any combination thereof. An one example, hard mask **106** comprises silicon nitride.

[0023] Step **202** in method **200** can also comprise forming other portions (not shown) of a semiconductor device on or above semiconductor substrate **101**, besides control gate **104** and memory gate **108**. For example, the other portions can include one or more of a buffer layer, an isolator layer or isolation structure such as a shallow trench isolation (STI) structure, channel layers, source regions, drain regions and gate dielectric layers such as a gate oxide layer **121** underneath control gate **104**. The method comprises in-situ doping to form a source region and a drain region in the surface of substrate **101** in some embodiments.

[0024] Other portions can include source regions, channel layers and drain regions (not shown). For example, in some embodiments, memory gate **108** is disposed over a source region of the respective gate structure **103**. Control gate **104** is disposed over a drain region of the respective gate structure **103**. Adjacent gate structures **103** share a source region or a drain region; and each of the plurality of regions **105** and **107** is alternatingly over a source region or a drain region. For example, region **105** is above a drain region while region **107** is above a source region in FIG. **1**A. Region **105** has a high aspect ratio, for example, higher than 5 or 10 in some embodiments. Region **105** is the tall side-tall side region while region **107** is the short side-short side region. Region **105** has an aspect ratio of higher than 40 in some embodiments. The ONO layer **110** can be further disposed between a memory gate **108** and a channel layer (not shown) of the memory gate **108** in some embodiments.

[0025] At step **204**, a spacer layer **112** is formed over the plurality of gate structures **103** and the bottom surfaces of a plurality of regions **105** and **107**. Spacer layer **112** can be formed of oxides, nitrides, oxynitrides, combinations thereof and other suitable insulating materials. In some embodiments, spacers are formed of silicon nitrides (e.g., Si_3N_4). Spacer layer **112** can be formed by a deposition process including, for example, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), physical vapor deposition (PVD), sputtering, chemical solution deposition and plating.

[0026] At step **206** of FIG. **2**, a conformal oxide layer **114** is deposited over spacer layer **112**. A suitable material for oxide layer **114** comprises silicon oxide in some embodiments. Oxide layer **114** can be formed by an isotropic deposition process including, for example, CVD, PECVD, ALD or any other isotropic deposition techniques. Oxide layer **114** comprises bottom surface portions **114-1** over the bottom surfaces of the plurality of regions **105** and **107**, and sidewall portions (**114-2** and **114-3**) over the spacer layer **112** along a side wall of the plurality of regions **105** and **107**. The structure of the semiconductor device after step **206** is illustrated in FIG. **1**A.

[0027] At step **208**, the horizontal portions of oxide layer **114** (including bottom surface portions over the bottom surfaces of the plurality of regions **105** and **107**) are etched by an anisotropic etch. The anisotropic etch leaves the vertical sidewall portions of layer **114** substantially intact. The structure of the semiconductor device after step **208** is illustrated in FIG. **1**B. Examples of a suitable etching process include but are not limited to plasma etching and any other suitable technique. A directional etching process is desirable at step **206**. Portions of oxide layer **114** on a horizontal surface are etched away while the sidewall portions over the spacer layer **112** along a side wall of the plurality of regions **105** and **107** are not removed.

[0028] At step **210**, exemplary method **200** comprises selectively masking at least one region while leaving at least one region unmasked. The structure of the semiconductor device after step **208** is illustrated in FIG. **1**C.

[0029] As shown in FIG. **1**C, at least one of the plurality of regions **105** and **107** can be masked. In some embodiments, the unmasked at least one region, for example, **105** in FIG. **1**C, has a high aspect ratio. The unmasked at least one region can have an aspect ratio equal to or higher than, 10 or 20 in some embodiments. The unmasked region can have an aspect ratio equal to or higher than 40 in some embodiments. In some embodiments, the short side-short side region **107** is

selectively masked. The tall side-tall side region **105** is left unmasked. The unmasked tall side-tall side region **105** has an aspect ratio equal to or higher than 40.

[0030] Taking a MONOS device described for step **202** as an example, in some embodiments, ones of the plurality of regions **107** over a source region are masked and ones of the plurality of regions over drain regions **105** are not masked in step **210** of selectively masking. Regions **105** have an aspect ratio equal to or high than 40 in some embodiments.

[0031] The step of selectively masking at least one region is performed using a photoresist material **116** (FIG. **1**C) in some embodiments. In such a fabrication process, a photoresist is used for patterning. Photoresist patterning includes process steps such as photoresist coating, softbaking, mask aligning, pattern exposing, photoresist development, and hard baking.

[0032] At step **212**, an etching process is performed to remove the sidewall portions of oxide layer **114** in the at least one unmasked region **105**. The etching process at step **212** can be performed by a suitable etch process having an isotropic etch component. Examples of a suitable etching process include but are not limited to plasma etching, reactive ion etching and wet etching. Examples of suitable plasma include but are not limited to plasma comprising fluorine or fluorine compounds. After etching the sidewall portions of oxide layer **114**, photoresist **116** is removed through dry or wet etching, stripping and/or other cleaning processes. In some embodiments, photoresist **116** is completely removed through a wet removal process. For example, photoresist **116** can be stripped by a solution comprising an ingredient such as H_2SO_4, H_2O_2, and NH_4OH. The structure of the semiconductor device after step **212** including possible photoresist removal is illustrated in FIG. **1**D.

[0033] At step **214** (FIG. **2**B), a process of etching spacer layer **112** is performed on spacer layer **112** over the bottom surfaces of the plurality of regions **105** and **107**. The structure of the semiconductor device after step **214** is illustrated in FIG. **1**E. Such a process of etching can be performed using dry etching, wet etching or any other suitable technique. Examples of a suitable etching process include but are not limited to using plasma, for example, fluorine-containing plasma.

[0034] At step **216**, a contact etching stop layer (CESL) **118** and an interlayer dielectric (ILD) layer **120** are formed over a transistor array structure including the plurality of gate structures **103**. The CESL **118** is deposited first. The ILD layer **120** is then formed over the CESL **118**. The ILD layer **120** fills the plurality of regions **105** and **107**. The structure of the semiconductor device after step **216** is illustrated in FIG. **1**F.

[0035] The CESL **118** can be formed of silicon nitride, silicon oxynitride, silicon carbide, silicon oxycarbide, combinations thereof, or other suitable materials. In some embodiments, the CESL **118** is formed of silicon nitride. The CESL **118** can be formed by using chemical vapor deposition (CVD), high density plasma CVD, sputtering, or other suitable method.

[0036] Examples of suitable materials for the ILD layer **120** include but are not limited to silicon oxide, silicon oxynitride, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), combinations thereof, or other suitable material. The ILD layer **120** can be formed by using CVD, high density plasma CVD, spin-on, sputtering, or other suitable method.

[0037] At step **218**, a trench **111** is formed inside the ILD layer **120** and the CESL **118**. The structure of the semiconductor device after step **218** is illustrated in FIG. **1**G. A trench **109** can be formed inside the CESL **118** and the ILD layer **120** through a suitable process, for example, photoresist patterning. In some embodiments, the step of forming trench **111** includes a dry etch process. For example, a suitable photoresist can be applied and exposed to UV light or other irradiation under a mask. After the photoresist is developed, a portion of the CESL **118** and a portion of the ILD layer **120** are removed to form a trench **111** as shown in FIG. **1**G.

[0038] At step **220**, a conductive material **122** is deposited to fill trench **111** to form a contact. The structure of the semiconductor device after step **220** is illustrated in FIG. **1**H. Examples of a suitable material **122** include but are not limited to tungsten and copper. Although FIG. **1**H only shows one contact **122**, any number of contacts **122** can be formed. For example, in some embodiments, each source/drain region has a contact **122** formed by this process.

[0039] In some embodiments, when step **210** of selective masking is not used, the ILD layer **120** may contain undesirable voids or tunnels formed inside regions **105** having a high aspect ratio. After step **220**, conductive material **122** may fill such voids or tunnels, causing defects. In some embodiments, when step **210** of selective masking is used, the ILD layer **120** does not contain voids or defects.

[0040] The present disclosure also provides a semiconductor device. An exemplary device **100** is shown in FIG. **1**F. The exemplary device **100** comprises a transistor array structure **115** over a semiconductor substrate **101**. The transistor array structure **115** comprises a plurality of gate structures **103** having asymmetric sidewalls including a tall side and a short side. Adjacent gate structures **103** are separated by a tall side-tall-side region **105** and a short side-short side region **107**. The device **100** further comprises a spacer layer **112** (including **112-1** and **112-2**) disposed along the sidewalls of the tall side-tall-side region **105** and the short side-short side region **107**. The spacer layer **112-1** disposed along the sidewalls of the tall side-tall side region **105** has a curved surface. The spacer layer **112-2** disposed along the sidewalls of the short side-short side region **107** can have a sharp corner in some embodiment. In some embodiments, spacer layer **112-1** can have a thickness thinner than that of spacer layer **112-2**. In some embodiments, the tall side-tall side region **105** has an aspect ratio equal to or higher than 40. In some embodiments, device **100** is a metal oxide nitride oxide semiconductor (MONOS) device. Each gate structure **103** comprises a control gate **104**, a memory gate **108**, and an oxide-nitride-oxide (ONO) layer **110** between control gate **104** and memory gate **108**. Control gate **104** is disposed adjacent to the short side-short side region **107** and memory gate **104** is disposed adjacent to the tall side-tall side region **107**. In some embodiments, device **100** further comprises a hard mask layer **106** above control gate **104**, a CESL layer **118** over the transistor array structure **115**, an ILD layer **120** over the transistor array structure **115** and inside the tall side-tall-side region **105** and the short side-short side region **107**, a conductive material **122** filled in a trench inside the ILD layer **120** and the CESL layer **118**.

[0041] The present disclosure provides a method for fabricating a semiconductor device. In some embodiments, the method comprises forming a plurality of gate structures having asymmetric sidewalls including a tall side and a short side. Adjacent ones of the plurality of gate structures are separated by a tall side-tall side region and a short side-short side region. The plurality of gate structures are included in a metal oxide nitride oxide semiconductor (MONOS) device in some

embodiments. The plurality of gate structures are included in a static random access memory (SRAM) semiconductor device in some other embodiments.

[0042] The method further comprises forming a spacer layer over the plurality of gate structures and a bottom surface of the tall side-tall side region and the short side-short side region, and depositing an oxide layer over the spacer layer. The oxide layer comprises bottom surface portions, and sidewall portions over the spacer layer tall side-tall side region and the short side-short side region. The method further comprises etching the bottom surface portions of the oxide layer, and selectively etching the sidewall portions of the oxide layer in the tall side-tall side region. In some embodiments, the method comprises selectively masking the short side-short side region while leaving the tall side-tall side region unmasked, before selectively etching the sidewall portion of the oxide layer. The unmasked tall side-tall side region has an aspect ratio equal to or higher than 40 in some embodiments. The step of selectively masking at least one region is performed using a photoresist material in some embodiments.

[0043] In some embodiments, the method further comprises etching the spacer layer to remove the spacer layer over the bottom surfaces of the tall side-tall side region and the short side-short-side region, and forming a contact etching stop layer (CESL) and an interlayer dielectric (ILD) layer over a transistor array structure including the plurality of gate structures to fill the plurality of regions. In some embodiments, the method further comprises forming a trench inside the ILD layer and the CESL layer, and depositing a conductive material to fill the trench.

[0044] In some embodiments, a method in this disclosure is a method for fabricating a semiconductor device such as a MONOS device. The method comprises forming a transistor array structure over a semiconductor substrate. The transistor array structure comprises a plurality of gate structures separated by a plurality of regions. Adjacent gate structures are separated by a region having a bottom surface over the semiconductor substrate and a side wall shared with the at least one gate structure.

[0045] The method further comprises forming a spacer layer over the plurality of gate structures and the bottom surfaces of the plurality of regions, and depositing an oxide layer over the spacer layer. The oxide layer comprises bottom surface portions over the bottom surfaces of the plurality of regions, and sidewall portions over the spacer layer along a side wall of the plurality of regions. The method further comprises etching the bottom surface portions of the oxide layer over the bottom surfaces of the plurality of regions; selectively masking at least one region while leaving at least one region unmasked, and etching the sidewall portions of the oxide layer in the unmasked at least one region. The unmasked at least one region has an aspect ratio equal to or higher than 40 in some embodiments. The step of selectively masking at least one region can be performed using a photoresist material.

[0046] In some embodiments, each respective gate structure in the transistor array structure comprises a control gate, a memory gate, and an oxide-nitride-oxide (ONO) layer between the control gate and the memory gate. The control gate and the memory gate are disposed side-by-side over the semiconductor substrate. Each gate structure can further comprise a hard mask layer above the control gate. In some embodiments, the memory gate is disposed over a source region of the respective gate structure. The control gate is disposed over a drain region of the respective gate structure. Adjacent gate structures share a source region or a drain region; and each of the plurality of regions is alternatingly over a source region or a drain region. In some embodiments, ones of the plurality of regions over a source region are masked and ones of the plurality of regions over a drain region are not masked in the step of selectively masking at least one of the plurality of the regions.

[0047] In some embodiments, the method for fabricating a MONOS device further comprises etching the spacer layer to remove the spacer layer over the bottom surfaces of the plurality of regions, and forming a CESL and an ILD layer over the transistor array structure to fill the plurality of regions, forming a trench inside the ILD layer and the CESL layer, and depositing a conductive material to fill the trench.

[0048] In another aspect, the present disclosure provides a semiconductor device. The semiconductor device comprises a transistor array structure over a semiconductor substrate. The transistor array structure comprises a plurality of gate structures having asymmetric sidewalls including a tall side and a short side. Adjacent gate structures are separated by a tall side-tall-side region and a short side-short side region. The device further comprises a spacer layer disposed along the sidewalls of the tall side-tall-side region and the short side-short side region. The spacer layer disposed along the sidewalls of the tall side-tall side region has a curved surface. In some embodiments, the tall side-tall side region has an aspect ratio equal to or higher than 40. In some embodiments, the device is a metal oxide nitride oxide semiconductor (MONOS) device. Each gate structure comprises a control gate, a memory gate, and an oxide-nitride-oxide (ONO) layer between the control gate and the memory gate. The control gate is disposed adjacent to the short side-short side region and the memory gate is disposed adjacent to the tall side-tall side region. In some embodiments, the device further comprises a hard mask layer above the control gate, a contact etching stop layer (CESL) over the transistor array structure, an interlayer dielectric (ILD) layer over the transistor array structure and inside the tall side-tall-side region and the short side-short side region, a conductive material filled in a trench inside the ILD layer and the CESL layer.

[0049] Although the subject matter has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments, which may be made by those skilled in the art.

What is claimed is:

1. A method for fabricating a semiconductor device, comprising:

forming a plurality of gate structures having asymmetric sidewalls including a tall side and a short side, wherein adjacent ones of the plurality of gate structures are separated by a tall side-tall side region and a short side-short side region;

forming a spacer layer over the plurality of gate structures and a bottom surface of the tall side-tall side region and the short side-short side region;

depositing an oxide layer over the spacer layer, the oxide layer comprising bottom surface portions and sidewall portions in the tall side-tall side region and the short side-short side region;

etching the bottom surface portions of the oxide layer; and

selectively etching the sidewall portions of the oxide layer in the tall side-tall side region.

2. The method of claim 1, further comprising:
etching the spacer layer to remove the spacer layer over the bottom surfaces of the tall side-tall side region and the short side-short side region; and
forming a contact etching stop layer (CESL) and an interlayer dielectric (ILD) layer over a transistor array structure including the plurality of gate structures.
3. The method of claim 2, further comprising:
forming a trench inside the ILD layer and the CESL layer; and
depositing a conductive material to fill the trench.
4. The method of claim 1, further comprising
selectively masking the short side-short side region while leaving the tall side-tall side region unmasked, before selectively etching the sidewall portion of the oxide layer, wherein the unmasked tall side-tall side region has an aspect ratio equal to or higher than 40.
5. The method of claim 4, wherein
the step of selectively masking is performed using a photoresist material.
6. The method of claim 1, wherein
the plurality of gate structures are included in a metal oxide nitride oxide semiconductor (MONOS) device.
7. The method of claim 1, wherein
the plurality of gate structures are included in a static random access memory (SRAM) semiconductor device.
8. A method for fabricating a semiconductor device, comprising:
forming a transistor array structure over a semiconductor substrate, the transistor array structure comprising a plurality of gate structures separated by a plurality of regions, adjacent gate structures separated by a region having a bottom surface over the semiconductor substrate and a side wall shared with the at least one gate structure;
forming a spacer layer over the plurality of gate structures and the bottom surfaces of the plurality of regions;
depositing an oxide layer over the spacer layer, the oxide layer comprising bottom surface portions over the bottom surfaces of the plurality of regions, and sidewall portions over the spacer layer along a side wall of the plurality of regions;
etching the bottom surface portions of the oxide layer over the bottom surfaces of the plurality of regions;
selectively masking at least one region while leaving at least one region unmasked; and
etching the sidewall portions of the oxide layer in the unmasked at least one region.
9. The method of claim 8, wherein
each respective gate structure in the transistor array structure comprises a control gate, a memory gate, and an oxide-nitride-oxide (ONO) layer between the control gate and the memory gate, the control gate and the memory gate disposed side-by-side over the semiconductor substrate.
10. The method of claim 9, wherein
each gate structure further comprises a hard mask layer above the control gate.
11. The method of claim 9, wherein
the memory gate is disposed over a source region of the respective gate structure;
the control gate is disposed over a drain region of the respective gate structure;
adjacent gate structures share a source region or a drain region; and
each of the plurality of regions is alternatingly over a source region or a drain region.
12. The method of claim 11, wherein
ones of the plurality of regions over a source region are masked and ones of the plurality of regions over a drain region are not masked in the step of selectively masking at least one of the plurality of the regions.
13. The method of claim 8, wherein
the step of selectively masking at least one of the plurality of the regions is performed using a photoresist material.
14. The method of claim 8, wherein
the unmasked at least one region has an aspect ratio equal to or higher than 40.
15. The method of claim 8, further comprising:
etching the spacer layer to remove the spacer layer over the bottom surfaces of the plurality of regions; and
forming a contact etching stop layer (CESL) and an interlayer dielectric (ILD) layer over the transistor array structure to fill the plurality of regions;
16. The method of claim 15, further comprising:
forming a trench inside the ILD layer and the CESL layer; and
depositing a conductive material to fill the trench.
17. A semiconductor device, comprising:
a transistor array structure over a semiconductor substrate, the transistor array structure comprising a plurality of gate structures having asymmetric sidewalls including a tall side and a short side, wherein adjacent gate structures are separated by a tall side-tall-side region and a short side-short side region; and
a spacer layer disposed along the sidewalls of the tall side-tall-side region and the short side-short side region, wherein the spacer layer disposed along the sidewalls of the tall side-tall side region has a curved surface.
18. The device of claim 17, wherein
the tall side-tall side region has an aspect ratio equal to or higher than 40.
19. The device of claim 17, wherein
the device is a metal oxide nitride oxide semiconductor (MONOS) device; and
each gate structure comprises a control gate, a memory gate, and an oxide-nitride-oxide (ONO) layer between the control gate and the memory gate;
the control gate is disposed adjacent to the short side-short side region and the memory gate is disposed adjacent to the tall side-tall side region.
20. The device of claim 19, further comprising:
a hard mask layer above the control gate;
a contact etching stop layer (CESL) over the transistor array structure;
an interlayer dielectric (ILD) layer over the transistor array structure and inside the tall side-tall-side region and the short side-short side region;
a conductive material filled in a trench inside the ILD layer and the CESL layer.

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