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Ramachandran et al.

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(54) **STRUCTURE AND METHOD FOR FABRICATING A COMPUTING SYSTEM WITH AN INTEGRATED VOLTAGE REGULATOR MODULE**

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(Continued)

(51) **Int. Cl.**

H01L 21/77	(2017.01)
H01L 21/66	(2006.01)

(Continued)

(52) **U.S. Cl.**
CPC ***H01L 21/77*** (2013.01); ***H01L 22/20*** (2013.01); ***H01L 24/32*** (2013.01); ***H01L 24/73*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 21/77; H01L 22/20; H01L 24/32; H01L 24/73; H01L 25/03; H01L 25/16;
(Continued)

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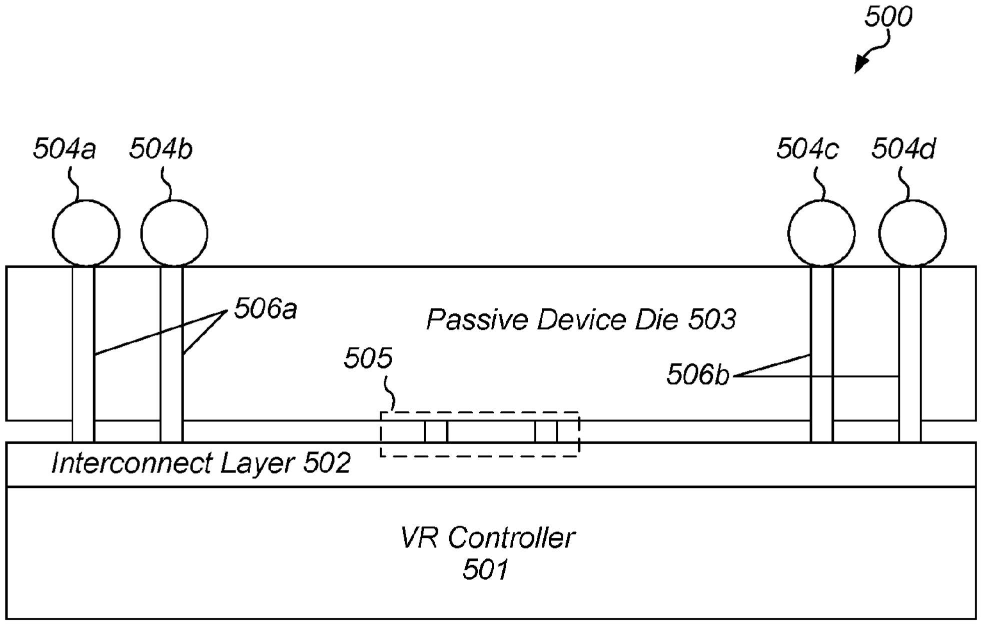
(57) **ABSTRACT**

Systems that include integrated circuit dies and voltage regulator units are disclosed. Such systems may include a voltage regulator module and an integrated circuit mounted in a common system package. The voltage regulator module may include a voltage regulator circuit and one or more passive devices mounted to a common substrate, and the integrated circuit may include a System-on-a-chip. The system package may include an interconnect region that includes wires fabricated on multiple conductive layers within the interconnect region. At least one power supply terminal of the integrated circuit may be coupled to an output of the voltage regulator module via a wire included in the interconnect region.

20 Claims, 16 Drawing Sheets



Related U.S. Application Data

continuation of application No. 15/943,673, filed on Apr. 2, 2018, now Pat. No. 10,818,632, which is a continuation of application No. 15/264,087, filed on Sep. 13, 2016, now Pat. No. 9,935,076.

(60) Provisional application No. 62/234,776, filed on Sep. 30, 2015.

(51) **Int. Cl.**

H01L 23/00	(2006.01)
H01L 25/03	(2006.01)
H01L 25/16	(2023.01)
H01L 25/18	(2023.01)

(52) **U.S. Cl.**

CPC ***H01L 25/03*** (2013.01); ***H01L 25/16*** (2013.01); ***H01L 25/18*** (2013.01); *H01L 24/17* (2013.01); *H01L 2224/12105* (2013.01); *H01L 2224/1403* (2013.01); *H01L 2224/16145* (2013.01); *H01L 2224/16227* (2013.01); *H01L 2224/16235* (2013.01); *H01L 2224/16265* (2013.01); *H01L 2224/1703* (2013.01); *H01L 2224/17181* (2013.01); *H01L 2224/24195* (2013.01); *H01L 2924/12* (2013.01); *H01L 2924/1205* (2013.01); *H01L 2924/1206* (2013.01); *H01L 2924/1427* (2013.01); *H01L 2924/1432* (2013.01); *H01L 2924/1433* (2013.01); *H01L 2924/1436* (2013.01); *H01L 2924/15192* (2013.01); *H01L 2924/15311* (2013.01); *H01L 2924/18161* (2013.01); *H01L 2924/18162* (2013.01); *H01L 2924/19041* (2013.01); *H01L 2924/19042* (2013.01); *H01L 2924/19103* (2013.01); *H01L 2924/19104* (2013.01)

(58) **Field of Classification Search**

CPC H01L 25/18; H01L 24/17; H01L 2224/12105; H01L 2224/1403; H01L 2224/16145; H01L 2224/16227; H01L 2224/16235; H01L 2224/16265; H01L 2224/1703; H01L 2224/17181; H01L 2224/24195; H01L 2924/12; H01L 2924/1205; H01L 2924/1206; H01L 2924/1427; H01L 2924/1432; H01L 2924/1433; H01L 2924/1436; H01L 2924/15192; H01L 2924/15311; H01L 2924/18161; H01L 2924/18162; H01L 2924/19041; H01L 2924/19042; H01L 2924/19103; H01L 2924/19104

See application file for complete search history.

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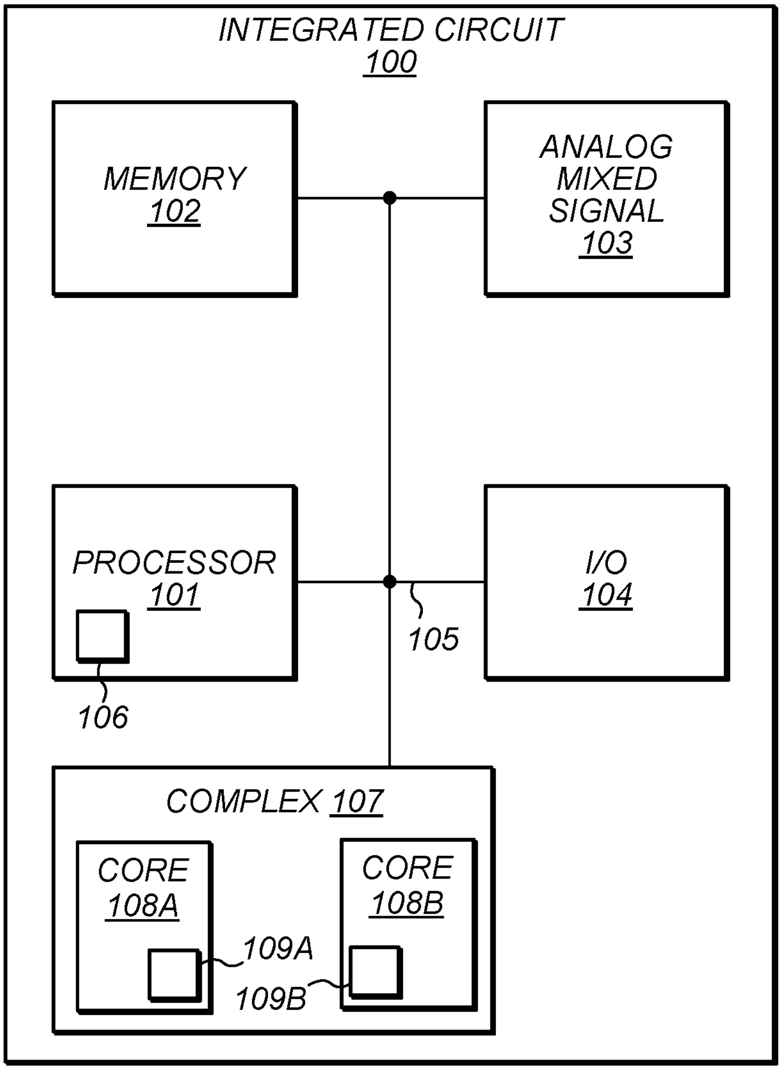
INTEGRATED CIRCUIT
100
MEMORY
102
ANALOG
MIXED
SIGNAL
103
PROCESSOR
101
106
105
I/O
104
COMPLEX 107
CORE
108A
109A
109B
CORE
108B

FIG. 1

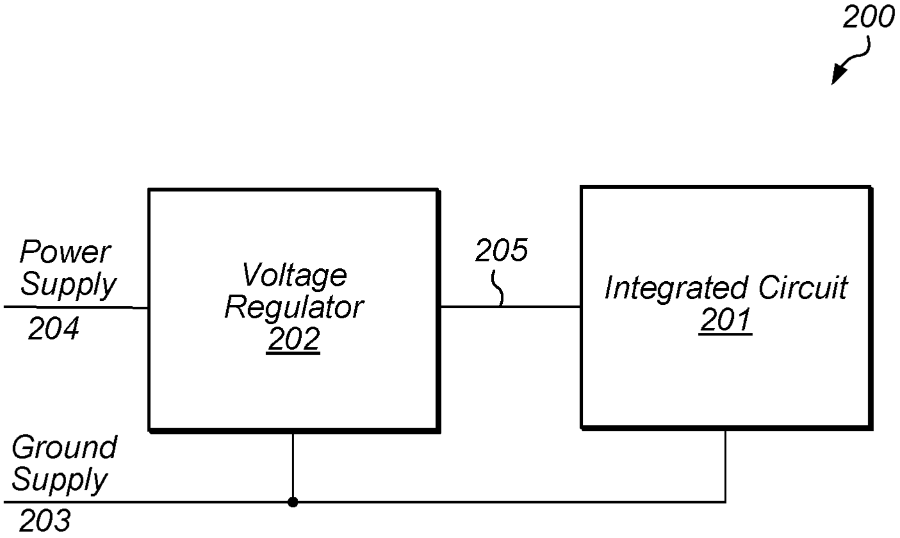
200
Power Supply
204
Voltage Regulator
202
205
Integrated Circuit
201
Ground Supply
203

FIG. 2

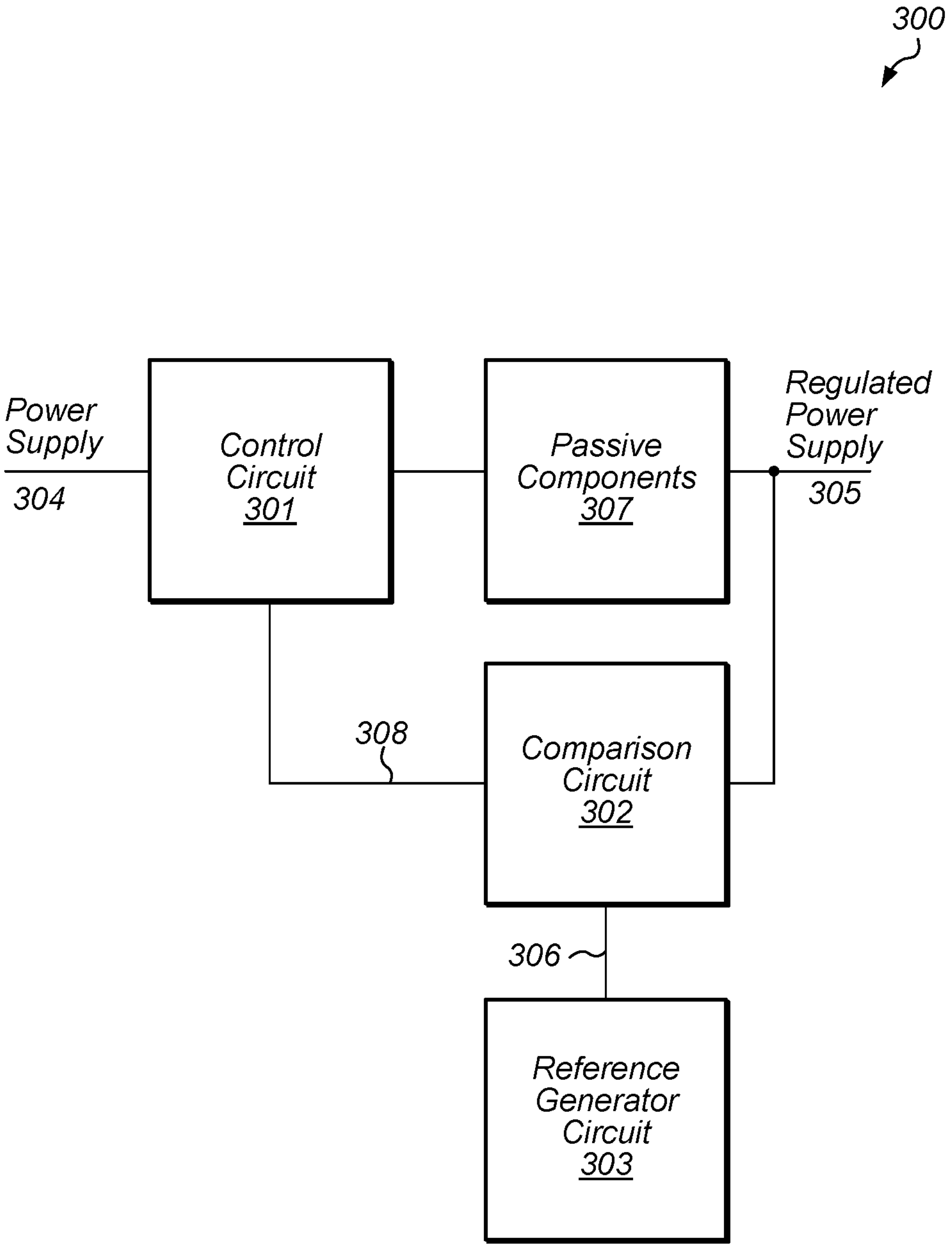
300
Power Supply
304
Control Circuit
301
Passive Components
307
Regulated Power Supply
305
308
Comparison Circuit
302
306
Reference Generator Circuit
303

FIG. 3

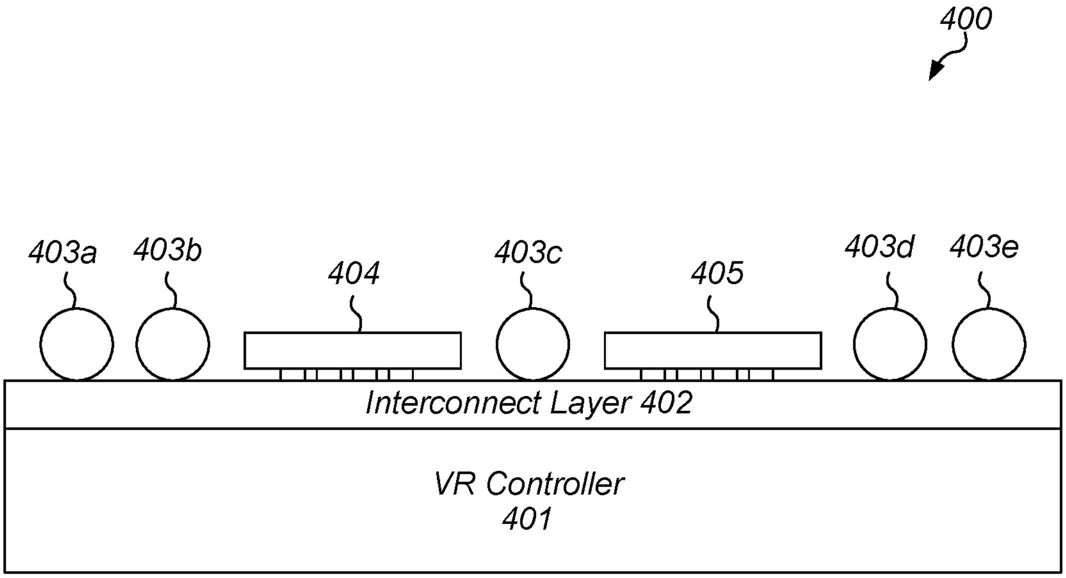
400
403a
403b
404
403c
405
403d
403e
Interconnect Layer 402
VR Controller
401

FIG. 4

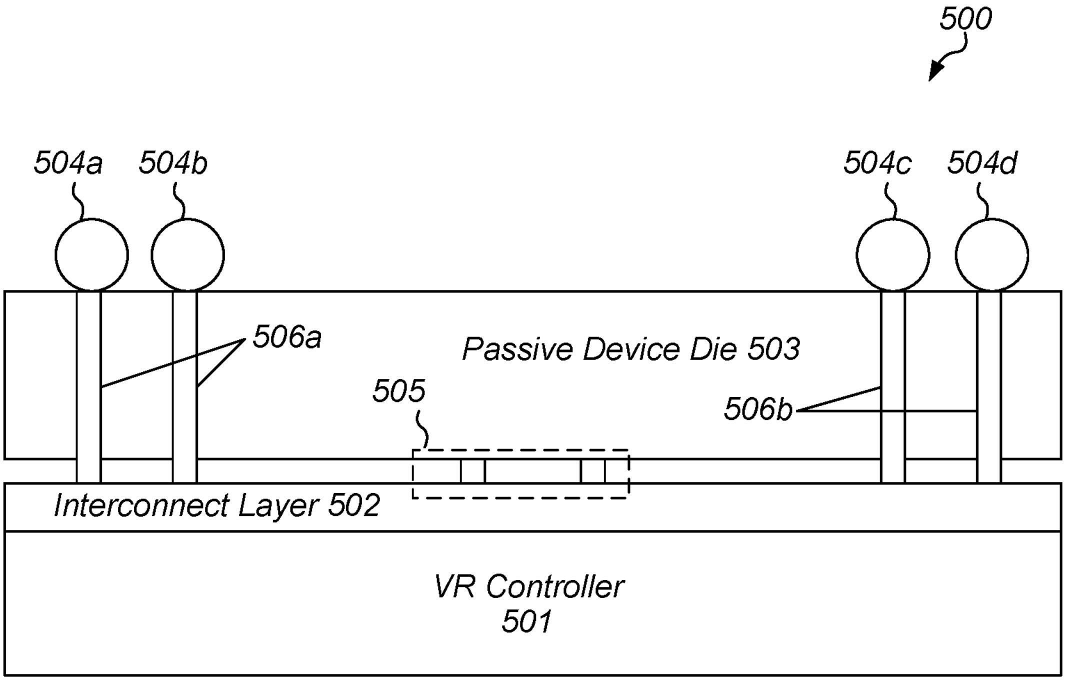
500
504a
504b
504c
504d
506a
Passive Device Die 503
505
506b
Interconnect Layer 502
VR Controller
501

FIG. 5

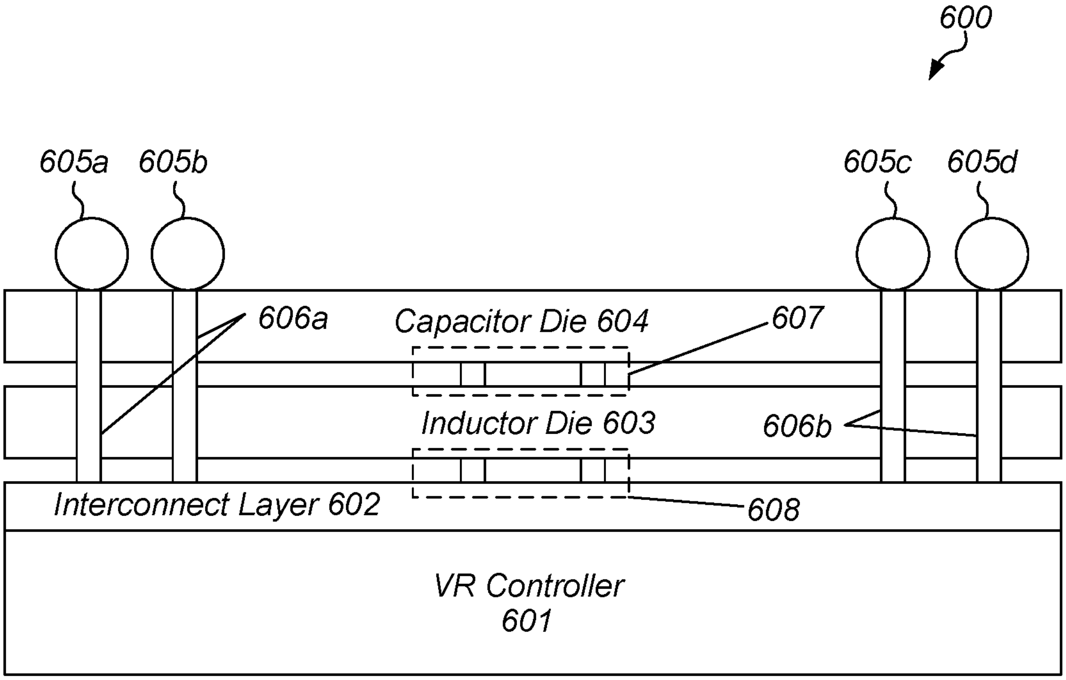
600
605a
605b
605c
605d
606a
Capacitor Die 604
607
Inductor Die 603
606b
Interconnect Layer 602
608
VR Controller
601

FIG. 6

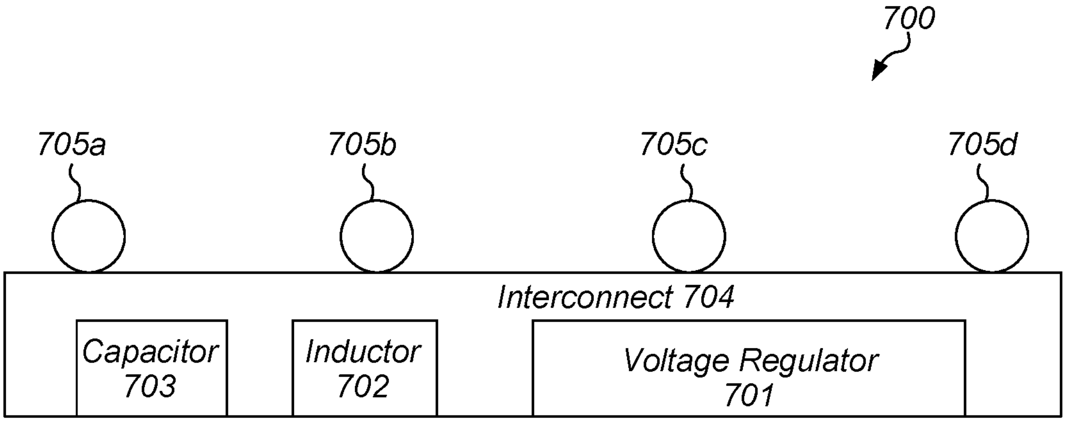
700
705a
705b
705c
705d
Interconnect 704
Capacitor 703
Inductor 702
Voltage Regulator 701

FIG. 7

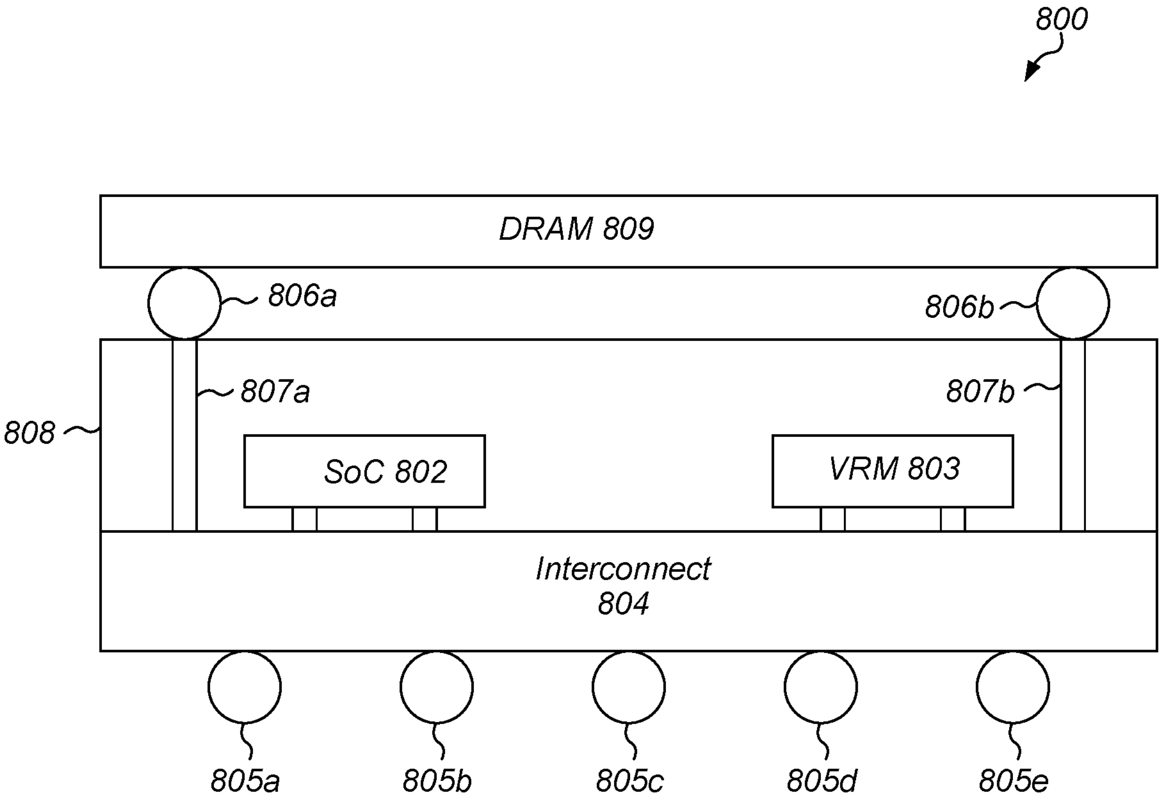
800
DRAM 809
806a
806b
807a
807b
808
SoC 802
VRM 803
Interconnect
804
805a
805b
805c
805d
805e

FIG. 8

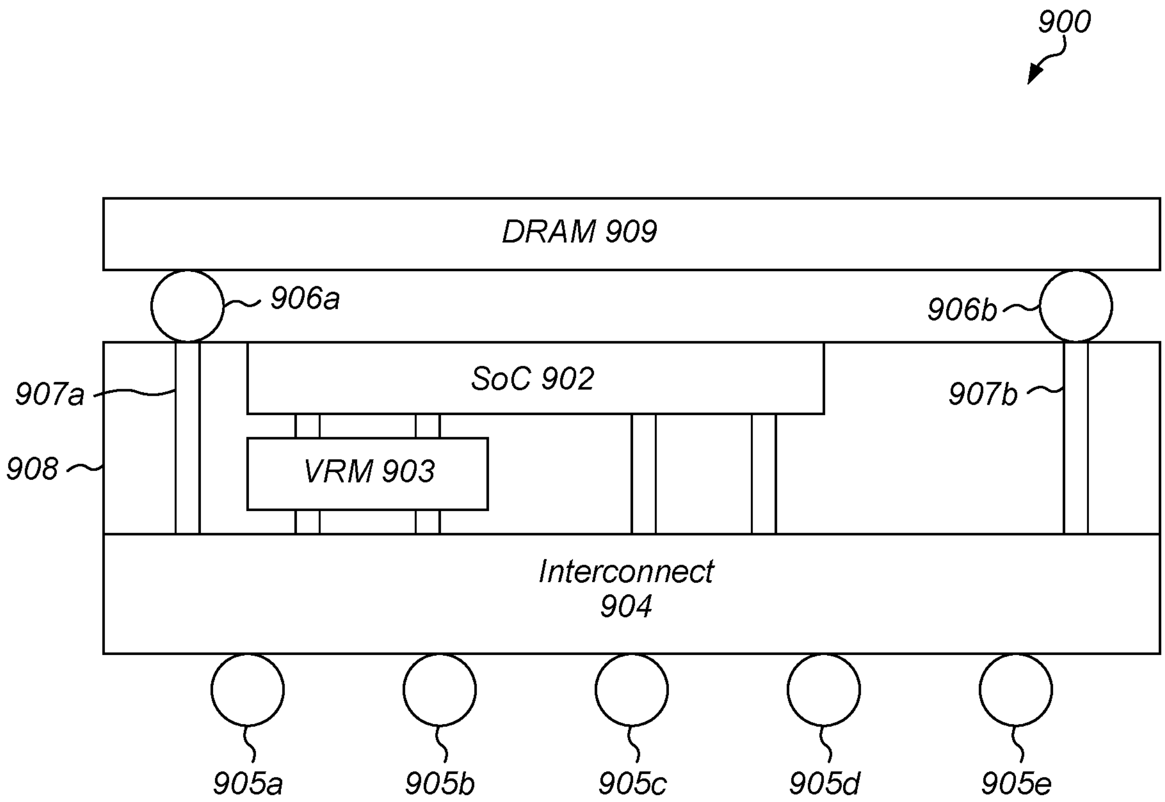
900
DRAM 909
906a
906b
907a
907b
908
SoC 902
VRM 903
Interconnect
904
905a
905b
905c
905d
905e

FIG. 9

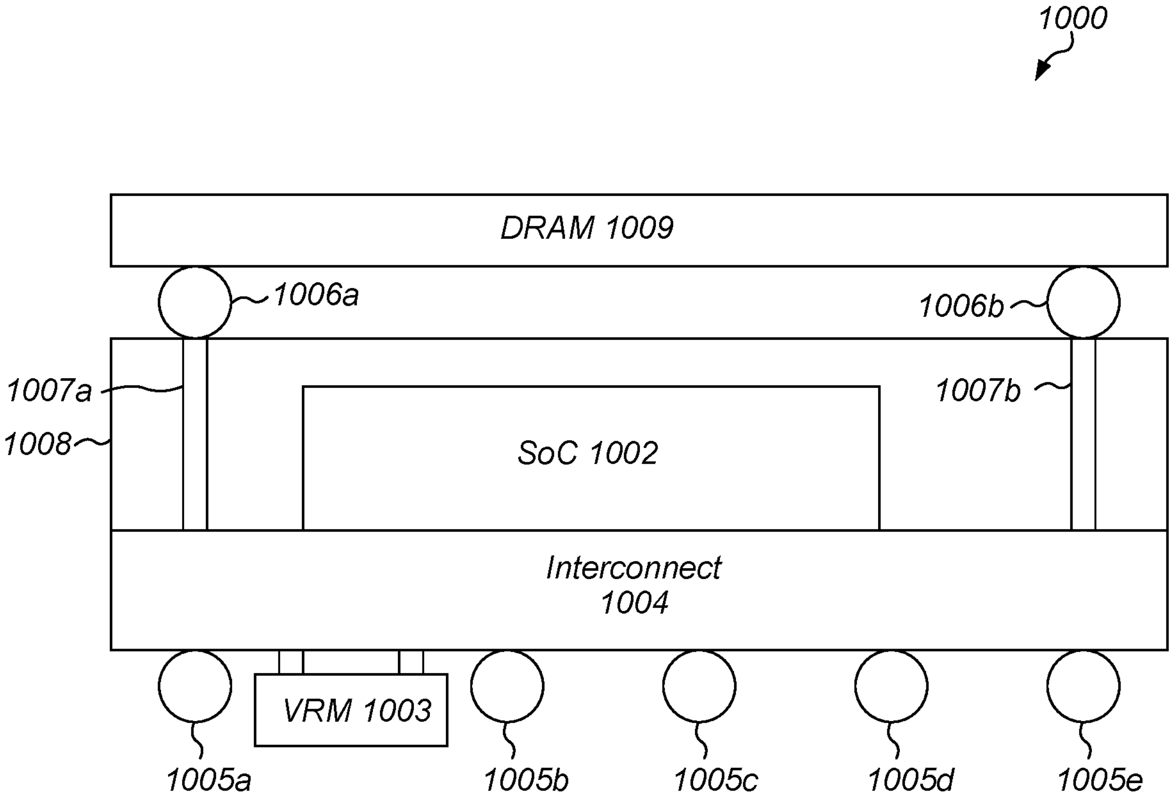
1000
DRAM 1009
1006a
1006b
1007a
1007b
1008
SoC 1002
Interconnect
1004
VRM 1003
1005a
1005b
1005c
1005d
1005e

FIG. 10

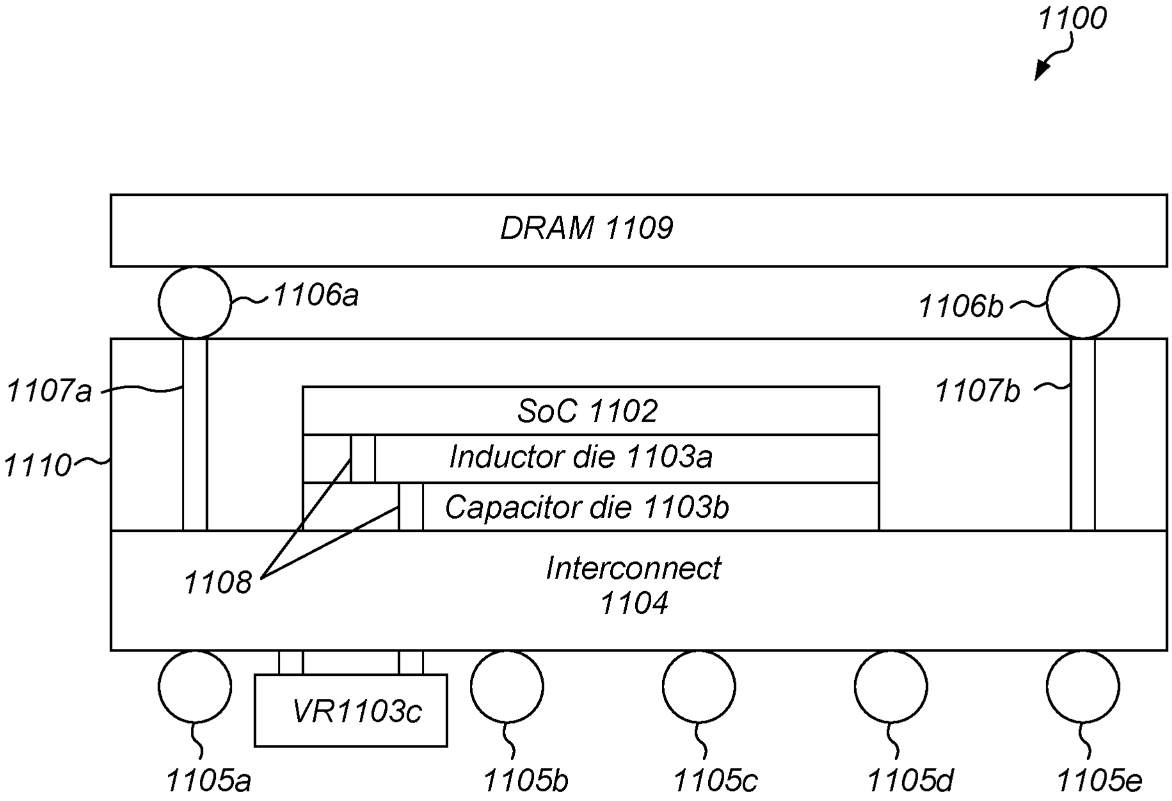
1100
DRAM 1109
1106a
1106b
1107a
1107b
1110
SoC 1102
Inductor die 1103a
Capacitor die 1103b
Interconnect
1104
1108
VR1103c
1105a
1105b
1105c
1105d
1105e

FIG. 11

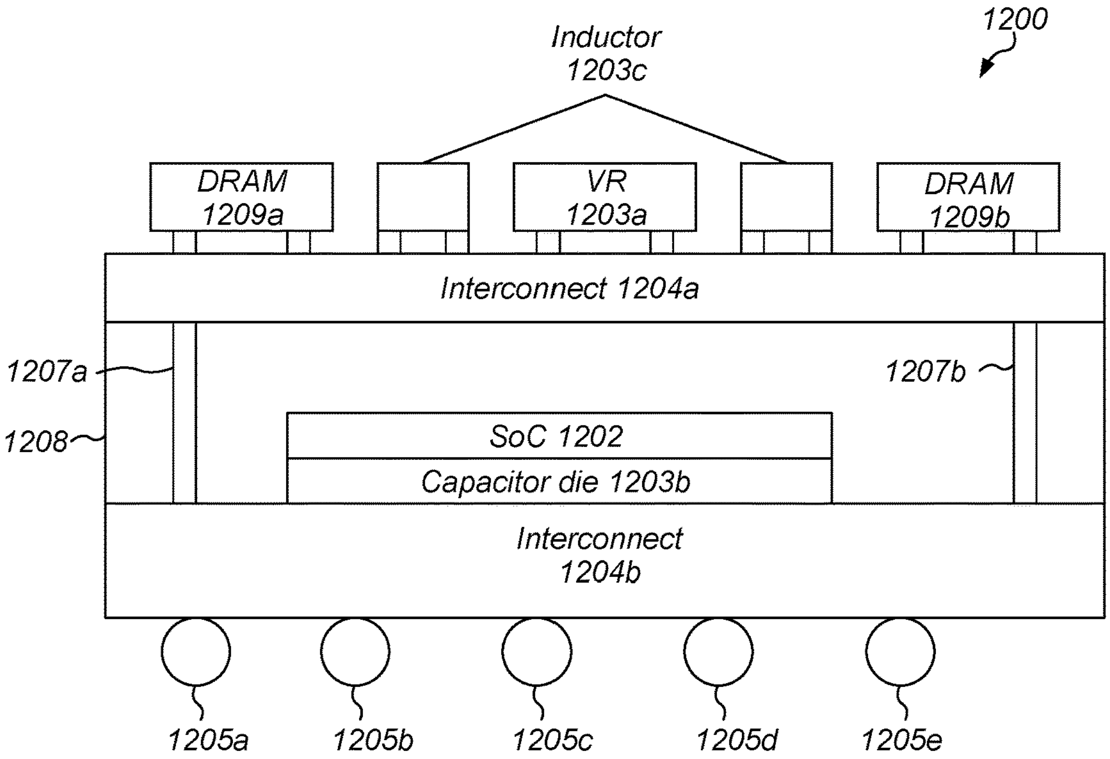

FIG. 12A

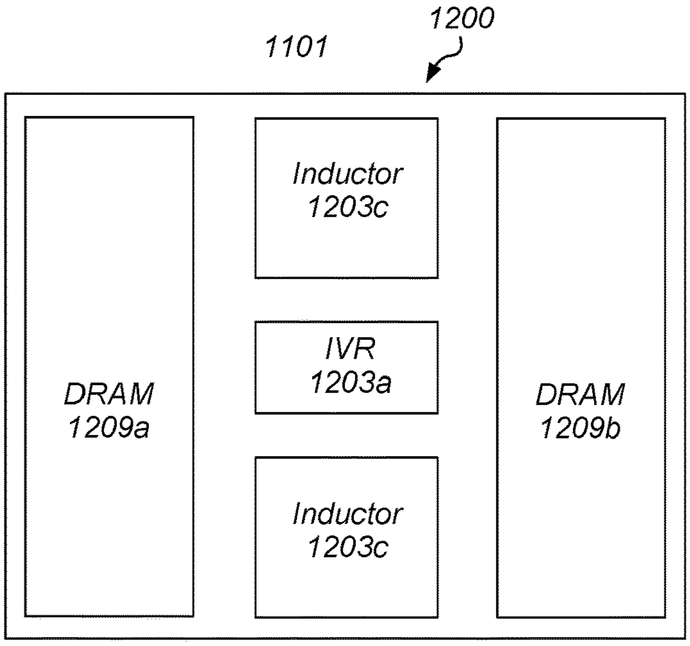

FIG. 12B

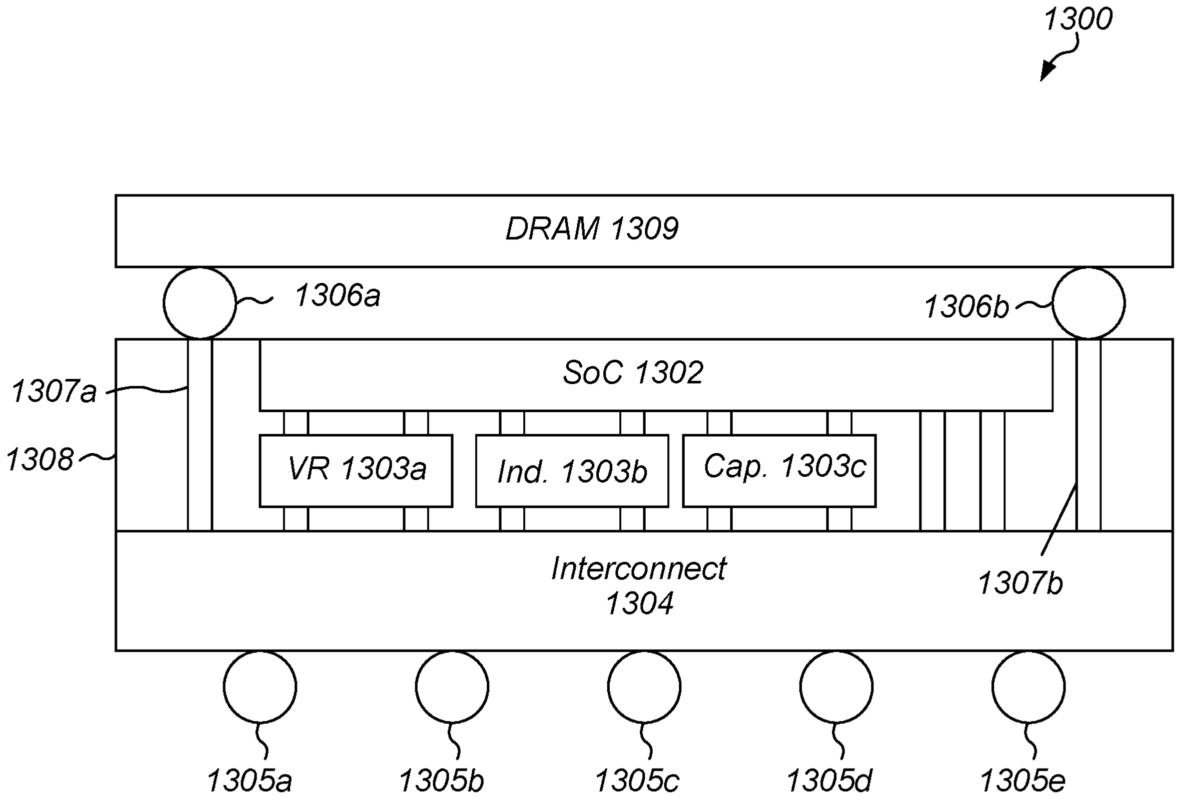
1300
DRAM 1309
1306a
1306b
1307a
1308
SoC 1302
VR 1303a
Ind. 1303b
Cap. 1303c
Interconnect
1304
1307b
1305a
1305b
1305c
1305d
1305e

FIG. 13

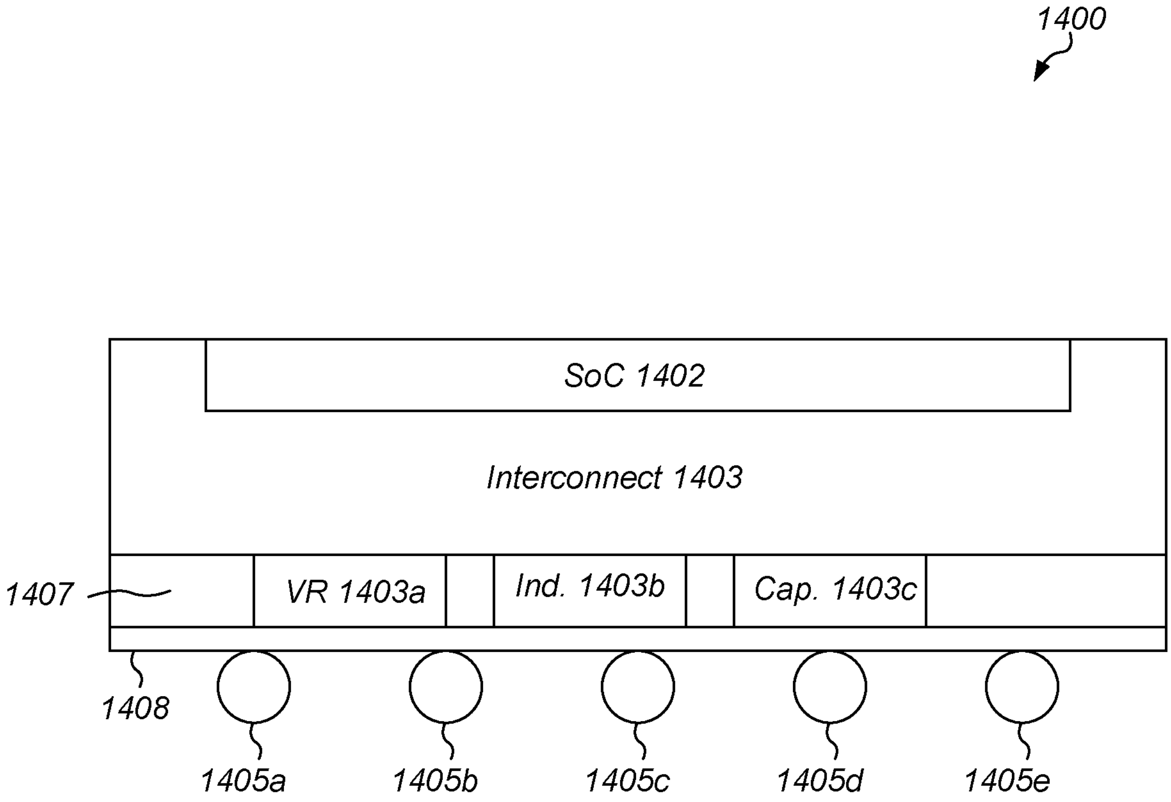
1400
SoC 1402
Interconnect 1403
1407
VR 1403a
Ind. 1403b
Cap. 1403c
1408
1405a
1405b
1405c
1405d
1405e

FIG. 14

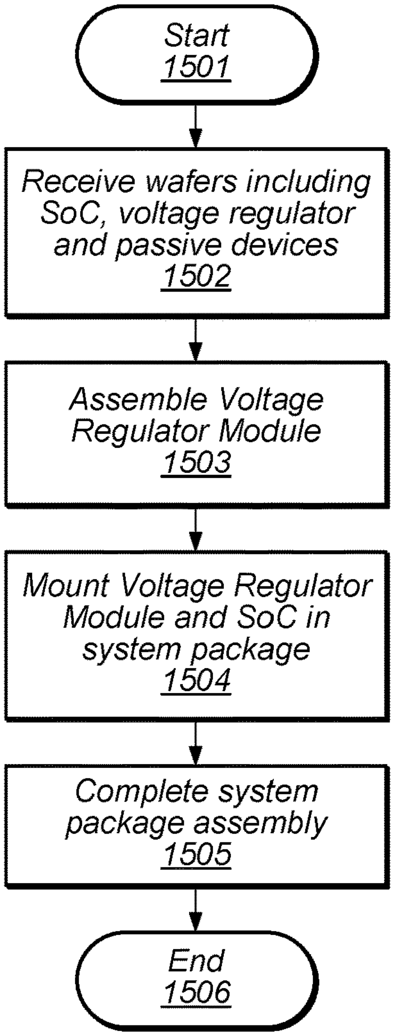
Start
1501
Receive wafers including SoC, voltage regulator and passive devices
1502
Assemble Voltage Regulator Module
1503
Mount Voltage Regulator Module and SoC in system package
1504
Complete system package assembly
1505
End
1506

FIG. 15

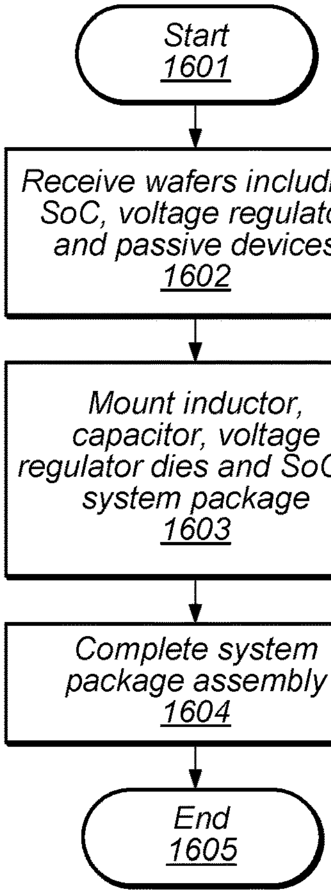
Start
1601
Receive wafers including SoC, voltage regulator and passive devices
1602
Mount inductor, capacitor, voltage regulator dies and SoC in system package
1603
Complete system package assembly
1604
End
1605

FIG. 16

STRUCTURE AND METHOD FOR FABRICATING A COMPUTING SYSTEM WITH AN INTEGRATED VOLTAGE REGULATOR MODULE

PRIORITY CLAIM

The present application is a continuation of U.S. application Ser. No. 17/080,609, entitled "Structure and Method for Fabricating a Computing System with an Integrated Voltage Regulator Module," filed Oct. 26, 2020, which is a continuation of U.S. application Ser. No. 15/943,673, entitled "Structure and Method for Fabricating a Computing System with an Integrated Voltage Regulator Module," filed Apr. 2, 2018 (now U.S. Pat. No. 10,818,632), which is a continuation of U.S. application Ser. No. 15/264,087, entitled "Structure and Method for Fabricating a Computing System with an Integrated Voltage Regulator Module," filed Sep. 13, 2016 (now U.S. Pat. No. 9,935,076), which claims priority to U.S. Provisional Appl. No. 62/234,776, entitled "Structure and Method for Fabricating a Computing System with an Integrated Voltage Regulator Module," filed Sep. 30, 2015; the disclosures of each of the above-referenced applications are incorporated by reference herein in their entireties.

BACKGROUND

Technical Field

Embodiments described herein relate to integrated circuit packages, and more particularly, to techniques for packaging voltage regulators.

Description of the Related Art

A variety of electronic devices are now in daily use with consumers. Particularly, mobile devices have become ubiquitous. Mobile devices may include cell phones, personal digital assistants (PDAs), smart phones that combine phone functionality and other computing functionality such as various PDA functionality and/or general application support, tablets, laptops, net tops, smart watches, wearable electronics, etc.

Such mobile devices may include multiple integrated circuits, each performing different tasks. In some cases, circuits that perform different tasks may be integrated into a single integrated forming a system on a chip (SoC). The different functional units within a SoC may operate at different power supply voltage levels. In some designs, power supply or regulator circuits may be included in the SoC to generate different voltage levels for the myriad functional units included in the SoC.

Voltage regulators may employ one or more passive components, such as, e.g., inductors and capacitors in order to improve performance. The fabrication of such passive components may employ different processing steps and materials than those used in manufacturing an SoC. In such cases, the passive components may be manufactured separately from the SoC.

SUMMARY OF THE EMBODIMENTS

Various embodiments of a system package are disclosed. Broadly speaking, a system is contemplated in which a module includes one or more passive circuit elements, an interconnect region, and a voltage regulator controller die configured to generate a regulated power supply using the one or more passive circuit elements. The interconnect region may include a plurality of conductive paths, and each conductive path may include a plurality of wires fabricated on a plurality of conductive layers. The voltage regulator controller die may include a plurality of terminals, and a first subset of the plurality of terminals may be coupled to respective terminals of a given passive circuit element via a first subset of the plurality of conductive paths. Each terminal of a second subset of the plurality of terminals may be coupled to respective solder balls of a plurality of solder balls via a given path of a second subset of the plurality of conductive paths.

In one embodiment, each of the one or more passive circuit elements includes at least one inductor and one capacitor.

In a further embodiment, the at least one inductor is included in a first integrated circuit die, and the at least one capacitor is included in a second integrated circuit die.

BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description makes reference to the accompanying drawings, which are now briefly described.

FIG. **1** illustrates an embodiment of an integrated circuit.

FIG. **2** illustrates an embodiment of a computing system employing a voltage regulator.

FIG. **3** illustrates a block diagram depicting an embodiment of a voltage regulator.

FIG. **4** illustrates an embodiment of a voltage regulator module.

FIG. **5** illustrates an embodiment of a voltage regulator module.

FIG. **6** illustrates an embodiment of a voltage regulator module.

FIG. **7** illustrates an embodiment of a voltage regulator module.

FIG. **8** illustrates an embodiment of a system package.

FIG. **9** illustrated an embodiment of a system package.

FIG. **10** illustrates an embodiment of a system package.

FIG. **11** illustrates an embodiment of a system package.

FIG. **12**A illustrates an embodiment of a system package.

FIG. **12**B illustrates a top view of the embodiment depicted in FIG. **12**A.

FIG. **13** illustrates an embodiment of a system package.

FIG. **14** illustrates an embodiment of a system package.

FIG. **15** illustrates a flow diagram depicting an embodiment of a method for assembling a system package.

FIG. **16** illustrates a flow diagram depicting another embodiment of a method for assembling a system package.

While the disclosure is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the disclosure to the particular form illustrated, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present disclosure as defined by the appended claims. The headings used herein are for organizational purposes only and are not meant to be used to limit the scope of the description. As used throughout this application, the word "may" is used in a permissive sense (i.e., meaning having the potential to), rather than the mandatory sense (i.e., meaning must). Similarly, the words "include," "including," and "includes" mean including, but not limited to.

Various units, circuits, or other components may be described as "configured to" perform a task or tasks. In such contexts, "configured to" is a broad recitation of structure generally meaning "having circuitry that" performs the task or tasks during operation. As such, the unit/circuit/component can be configured to perform the task even when the unit/circuit/component is not currently on. In general, the circuitry that forms the structure corresponding to "configured to" may include hardware circuits. Similarly, various units/circuits/components may be described as performing a task or tasks, for convenience in the description. Such descriptions should be interpreted as including the phrase "configured to." Reciting a unit/circuit/component that is configured to perform one or more tasks is expressly intended not to invoke 35 U.S.C. § 112, paragraph (f) interpretation for that unit/circuit/component. More generally, the recitation of any element is expressly intended not to invoke 35 U.S.C. § 112, paragraph (f) interpretation for that element unless the language "means for" or "step for" is specifically recited.

DETAILED DESCRIPTION OF EMBODIMENTS

In a computing system, it may be desirable to operate different functional units of a System-on-a-chip (SoC) at different power supply voltages. In some cases, the computing system that includes such an SoC may only receive a particular power supply voltage from a battery or other suitable DC power supply. In order to generate the desired power supply voltage levels, a voltage regulator circuit may be employed.

Voltage regulator circuit may be designed according to one of various design styles. In some cases, passive components, such as, e.g., inductors and capacitors, are employed to improve the efficiency of voltage regulator circuits.

A manufacturing process used to fabricate voltage regulator circuits or SoCs may not be well suited for fabricating inductors and capacitors. As such, in some cases, inductors and capacitors to be used with voltage regulator circuits may be fabricated separately from the voltage regulator circuits and SoCs, and the mounted on a common circuit board or other suitable medium.

In small form factor applications, such as, e.g., mobile computing devices, reduced footprint assemblies of the voltage regulator circuit, SoC, and passive devices may be desirable. The embodiments illustrated in the drawings and described below may provide techniques assembling voltage regulator circuits, their related passive circuit elements, and other integrated circuits in a common system package while minimizing the package footprint.

A block diagram of an integrated circuit including multiple functional units is illustrated in FIG. **1**. In the illustrated embodiment, the integrated circuit **100** includes a processor **101**, and a processor complex (or simply a "complex") **107** coupled to memory block **102**, and analog/mixed-signal block **103**, and I/O block **104** through internal bus **105**. In various embodiments, integrated circuit **100** may be configured for use in a desktop computer, server, or in a mobile computing application such as, e.g., a tablet or laptop computer.

As described below in more detail, processor **101** may, in various embodiments, be representative of a general-purpose processor that performs computational operations. For example, processor **101** may be a central processing unit (CPU) such as a microprocessor, a microcontroller, an application-specific integrated circuit (ASIC), or a field-programmable gate array (FPGA). In some embodiments, processor **101** may include one or more energy modeling units **106** which may be configured to estimate both dynamic and leakage power consumption on a cycle and execution thread basis. In other embodiments, any functional unit, such as, e.g., I/O block **104**, may include an energy modeling unit.

Complex **107** includes processor cores **108**A and **108**B. Each of processor cores **108**A and **108**B may be representative of a general-purpose processor configured to execute software instructions in order to perform one or more computational operations. Processor cores **108**A and **108**B may be designed in accordance with one of various design styles. For example, processor cores **108**A and **108**B may be implemented as an ASIC, FPGA, or any other suitable processor design. Each of processor cores **108**A and **108**B may, in various embodiments, include energy modeling units **109**A and **109**B, respectively. Energy modeling units **109**A and **109**B may each monitor energy usage within their respective processor cores thereby allowing, in some embodiments, accounting of energy associated with a given process being executed across multiple processor cores.

Memory block **102** may include any suitable type of memory such as a Dynamic Random Access Memory (DRAM), a Static Random Access Memory (SRAM), a Read-only Memory (ROM), Electrically Erasable Programmable Read-only Memory (EEPROM), or a non-volatile memory, for example. It is noted that in the embodiment of an integrated circuit illustrated in FIG. **1**, a single memory block is depicted. In other embodiments, any suitable number of memory blocks may be employed.

Analog/mixed-signal block **103** may include a variety of circuits including, for example, a crystal oscillator, a phase-locked loop (PLL), an analog-to-digital converter (ADC), and a digital-to-analog converter (DAC) (all not shown). In other embodiments, analog/mixed-signal block **103** may be configured to perform power management tasks with the inclusion of on-chip power supplies and voltage regulators. Analog/mixed-signal block **103** may also include, in some embodiments, radio frequency (RF) circuits that may be configured for operation with wireless networks.

I/O block **104** may be configured to coordinate data transfer between integrated circuit **100** and one or more peripheral devices. Such peripheral devices may include, without limitation, storage devices (e.g., magnetic or optical media-based storage devices including hard drives, tape drives, CD drives, DVD drives, etc.), audio processing subsystems, or any other suitable type of peripheral devices. In some embodiments, I/O block **104** may be configured to implement a version of Universal Serial Bus (USB) protocol or IEEE 1394 (Firewire®) protocol.

I/O block **104** may also be configured to coordinate data transfer between integrated circuit **100** and one or more devices (e.g., other computer systems or integrated circuits) coupled to integrated circuit **100** via a network. In one embodiment, I/O block **104** may be configured to perform the data processing necessary to implement an Ethernet (IEEE 802.3) networking standard such as Gigabit Ethernet or 10-Gigabit Ethernet, for example, although it is contemplated that any suitable networking standard may be implemented. In some embodiments, I/O block **104** may be configured to implement multiple discrete network interface ports.

In some embodiments, each of the aforementioned functional units may include multiple circuits, each of which may include multiple devices, such as, e.g., metal-oxide semiconductor field-effect transistors (MOSFETs) connected via multiple wires fabricated on multiple conductive layers. The conductive layers may be interspersed with insulating layers, such as, silicon dioxide, for example. Each circuit may also contain wiring, fabricated on the conductive layers, designated for a power supply net or a ground supply net.

Integrated circuit **100** may, in various embodiments, be fabricated on a silicon wafer (or simply "wafer") along with numerous identical copies of integrated circuit **100**, each of which may be referred to as a "chip" or "die." During manufacture, various manufacturing steps may be performed on each chip in parallel. Once the manufacturing process has been completed, the individual chips may be removed from the wafer by cutting or slicing through unused areas between each chip.

It is noted that the embodiment illustrated in FIG. **1** is merely an example. In other embodiments, different functional units, and different arrangements of functional units may be employed.

Turning now to FIG. **2**, an embodiment of a computing system that includes a voltage regulator is illustrated. In the illustrated embodiment, computing system **200** includes voltage regulator **202**, which is coupled to integrated circuit **201** via regulated power supply **205**. Each of voltage regulator **202** and integrated circuit **201** is coupled to ground supply **203**, and voltage regulator **202** is further coupled to power supply **204**. In various embodiments, integrated circuit **201** may correspond to integrated circuit **100** as illustrated in FIG. **1**.

During operation, voltage regulator **202** may generate a voltage level on regulated supply **205**. Depending on integrated circuit **201**, the voltage level of regulated supply **205** may be higher or lower than the voltage level on power supply **204**. The voltage level on regulated supply **205** may vary within predetermined limits from a desired voltage level. The variation may result from changes in the voltage level on power supply **204**, variations in temperature, or changes in current demand from integrated circuit **201**. Although only a single regulated power supply is depicted in the embodiment illustrated in FIG. **2**, in other embodiments, voltage regulator **202** may be configured to generate multiple regulated power supplied.

Voltage regulator **202** may be designed in accordance with one of varying design styles. In some embodiments, voltage regulator **202** may employ a combination of active and passive devices (not shown). Such passive devices may, in some embodiments, include any suitable combination of inductors and capacitors. In various embodiments, integrated circuit **201** and voltage regulator may be fabricated using different semiconductor manufacturing processes, and may be mounted in a common integrated circuit package or mounted on a common substrate.

It is noted that the embodiment illustrated in FIG. **2** is merely an example. In other embodiments, different numbers of integrated circuits, and different numbers of voltage regulators providing different voltages levels are possible and contemplated.

A block diagram of an embodiment of a voltage regulator unit is illustrated in FIG. **3**. In the illustrated embodiment, voltage regulator **300** includes control circuit **301**, passive components **307**, comparison circuit **302**, and reference generator circuit **303**. In various embodiments, voltage regulator **300** may correspond to voltage regulator **200** as depicted in FIG. **2**. Each of control circuit **301**, comparison circuit **302**, reference generator circuit **303**, and passive components **307** may be mounted together on a single substrate. In some embodiments, control circuit **301**, comparison circuit **302**, and reference generator circuit **303** may be fabricated together on a common integrated circuit or other suitable substrate compatible with a semiconductor manufacturing process.

Control circuit **301** may be configured to receive power supply **304**, and source current to regulator power supply **305** through passive components **307** dependent on control signal **308**. In various embodiments, control circuit **301** may include multiple metal-oxide semiconductor field-effect transistors (MOSFETs) or other suitable transconductance devices capable of selectively applying current to regulated power supply **305**. Passive components **307** may, in some embodiments, include one or more inductors, and one or more capacitors, or any other suitable passive component. In various embodiments, the components included in passive components **307** may be fabricated together on a single silicon substrate, or they may be manufactured on separate silicon substrates using different semiconductor manufacturing processes.

Comparison circuit **302** may, in various embodiments, be configured to compare a voltage level on regulated power supply **305** and a voltage level on reference voltage **306**. In response to the comparison, comparison circuit **302** may adjust a voltage level on control signal **308**. In some embodiments, control signal **308** may switch between multiple discrete voltage levels, each of which represents a logic level. Alternatively, control signal **308** may be an analog signal, which may assume a continuous spectrum of voltage levels.

In various embodiments, reference generator circuit **303** may be configured to generate a voltage level on reference voltage **306** dependent on the voltage level on power supply **304**. The voltage level on reference voltage **306** may, in some embodiments, correspond to a desired voltage level for an integrated circuit, such as integrated circuit **100** as illustrated in FIG. **1**, for example. In some embodiments, reference generator circuit **303** may include one or more sub-circuits (not shown), such as, band gap reference circuits, current mirrors, and the like.

The embodiment illustrated in FIG. **3** is merely an example. In other embodiments, different functional units and different circuit topologies may be employed.

Turning to FIG. **4**, an embodiment of a voltage regulator module (VRM) is illustrated. In the illustrated embodiment, VRM **400** includes VR Controller **401**, interconnect layer **402**, inductor **404**, and capacitor **405**. In various embodiments, VR Controller **401** may correspond to portions of voltage regulator **300**, namely control circuit **301**, comparison circuit **302**, and reference generator **303**.

Interconnect layer **402** is coupled to the top of VR Controller **401**. In various embodiments, interconnect layer **402** may include multiple wires fabricated on multiple conductive layers included within interconnect layer **402**. Such wires may provide routing paths from signal and power terminals on VR Controller **401** to solder bumps **403***a*-**403***e*, and terminals on inductor **404** and capacitor **403**. In some embodiments, interconnect layer **402** may be fabricated onto VR Controller **401** using a wafer scale packaging process or other suitable assembly process. As used and described herein, a signal terminal may refer to a terminal on an integrated circuit, passive device, or interconnect layer or region, through which an electrical signal may be transmitted. Such an electrical signal may include either analog or digital signals. Additionally, a power terminal, as used and described herein, may refer to a terminal on an integrated circuit, passive device, or interconnect layer or region dedicated to power supply or ground supply connections.

In various embodiments, inductor **404** and capacitor **405** may be fabricated on a silicon or other suitable substrate using a semiconductor manufacturing process. Alternatively, or additionally, inductor **404** and capacitor **405** may be discrete components manufactured using any suitable manufacturing process.

It is noted that the embodiment illustrated in FIG. **4** is merely an example. In other embodiments, different number of inductors and capacitors, and different arrangements of the inductors and capacitors are possible and contemplated.

A different embodiment of a VRM is depicted in FIG. **5**. In the illustrated embodiment, VRM **500** includes VR Controller **501**, interconnect layer **502**, and passive device die **503**. In various embodiments, VR Controller **501** and interconnect layer **502** may correspond to VR Controller **401** and interconnect layer **402**, respectively, as depicted in the embodiment illustrated in FIG. **4**.

Passive device die **503** may, in various embodiments, include one or more inductors and capacitors, and may be manufactured using a semiconductor manufacturing process. During manufacture, connection paths **506***a* and **506***b* (also referred to herein as "vias" or "through silicon vias") are created in passive device die **503** to allow connections from solder bumps **504***a*-**504***d* to terminals on interconnect layer **502**, which, in turn, are coupled to terminals on VR controller **501**. The passive devices included in passive device die **503** may be coupled to circuitry included in VR Controller **501** through connectors **505**. In various embodiments, connectors **505** may be solder bumps or any other medium suitable for coupling passive device die **503** to VR controller **501**.

The embodiment illustrated in FIG. **5** is a particular example of a VRM. In other embodiments, different numbers of vias and connectors may be employed.

Turning to FIG. **6**, another embodiment of a VRM is illustrated. In the illustrated embodiment, VRM **600** includes VR Controller **601**, inductor die **603**, and capacitor die **604**. In various embodiments, VR Controller **601** may correspond to VR Controller **401** as depicted in the embodiment illustrated in FIG. **4**.

Capacitor die **604** may include one or more capacitors, and inductor die **603** may include one or more inductors. Capacitor die **604** and inductor die **603** may be manufactured using respective semiconductor manufacturing processes. Each of capacitor die **640** and inductor die **603** include routing paths through the die that form vias **606***a* and **606***b*, thereby allowing connects from solder bumps **605***a*-**605***d* to terminals on interconnect layer **602**. In various embodiments, interconnect layer **602** may include multiple wires fabricated on multiple conductor layers forming connections between terminals on VR Controller **601** and terminals on interconnect layer **602**.

Terminals on capacitor die **604** are coupled to a first set of terminals on inductor die **603** via connectors **607**. Additionally, a second set of terminals on inductor die **603** are coupled to terminals on interconnect layer **602** via connectors **608**. In various embodiments, connectors **607** and **608** may include solder bumps or any other suitable medium. In some embodiments, space between capacitor die **604** and inductor die **603** may be filled with an electrically insulating material (not shown), such as, silicon dioxide, for example. In a similar fashion, space between inductor die **603** and interconnect layer **602** may also be filled with the insulating material.

It is noted that the embodiment depicted in FIG. **6** is merely an example. In other embodiments, different arrangements of the inductor and capacitor dies may be employed.

A different embodiment of a VRM is illustrated in FIG. **7**. In the illustrated embodiment, VRM **700** includes voltage regulator **701**, inductor **702**, and capacitor **703**. In various embodiments, voltage regulator **701** may correspond to VR Controller **401** as illustrated in the embodiment of FIG. **4**. In some embodiments, each of voltage regulator **701**, inductor **702**, and capacitor **703** may be chips or dies manufactured using respective semiconductor manufacturing processes.

Voltage regulator **701**, inductor **702**, and capacitor **703** may be arranged in a planar fashion. Interconnect **704** may be fabricated or assembled on top of the arrangement of voltage regulator **701**, inductor **702**, and capacitor **703**. In various embodiments, interconnect **704** may include multiple wires (not shown), fabricated on multiple metal layers separated by multiple insulating layers, that connect terminals of voltage regulator **701** to terminals on inductor **702** and capacitor **703**. Additionally, some of the multiple wires included in interconnect **704** may couple terminals of voltage regulator **701** to solder bumps **705***a*-**705***d*.

The embodiment illustrated in FIG. **7** is merely an example. In other embodiments, different arrangements of voltage regulator **701**, inductor **702**, and capacitor **703** are possible and contemplated.

To reduce parasitic circuit effects in connections between voltage regulators and SoCs, VRMs and SoCs may be mounted in a common package, commonly referred to as a "system package." An embodiment of a system package is illustrated in FIG. **8**. In the illustrated embodiments, system package **800** includes interconnect **804**, SoC **802**, and VRM **803**. In various embodiments, VRM **803** may correspond to any of the embodiments illustrated in FIG. **4** through FIG. **7**, and SoC **802** may correspond integrated circuit **100** as illustrated in FIG. **1**.

Each of SoC **802** and VRM **803** are coupled to interconnect **804**. In various embodiments, interconnect **804** includes multiple wires fabricated on multiple wiring layers. Some of the multiple wires of interconnect **804** may couple terminals on SoC **802** to terminals on VRM **803**, thereby allowing a regulated power supply from VRM **803** to be coupled to SoC **802**. Additionally, some of the multiple wires included in interconnect **804** may couple terminals on SoC **802** and VRM **803** to solder bumps **805***a*-**805***e*.

On a side of the package body **808** opposite from solder bumps **805***a*-**805***e*, solder bumps **806***a*-*b* couple DRAM **809** to package body **808**. In various embodiments, package body **808** includes vias **807***a*-*b* that couple solder bumps **806***a*-*b* to terminals on interconnect **804**. Wires included in interconnect **804** may then connect the aforementioned terminals of interconnect **804** to terminals of SoC **802**. Although a DRAM is included in system package **800**, in other embodiments, any suitable memory may be employed.

It is noted that the embodiment illustrated in FIG. **8** is merely an example. In other embodiments, chips or dies other than SoC **802** and VRM **803** may be included in system package **800**.

Turning to FIG. **9**, another embodiment of a system package is illustrated. In the illustrated embodiment, system package **900** includes interconnect **904**, VRM **903**, and SoC **902**. In various embodiments, VRM **903** may correspond to any of the embodiments illustrated in FIG. **4** through FIG. **7**, and SoC **902** may correspond integrated circuit **100** as illustrated in FIG. **1**.

Interconnect **904** includes multiple wires fabricated on multiple wiring layers. Some of the multiple wires of interconnect **904** may couple terminals on SoC **902** and VRM **903**, to solder bumps **905***a*-**905***e*. In contrast to the embodiment depicted in FIG. **8**, some power terminals of SoC **902** are coupled directly to output terminals of VRM **903**, allowing VRM **903** to provide a regulated power supply to SoC **902**.

In a similar fashion to the embodiment of FIG. **8**, DRAM **909** is mounted to package body **908** allowing connections to terminals on interconnect **904**. Wires included in interconnect **904** may couple vias **907***a-b* to terminals of SoC **902**. As noted above, in regard to FIG. **8**, DRAM **909** may, in other embodiments, include as any suitable type of memory.

It is noted that the embodiment illustrated in FIG. **9** is merely an example. In other embodiments, different arrangements of VRM **903** and SoC **902** may be employed.

A different embodiment of a system package is illustrated in FIG. **10**. In the illustrated embodiment, system package **1000** includes interconnect **1004**, SoC **1002**, and VRM **1003**. In various embodiments, VRM **1003** may correspond to any of the embodiments depicted in FIG. **4** through FIG. **7**, and SoC **1002** may correspond to integrated circuit **100** as illustrated in the embodiment of FIG. **1**.

Terminals of SoC **1002** are coupled to terminals of interconnect **1004**, which are, in turn, coupled to wires included interconnect **1004**. In various embodiments, the wires included in interconnect **1004** may be fabricated on multiple metal layers separated by insulating layers. Some of the wires included in interconnect **1004** may be coupled to solder bumps **1005***a-e*, thereby allowing connections from SoC **1002** to solder bumps **1005***a-e*.

In contrast to the embodiment depicted in FIG. **9**, VRM **1003** is mounted on a side of interconnect **1004** opposite the side on which SoC **1002** is mounted. Some of the wires included in interconnect **1004** may couple output terminals of VRM **1003** to power terminals of SoC **1002**, thereby allowing VRM **1003** to source a regulated power supply to SoC **1002**. Other wires included in interconnect **1004** may connect power terminals of VRM **1003** to one or more of solder bumps **1005***a-e*, providing power and ground paths to VRM **1003**.

DRAM **1009** is coupled to package body **1008** using solder bumps **1006***a-b*. Vias **1007***a-b* couple solder bumps **1006***a-b* to terminals on interconnect **1004**. Wires included in interconnect **1004** may couple the aforementioned terminals on interconnect **1004** to terminals on SoC **1002**. In some embodiments, the terminals on interconnect **1004** coupled to vias **1007***a-b* may be coupled one or more of solder bumps **1005***a-b*.

It is noted that the relative placement between SoC **1002** and VRM **1003** as depicted in the embodiment of FIG. **10** is merely an example.

Turning to FIG. **11**, a different embodiment of a system package is illustrated. In the illustrated embodiment, system package **1100** includes SoC **1102**, VR **1103***c*, inductor die **103***a*, and capacitor die **1103***b*. In various embodiments, voltage regulator (also referred to herein as "VR") **1103***c* may correspond to portions of voltage regulator **300**, namely control circuit **301**, comparison circuit **302**, and reference generator circuit **303** as illustrated in FIG. **3**, and SoC **1102** may correspond to integrated circuit **100** as illustrated in FIG. **1**.

Capacitor die **1103***b*, inductor die **1103***a*, and SoC **1102** are arranged in a stack and mounted on interconnect **1104**. In various embodiments, inductor die **1103***a* and capacitor die **1103***b* may include vias that allow terminals on SoC **1102** to be coupled to terminals of interconnect **1104** through inductor die **1103***a* and capacitor die **1103***b*. It is noted that, in various embodiments, inductor die **1103***a* may include multiple inductors fabricated using a semiconductor manufacturing process, and capacitor die **1103***b* may include multiple capacitors fabricated using a similar semiconductor manufacturing process.

Package body **1110** includes vias **1107***a-b*, which couple solder bumps **1106***a-b* to terminals on interconnect **1104**. Wires included in interconnect **1104** may be used to connect terminals on interconnect **1104**, which are coupled to vias **1107***a-b*, to vias through inductor die **1103***a* and capacitor die **1103***b*, thereby allowing a signal path from DRAM **1109** to SoC **1102**. Other wires included in interconnect **1104** may provide a path from terminals on SoC **1102**, through inductor die **1103***a* and capacitor die **1103***b*, to solder bumps **1105***a-e*. It is noted that although a single DRAM is depicted in the embodiment of FIG. **11**, in other embodiments, any suitable number and type of memory devices, may be employed.

VR **1103***c* may be mounted on a side of interconnect **1104** opposite of a side where SoC **1102**, inductor die **1103***a*, and capacitor die **1103***b* are mounted. Wires included in interconnect **1104** may couple input/output terminals of VR **1103***c* to capacitor die **1103***b*. Vias included in inductor die **1103***a* and capacitor die **1103***b* may provide a wiring path from VR **1103***c* to SoC **1102**, allowing VR **1103***c* to source a regulated power supply voltage to SoC **1102**.

Although a particular arrangement of SoC **1102**, inductor die **1103***a*, and capacitor die **1103***b* is depicted in the embodiment of FIG. **11**, it is noted that the present embodiment is merely an example. In other embodiments, different arrangements of SoC **1102**, inductor die **1103***a*, and capacitor die **1103***b* are possible and contemplated.

A different embodiment of a system package is illustrated in FIG. **12**A and FIG. **12**B. In the illustrated embodiment, system package **1200** includes SoC **1202**, capacitor die **1203***b*, VR **1203***a*, and inductor **1203***c*. In various embodiments, VR **1203***a* may correspond to portions of voltage regulator **300**, namely control circuit **301**, comparison circuit **302**, and reference generator circuit **303** as illustrated in FIG. **3**, and SoC **1202** may correspond to integrated circuit **100** as illustrated in FIG. **1**.

SoC **1202** and capacitor die **1203***b* are arranged in a stacked fashion in package body **1208**. In some embodiments, capacitor die **1203***b* includes vias (not shown) that allow terminals of SoC **1202** to be coupled to interconnect **1204***b*. In various embodiments, interconnect **1204***b* includes multiple wires fabricated on multiple metal layers separated by insulating layers. Such wires may be used to connect solder bumps **1205***a-e* to terminals on capacitor die **1203***b*.

In a similar fashion, interconnect **1204***a* includes multiple wires that may be used to connect terminals of DRAM **1209***a-b*, inductor **1203***c*, and VR **1203***a* to vias **1207***a-b* included in package body **1208**. Although only two vias are shown, in various embodiments, any suitable number of vias may be employed.

As depicted in FIG. **12**, DRAM **1209***a-b*, inductor **1203***c*, and VR **1203***a* are mounted on the top of system package **1200**. As described above, using wires in interconnect **1204***a-b*, and vias **1207***a-b*, signals and power supplies for DRAM **1209***a-b*, inductor **1203***c*, and VR **1203***a* may be routed to solder bumps **1205***a-e* or the stack of SoC **1202** and capacitor die **1203***b*.

It is noted that the embodiment illustrated in FIG. **12**A-B is merely an example. In other embodiments, different arrangements of inductor **1203***c* may be employed.

Turning to FIG. **13**, another embodiment of a system package is illustrated. In the illustrated embodiment, system package **1300** includes SoC **1302**, VR **1303***a*, inductor **1303***b*, and capacitor **1303***c*. In various embodiments, VR **1303***a* may correspond to portions of voltage regulator **300**, namely control circuit **301**, comparison circuit **302**, and reference generator circuit **303** as illustrated in FIG. **3**, and SoC **1302** may correspond to integrated circuit **100** as illustrated in FIG. **1**.

Within package body **1308**, VR **1303***a*, inductor **1303***b*, and capacitor **1303***c* are arranged in a first layer, and SoC **1302** is arranged in a second layer. Wire and vias included within package body **1308** are employed to couple terminals of VR **1303***a*, inductor **1303***b*, and capacitor **1303***c* to terminals included in SoC **1302**. Additionally, other wires and vias included in package body **1308** may be used to couple terminals of SoC **1302**, VR **1303***a*, inductor **1303***b*, and capacitor **1303***c* to interconnect **1304**.

Interconnect **1304** may, in various embodiments, include multiple wires fabricated on multiple metal layers separated by a insulating layers. In some embodiments, wires included in interconnect **1304** may provide connections between solder bumps **1305***a-e* to terminals on interconnect **1304** which are coupled to SoC **1302**, VR **1303***a*, inductor **1303***b*, and capacitor **1303***c* using wires and vias included in package body **1308**. Additionally, other wires included in interconnect **1304** may be employed to connect vias **1307***a-b* of package body **1308** to terminals of any of SoC **1302**, VR **1303**, inductor **1303***b*, and capacitor **1303***c*, to provide a wiring path between DRAM **1309** and the aforementioned subcomponents.

DRAM **1309** is coupled to solder bumps **1306***a-b*, which, in turn, are coupled to vias **1307***a-b* included in package body **1308**. Although a single DRAM is depicted in the embodiment of FIG. **13**, in other embodiments, any suitable number of DRAMs or other memory devices may be employed.

It is noted that the embodiment illustrated in FIG. **13** is one example of a system package. In other embodiments, different subcomponents and different arrangements of subcomponents are possible and contemplated.

Another embodiment of a system package is illustrated in FIG. **14**. In the illustrated embodiment, system package **1400** includes SoC **1402**, VR **1403***a*, inductor **1403***b*, and capacitor **1403***c*. In various embodiments, VR **1403***a* may correspond to portions of voltage regulator **300**, namely control circuit **301**, comparison circuit **302**, and reference generator circuit **303** as illustrated in FIG. **3**, and SoC **1402** may correspond to integrated circuit **100** as illustrated in FIG. **1**.

VR **1403***a*, inductor **1403***b*, and capacitor **1403***c* are mounted on substrate core **1407**, which is, in turn, mounted on interconnect **1408**. In various embodiments, interconnect **1408** may include multiple wires fabricated on multiple metal layers separated by insulating layers. Some of the multiple wires included in interconnect **1408** may couple terminals of VR **1403***a* to one or more of solder bumps **1405***a-e*. Additionally, other wires included in interconnect **1408** may couple terminals of VR **1403***a* to terminals of inductor **1403***b* and capacitor **1403***c*.

Interconnect **1403** may also include multiple wires fabricated on multiple metal layers separated by insulating layers. In various embodiments, some of the wires included in interconnect **1403** may couple terminals of SoC **1402** to terminals of VR **1403***a*, thereby allowing VR **1403***a* to source a regulated power supply to SoC **1402**. Other wires included in interconnect **1403** may couple terminals of SoC **1402** to one or more of solder bumps **1405***a-e*, using vias included in substrate core **1407** (not shown).

In various embodiments, interconnect **1403** may be fabricated on top of substrate core **1407** once VR **1403***a*, inductor **1403***b*, and capacitor **1403***c* have been mounted. The fabrication process may, in some embodiments, include the deposition and etching of metal layers, deposition of insulating layers, and the like. In other embodiments, interconnect **1403** may be fabricated separately from substrate core **1407**, and then attached to substrate core **1407** using any suitable attachment method.

It is noted that the embodiment illustrated in FIG. **14** is merely an example. In other embodiments, different arrangement of the components, such as, e.g., VR **1403***a*, may be employed.

Turning to FIG. **15**, a flow diagram of an embodiment of a method for assembling a system package is illustrated. The method begins in block **1501**. Wafers including multiple SoC dies, voltage regulator dies, and passive device dies may then be received (block **1502**). In some embodiments, wafers for each type of die, such as, e.g., voltage regulator dies, may be fabricated using a dedicated semiconductor manufacturing process. Prior to further assembly steps, each of the wafers may be tested, and failing dies included within a given wafer may be marked so that such failing dies are not assembled into a package.

A voltage regulator die and one or more passive device dies may then be assembled into a VRM (block **1503**). In various embodiments, the voltage regulator die and the one or more passive device dies may be assembled into a VRM corresponding to one of the embodiments illustrated in FIG. **4** through FIG. **7**. Once the VRM is assembled, the VRM may then be mounted in a system package along with one of the SoC dies (block **1504**). The system package may, in various embodiments, correspond to one of the particular embodiments of a system package illustrated in FIG. **8** through FIG. **14**.

Assembly of the system package may then be completed (block **1505**). In some embodiments, the final assembly may include mounting one or more memory devices into the system package. The one or more memory devices may be arranged, in various embodiments, as depicted in the embodiments illustrated in FIG. **8** through FIG. **10**. In some embodiments, once the system package is assembled, a final test operation may be performed. The method may then conclude in block **1506**.

Although some of the operations included in the flow diagram of FIG. **15** are depicted as being performed in parallel, in other embodiments, one or more of the operations may be performed in parallel.

Turning to FIG. **16**, a flow diagram depicting another embodiment of a method of assembling a system package is illustrated. The method begins in block **1501**. Wafers including multiple SoC dies, voltage regulator dies, and passive device dies may then be received (block **1502**). In some embodiments, wafers for each type of die, such as, e.g., voltage regulator dies, may be fabricated using a dedicated semiconductor manufacturing process. Prior to further assembly steps, each of the wafers may be tested, and failing dies included within a given wafer may be marked so that such failing dies are not assembled into a package.

One each of a voltage regulator die, an inductor die, a capacitor die, and an SoC die may then be mounted in the system package (block **1603**). The system package may, in various embodiments, correspond to one of the particular embodiments of a system package illustrated in FIG. **8** through FIG. **14**.

Assembly of the system package may then be completed (block **1604**). In some embodiments, the final assembly may include mounting one or more memory devices into the system package. The one or more memory devices may be arranged, in various embodiments, as depicted in the embodiments illustrated in FIG. **8** through FIG. **10**. In some embodiments, once the system package is assembled, a final test operation may be performed. The method may then conclude in block **1605**.

It is noted that the embodiment of the method depicted in the flow diagram of FIG. **16** is merely an example. In other embodiments, different operations and different orders of operations may be employed.

Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of this disclosure.

The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of this application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

What is claimed is:

1. An apparatus comprising:

a passive device integrated circuit (IC) die having one or more passive circuit devices implemented thereon;

a plurality of solder balls coupled to the passive device IC die;

a voltage regulator controller circuit comprising one or more circuit elements of a voltage regulator circuit; and

an interconnect layer arranged between the passive device IC die and the voltage regulator controller circuit, wherein the interconnect layer is electrically coupled to the voltage regulator controller circuit and further coupled to the passive device IC die by a first plurality of electrical connectors, and further coupled to the plurality of solder balls by corresponding ones of a second plurality of electrical connectors, wherein the second plurality of electrical connector comprise a plurality of connecting vias passing through the passive device IC die.

2. The apparatus of claim **1**, wherein the passive device IC die includes one or more inductors implemented thereon.

3. The apparatus of claim **1**, wherein the passive device IC die includes one or more capacitors implemented thereon.

4. The apparatus of claim **1**, wherein the voltage regulator controller circuit and the one or more passive circuit devices form a voltage regulator circuit that is configured to generate a regulated supply voltage on a regulated supply voltage node, and wherein the voltage regulator controller circuit includes:

a reference generator circuit configured to generate a reference voltage;

a comparison circuit configured to compare the reference voltage to the regulated supply voltage; and

a control circuit configured to control operation of the voltage regulator circuit based on comparing the reference voltage and the regulated supply voltage.

5. The apparatus of claim **4**, wherein the control circuit includes one or more devices configured to source current, through the one or more passive circuit devices, to the regulated supply voltage node.

6. The apparatus of claim **4**, further comprising an integrated circuit coupled to the voltage regulator circuit, wherein the integrated circuit includes one or more functional circuit blocks coupled to receive the regulated supply voltage.

7. The apparatus of claim **6**, wherein the one or more functional circuit blocks includes at least one of a general purpose processor circuit and a memory.

8. The apparatus of claim **1**, wherein the first plurality of electrical connectors comprises one or more solder bumps.

9. A method comprising:

manufacturing a voltage regulator assembly, wherein manufacturing the voltage regulator assembly comprises:

receiving a passive device integrated circuit (IC) die having one or more passive circuit elements implemented thereon;

coupling a plurality of solder balls coupled to the passive device IC die;

receiving a voltage regulator controller circuit comprising one or more circuit elements of a voltage regulator circuit;

arranging an interconnect layer between the passive device IC die and the voltage regulator controller circuit;

electrically coupling the interconnect layer to the passive device IC die by a first plurality of electrical connectors;

electrically coupling the voltage regulator controller circuit to the one or more passive circuit elements using the interconnect layer; and

electrically coupling the interconnect layer to ones of the plurality of solder balls using corresponding ones of a second plurality of electrical connectors, the second plurality of electrical connectors comprising a plurality of connecting vias passing through the passive device IC die.

10. The method of claim **9**, further comprising assembling a system package, wherein assembling the system package comprises:

receiving an integrated circuit having one or more functional circuit blocks implemented thereon; and

coupling the voltage regulator assembly to the integrated circuit.

11. The method of claim **10**, further comprising performing a final test procedure on the system package.

12. The method of claim **9**, wherein the passive device IC die includes one or more inductors implemented thereon.

13. The method of claim **9**, wherein the passive device IC die includes one or more capacitors implemented thereon.

14. The method of claim **9**, wherein electrically coupling the interconnect layer to the passive device IC die by the first plurality of electrical connectors comprises connecting the interconnect layer to the passive device IC die using a plurality of solder bumps.

15. An apparatus comprising:

an integrated circuit having a plurality of functional circuit blocks implemented thereon;

a voltage regulator assembly coupled to the integrated circuit, the voltage regulator assembly including:

a passive device integrated circuit (IC) die coupled to the integrated circuit, the passive device IC die having one or more passive circuit components implemented thereon and further including a plurality of solder balls;

a voltage regulator controller circuit having one or more components of a voltage regulator circuit; and

an interconnect layer disposed between the passive device IC die and the voltage regulator controller circuit, wherein the voltage regulator circuit is electrically coupled to the passive device IC die by the interconnect layer, and wherein the passive device IC die is further coupled to the integrated circuit through a plurality of electrical connectors extending through the passive device IC die from the interconnect layer to one or more corresponding ones of the plurality of solder balls.

16. The apparatus of claim **15**, wherein the passive device IC die includes one or more inductors implemented thereon.

17. The apparatus of claim **15**, wherein the passive device IC die includes one or more capacitors implemented thereon.

18. The apparatus of claim **15**, wherein the voltage regulator controller circuit and the one or more passive circuit components form a voltage regulator circuit that is configured to generate a regulated supply voltage on a regulated supply voltage node, and wherein the voltage regulator controller circuit includes:

a reference generator circuit configured to generate a reference voltage;

a comparison circuit configured to compare the reference voltage to the regulated supply voltage; and

a control circuit configured to control operation of the voltage regulator circuit based on comparing the reference voltage and the regulated supply voltage.

19. The apparatus of claim **18**, wherein at least one of the plurality of functional circuit blocks is configured to operate using the regulated supply voltage.

20. The apparatus of claim **15**, wherein the plurality of functional circuit blocks includes at least one of a general purpose processor circuit and a memory.

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