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(54) CURRENT-GENERATOR CIRCUIT, DEVICE INCLUDING THE CURRENT-GENERATOR CIRCUIT AND ELECTRONIC SYSTEM

(57) Current-generator circuit (100) for supplying a resistive load (102) through a driver (110, 128), comprising a compensation circuit (112) including a resistive block (120) having an electrical resistance (R_{load}') which is a function of the resistance of the resistive load (102). The resistive block (120) mimics the resistance seen by the driver during the supplying operation. The driver is driven in such a way to generate a compensated current pulse (I_{CTR}) which balances non-idealities and channel-modulation effects introduced by the resistance of the load during the supplying operation.

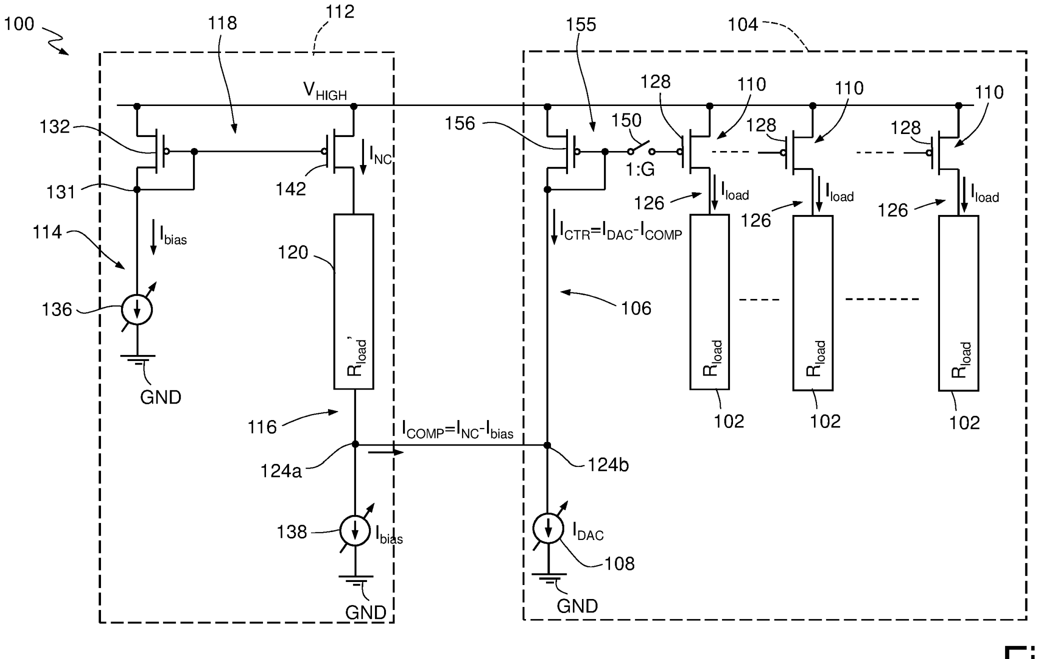

Fig.6

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Description

[0001] The present invention relates to a current-generator circuit (e.g., a programming circuit for writing data in a phase-change memory cell), to a phase-change memory device (e.g., a phase-change memory) including the current-generator circuit, and to a system including said device.

[0002] Phase change non-volatile memories (also known as PCMs - "Phase Change Memories") are known in the art. To store information, the characteristics of materials that have the property of switching between phases having different electrical characteristics are exploited. For example, such materials can switch between an amorphous, disordered phase and an ordered crystalline or polycrystalline phase; the two phases are associated with resistivities of a considerably different value, and consequently to a different value of a stored data. For example, the elements of the VI group of the periodic table, such as Tellurium (Te), Selenium (Se), or Antimony (Sb), called chalcogenides or chalcogenic materials, can be used advantageously for the realization of phase change memory cells. The phase changes are obtained by locally increasing the temperature of the chalcogenic material, through resistive electrodes (generally known as heaters) arranged in contact with respective regions of chalcogenic material. Selection devices (for example MOSFET transistors) are connected to the heaters, and enable the passage of an electrical programming current through a respective heater (electrical pulses known as "SET" and "RESET", adapted to set a respective phase of the material); the electric current generates, through Joule effect, the temperature increase required for the phase change. During reading operations, the state of the chalcogenic material is detected by applying a sufficiently low voltage across the selected cell, so as not to cause a significant heating, and then by reading the value of the current flowing in the cell. Since the current is proportional to the conductivity of the chalcogenic material, it is possible to determine the state of the material, and therefore the data stored in the memory cell.

[0003] In a known way, non-volatile memories comprise a matrix of memory cells organized in rows (word lines) and columns (bit lines); each memory cell is made, in the case of PCM memories, of a phase-change storage element and a selector transistor connected in series. A column decoder and a row decoder allow to select, on the basis of received input logic signals and a decoding scheme, the addressed memory cells, and in particular the respective word lines and bit lines.

[0004] The column decoder comprises a plurality of analog selection switches (implemented by transistors), receiving the address signals at the respective control terminals; the selection switches are organized according to a tree structure in hierarchical levels, and their number in each hierarchical level is linked to the organization and size of the memory matrix. The selection switches, when enabled, allow the selected bit line to be biased at a defined voltage and / or current value, depending on the operations to be implemented; in particular, a current path is created between a programming stage or a reading stage and the selected bit line. This current path is defined by the series of a certain number of selection switches.

[0005] In a known way, reading amplifiers ("sense amplifiers") read the data stored in the memory cells by comparing the current (or an electrical quantity correlated to it) that flows into the selected memory cell (also called "direct cell") with a reference current flowing in a complementary cell (so-called "double-ended" reading). Obviously, also the programming step must provide for the writing of the logical data both in the direct memory cell and in the complementary cell. For example, the bit written in the complementary cell (e.g., logic "1") is associated with a RESET state (by means of a RESET impulse), while the same bit ("1") is written in the direct cell by means of a SET impulse.

[0006] Figure 1 shows a circuit typically used to implement the column decoder 1. Any local bitline BL is selected only when the corresponding path to V_{HIGH} is enabled. The first addressing level is formed by PMOS transistors YM (here, 4 transistors YM[0] to YM[3]) which are connected to the drain terminal of transistors M (here, a number "J" of transistors M[0], ..., M[J] - e.g. J=32) . Moreover, PMOS transistors YO (i.e., one transistor for each bit line BL) implement a second addressing level. In order to guarantee that the programming current generated by transistors M is fed correctly into the selected PCM cell, only one of the four YM transistors, connected to its drain terminal, as well as only one of the transistors YO that are connected to the active transistor YM is turned on at a given time. Furthermore, each transistor M can program one cell belonging to any of the associated bit lines BL. The row decoder selects the addressed cell by raising the corresponding word line WL to a bias voltage generated by a row voltage regulator.

[0007] Figure 2 shows a circuit 11 for generating a programming current for programming PCM memory cells, according to the known art.

[0008] Circuit 11 comprises a control branch 2, including: a current generator 4, configured to cooperate to the generation of a RESET or SET pulse, depending on the operating condition, connected between a reference terminal 4a (ground, GND) and a biasing terminal 4b; and a control transistor 6 (here, a diode-connected P-type MOSFET), forming a first element of a current mirror 5.

[0009] The current generator 4 is, e.g., a Digital-to-analog-Converter, DAC, and is configured to generate a current pulse I_{DAC} in the control branch 2.

[0010] The current generator 4 and the control transistor 6 are connected in series between the ground reference terminal 4a and a line 34 at V_{HIGH} voltage, for example equal to 5 V. The control branch 2 further includes, between the current generator 4 and the transistor 6, in series to the current generator 4 and the control transistor 6, a switch 3, adapted to be switched on and off with the aim of connecting and, respectively disconnecting, the current generator 4 to, respectively from, the rest of the control branch 2 (in particular, to connect/disconnect the current generator 4 to/from the current mirror 5); the switch 28 is, e.g., a n-type MOFET device controlled by a Vdd signal generated by a control logic which is not part of the present invention. The Vdd signal has a value adapted to turn on the switch 3 when the memory is being programmed and to turn off the switch 3 otherwise, so that no undesired current can flow to the memory cells through the mirror 5. The switch 3 is optional, and may be omitted or designed in a different way.

[0011] The control branch 2 further comprises a cascode switch 7, e.g. a n-type MOSFET device, arranged in series to the switch 3, electrically arranged between the switch 3 and the mirror device 5. The cascode switch 7 has a control terminal (gate) controlled by a signal Vcasc, provided by a regulator of a known type. The cascode switch 7 has the function of improving the electrical isolation between the part of the control branch 2 which includes the current generator 4 (low voltage portion of the branch 2, where voltage is in the range 0.5-0.9 V) and the part of the control branch 2 that includes the current mirror 5 (high voltage portion of the control branch 2, at voltage V_{HIGH}), so that reverse transmission is reduced as there is no direct coupling between the two portions at different voltages.

[0012] During use, when the current generator 4 is controlled to generate current I_{DAC} (SET or RESET pulse), said current I_{DAC} flows through the control branch 2 between the line at V_{HIGH} and the ground reference terminal GND, and is mirrored, through the current mirror 5, in respective programming currents I_{PROG} of a plurality of main bitlines MBL_1, ..., MBL_J.

[0013] The current I_{PROG} (SET/RESET pulse) flows through the respective main bitline MBL_1, ..., MBL_J, depending on the activation of transistors M (here, P-type MOSFETs). The transistors M are connected in a current-mirror configuration to the transistor 6. In particular, the activation of the transistors M is controlled by two respective switches which are turned on and off by enabling signals EN_PULSE, /EN_PULSE (wherein /EN_PULSE has a logic value complementary to that of EN_PULSE).

[0014] With reference to the main bitline MBL_1, a switch 10 (e.g., P-channel transistor) is coupled between the gate of the transistor M[0] and the gate of the control transistor 6; and a switch 12 (e.g., P-channel transistor) is coupled between the gate of the transistor M[0] and the V_{HIGH} line. In this way, as apparent to the skilled person in the art, the current I_{DAC} on the control branch 2 is mirrored in the main bitline MBL_1 only when switch 10 is turned on and, at the same time, switch 12 is turned off, i.e., only when the signals EN_PULSE and /EN_PULSE have a respective (complementary) value such as to bring the switch 10 in a conduction state and the switch 12 in interdiction.

[0015] The same configuration is then repeated for all the "J" main bitlines forming the memory device 1.

[0016] To sum up, the programming current I_{PROG} (SET/RESET pulse) is supplied to each phase-change memory element which must be programmed by means of this current. It is apparent that the current pulses should be shaped and have an amplitude such as to induce the phase transition in the phase change memory elements to which they are applied. Moreover, it is known to the Applicant to apply current pulses to several memory elements in parallel, to speed up the writing operation.

[0017] The transistors M are affected by channel modulation due to the undesired variation of their drain-source voltage V_{DS} due to an uncontrolled variation of the resistance on the main bitlines MBL_1, ..., MBL_J. This effect is due to the fact that the resistance of each PCM cell is not perfectly equal to the resistance of the other PCM cells, because of variations occurring during the manufacturing process and during use and, at the same time, the intensity of the programming pulses can vary unexpectedly from one cycle to another due to non-idealities.

[0018] In other words, the voltages at nodes 8a, 9a (terminals of driving transistors M[0], ..., M[J]) of the main bitlines MBL_1, ..., MBL_J, depend unpredictably on the electrical resistance value of the phase change memory elements being programmed and on the amplitude of the current pulses applied to them.

[0019] The channel modulation effect has an impact on current pulse amplitude precision. This means that not all the programming pulses are equally effective and suitable to set the desired resistive state (SET or RESET) to the memory element to which they are applied.

[0020] The same problem can be found in other kind of circuits or applications, in particular where a current-generation circuit, using a current-mirror configuration, is employed to supply an output current to a resistive load.

[0021] Patent document US2008/298122 relates to a phase change memory device comprising a plurality of cells including a phase change memory element and a select device, wherein the select device is configured to cause the cells to operate during reading at a voltage and current below a level that would cause a read disturb.

[0022] Patent document US2013/229863 relates to a driving stage for phase change non-volatile memory devices, designed for the supply of driving currents during programming operations of the memory cells.

[0023] Patent document US2009/091969 relates to a resistance change memory, e.g., a write-system circuit of a resistance change memory.

[0024] However, the above-mentioned issues remain unsolved.

[0025] According to the present invention, a current-generator circuit, a device including the current-generator circuit and a system including the device are provided, as defined in the annexed claims.

[0026] According to an embodiment, the present invention relates to a current-generator circuit operable to generate an output current pulse to be fed to a resistive load, comprising:

- a current generator circuit (11), including:
    - a control branch coupled to a control current generator adapted to generate a control current pulse, and
    - a driver, electrically coupled to the control branch and the resistive load; and
- a compensation circuit, comprising:
    - a first compensation branch, configured to generate a first compensation current pulse which is a fraction of the control current pulse;
    - a second compensation branch, coupled in a current mirror configuration to the first compensation branch for receiving the first compensation current pulse, including a resistive block having an electrical resistance that mimics the resistance of the resistive load,

wherein the second compensation branch is electrically coupled to the control branch to supply the control branch with the compensation current pulse in such a way that the compensation current pulse is added/subtracted to/from the control current pulse to generate a compensated current pulse,
and wherein the driver is electrically coupled to the control branch and to the resistive load to receive from the control branch the compensated current pulse and to generate the output current pulse as a function of the compensated current pulse.

[0027] For a better understanding of the present invention, preferred embodiments thereof are now described, purely by way of non-limiting example and with reference to the attached drawings, wherein:

- Figure 1 is a circuit representation of a portion of a known phase-change memory device including a column decoder;
- Figure 2 is a circuit representation of a programming circuit for writing logic data in a phase-change memory cell, according to the known art;
- Figure 3 is a circuit representation of a programming circuit for writing logic data in a phase-change memory cell, according to the present invention;
- Figure 4 is a simplified block diagram of a PCM device including the programming circuit of Figure 3;
- Figure 5 is a simplified block diagram of an electronic system incorporating the PCM device of Figure 4; and
- Figure 6 is a circuit representation of a generic current-generator circuit for supplying an output current to a resistive load, according to an embodiment of the present invention.

[0028] The present invention will be now described with specific reference to a programming circuit adapted for generating programming current pulses suitable for programming one or more memory cells of a phase-change type, without losing generality. In particular, as it will be apparent from Figure 6 and related description, the present invention finds application as programming circuit for any kind of resistive memory (e.g., conductive bridge RAM - CBRAM, Oxide based RAM - OxRAM, etc.), as well as current generator for resistive heaters that are employed in high temperature gas sensors, for reconfigurable integrated antennas, for dispenser cathodes, for beam control in semiconductor laser, and for still other applications, devices and systems requiring a current generator which is insensitive to the effect of the resistive load.

[0029] Figure 3 shows a programming circuit 21 for generating programming current pulses suitable for programming one or more memory cells of a phase-change type. The programming circuit 21 includes a compensation circuit 20 operatively coupled to the circuit 11 of Figure 2, with the aim of compensating or reducing the channel modulation effect discussed above.

[0030] The compensation circuit 20 includes a biasing branch 22 and a compensation branch 24; the biasing branch 22 extends between the high-voltage line 34 at voltage V_{HIGH} (e.g., between 4 and 6 V) and the reference terminal GND at reference voltage (e.g., at 0 V). The biasing branch 22 is configured to generate a biasing current I_{bias} and to mirror the biasing current I_{bias} to the compensation branch 24 through a current mirror 23 (in particular, with unitary gain).

[0031] The compensation branch 24 analogously extends between the high-voltage line 34 and the reference terminal GND.

[0032] In greater detail, the biasing branch 22 comprises a current generator 26 (e.g., a Digital-to-analog-Converter, DAC, to allow digital current control), configured to generate a current pulse in the biasing branch 22 having an amplitude that is a fraction of the amplitude of the current pulse I_{DAC} generated by the control branch 2 of the circuit 11 of Figure 2. Provided that the current pulse I_{DAC} generated by the control branch 2 has an amplitude "A", the current pulse I_{bias} generated by the DAC 26 has an amplitude "$\alpha \cdot A$", with $\alpha \leq 1$ (preferably, $\alpha < 1$, more specifically $0.5 < \alpha < 0.8$).

[0033] The biasing branch 22 is arranged in parallel to the control branch 2, between V_{HIGH} and GND. Current generators 4 and 26 are chosen or manufactured or operated so that the can supply a respective current pulse I_{DAC} and I_{bias} having the desired ratio, as discussed above. Being the two branches 2 and 22 in parallel to one another, the choice of the respective electrical resistances or of the maximum current that can be generated by the respective current generators 4 and 26 determines the amount of actual current I_{DAC} and I_{bias} that can flow through the branches 2 and 22.

[0034] The biasing branch 22 further includes a first control switch 28, adapted to be switched on and off with the aim of connecting and, respectively disconnecting, the DAC 26 to, respectively from, the rest of the biasing branch 22 (in particular, connect/disconnect the DAC 26 to/from the current mirror 23); the first control switch 28 is, e.g., a n-type MOFET device controlled by the Vdd signal, as discussed with reference to Figure 2. The Vdd signal has a value adapted to turn on the first control switch 28 when the memory is being programmed and to turn off the first control switch 28 when no programming operation is required. The first control switch 28 is optional, and may be omitted.

[0035] The biasing branch 22 further comprises a cascode switch 30, e.g. a n-type MOSFET device, arranged in series to the first control switch 28, electrically between the DAC 26 and the high-voltage line 34 (in particular, between the first control switch 28, when present, and the high-voltage line 34). The cascode switch 30 has a control terminal (gate) controlled by the signal V_{casc}, provided by the regulator as already discussed with reference to Figure 2. The cascode switch 30 has the function of improving the electrical isolation between the part of the biasing branch 22 which includes the DAC 26 (low voltage portion of the biasing branch 22, where voltage is in the range 0.5-0.9 V) and the part of the biasing branch 22 that includes the current mirror 23 (high voltage portion of the biasing branch 22, at voltage V_{HIGH} in the range 4-6V), so that reverse transmission is reduced as there is no direct coupling between the two portions at different voltages.

[0036] The current mirror 23 is formed in part by a mirror device 32 (here, a p-type MOSFET) arranged in the biasing branch 22 in series to the cascode switch 30, more specifically between the cascode switch 30 and the high-voltage line 34. The mirror device 32 is diode-connected, i.e. its control terminal (gate) is electrically connected to its drain terminal.

[0037] During use, when the DAC 26 is controlled to generate current I_{bias}, said current I_{bias} flows through the biasing branch 22 and is mirrored to the compensation branch 24.

[0038] Circuitally, the compensation branch 24 substantially replicates the biasing branch 22, as it comprises:

- a current generator 36 (e.g., a Digital-to-analog-Converter, DAC, to allow digital current control), configured to generate a current pulse in the compensation branch 24 having an amplitude equal to that of the current pulse generated by the current generator 26 in the biasing branch 22 ($I_{bias}=\alpha\cdot A$, with $\alpha<1$);
- a second control switch 38 (e.g., a n-type MOFET) adapted to be switched on and off with the aim of connecting and, respectively disconnecting, the DAC 36 to, respectively from, the rest of the compensation branch 24. The second control switch 38 is controlled by the Vdd signal generated by the control logic; the second control switch 38 is optional and may be omitted;
- a cascode switch 40 (e.g. a n-type MOSFET device) electrically coupled in series to the DAC 36, between the DAC 36 and the high-voltage line 34 (in particular, arranged in series to the second control switch 38, electrically coupled between the second control switch 38 and the high-voltage line 34). The cascode switch 40 has a control terminal (gate) controlled by the signal Vcasc.

[0039] The current mirror 23 is moreover formed in part by a second mirror device 42 (here, a p-type MOSFET), which is arranged in the compensation branch 24 in series to the cascode switch 40, more specifically between the cascode switch 40 and the high-voltage biasing line 34 at voltage V_{HIGH}. The second mirror device 42 has a control terminal (gate) connected to the control terminal (gate) of the mirror device 32, thus forming the current mirror 23.

[0040] According to an aspect of the present invention, the compensation branch 24 further comprises a resistive block 50 that mimics (in an embodiment, is equal to) the equivalent electrical resistance at node 8a, 9a of each main bitline MBL_1, ..., MBL_J during a programming step (i.e., during logic data writing in the phase-change element). The main source of electrical resistance is given by the series of the electrical resistance(s) of the selector device(s) of the column decoder 1 and the electrical resistance of the phase-change element of the memory cell to be addressed (i.e., to be programmed).

[0041] When, for example, transistor M[0] is activated to propagate a current pulse I_{prog} (SET or RESET pulse) on the main bitline MBL_1, the main sources of electrical resistance in the electrical path between terminal 8a of transistor M[0] and the cell to be programmed is given by the series resistance of the PCM memory cell itself and any resistance introduced by selector device(s) on that path. In the disclosed embodiment, the selector devices include, in particular, the transistor YM and the transistor YO which are activated (turned on) to address the PCM memory cell to be programmed, i.e. activated to connect the local bitline BL (to which the PCM memory cell to be programmed is coupled) to the main bitline MBL_1. Further selector devices, not shown in the present embodiment, may be coupled to the main bitline MBL_1 and/or to the local bitline BL, according to the specific design of the memory considered.

[0042] An analogous electrical resistance is seen at the terminal 9a of transistor M[J] during the programming step of a PCM memory cell coupled to the transistor M[J] through selector devices YM and YO of the column decoder 1.

[0043] In order to reproduce/mimic the above-identified series resistance, the resistive block 50 is designed in such a way to have an electrical resistance which is given by the sum of the electrical resistance of the phase-change memory cell during the programming step, plus any resistance introduced by the one or more selector YM, YO devices present on the path between the driving transistor and the phase-change memory cell being programmed (programming path). In the disclosed embodiment, the resistance R_{COMP} of the block 50 is $R_{COMP}=R_{PCM}+R_{YO}+R_{YM}$.

[0044] The electrical resistance R_{PCM} is that of the phase-change material of the memory cell at its melting point. Resistances R_{YO} and R_{YM} are the resistances of the transistors YO, respectively, YM when activated (i.e., during conduction).

[0045] Since the electrical resistance R_{PCM} of the phase-change memory cell is higher than the resistances R_{YO} and R_{YM} of the transistors YO, YM, in an embodiment of the present invention the resistances R_{YO}, R_{YM} of transistors YO, YM is omitted, so that the resistance of the resistive block 50 is approximated by the resistance R_{PCM} of the memory cell during the programming step $R_{COMP}=R_{PCM}$ (that, in case of PCM, is the resistance of the phase-change material of the memory cell at its melting point).

[0046] A node 24a is identified in the compensation branch 24 between the cascode switch 40 and the DAC 36, more precisely between the cascode switch 40 and the second control switch 38. Analogously, a node 2a is identified in the control branch 2 of circuit 11 between the cascode switch 7 and the current generator 4, more precisely between the cascode switch 7 and the switch 3.

[0047] It is noted that current generator 36 sinks the current I_{bias} from branch 22 through the mirror 23, however, due to the channel modulation effect of transistor 42 caused by the difference between the drain-to-source voltages of transistor 42 and transistor 32, a current $I_{NC}\neq I_{bias}$ flows through transistor 42.

[0048] The node 24a is electrically connected (in particular, short-circuited) to the node 2a, so that a current $I_{COMP}=I_{NC}-I_{bias}$ is supplied from the compensation branch 24 to the control branch 2. Current I_{COMP} may either be a positive current that is summed to the current I_{DAC} generated by the current generator 4, or a negative current that is subtracted from the current I_{DAC}. Accordingly, a current I_{CTR} flowing in the control branch 2 is given by $I_{DAC}-I_{COMP}$; the current I_{CTR} is mirrored through the current mirror 5 in the program current I_{prog}. If the resistive block 50 is designed as identified above, then a voltage drop V_{DS_COMP} on the second mirror device 43 (substantially) equals a voltage drop V_{DS_PROG} on transistor M[0] (analogously, on transistor M[J]), and $I_{prog} \approx I_{DAC}$. Typically, the current mirror 5 is designed with a gain G (e.g., G=10), so that $I_{prog} \approx G \cdot I_{DAC}$.

[0049] According to the above, the programming current I_{prog} is no more dependent (or minimally dependent) from the resistance of the phase-change material of the memory cell being programmed, since the modulation effect on the drain-source voltage of transistors M is balanced by the compensation current I_{COMP}.

[0050] The schematic block of Figure 4 shows a memory system 50 comprising the circuits 11 and 20 previously disclosed, and includes:

- a PCM memory array 52;
- a finite state machine, FSM, 54;
- two decoders (namely, the row decoder 56 and the column decoder 1);
- voltage regulators 58;
- an internal oscillator 60;
- a digital-to-analog converter, DAC, 62; and
- several internal registers 64.

[0051] The majority of the area of the memory system 50 is occupied by the PCM memory array 52, which contains for example 557568 memory cells divided in 528 row (WLs) and 1056 column (BLs). Data are stored in the memory using a differential approach and, therefore, cells are split into two categories: Direct Cells (DCs) and Complementary Cells (CCs). When a program operation is issued in order to store a given data, the information is written as it was received into DCs, but is also complemented and, then, written into the corresponding CCs. In this way, each data present in the memory has a complementary counterpart. The FSM 54 controls the internal operations of the memory system 50 (e.g., boot, write, read, etc.), and manages data reception and transmission through, e.g., a 32 bit Advanced High-performance Bus (AHB), which exploits a AMBA (Advanced Microcontroller Bus Architecture) protocol. This protocol is open source and is commonly used to carry out the communications inside a SoC, and is not part of the present invention. A clock is provided to the FSM 54 by the internal oscillator 60 that is designed to work at 10 MHz and is trimmed during the EWS phase to adjust its frequency in order to attenuate the effect of process spreads. Furthermore, during boot operation, the FSM 54 loads the trimming configurations and the pulse settings from the memory reserved sector to the registers.

[0052] Figure 5 illustrates a portion of an electronic system 70, which may be used in electronic devices, such as: a PDA (Personal Digital Assistant); a portable or fixed computer, possibly with wireless data-transfer capacity; a cellphone; a digital audio player; a photographic camera or video camera; a wearable electronic device; or further devices that are able to process, store, transmit and receive information.

[0053] In detail, as a non-limiting example, the electronic system 70 comprises a controller 71 (for example, provided with a microprocessor, a DSP, or a microcontroller), an input/output device 72 (for example, provided with a keypad and a display), for entering and displaying data, the memory system 50, a wireless interface 74, for example an antenna, for transmitting and receiving data through a radiofrequency wireless communication network and a RAM 75, all coupled through a bus 76. A battery 77 may be used as electric power supply source in the electronic system 70, which may further be provided with a photographic or video camera 78.

[0054] Figure 6 shows a current-generator circuit 100 operable to generate an output current pulse I_{load} to be fed to one or more resistive loads 102 (a plurality of resistive loads is shown in Figure 6). Elements which are common to the circuit of Figure 3 are apparent, and therefore reference to them may be made to better understand the following description of Figure 6.

[0055] The invention of Figure 6 finds application as current-generation circuit for any kind of resistive memories (e.g., conductive bridge RAM - CBRAM, Oxide based RAM - OxRAM, etc.), or as current generator for resistive heaters that are employed in high temperature gas sensors, for reconfigurable integrated antennas, for dispenser cathodes, for beam control in semiconductor laser, and for still other applications, devices and systems requiring a current generator which is insensitive to the effect of the resistive load.

[0056] In figure 6, each resistive load 102 has a resistance Rioad which is approximately the same of the resistance Rioad of the other resistive loads 102.

[0057] The current-generator circuit 100 comprises:

- a current generator circuit 104, including:
  - a control branch 106 coupled to a control current generator 108 adapted to generate a control current pulse I_{DAC}, and
  - one or more drivers 110, each of them being electrically coupled to the control branch 106 and to a respective resistive load 102; and
- a compensation circuit 112, comprising:
  - a first compensation branch 114, configured to generate a first compensation current pulse I_{bias} which is a function (e.g., a multiple or submultiple or a fraction) of the control current pulse I_{DAC}; and
  - a second compensation branch 116, coupled in a current mirror configuration 118 to the first compensation branch 114 for receiving the first compensation current pulse I_{bias}, and including a resistive block 120 having an electrical resistance $R_{load'}$ that mimics the resistance R_{load} of each of the resistive loads 102.

[0058] The second compensation branch 116 is electrically coupled to the control branch 106 to supply the control branch 106 with the compensation current pulse I_{COMP} in such a way that the compensation current pulse I_{COMP} is subtracted from the control current pulse I_{DAC} to generate a compensated current pulse I_{CTR}. Each driver 110 is electrically coupled to the control branch 106 and to the respective resistive load 102 to receive from the control branch 106 the compensated current pulse I_{CTR} and to generate the output current pulse I_{load} as a function of the compensated current pulse I_{CTR}.

[0059] In greater details, according to an exemplary embodiment of the present invention, the first and second compensation branches 114, 116 are connected, as said, in a current mirror configuration 118, to this end, the first compensation branch 114 includes a p-channel transistor 132 having a source node, a gate node and a drain node. The source node is coupled to a supply voltage node V_{HIGH} and the gate node (also referred to herein as the mirror node) is coupled to the drain node at an intermediate node 131. The p-channel transistor 132 is accordingly a diode-connected device.

[0060] A current generator (or current source) 136 (e.g., a Digital-to-analog-Converter, DAC, to allow digital current control) is configured to generate the current pulse I_{bias} in the first biasing branch 114, and accordingly is coupled between the drain node of transistor 132 and a ground reference node GND, in series to the transistor 132.

[0061] The second compensation branch 116 includes a p-channel transistor 142 having a source node, a gate node and a drain node. The source node is coupled to the supply voltage node V_{HIGH} and the gate node is connected to the gate (mirror) node of the transistor 132, thus forming the current mirror 118.

[0062] A current generator (current source) 138 is coupled to the drain node of transistor 142, in series connection, and to the ground reference node GND. The current source 138 sinks the current I_{DAC} from the gate (mirror) node of transistor 132.

[0063] According to the present invention, the resistive block 120, has an electrical resistance $R_{load'}$ that is a function (i.e., "mimics") of the electrical resistance R_{load} of each of the resistive loads 102. In an embodiment, $R_{load'}$ is approximately equal to R_{load} (e.g., the actual resistance value of $R_{load'}$ differs from the resistance value of R_{load} no more than $\pm 20\%$ of R_{load}); in another embodiment $R_{load'}=R_{load}$.

[0064] The circuit 100 further includes the control branch 106, which in turn includes the current generator 108 and a control transistor 156 (here, a diode-connected P-type MOSFET). The current generator 108 is, e.g., a Digital-to-analog-Converter, DAC, and is configured to generate a current pulse I_{DAC} in the control branch 106. The current generator 108 and the control transistor 156 are connected in series to one another, between the supply voltage node V_{HIGH} and the ground reference node GND, in such a way that the source node of the control transistor 156 is coupled to the supply voltage node V_{HIGH} and the drain node of the control transistor 156 is coupled to the current generator 108. The

[0065] It is noted that current generator 138 sinks the current I_{bias} from branch 114 through the mirror 118; however, due to the channel modulation effect of transistor 142 caused by the difference between the drain-to-source voltages of transistor 142 and transistor 132, a current $I_{NC} \neq I_{bias}$ flows through transistor 142.

[0066] A node 124a (defined in the compensation branch 116 between the resistive block 120 and the current generator 138) is electrically connected (in particular, short-circuited) to a node 124b (defined in the control branch 106 between the control transistor 156 and the current generator 108), so that the current $I_{COMP}=I_{NC}-I_{bias}$ is supplied from the compensation branch 116 to the control branch 106. Current I_{COMP} may either be a positive current that is summed to the current I_{DAC} generated by the current generator 108, or a negative current that is subtracted from the current I_{DAC}. Accordingly, a current I_{CTR} flowing in the control branch 106 is given by I_{DAC}-I_{COMP}.

[0067] The circuit 100 further includes a plurality of output legs 126. Each output leg 126 is formed by a respective p-channel transistor 128 having a source node, a gate node and a drain node. The source node is coupled to the supply voltage node V_{HIGH} and the gate node is connected to the gate node of the transistor 156 (current-mirror configuration 155) through a switch circuit 150. The switch circuit 150 is actuated to a closed state in response to an enable signal EN in order to enable the current mirroring operation in each output leg 126, outputting an output current I_{load} that mirrors the control current I_{CTR}. A mirroring ratio 1:G between the transistor 156 and each transistor 128 may be present (e.g., 1:10), and is defined by the difference in transistor size (width/length). Each electric (resistive) loads 102 is connected in series to one respective transistor 128 in the respective output leg 126.

[0068] According to the above, the output current I_{load} is no more dependent (or minimally dependent) from the resistance R_{load} of the loads 102.

[0069] It is noted that each of branches 114, 116 and 106 of the circuit 100 may include one or more switches (transistors) as the transistors 28, 30, 38, 40, 3, 7 previously discussed with reference to Figures 2 and 3, according to the needs and the specific application.

[0070] From what has been described and illustrated previously, the advantages that the column decoder according to the invention affords are evident.

[0071] In particular, the mirroring ratio has been enhanced and a more accurate pulse shape is achieved.

[0072] Furthermore, the impact on area is negligible respect to PCM programming circuitry.

[0073] Furthermore, the dependency of the current with respect to the power supply is significantly reduced and there is no need of an added voltage regulator to supply the circuit.

[0074] Furthermore, the added power consumption is negligible with respect to the power consumption of the writing pulses.

[0075] Finally, it is noted that, when a ramp is generated switching DAC configurations (as needed in the program pulse to SET PCM cell), the slope obtained has a higher accuracy with respect to standard solutions.

[0076] Finally, it is clear that modifications and variations may be made to what has been described and illustrated herein, without thereby departing from the scope of the present invention, as defined in the annexed claims.

Claims

1. A current-generator circuit (100; 21) operable to generate an output current pulse (I_{load}; I_{PROG}) to be fed to an output load (102) through an output leg (126; MBL_J) to which the output load (102) is coupled, comprising:

- an output-current generator circuit (104; 11), including:
  - a control branch (106; 2) coupled to a control current generator (108; 4) that is configured to supply a control current pulse (I_{DAC}), and
  - a program driver (110, 128; 5, 6, M[J]), electrically coupled between the control branch (106; 2) and to the output leg (126; MBL_J); and
- a compensation circuit (112; 20), comprising:
  - a first compensation branch (114; 22), electrically connected in parallel to the control branch (106; 2), including a first compensation current generator (136; 26) configured to supply a first compensation current pulse (I_{bias}) which is equal to, or a fraction (a) of, the control current pulse (I_{DAC});
  - a second compensation branch (116; 24), electrically connected in a current mirror configuration (118; 23) to the first compensation branch (114; 22) for receiving the first compensation current pulse (I_{bias}), including a resistive block (120; 50) having an electrical resistance (R_{load}'; R_{COMP}) approximately equal to the resistance (R_{load}) of the output load (102),

wherein the second compensation branch (116; 24) is electrically connected to the control branch (106; 2) to supply the control branch (106; 2) with the compensation current pulse (I_{COMP}) so that the compensation current pulse (I_{COMP}) is added/subtracted to/from the control current pulse (I_{DAC}) to generate a compensated current pulse (I_{CTR}),
and wherein the program driver (110, 128; 5, 6, M[J]) is electrically connected, by means of a current mirror circuitry having a mirror gain (G), to the control branch (106; 2) and further electrically connected to the output leg (126; MBL_J), to receive from the control branch (106; 2), through said current mirror circuitry, the compensated current pulse (I_{CTR}) and to supply the program current pulse (I_{PROG}) that has a value equal to the value of compensated current pulse (I_{CTR}) amplified by said gain (G).

2. The circuit (100; 21) according to claim 1, wherein the current mirror circuitry (155; 5) includes a first mirror transistor (156; 6) connected in current mirror

configuration to a second mirror transistor (128; M[J]),
and wherein the first mirror transistor (156; 6) is coupled to the control current generator (108; 4), and the second mirror transistor (128; M[J]) is coupled to the output leg (126; MBL_J), so that the program current pulse (I_{prog}) is a copy, amplified by said gain (G), of the compensated current pulse (I_{CTR}).

3. The circuit (100; 21) according to claim 1 or claim 2, wherein the first compensation branch (114; 22) is coupled between a biasing line (34) at a first voltage (V_{HIGH}) and a reference line (GND) at a second voltage lower than the first voltage, and includes: the first compensation current generator (136; 26), electrically coupled to the reference line (GND); a first cascode transistor (30) electrically coupled between the first compensation current generator (136; 26) and the biasing line (34); and a third mirror transistor (132; 32) electrically coupled between the first cascode transistor (30) and the biasing line (34),
and wherein the second compensation branch (116; 24) is coupled between the biasing line (34) and the reference line (GND), and includes: a second compensation current generator (138; 36), electrically coupled to the reference line (GND) and configured to generate said first compensation current pulse (I_{bias}); a second cascode transistor (40) electrically coupled between the second compensation current generator (36) and the biasing line (34); and a fourth mirror transistor (142; 42) electrically coupled between the second cascode transistor (40) and the biasing line (34),
the third and the fourth mirror transistors (132, 142; 32, 42) being connected to one another according to said current mirror configuration (118; 23) to sink the first compensation current pulse (I_{bias}) from the first compensation branch (114; 22).

4. The circuit (100; 21) according to claims 2 and 3, wherein the control branch (106; 2) comprises a third cascode transistor (7) electrically coupled in series to, and between, the first mirror transistor (156; 6) and the control current generator (108; 4),
wherein a first node (124a; 24a) is defined between the second cascode transistor (40) and the second compensation current generator (138; 36) and a second node (124b; 2a) is defined between the third cascode transistor (7) and the control current generator (108; 4), the first and the second node (124a, 124b; 24a, 2a) being short-circuited to one another to supply the compensation current pulse (I_{COMP}) from the second compensation branch (116; 24) to the control branch (106; 2).

5. The circuit (100; 21) according to claim 3 or 4, wherein said resistive block (120; 50) is electrically coupled in series to, and between, the fourth mirror transistor (142; 42) and the second cascode transistor (40).

6. The circuit (100; 21) according to anyone of the preceding claims, wherein said output leg (126; MBL_J) is coupled to a column decoder (1) of a memory array including at least one bitline (BL) to which a phase-change memory cell, to be programmed by said program current pulse (I_{PROG}), is coupled,
wherein said column decoder (1) includes one or more selector devices (YM, YO) operable to address said bitline (BL),
and wherein the resistive block (50) has an electrical resistance (R_{load}' ; R_{COMP}) which is a function of the resistance of the phase-change memory cell during a programming operation of said phase-change memory cell.

7. The programming circuit (100; 21) according to claim 6, wherein the resistive block (50) has an electrical resistance (R_{COMP}) that is moreover a function of the electrical resistance of said one or more selector devices (YM, YO), in such a way that the electrical resistance (R_{COMP}) of the resistive block (50) is given by the sum of the electrical resistances of said one or more selector devices (YM, YO) and of the phase-change memory cell during the programming operation.

8. The circuit (100; 21) according to claim 6 or 7, wherein the electrical resistance of the phase-change memory cell during programming operation is the electrical resistance of the phase-change material of phase-change memory cell at its melting point.

9. A phase change memory device (50), comprising:

- a memory array (52) provided with a plurality of local bitlines (BL) connected to respective memory cells that store respective logic data;
- a column decoder (1), coupled to the memory array for addressing one local bitline (BL) connected to a memory cell that has to be programmed;
- a current-generator circuit (100; 21) according to anyone of claims 1-8, coupled to the memory array through said column decoder (1), for writing a logic data in said memory cell connected to the addressed local bitline (BL).

10. The phase change memory device according to claim 9, further comprising at least one main bitline (MBL_J), connecting the programming circuit (21) with the addressed local bitline (BL); and

- one or more selector devices (YM, YO) coupled to the addressed local bitline (BL) and operable to electrically connect said addressed local bitline (BL) to the main bitline (MBL_J) in order to set up an electrical path between the memory cell to be written and the main bitline (MBL_J).

11. An electronic device, including a current generator circuit (100; 21) according to anyone of claims 1-8.

12. The electronic device of claim 11, chosen among: a resistive memory, a resistive heater, a reconfigurable integrated antenna, a dispenser cathode, a beam control for semiconductor laser.

13. A system (70), comprising a phase change memory device according to claim 9 or 10, and/or an electronic device according to claim 11 or 12, chosen from among: a PDA (Personal Digital Assistant); a portable computer; a cellphone; a digital audio player; a photographic camera or video camera; a wearable electronic device; a portable electronic device; a semiconductor laser; a high temperature gas sensor; a sensor device.

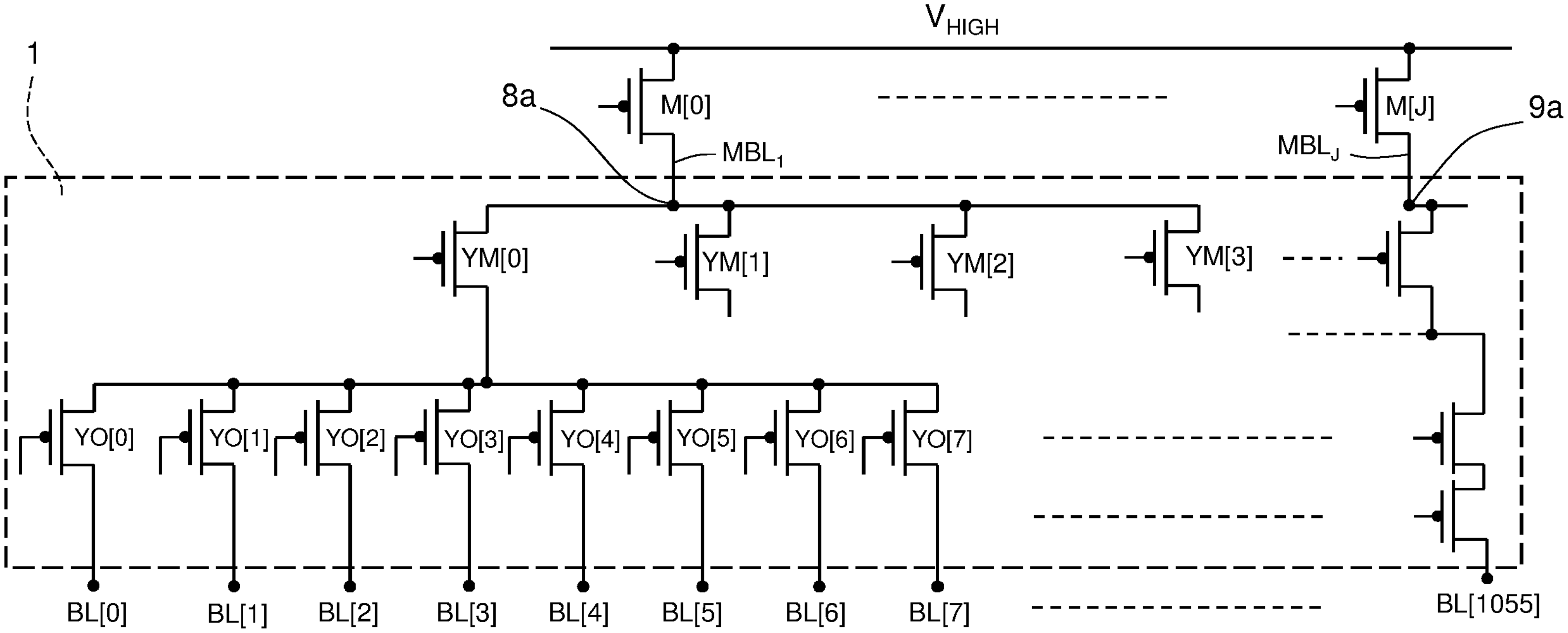
1
V_HIGH
M[0]
M[J]
8a
9a
MBL_1
MBL_J
YM[0]
YM[1]
YM[2]
YM[3]
YO[0]
YO[1]
YO[2]
YO[3]
YO[4]
YO[5]
YO[6]
YO[7]
BL[0]
BL[1]
BL[2]
BL[3]
BL[4]
BL[5]
BL[6]
BL[7]
BL[1055]

Fig.1

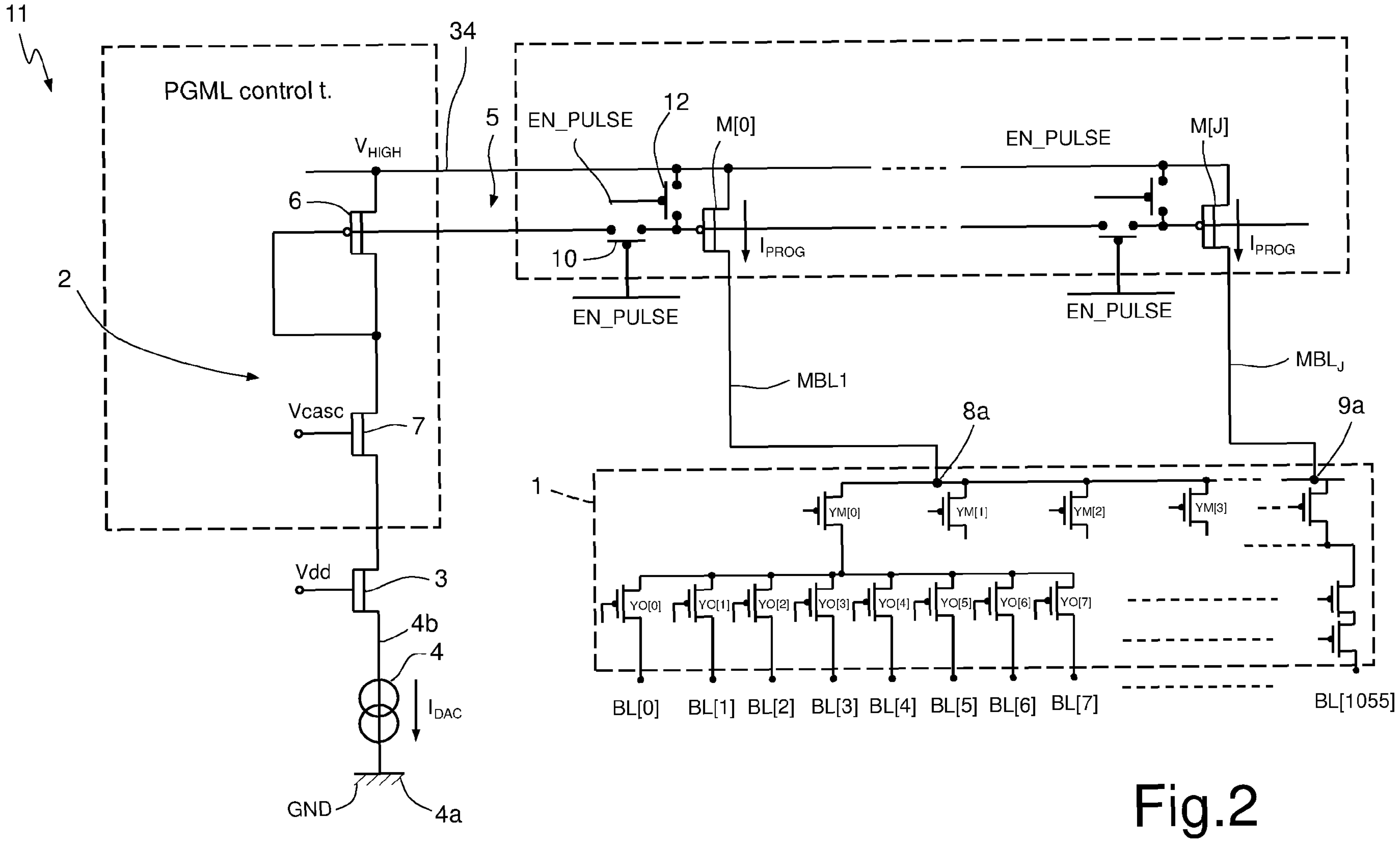
11
PGML control t.
34
5
VHIGH
6
2
Vcasc
7
Vdd
3
4b
4
IDAC
GND
4a
EN_PULSE
12
M[0]
10
IPROG
EN_PULSE
MBL1
EN_PULSE
M[J]
IPROG
EN_PULSE
MBLJ
8a
9a
1
YM[0]
YM[1]
YM[2]
YM[3]
YO[0]
YO[1]
YO[2]
YO[3]
YO[4]
YO[5]
YO[6]
YO[7]
BL[0]
BL[1]
BL[2]
BL[3]
BL[4]
BL[5]
BL[6]
BL[7]
BL[1055]

Fig.2

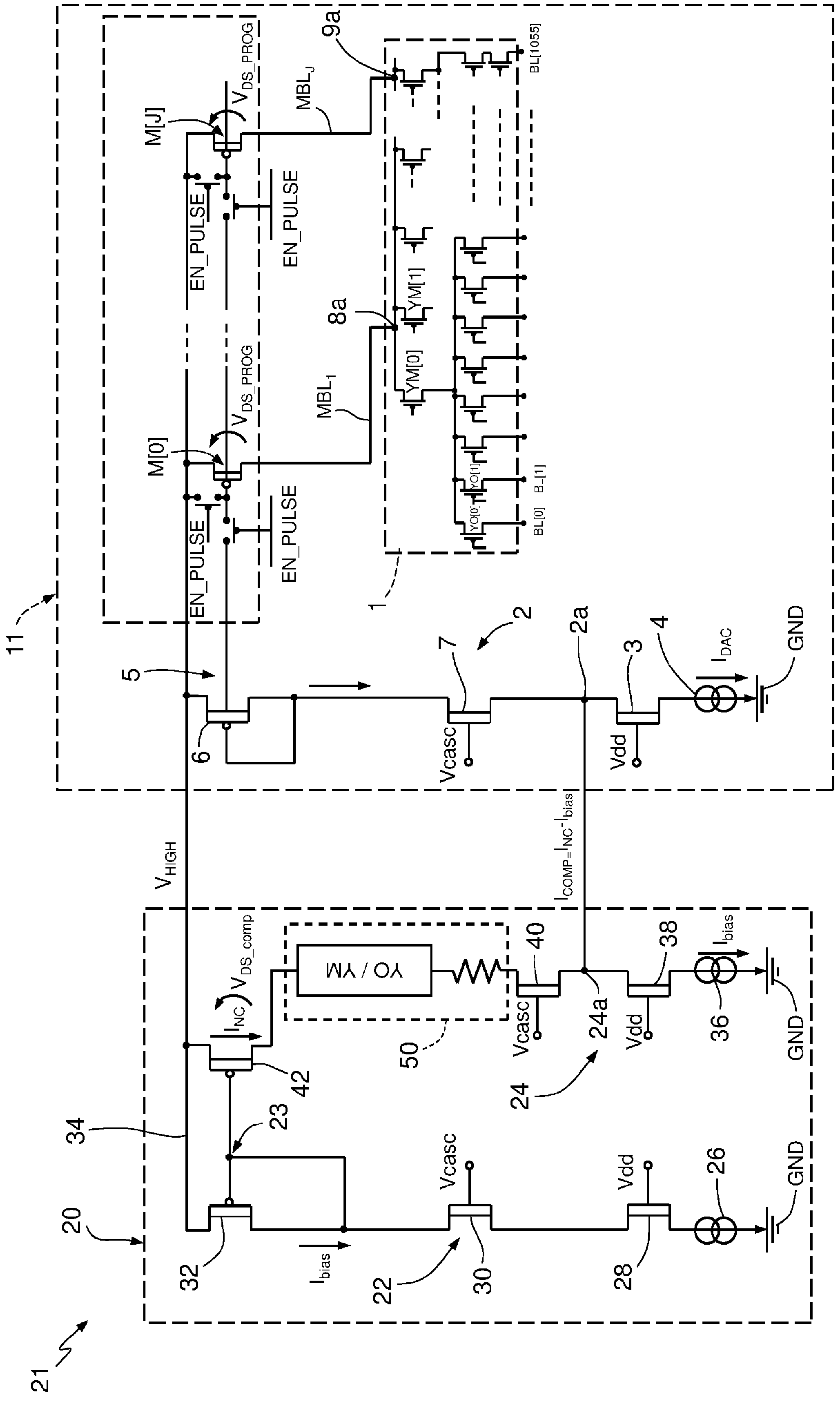
11
5
6
EN_PULSE
EN_PULSE
M[0]
V_{DS_PROG}
MBL$_1$
EN_PULSE
EN_PULSE
M[J]
V_{DS_PROG}
MBL$_J$
9a
8a
YM[0]
YM[1]
YO[0]
YO[1]
BL[0]
BL[1]
BL[1055]
1
2
7
Vcasc
2a
3
Vdd
4
I_{DAC}
GND
V_{HIGH}
$I_{COMP}=I_{NC}-I_{bias}$
20
34
32
23
I_{bias}
22
30
Vcasc
28
Vdd
26
GND
42
I_{NC}
V_{DS_comp}
50
YO / YM
40
Vcasc
24a
24
38
Vdd
36
I_{bias}
GND
21

Fig.3

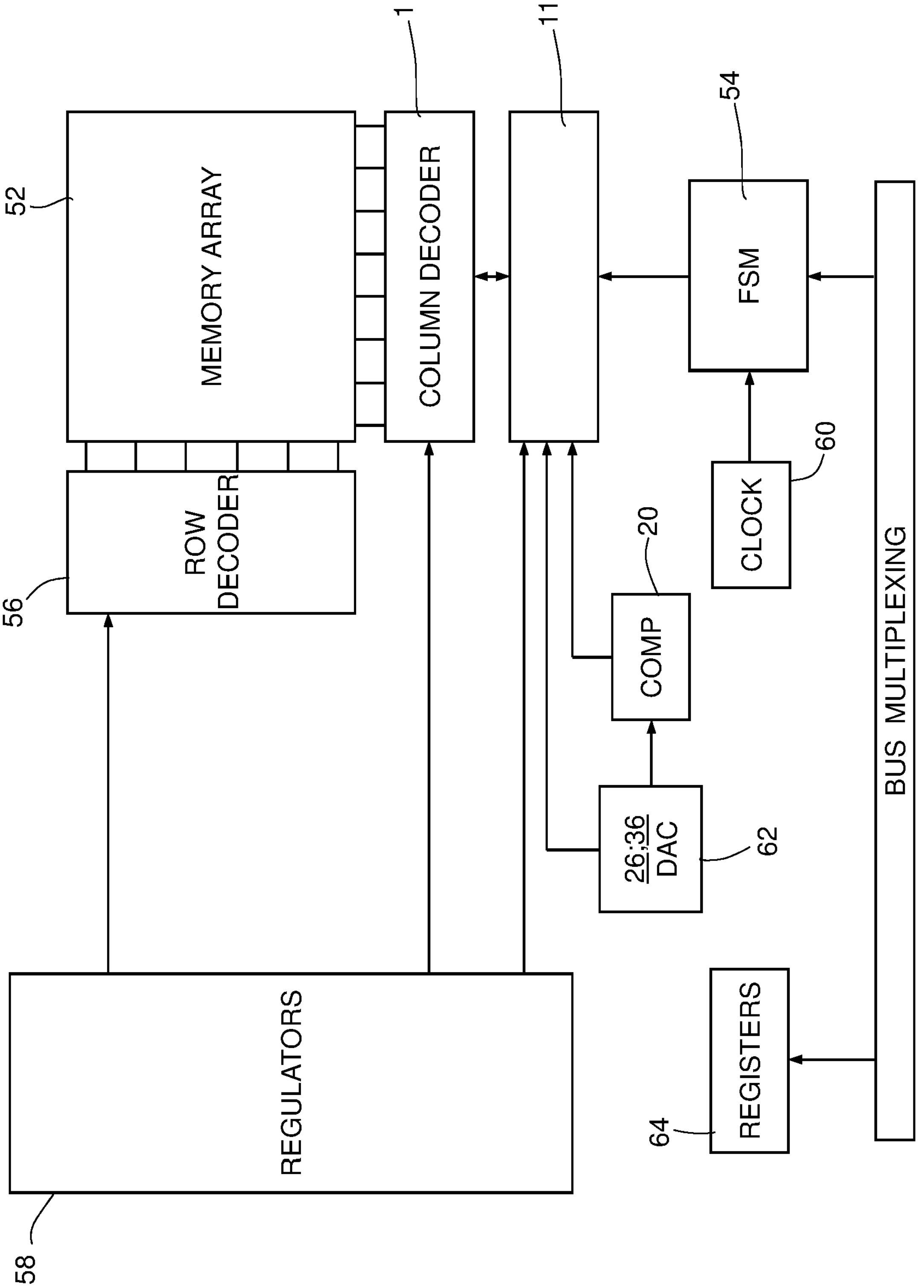
52
MEMORY ARRAY
1
COLUMN DECODER
11
54
FSM
56
ROW DECODER
60
CLOCK
20
COMP
26;36
DAC
62
BUS MULTIPLEXING
58
REGULATORS
64
REGISTERS

Fig.4

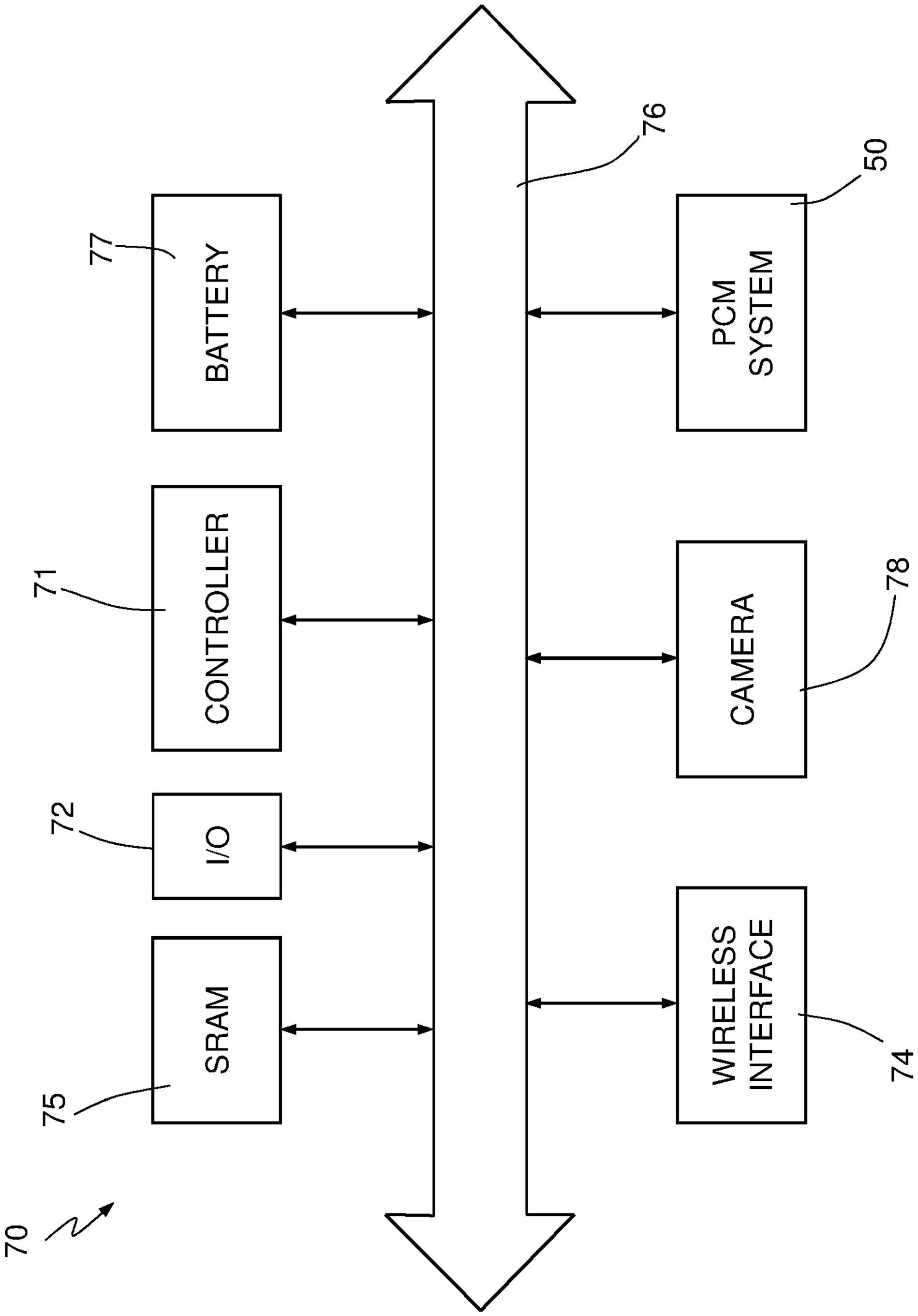
70
SRAM
75
I/O
72
CONTROLLER
71
BATTERY
77
76
PCM SYSTEM
50
CAMERA
78
WIRELESS INTERFACE
74

Fig.5

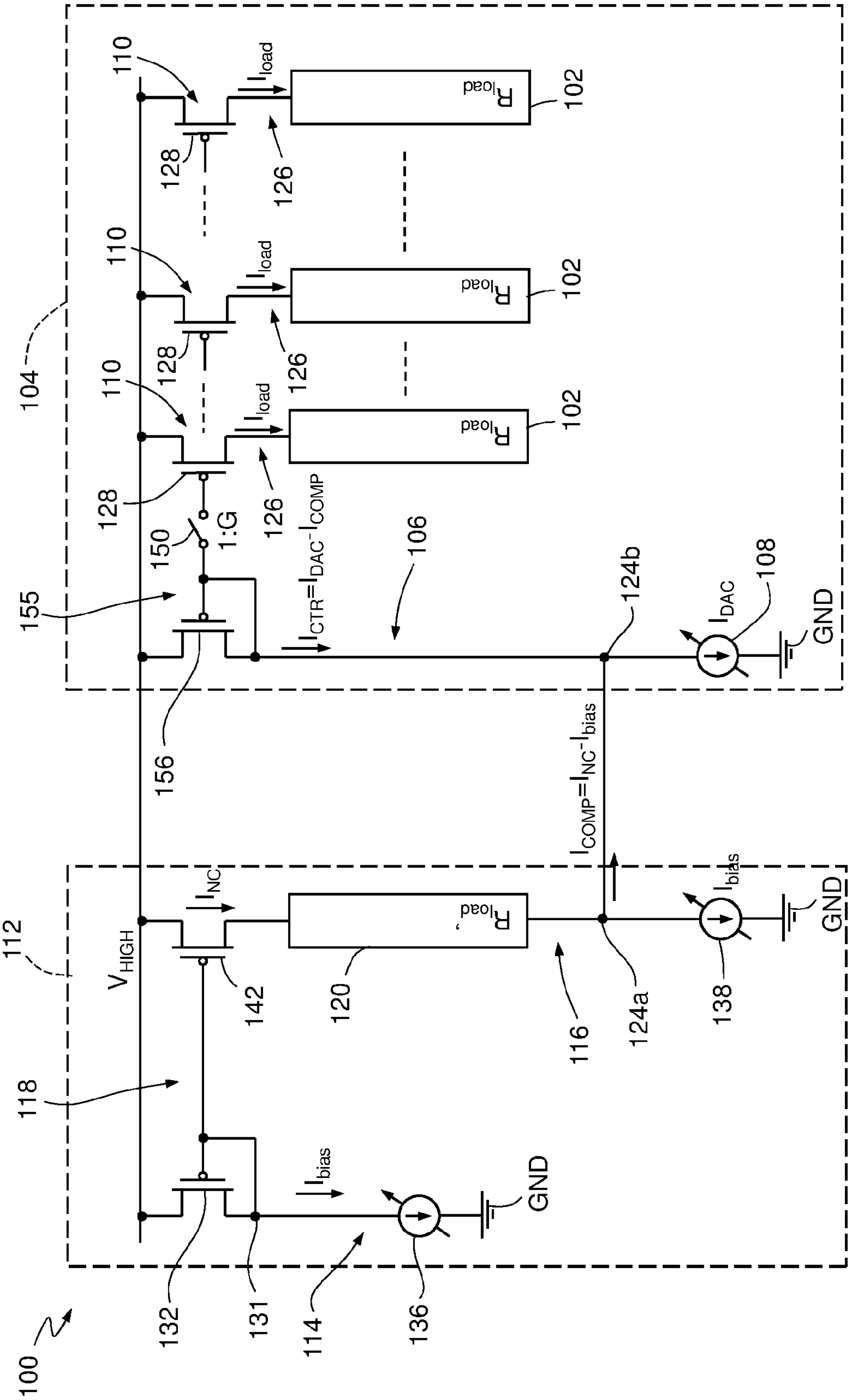
100
104
106
108
110
110
110
102
102
102
126
126
126
128
128
128
R_{load}
R_{load}
R_{load}
I_{load}
I_{load}
I_{load}
150
1:G
155
156
$I_{CTR}=I_{DAC}-I_{COMP}$
124b
I_{DAC}
GND
$I_{COMP}=I_{NC}-I_{bias}$
112
V_{HIGH}
I_{NC}
142
R_{load}'
120
116
124a
I_{bias}
138
GND
118
I_{bias}
GND
132
131
114
136

Fig.6

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EUROPEAN SEARCH REPORT

Application Number
EP 20 18 8675

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2008/298122 A1 (BEDESCHI FERDINANDO [IT] ET AL) 4 December 2008 (2008-12-04) * paragraph [0033] - paragraph [0053]; figure 4 * -----	1,9-13	INV. G11C5/14 G11C8/08 G11C13/00 G11C7/14
A	US 2013/229863 A1 (CONTE ANTONINO [IT] ET AL) 5 September 2013 (2013-09-05) * figure 6 * -----	1-13	
A	US 2009/091969 A1 (UEDA YOSHIHIRO [JP]) 9 April 2009 (2009-04-09) * abstract; figure 2 * -----	1-13	
			TECHNICAL FIELDS SEARCHED (IPC)
			G11C

The present search report has been drawn up for all claims

1

Place of search	Date of completion of the search	Examiner
The Hague	30 November 2020	Wolff, Norbert

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 20 18 8675

30-11-2020

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008298122 A1	04-12-2008	TW 200915323 A	01-04-2009
		US 2008298122 A1	04-12-2008
		WO 2008150693 A1	11-12-2008
US 2013229863 A1	05-09-2013	NONE	
US 2009091969 A1	09-04-2009	JP 5002401 B2	15-08-2012
		JP 2009093687 A	30-04-2009
		US 2009091969 A1	09-04-2009

REFERENCES CITED IN THE DESCRIPTION

Patent documents cited in the description

- US 2008298122 A **[0021]**
- US 2013229863 A **[0022]**
- US 2009091969 A **[0023]**