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(54) **SELECTIVE DEPOSITION OF NOBLE METAL THIN FILMS**

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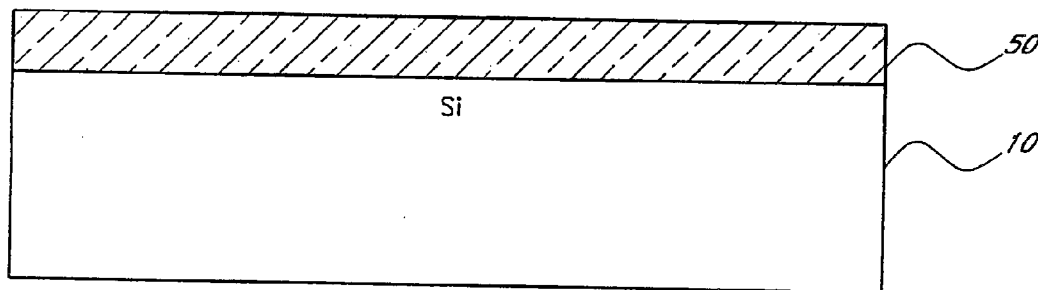
(52) **U.S. Cl.**
CPC ***C23C 16/45525*** (2013.01); ***C23C 16/34*** (2013.01); ***C23C 16/32*** (2013.01); ***C23C 16/38*** (2013.01); ***C23C 16/40*** (2013.01)

(57) **ABSTRACT**

Processes are provided for selectively depositing thin films comprising one or more noble metals on a substrate by vapor deposition processes. In some embodiments, atomic layer deposition (ALD) processes are used to deposit a noble metal containing thin film on a high-k material, metal, metal nitride or other conductive metal compound while avoiding deposition on a lower k insulator such as silicon oxide. The ability to deposit on a first surface, such as a high-k material, while avoiding deposition on a second surface, such as a silicon oxide or silicon nitride surface, may be utilized, for example, in the formation of a gate electrode.



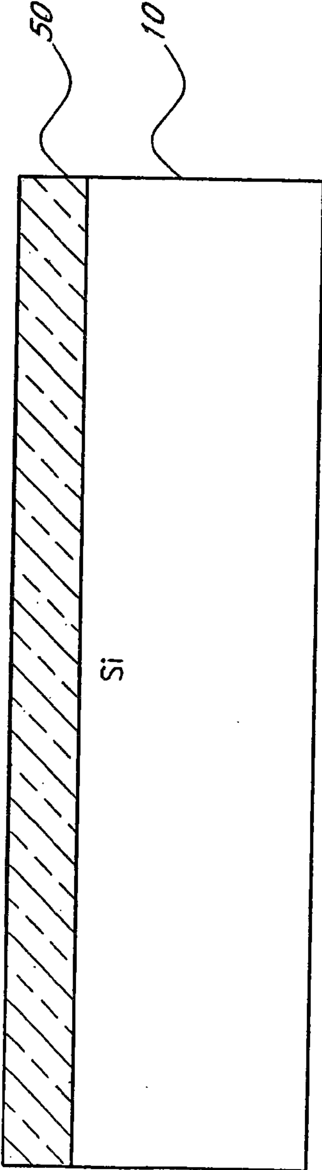


FIG. 1

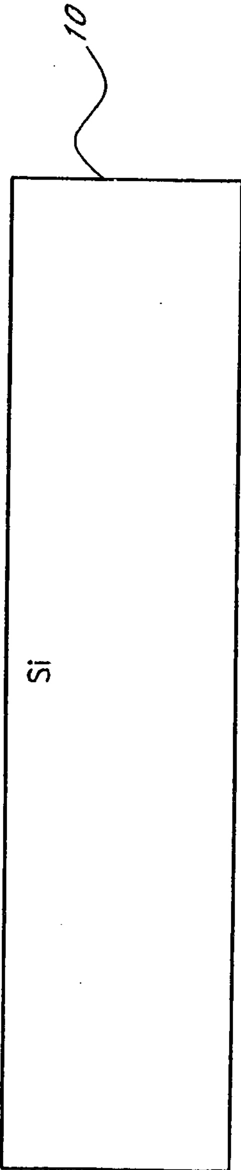


FIG. 2

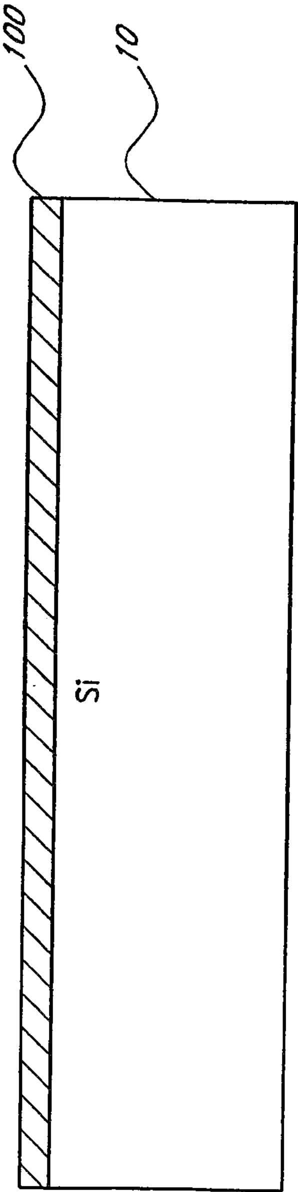


FIG. 3

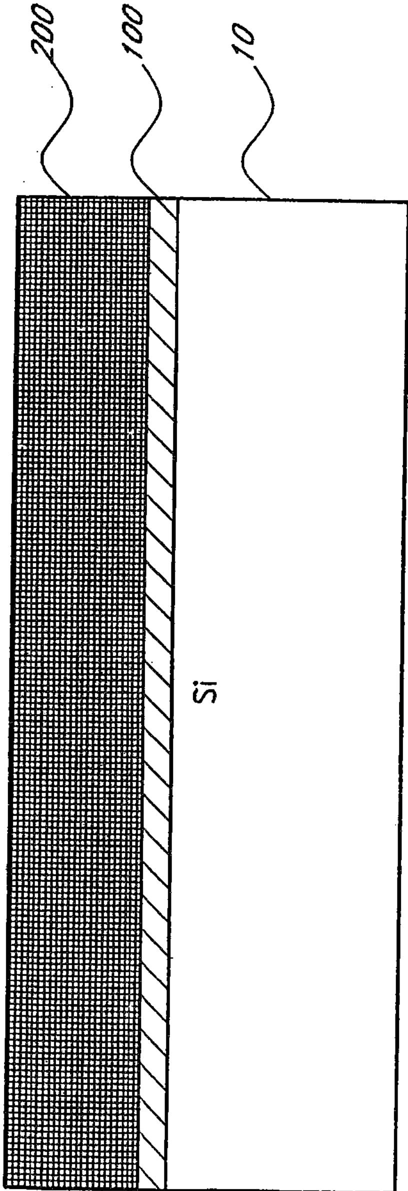


FIG. 4

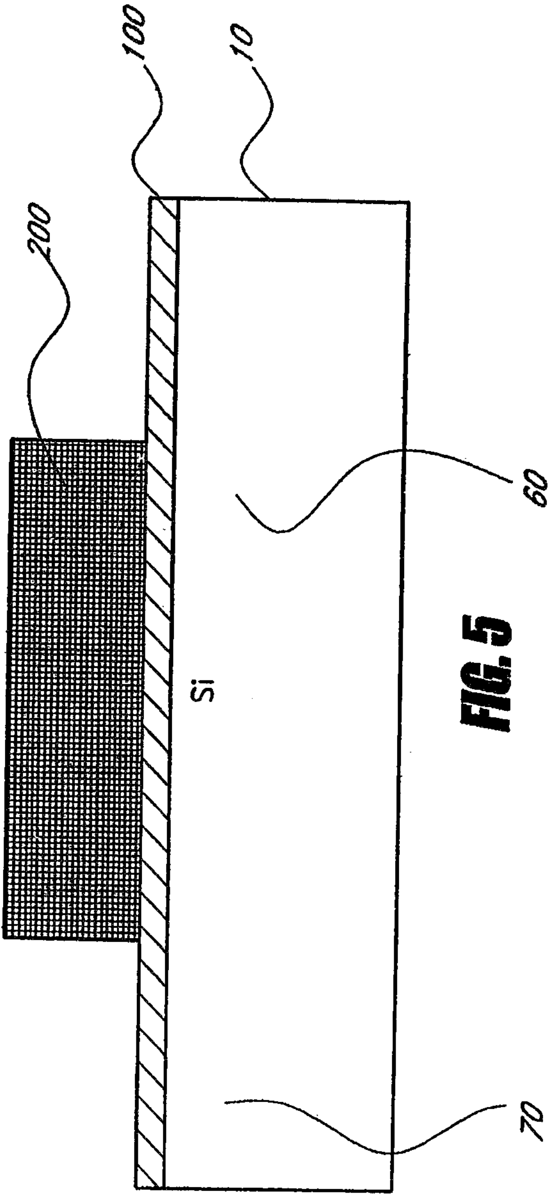


FIG. 5

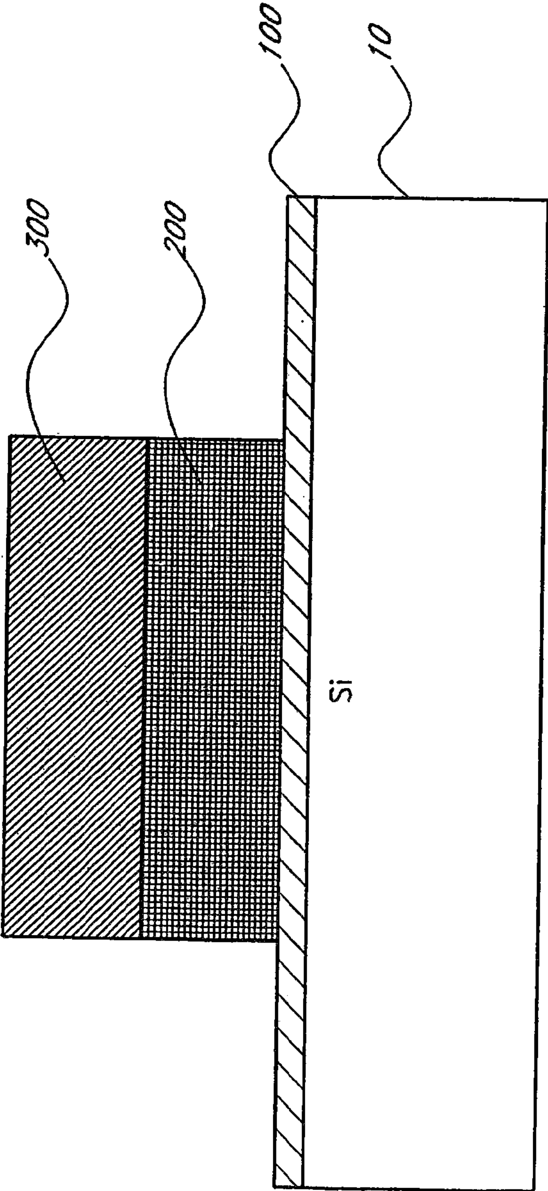


FIG. 6

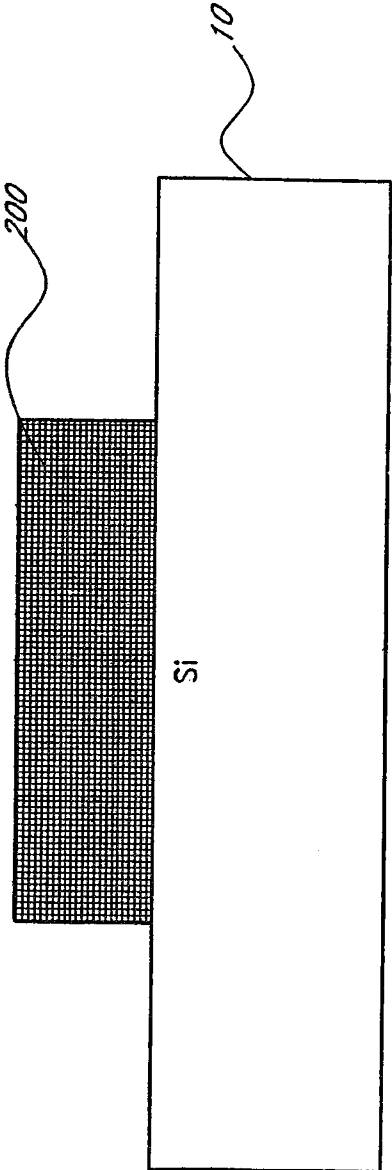


FIG. 7

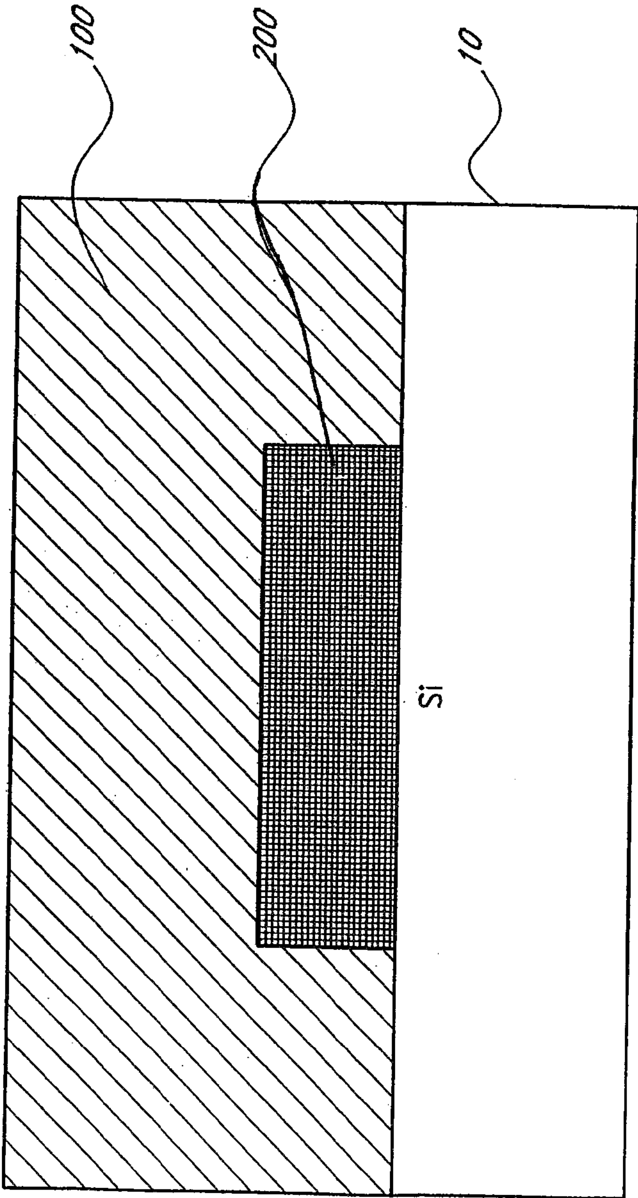


FIG. 8

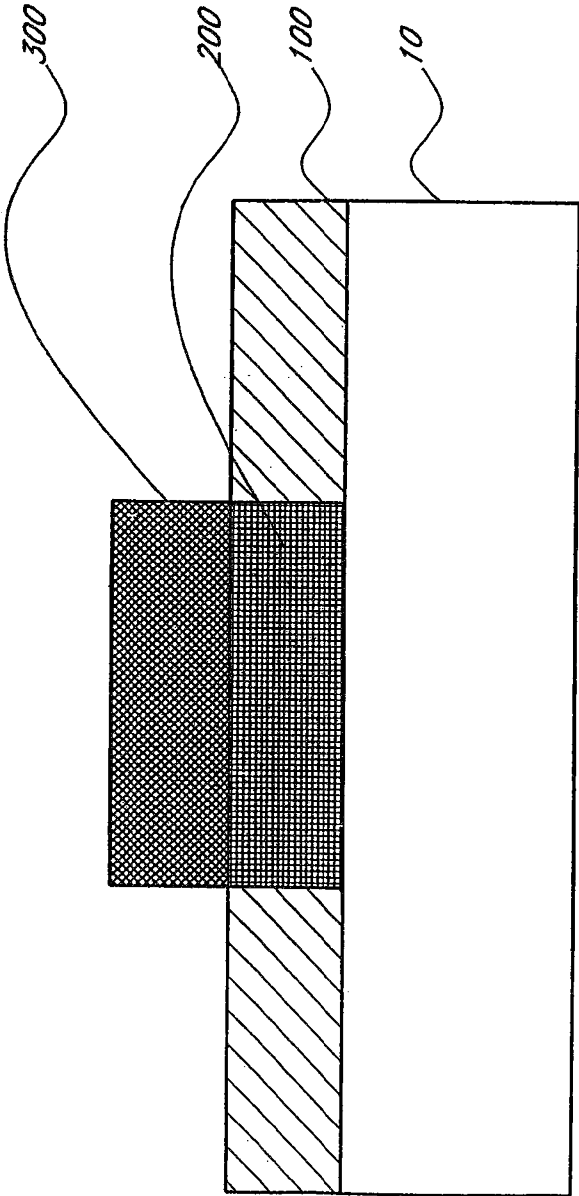


FIG. 9

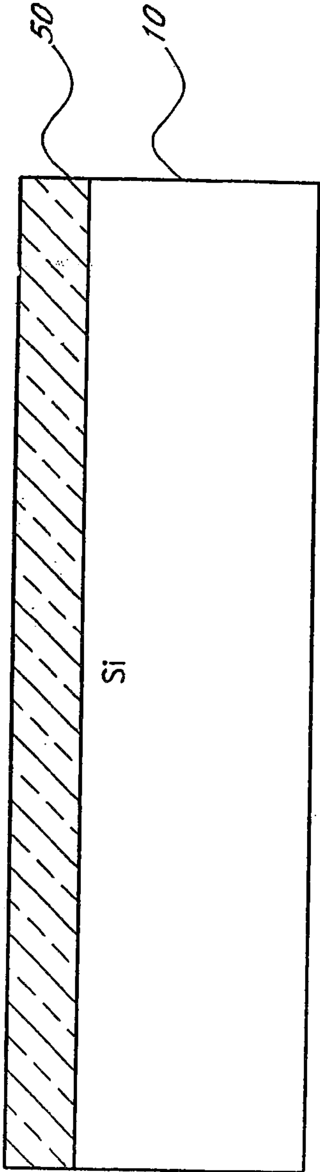


FIG. 10

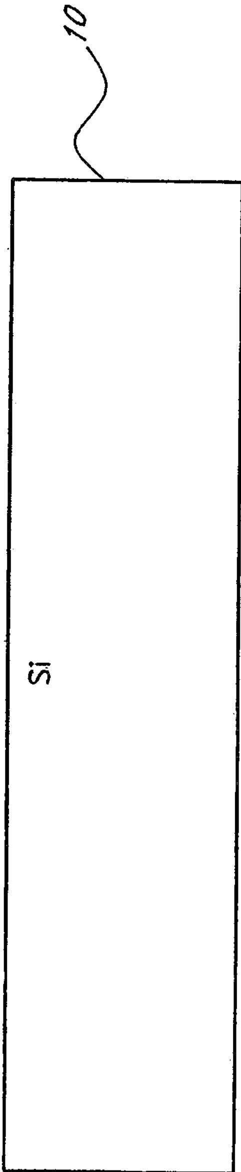


FIG. 11

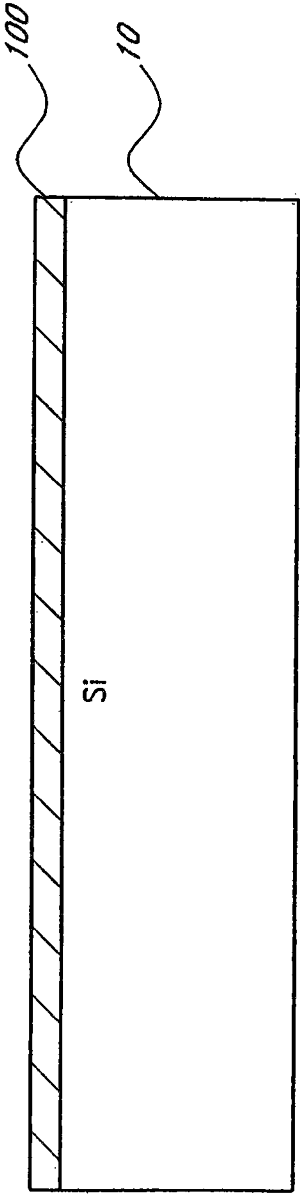


FIG. 12

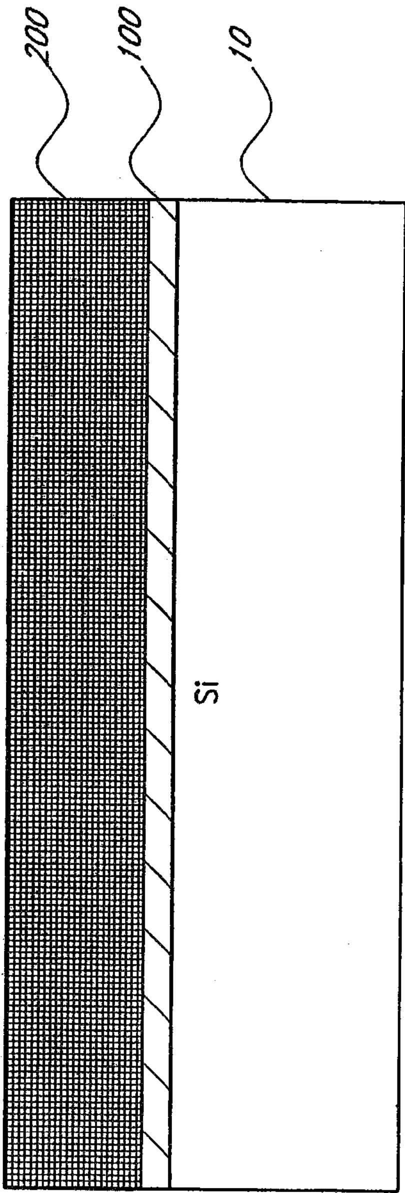


FIG. 13

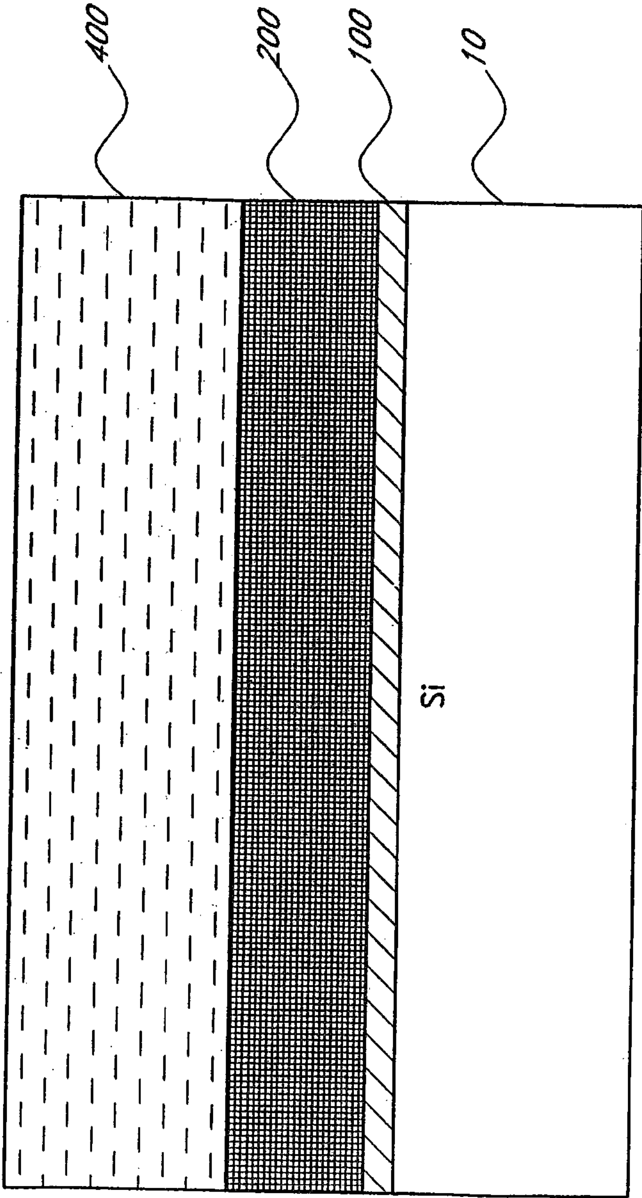


FIG. 14

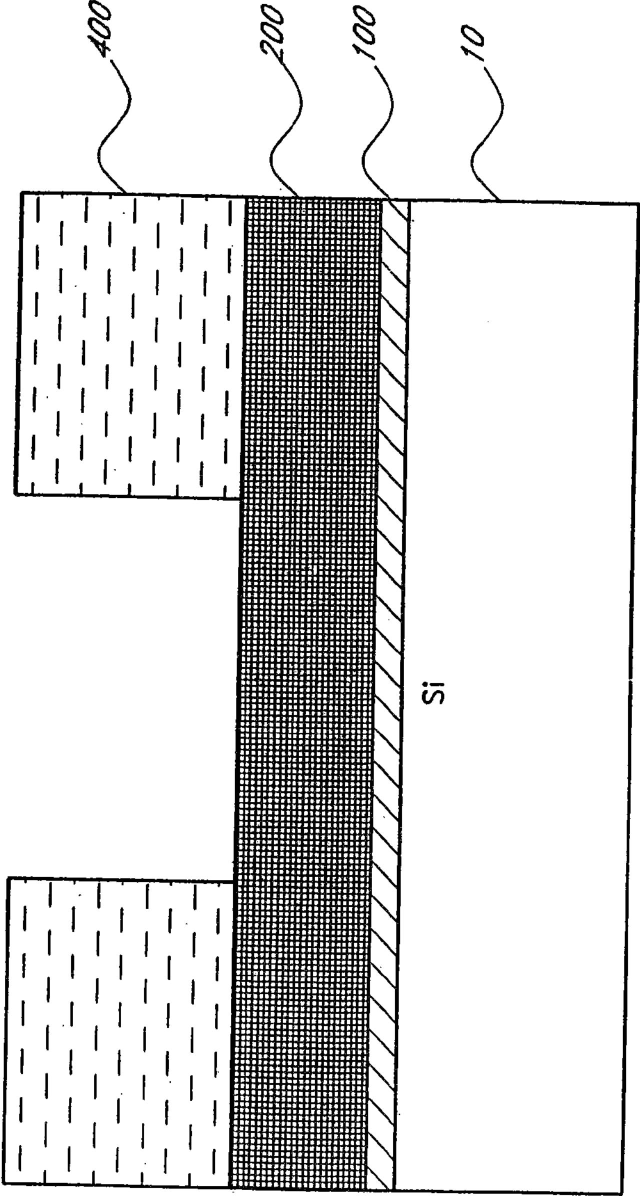


FIG. 15

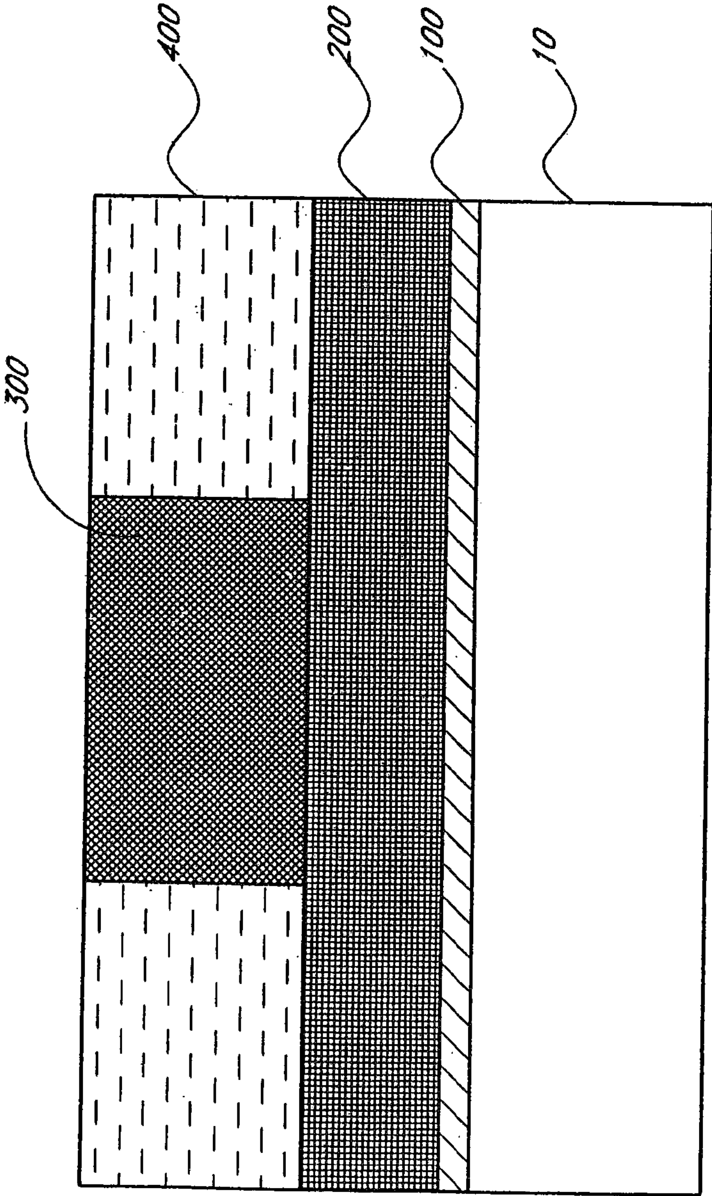


FIG 16A

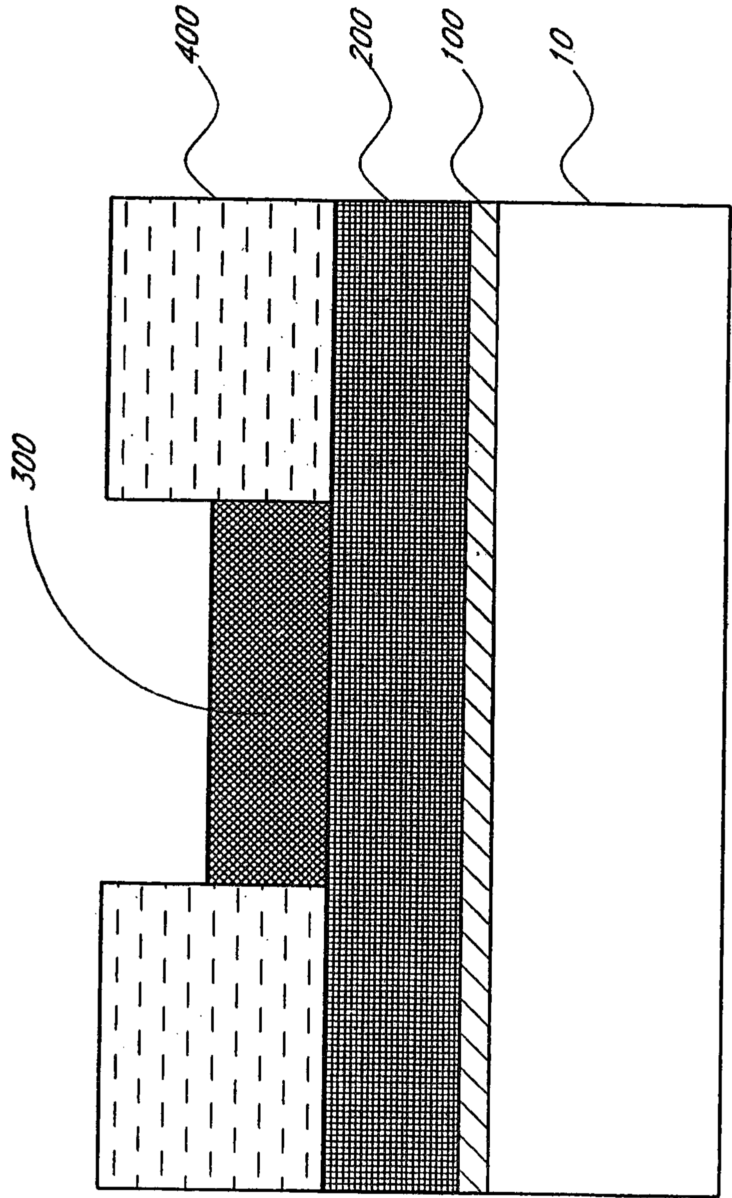


FIG. 16B

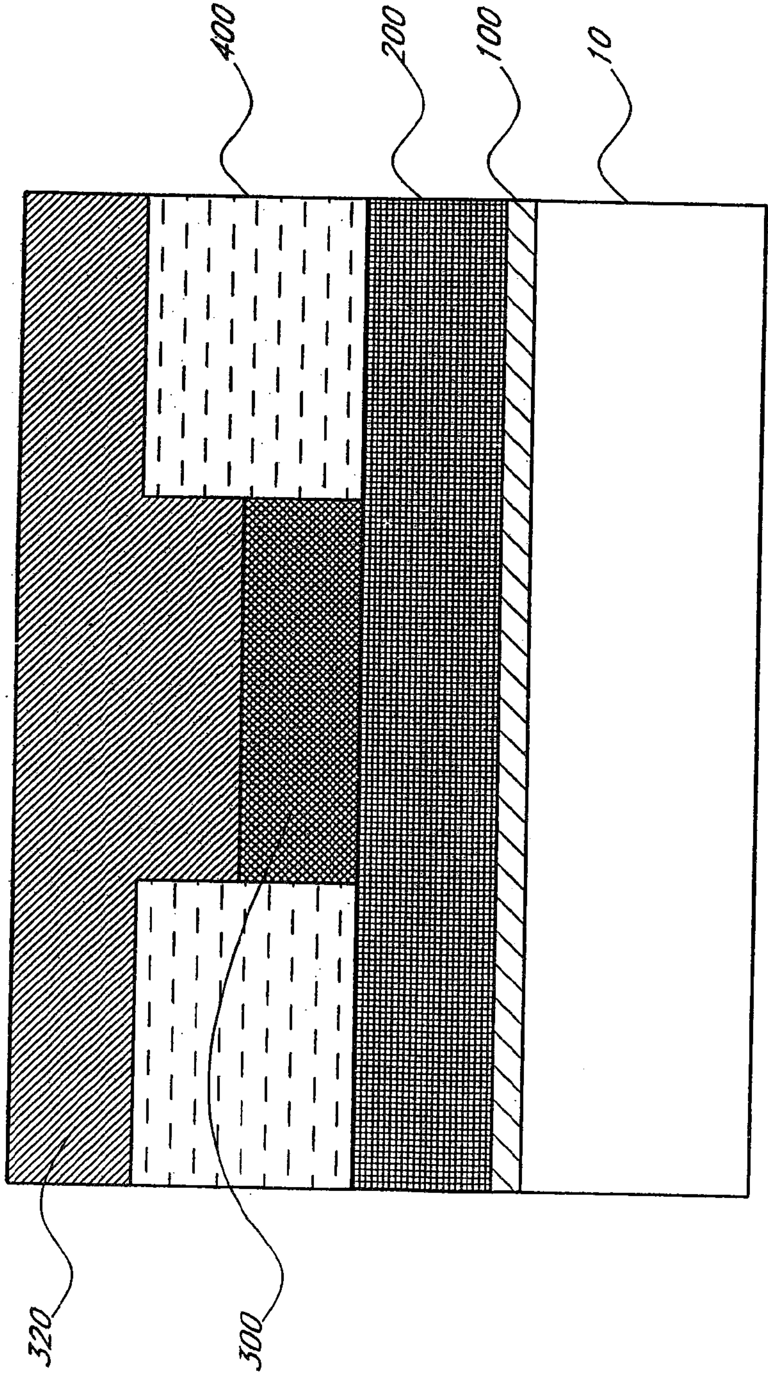


FIG. 16C

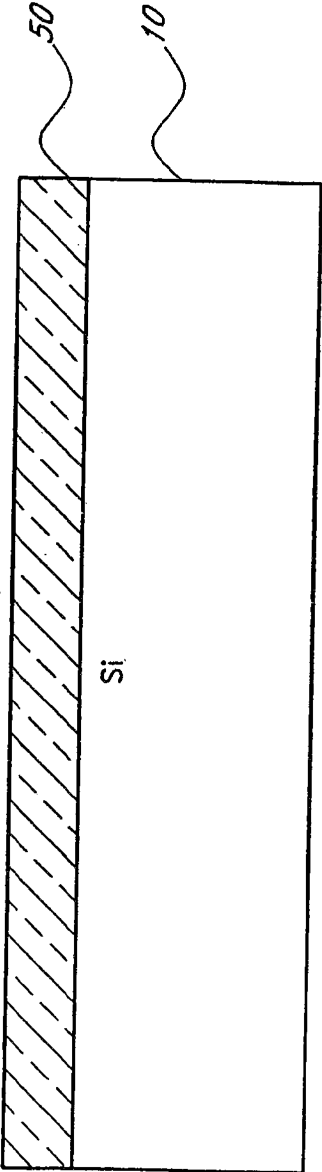


FIG. 17

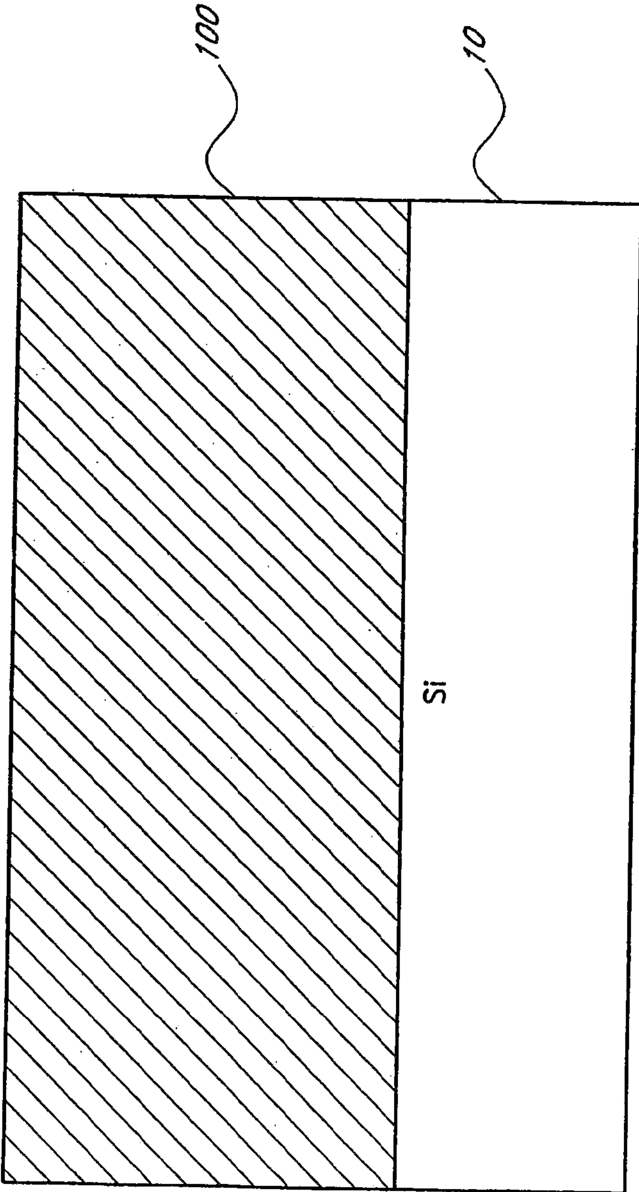


FIG. 18

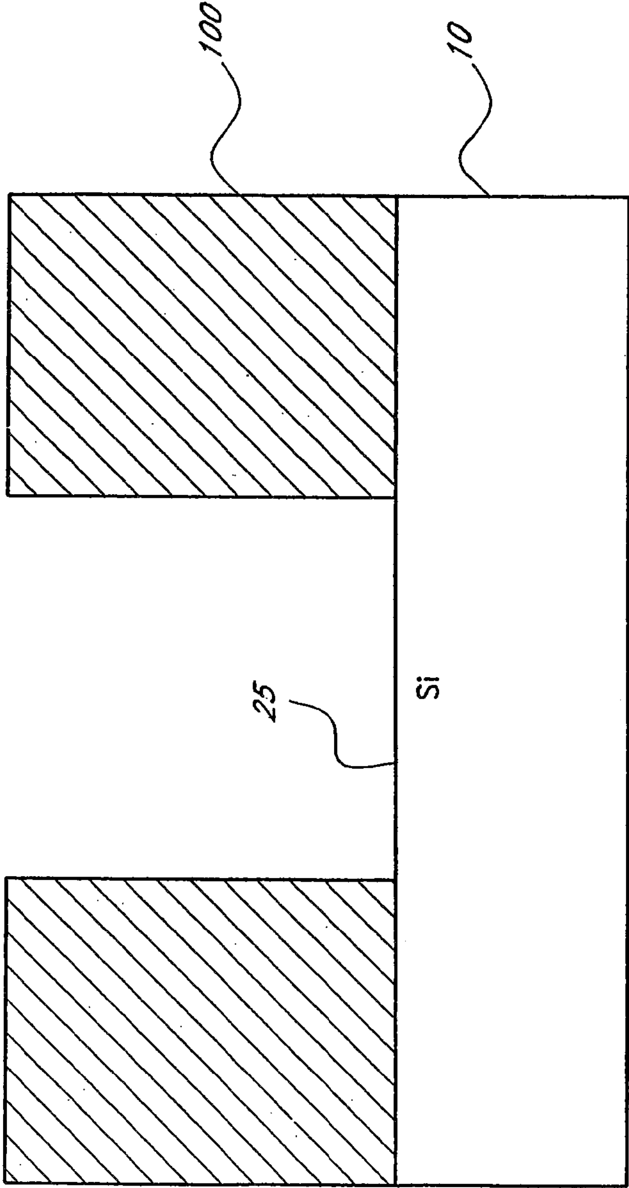


FIG. 19

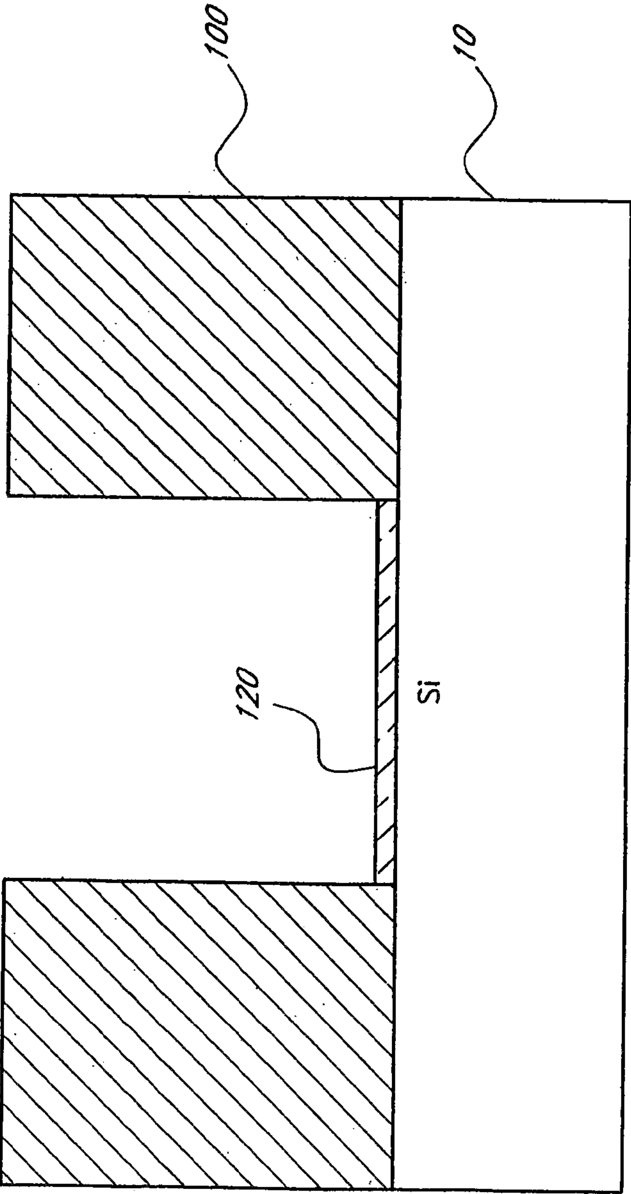


FIG. 20

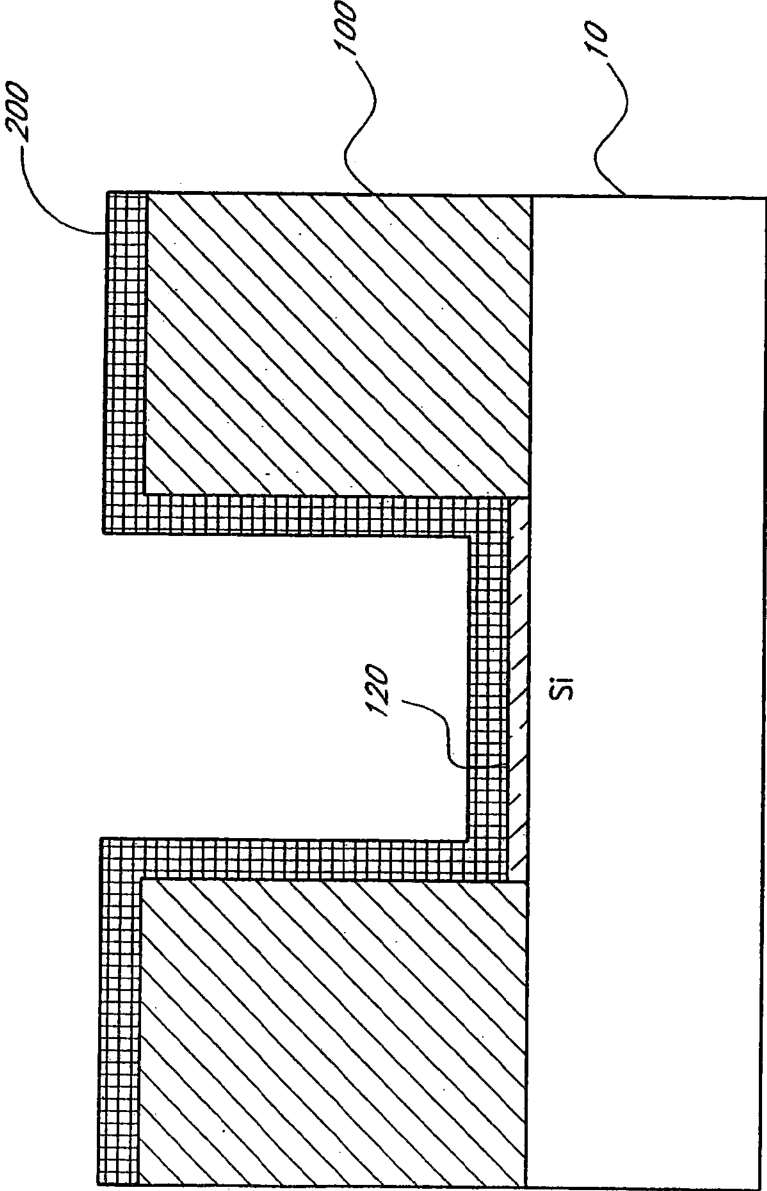


FIG. 21

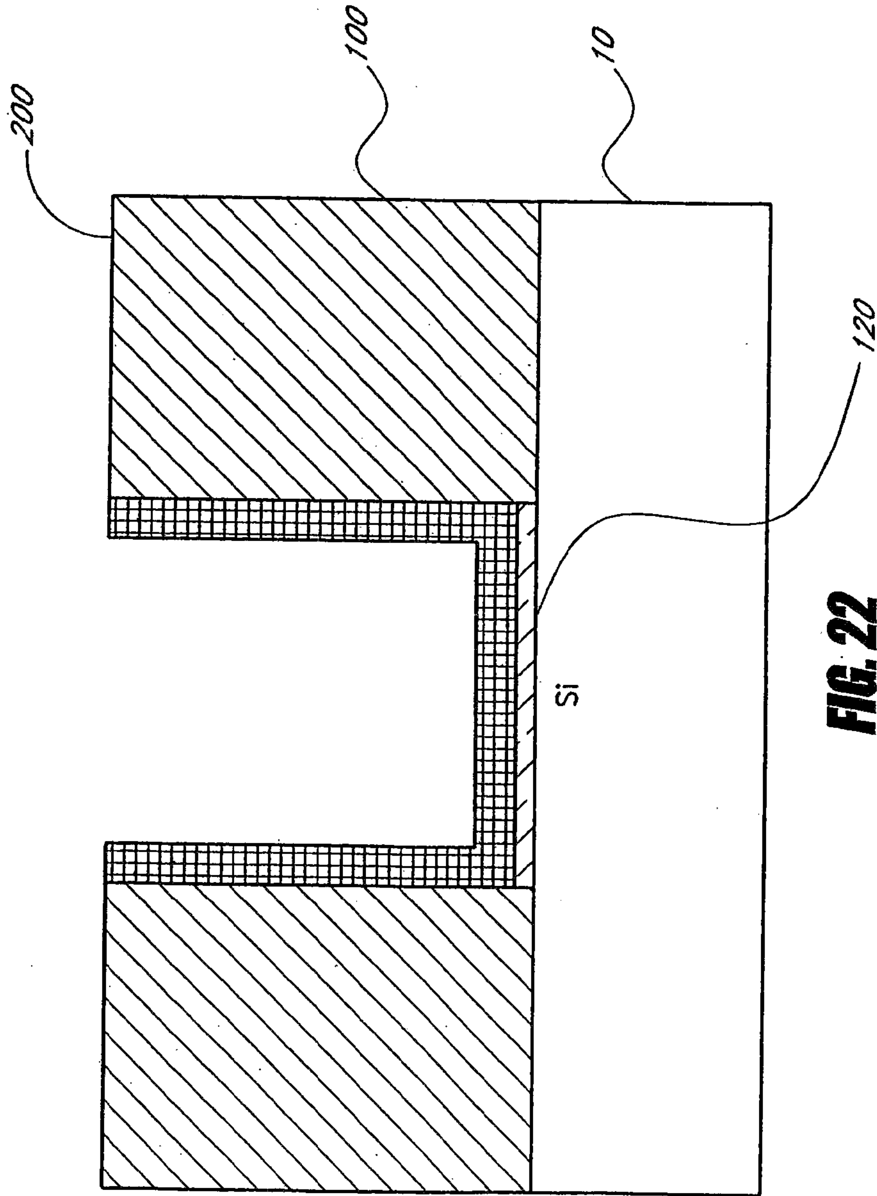


FIG. 22

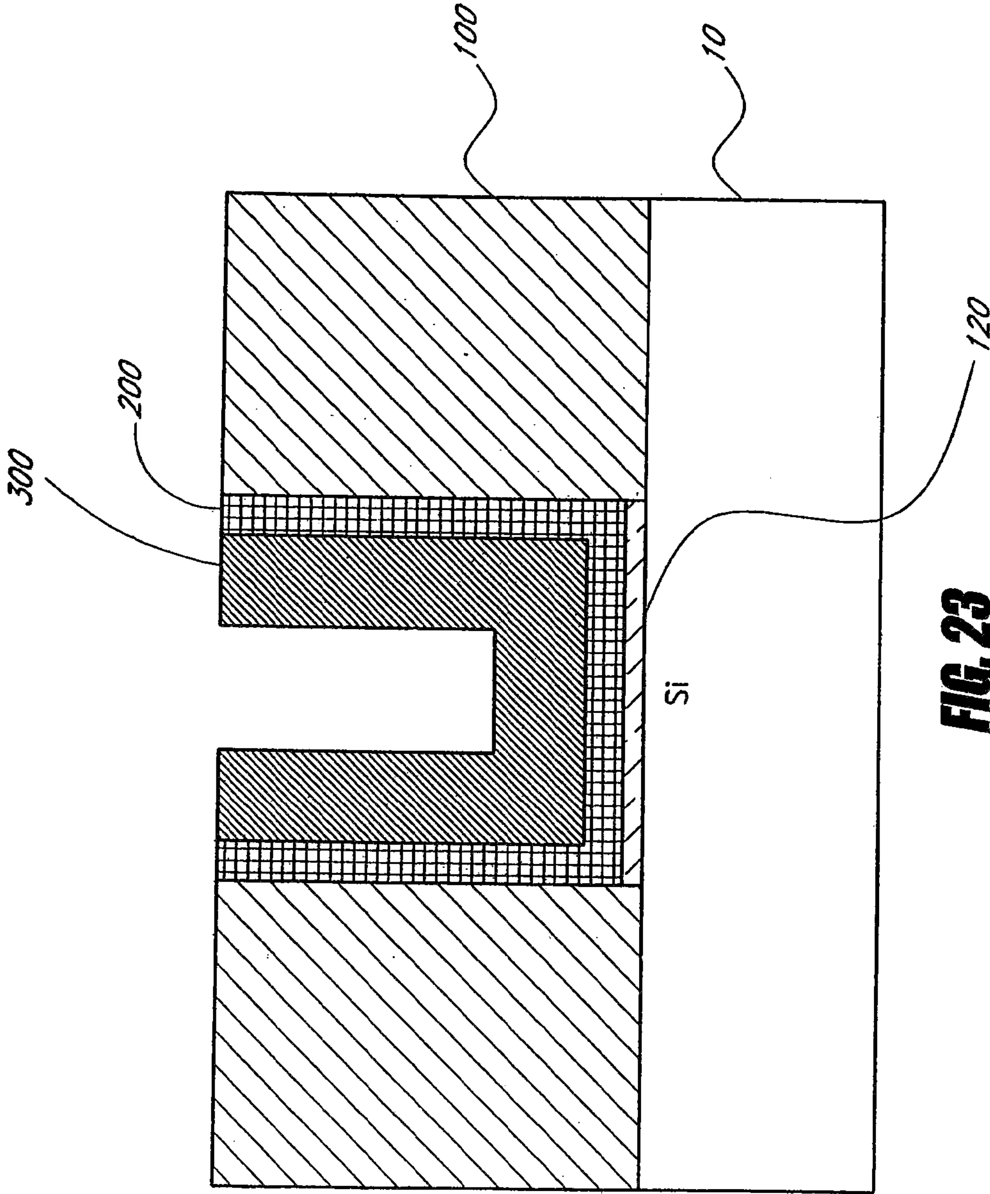


FIG. 23

SELECTIVE DEPOSITION OF NOBLE METAL THIN FILMS

REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 13/188,087 filed Jul. 21, 2011, which is a continuation of U.S. application Ser. No. 12/649,817 filed Dec. 30, 2009 and issued as U.S. Pat. No. 7,985,669, which is a continuation of U.S. application Ser. No. 11/376,704, filed Mar. 14, 2006 and issued as U.S. Pat. No. 7,666,773, which claims priority to U.S. provisional application No. 60/662,144, filed Mar. 15, 2005 and to U.S. provisional application No. 60/662,145, filed Mar. 15, 2005, each of which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Conductive thin films can be selectively deposited by vapor deposition processes, such as by atomic layer deposition type processes. Such films find use, for example, in integrated circuits (IC) and magnetic recording media.

[0004] 2. Description of the Related Art

[0005] Thin films of ruthenium and other noble metals can be used in a wide variety of applications including integrated circuits and magnetic recording media. For example, ruthenium may be used as an electrode material in transistors, particularly those where silicon oxide is replaced by high-k dielectrics. They can also be used as copper seed layers in metallization processes. Noble metals are advantageous because they tend not to oxidize or otherwise corrode.

[0006] Noble metal films can also be used for capacitor electrodes of dynamic random access memories (DRAMs). Noble metals are also a potential electrode material for non-volatile ferroelectric memories.

[0007] In addition to electrode applications, thin noble metal films find potential use in magnetic recording technology. In anti-ferromagnetically coupled recording media, for example, a thin Ru film may be used for separating two ferromagnetic layers.

SUMMARY OF THE INVENTION

[0008] Thin films of noble metals can be selectively deposited using vapor deposition processes, such as atomic layer deposition (ALD). In some embodiments, a preferred ALD process comprises alternately contacting a first surface and a second surface of a substrate with a noble metal precursor and a second reactant, such that a thin noble metal film is selectively formed on the first surface relative to the second surface. The first surface may be, for example, a high-k material, a metal or a conductive metal compound, such as a metal nitride or metal oxide. The second surface preferably comprises a lower k insulator, such as a form of silicon oxide or silicon nitride. For example and without limitation, the second surface may comprise SiO_2 or silicon oxynitride. The atomic layer deposition reactions are preferably carried out at a temperature less than about 400° C., more preferably less than about 350° C.

[0009] In some preferred embodiments, a gate electrode is formed by a method comprising depositing and patterning a gate dielectric layer and selectively depositing a noble metal such as ruthenium over the gate dielectric layer by a vapor phase deposition process, preferably an atomic layer deposition process.

[0010] In other preferred methods for forming a gate electrode on a silicon substrate, an interface layer is formed on the substrate. The interface layer may comprise, for example, silicon oxide or silicon nitride. A layer of high-k material is deposited over the interface layer and patterned. Ruthenium or another noble metal is selectively deposited over the high-k material by a vapor deposition process, more preferably an atomic layer deposition process.

[0011] ALD processes for depositing noble metal preferably comprise contacting the substrate with alternating and sequential pulses of a noble metal precursor, such as a ruthenium precursor, and a second reactant, such as an oxygen precursor. The noble metal precursor is preferably a cyclopentadienyl compound, more preferably an ethyl cyclopentadienyl compound, such as $Ru(EtCp)_2$.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGS. **1-6** are schematic cross-sections of partially fabricated integrated circuits, illustrating a process flow for the formation of a gate electrode utilizing a selective noble metal deposition process.

[0013] FIGS. **7-9** are schematic cross-sections of partially fabricated integrated circuits, illustrating another process flow for the formation of a gate electrode utilizing a selective noble metal deposition process.

[0014] FIGS. **10-15**, **16**A, **16**B and **16**C are schematic cross-sections of partially fabricated integrated circuits, illustrating a gate-last process flow for the formation of a gate electrode utilizing selective noble metal deposition.

[0015] FIGS. **17-23** are schematic cross-sections of partially fabricated integrated circuits, illustrating another gate-last process flow for the formation of a gate electrode utilizing selective noble metal deposition.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] Ruthenium thin films and thin films comprising other noble metals can be selectively deposited on a substrate by vapor phase deposition processes, such as atomic layer deposition (ALD) type processes. The substrate includes at least a first surface and a second surface, which differ in material composition and properties. The first surface is preferably susceptible to the vapor phase deposition process, such as an ALD process, used to form the desired noble metal layer while the second surface is substantially insensitive to the same deposition process. As a result, the noble metal is selectively deposited on the first surface relative to the second surface. In some embodiments deposition occurs on the first surface but not on the second surface. However, although the film is deposited selectively on the first surface, some deposition on the second surface is possible. Thus, in other embodiments deposition occurs to a greater extent on the first surface than the second surface in a given time.

[0017] At temperatures less than 450° C., noble metals are readily deposited on many high-k materials, metals, metal nitrides, and other conductive metal compounds from vapor phase reactants. For example, they can be deposited by ALD. However, they are not readily deposited on lower k materials, such as silicon oxides and silicon nitrides. Thus, in particular embodiments, a thin film containing noble metal is selectively deposited on a first surface comprising a high-k material while avoiding deposition on a second surface comprising a lower k insulator such as a silicon oxide, silicon nitride,

silicon oxynitride, fluorinated silica glass (FSG), carbon doped silicon oxide (SiOC) or material containing more than 50% of silicon oxide. In other embodiments the thin film comprising one or more noble metals is selectively deposited on a first surface comprising a metal, metal nitride, metal carbide, metal boride, other conductive metal compound or mixtures thereof, while avoiding deposition on a second surface comprising an insulating material., such as a low k insulator In preferred embodiments an ALD type process is employed to selectively deposit the noble metal containing film.

[0018] "High-k" generally refers to a dielectric material having a dielectric constant (k) value greater than that of silicon oxide. Preferably, the high-k material has a dielectric constant greater than 5, more preferably greater than about 10. Exemplary high-k materials include, without limitation, HfO_2, ZrO_2, Al_2O_3, TiO_2, Ta_2O_5, lanthanide oxides and mixtures thereof, silicates and materials such as YSZ (yttria-stabilized zirconia), BST, BT, ST, and SBT.

[0019] Metals, metal nitrides, metal carbides, metal borides, conductive oxides and other conductive metal compounds that can serve as substrate materials over which noble metals can be selectively deposited may include, for example and without limitation, selected from the group consisting of Ta, TaN, TaC_x, TaB_x, Ti, TiN, TiC_x, TiB_x, Nb, NbN, NbC_x, NbB_x Mo, MoN, MoC_x, MoB_x, W, WN, WC_x, WB_x, V, Cr, Fe, Cu, Co, Ni, Cd, Zn, Al, Ag, Au, Ru, RuO_x, Rh, Pt, Pd, Ir, IrO_x and Os.

[0020] While illustrated in the context of formation of a gate electrode by ALD, the skilled artisan will readily find application for the principles and advantages disclosed herein in other contexts, particularly where selective deposition is desired with high step coverage.

[0021] ALD type processes are based on controlled, self-limiting surface reactions of the precursor chemicals. Gas phase reactions are avoided by feeding the precursors alternately and sequentially into the reaction chamber. Vapor phase reactants are separated from each other in the reaction chamber, for example, by removing excess reactants and/or reactant by-products from the reaction chamber between reactant pulses. This may be accomplished with an evacuation step and/or with an inactive gas pulse or purge.

[0022] Briefly, the substrate is loaded in a reaction chamber and is heated to a suitable deposition temperature, generally at lowered pressure. Deposition temperatures are maintained below the precursor thermal decomposition temperature but at a high enough level to avoid condensation of reactants and to provide the activation energy for the desired surface reactions. Of course, the appropriate temperature window for any given ALD reaction will depend upon the surface termination and reactant species involved. Here, the temperature is also maintained low enough to ensure the selectivity of the deposition process. Preferably, the temperature is below about 450° C., more preferably below about 350° C., as discussed in more detail below.

[0023] A first reactant is conducted into the chamber in the form of gas phase pulse and contacted with the surface of the substrate. Preferably the deposition process is self-limiting. For ALD embodiments, conditions are selected such that no more than about one monolayer of the precursor is adsorbed on the substrate surface in a self-limiting manner. Excess first reactant and reaction byproducts, if any, are purged from the reaction chamber, often with a pulse of inert gas such as nitrogen or argon.

[0024] For ALD embodiments, the second gaseous reactant is pulsed into the chamber where it reacts with the first reactant adsorbed to the surface. Excess second reactant and gaseous by-products of the surface reaction are purged out of the reaction chamber, preferably with the aid of an inert gas. The steps of pulsing and purging are repeated until a thin film of the desired thickness has been selectively formed on the substrate, with each cycle leaving no more than a molecular monolayer.

[0025] As mentioned above, each pulse or phase of each cycle is preferably self-limiting. An excess of reactant precursors is supplied in each phase to saturate the susceptible structure surfaces. Surface saturation ensures reactant occupation of all available reactive sites (subject, for example, to physical size or "steric hindrance" restraints) and thus excellent step coverage.

[0026] According to a preferred embodiment, a noble metal thin film is selectively deposited on a first surface of a substrate relative to a second surface by an ALD type process comprising multiple pulsing cycles, each cycle comprising:

> **[0027]** pulsing a vaporized noble metal precursor into the reaction chamber to form a molecular layer of the metal precursor on the first surface of the substrate,
>
> **[0028]** purging the reaction chamber to remove excess noble metal precursor and reaction by products, if any,
>
> **[0029]** providing a pulse of a second reactant, such as an oxygen, ozone, ammonia or ammonia plasma product containing gas onto the substrate,
>
> **[0030]** purging the reaction chamber to remove excess second reactant and any gaseous by-products formed in the reaction between the metal precursor layer on the first surface of the substrate and the second reactant, and
>
> **[0031]** repeating the pulsing and purging steps until a noble metal thin film of the desired thickness has been formed.

[0032] The noble metal thin film typically comprises multiple monolayers of a single noble metal. However, in other embodiments, the final metal structure may comprise noble metal compounds or alloys comprising two or more different noble metals. For example, the growth can be started with the deposition of platinum and ended with the deposition of ruthenium metal. Noble metals are preferably selected from the group consisting of Pt, Au, Ru, Rh, Ir, Pd and Ag.

[0033] The substrate can comprise various types of materials. When manufacturing integrated circuits, the substrate typically comprises a number of thin films with varying chemical and physical properties. In preferred embodiments, at least one surface of the substrate is insensitive to the vapor phase deposition reaction. Preferably, this surface comprises a form of silicon oxide or a silicon nitride, such as silicon oxynitride. At least one other surface of the substrate is sensitive to the deposition reaction and may be, for example and without limitation, a dielectric layer, such as aluminum oxide or hafnium oxide, a metal, such as Ta, or a metal nitride, such as TaN. Further, the substrate surface may have been patterned and may comprise structures such as nodes, vias and trenches.

[0034] Suitable noble metal precursors may be selected by the skilled artisan. In general, metal compounds where the metal is bound or coordinated to oxygen, nitrogen, carbon or a combination thereof are preferred. More preferably metallocene compounds, beta-diketonate compounds and acetamidinato compounds are used. In some embodiments a cyclo-

pentadienyl precursor compound is used, preferably a bis (ethylcyclopentadienyl) compound.

[0035] When depositing ruthenium (Ru) thin films, preferred metal precursors may be selected from the group consisting of bis(cyclopentadienyl)ruthenium, tris(2,2, 6, 6-tetramethyl-3,5 -heptanedionato)ruthenium and tris(N,N'-diisopropylacetamidinato)ruthenium(III) and their derivatives, such as bis(N,N'-diisopropylacetamidinato)ruthenium(II) dicarbonyl, bis(ethylcyclopentadienyl)ruthenium, bis(pentamethylcyclopentadienyl)ruthenium and bis (2,2,6,6-tetramethyl-3,5-heptanedionato) (1,5-cyclooctadiene)ruthenium(II). In preferred embodiments, the precursor is bis(ethylcyclopentadienyl) ruthenium ($Ru(EtCp)_2$).

[0036] When depositing platinum films, preferred metal precursors include (trimethyl)methylcyclopentadienylplatinum(IV), platinum (II) acetylacetonato, bis(2,2,6,6-tetramethyl-3,5-heptanedionato)platinum(TI) and their derivatives.

[0037] As mentioned above, ALD processes for depositing noble metal containing films typically comprise alternating pulses of a noble metal precursor and an oxygen-containing reactant. The oxygen-containing reactant pulse may be provided, for example, by pulsing diatomic oxygen gas or a mixture of oxygen and another gas into the reaction chamber. In one embodiment, ammonia plasma products or ammonia is used as a second reactant. In other embodiments, oxygen is formed inside the reactor, such as by decomposing oxygen containing chemicals. Oxygen containing chemicals that can be decomposed in the reactor to produce oxygen include, without limitation, H_2O_2, N_2O and organic peroxides. Mixtures of such chemicals can also be used. In other embodiments, the catalytic formation of an oxygen containing pulse can be provided by introducing into the reactor a pulse of vaporized aqueous solution of H_2O_2 and conducting the pulse over a catalytic surface inside the reactor and thereafter into the reaction chamber. The catalytic surface is preferably a piece of platinum or palladium.

[0038] In preferred embodiments the oxygen-containing reagent comprises free-oxygen or ozone, more preferably molecular oxygen. The oxygen-containing reagent is preferably pure molecular diatomic oxygen, but can also be a mixture of oxygen and inactive gas, for example, nitrogen or argon.

[0039] A preferred oxygen-containing reagent is air.

[0040] The noble metal precursor employed in the ALD type processes may be solid, liquid or gaseous material, provided that the metal precursor is in vapor phase before it is conducted into the reaction chamber and contacted with the substrate surface. “Pulsing” a vaporized precursor onto the substrate means that the precursor vapor is conducted into the chamber for a limited period of time. Typically, the pulsing time is from about 0.05 to 10 seconds. However, depending on the substrate type and its surface area, the pulsing time may be even higher than 10 seconds. Preferably, for a 300 mm wafer in a single wafer ALD reactor, the noble metal precursor is pulsed for from 0.05 to 10 seconds, more preferably for from 0.5 to 3 seconds and most preferably for about 0.5 to 1.0 seconds. The oxygen-containing precursor is preferably pulsed for from about 0.05 to 10 seconds, more preferably for from 1 to 5 seconds, most preferably about for from 2 to 3 seconds. Pulsing times can be on the order of minutes in some cases. The optimum pulsing time can be readily determined by the skilled artisan based on the particular circumstances.

[0041] The mass flow rate of the noble metal precursor can be determined by the skilled artisan. In one embodiment, for deposition on 300 mm wafers the flow rate of noble metal precursor is preferably between about 1 and 1000 sccm without limitation, more preferably between about 100 and 500 sccm. The mass flow rate of the noble metal precursor is usually lower than the mass flow rate of oxygen, which is usually between about 10 and 10000 sccm without limitation, more preferably between about 100-2000 sccm and most preferably between 100-1000 sccm.

[0042] Purging the reaction chamber means that gaseous precursors and/or gaseous byproducts formed in the reaction between the precursors are removed from the reaction chamber, such as by evacuating the chamber with a vacuum pump and/or by replacing the gas inside the reactor with an inert gas such as argon or nitrogen. Typical purging times are from about 0.05 to 20 seconds, more preferably between about 1 and 10, and still more preferably between about 1 and 2 seconds.

[0043] The pressure in the reaction space is typically between about 0.01 and 20 mbar, more preferably between about 1 and 10 mbar.

[0044] Before starting the deposition of the film, the substrate is typically heated to a suitable growth temperature. Preferably, the growth temperature of the metal thin film is between about 150° C. and about 450° C., more preferably between about 200° C. and about 400° C. The preferred deposition temperature may vary depending on a number of factors such as, and without limitation, the reactant precursors, the pressure, flow rate, the arrangement of the reactor, and the composition of the substrate including the nature of the material to be deposited on and the nature of the material on which deposition is to be avoided. The specific growth temperature may be selected by the skilled artisan using routine experimentation in view of the present disclosure to maximize the selectivity of the process.

[0045] The processing time depends on the thickness of the layer to be produced and the growth rate of the film. In ALD, the growth rate of a thin film is determined as thickness increase per one cycle. One cycle consists of the pulsing and purging steps of the precursors and the duration of one cycle is typically between about 0.2 and 30 seconds, more preferably between about 1 and 10 seconds, but it can be on order of minutes or more in some cases.

[0046] Examples of suitable reactors that may be used for the deposition of thin films according to the processes of the present invention include commercially available ALD equipment such as the F-120® reactor, Pulsar® reactor and EmerALD™ reactor, available from ASM America, Inc of Phoenix, Ariz. In addition to these ALD reactors, many other kinds of reactors capable of ALD growth of thin films, including CVD reactors equipped with appropriate equipment and means for pulsing the precursors, can be employed for carrying out the processes of the present invention. Preferably, reactants are kept separate until reaching the reaction chamber, such that shared lines for the precursors are minimized. However, other arrangements are possible, such as the use of a pre-reaction chamber as described in U.S. application Ser. No. 10/929,348, filed Aug. 30, 2004 and 09/836,674, filed Apr. 16, 2001, incorporated herein by reference.

[0047] The growth processes can optionally be carried out in a reactor or reaction space connected to a cluster tool. In a cluster tool, because each reaction space is dedicated to one type of process, the temperature of the reaction space in each

module can be kept constant, which clearly improves the throughput compared to a reactor in which is the substrate is heated up to the process temperature before each run.

Formation of Gate Electrodes Using Selective Deposition

[0048] The ability to deposit on a first surface, such as a high-k material, while avoiding deposition on a second surface, such as a silicon oxide or a silicon nitride surface, can be utilized in the formation of a gate electrode.

[0049] Several embodiments are illustrated in FIGS. **1** through **21**. Other processes that take advantage of the ability to selectively deposit noble metals will be apparent to the skilled artisan.

[0050] In FIG. **1**, a silicon substrate **10** is illustrated comprising a layer of native oxide **50**. The native oxide **50** is removed by etching, leaving the bare substrate **10** as shown in FIG. **2**. The surface of the substrate is then prepared for deposition of a high-k layer by ALD, such as by the deposition of a thin interfacial layer. For example, a thin chemical oxide or oxynitride may be formed on the surface. In other embodiments a thermal oxide is grown on the substrate. In one embodiment the thin interfacial layer is from about 2 to about 15 angstroms thick. FIG. **3** illustrates a thin layer interfacial layer **100** of Silicon oxide grown over the substrate **10**.

[0051] A thin layer of high-k material **200** is subsequently deposited over the interfacial layer **100** to form the structure illustrated in FIG. **4**. The high-k material **200** is then patterned such that it remains over the channel region **60** and not over the regions **70** that will become the source and drain, as illustrated in FIG. **5**. Finally, a layer of Ru **300** is selectively deposited over the patterned high-k material **200** by a vapor deposition process, preferably ALD, and patterned (if necessary or desired) to form the structure illustrated in FIG. **6**.

[0052] In some embodiments the Ru forms the gate electrode. In other embodiments (not shown) another conductive material, such as a metal or poly-Si, is deposited over the selectively deposited Ru. In some embodiments the additional conductive material is selectively deposited over the ruthenium to form a gate electrode. The additional conductive material may be patterned, if necessary or desired. Further processing steps, such as spacer deposition and source/drain implantation will be apparent to the skilled artisan.

[0053] Another process flow is illustrated in FIGS. **7-9**. In FIG. **7**, a layer of high-k material **200** is deposited over a silicon substrate **10** and patterned. The substrate may have been treated prior to deposition of the high-k material **200**. For example, a layer of native oxide may have been removed and the surface treated to facilitate high-k deposition.

[0054] A layer of silicon oxide **100** is formed over the substrate **10** and covers the high-k material **200**, as illustrated in FIG. **8**. The silicon oxide layer **100** is planarized to expose the underlying high-k layer **200**. A layer of ruthenium **300** is selectively deposited over the high-k material **200** to form the gate electrode structure shown in FIG. **9**. In some embodiments the Ru layer forms the gate electrode, while in other embodiments a further conductive material may be deposited over the Ru and patterned, if necessary or desired, to form the gate electrode.

[0055] A gate-last approach is illustrated in FIGS. **10-15**. FIG. **10** shows a silicon substrate **10** with a layer of native oxide **50**. In FIG. **11**, the native oxide **50** is removed by etching, leaving the bare silicon substrate **10**. A silicon oxide or silicon nitride interface layer **100** with a thickness of about 2-15 Å is formed over the bare substrate **10** to produce the structure illustrated in FIG. **12**. A high-k layer **200** is deposited, preferably by ALD, over the interface layer **100** to form the structure of FIG. **13**. This is followed by deposition of a silicon oxide layer **400** (FIG. **14**). The silicon oxide layer **400** is patterned to expose the underlying high-k layer **200** (FIG. **15**). A layer of ruthenium or another noble metal **300** is subsequently deposited selectively over the exposed high-k layer **200** to form a gate electrode as illustrated in FIG. **16**A. Further process steps, such as deposition of conductor or contact metals and patterning will be apparent to the skilled artisan.

[0056] It will be understood by the skilled artisan that the ruthenium layer **300** need not fill the space over the high-k layer **200**. That is, in some embodiments the ruthenium layer **300** may not reach the upper surface of the silicon oxide layer **400** as illustrated in FIG. **16**B. In a further step, a conductor **320** is deposited over the ruthenium layer **300** (FIG. **16**C). The conductor is subsequently polished or otherwise etched back to form the gate electrode (not shown).

[0057] In another gate last approach a silicon substrate **10** covered with native oxide **50** is provided (FIG. **17**). The native oxide **50** is optionally removed, followed by deposition of a layer of silicon oxide **100** over the substrate as shown in FIG. **18**. The silicon oxide layer **100** is etched to form a trench and the exposed surface **25** (FIG. **19**) is prepared for deposition of a high-k dielectric layer by pretreatment or deposition of an interfacial layer **120** as shown in FIG. **20**. The interfacial layer **120** may comprise, for example, a thermally or chemically grown ultrathin silicon oxide or silicon nitride. A high-k layer **200** is then deposited by a vapor deposition process, preferably by an ALD process, over the entire structure (FIG. **21**). The high-k material is removed from over the silicon oxide **100** to produce the structure illustrated in FIG. **22**. This may be accomplished, for example, by filling the space over the interface layer **120** with a resist material, planarizing or otherwise etching back the resulting structure down to the top of the silicon oxide layer **100** and removing the resist material (not shown). Finally, a ruthenium layer **300** is selectively deposited over the high-k layer **200** by atomic layer deposition (FIG. **23**).

[0058] In each of the illustrated embodiments, additional processing is performed to produce the desired integrated circuit, as will be apparent to the skilled artisan.

[0059] Because ruthenium selectively deposits on the high-k material and not on the silicon oxide or oxynitride, it is not necessary to mask the oxide prior to deposition of the gate electrode material in each of these process flows. However, if necessary noble metal deposition can be followed with a short wet etch or other clean up process to ensure removal of any small amount of noble metal or noble metal compound left on the low k insulator, such as if there is less than perfect selectivity. The process flows can also save valuable and expensive materials and, depending on the particular circumstances, can avoid the sometimes difficult etching of noble metals or noble metal compounds.

[0060] As mentioned above, the ruthenium may form the entire gate electrode. However, in some embodiments the gate electrode comprises a further conductive material such as a metal or poly-silicon that has been deposited on the ruthenium. The additional conductive material may be deposited by ALD or by another deposition process, such as by CVD or PVD. The deposition may be selective, or may be followed by patterning steps. Preferably, the high-k material is also deposited by an ALD process.

[0061] The high-k material preferably has a k value of greater than or equal to **5**, more preferably greater than or equal to 10, and even more preferably greater than or equal to 20. Exemplary high-k materials include HfO_2, ZrO_2, Al_2O_3, TiO_2, Ta_2O_5, Sc_2O_3, lanthanide oxides and mixtures thereof, and complex oxides such as silicates, yttria-stabilized zirconia (YSZ), barium strontium titanate (BST), strontium titanate (ST), strontium bismuth tantalate (SBT) and bismuth tantalate (BT).

[0062] The following non-limiting examples will illustrate the invention in more detail.

EXAMPLE 1

[0063] Ruthenium thin films were deposited on 300 mm wafers with various materials formed thereover from alternating pulses of bis(ethylcyclopentadienyl)ruthenium (Ru $(EtCp)_2$) and oxygen (O_2) at a temperature of about 370° C.

[0064] The pulse length of the evaporated ruthenium precursor was about 0.7 seconds and was followed by a purge with an inert gas that lasted from about 2 seconds. The pulse length of the oxygen-containing reactant was about 2 seconds and the purge thereafter was about 2 seconds.

[0065] Ruthenium was found to grow using this process on TaN, Al_2O_3, Ta and HfO_2 surfaces. The typical growth rate was about from 0.5 to 0.9Å/cycle on these surfaces, not counting incubation time. The incubation time for Ru growth was found to be about 50-100 cycles on TaN, 50-100 cycles on Al_2O_3, about 50 cycles on Ta and virtually zero on HfO_2.

[0066] However, even 450 cycles of the same Ru process did not produce a measurable and conductive film on a thermal silicon oxide surface produced by a wet oxide process.

[0067] Where deposition was observed, the rate was independent of the $Ru(EtCp)_2$ dose, indicating that film growth proceeded in the self-limiting manner that is characteristic of ALD.

[0068] Although the foregoing invention has been described in terms of certain preferred embodiments, other embodiments will be apparent to those of ordinary skill in the art. Moreover, although illustrated in connection with particular process flows and structures, the skilled artisan will appreciate variations of such schemes for which the methods disclosed herein will have utility. Additionally, other combinations, omissions, substitutions and modification will be apparent to the skilled artisan, in view of the disclosure herein. Accordingly, the present invention is not intended to be limited by the recitation of the preferred embodiments, but is instead to be defined by reference to the appended claims.

We claim:

1. A method for selectively depositing a thin film comprising one or more noble metals on a substrate comprising a first surface and a second surface, the method comprising:

contacting the first and second surface of the substrate with a gaseous noble metal precursor;

providing a second reactant gas pulse to the reaction chamber; and

repeating until a thin film of a desired thickness is obtained selectively on the first surface relative to the second surface,

wherein the first surface comprises a material selected from the group consisting of metals, metal nitrides, metal carbides, metal borides, conductive oxides and mixtures thereof; and

wherein the second surface comprises a material selected from the group consisting of silicon oxides, silicon nitrides, silicon oxynitrides, fluorinated silica glass (FSG), carbon doped silicon oxide (SiOC) and materials containing more than about 50% silicon oxide and wherein the temperature is below about 400° C.

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