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Barrows et al.

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(54) **METHODS TO REDUCE THRESHOLD VOLTAGE TOLERANCE AND SKEW IN MULTI-THRESHOLD VOLTAGE APPLICATIONS**

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G05F 3/02 (2006.01)

(52) **U.S. Cl.** **327/537**; 327/534; 327/535; 327/564; 327/566

(58) **Field of Classification Search** 327/534–535, 327/537, 561–566
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,462,623	B1	10/2002	Horan et al.
6,695,475	B2	2/2004	Yin

(Continued)

OTHER PUBLICATIONS

Fet Modeling for Circuit Simulation by Dileep; pp. 73-76. Divekar; http://books.google.com/books?id=QdtbOnfOeEQC&pg=PP11&dq=5.9+threshold+voltage+shift&sig=bkHISy9OW5qq02vUPtwsn8HNplk#PPA75,M1.

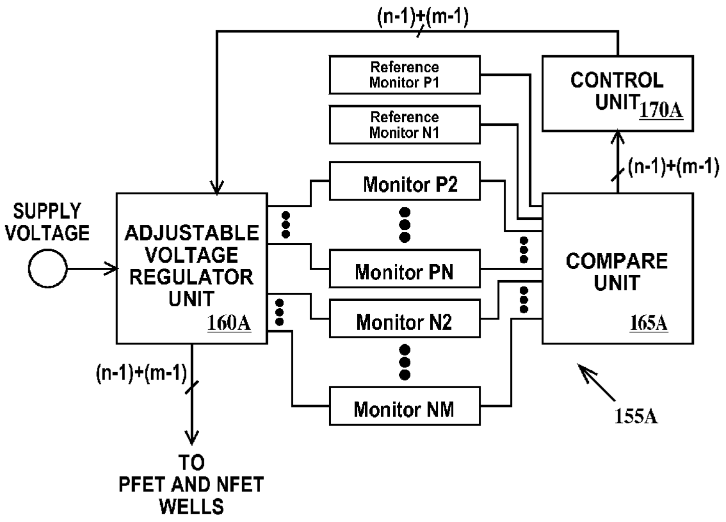
(Continued)

Primary Examiner—Lincoln Donovan
Assistant Examiner—Brandon S Cole
(74) *Attorney, Agent, or Firm*—Schmeiser, Olsen & Watts; Riyon W. Harding

(57) **ABSTRACT**

A circuit and a method for adjusting the performance of an integrated circuit, the method includes: comprising: (a) measuring the performance of a first monitor circuit having at least one field effect transistor (FET) of a first set of FETs, each FET of the first set of FETs having a designed first threshold voltage; (b) measuring the performance of a second monitor circuit having at least one field effect transistor (FET) of a second set of FETs, each FET of the second set of FETs having a designed second threshold voltage, the second threshold voltage different from the first threshold voltage; and (c) applying a bias voltage to wells of the FETs of the second set of FETs based on comparing a measured performance of the first and second monitor circuits to specified performances of the first and second monitor circuits.

10 Claims, 7 Drawing Sheets



U.S. PATENT DOCUMENTS

7,119,525	B1	10/2006	Yoshino	
7,197,104	B1	3/2007	Cheung et al.	
7,330,049	B2	2/2008	Perisetty	
7,459,958	B2	12/2008	Barrows et al.	
2005/0093619	A1 *	5/2005	Naffziger et al.	327/543
2005/0116765	A1 *	6/2005	Sakiyama et al.	327/534
2005/0210307	A1	9/2005	Lee et al.	
2006/0149983	A1	7/2006	Kondou	
2006/0170575	A1	8/2006	Jang et al.	
2007/0205802	A1 *	9/2007	Perisetty	326/27
2007/0228383	A1	10/2007	Bernstein et al.	
2008/0086706	A1	4/2008	Barrows et al.	

OTHER PUBLICATIONS

Office Action (Mail Date Feb. 20, 2009) for U.S. Appl. No. 12/138,514, filed Jun. 13, 2008; Confirmation No. 9555.

Office Action (Mail Date Mar. 19, 2009) for U.S. Appl. No. 11/941,342, filed Nov. 16, 2007; Confirmation No. 9468.

Office Action (Mail Date Jul. 1, 2009) for U.S. Appl. No. 12/138,514, filed Jun. 13, 2008; Confirmation No. 9555.

* cited by examiner

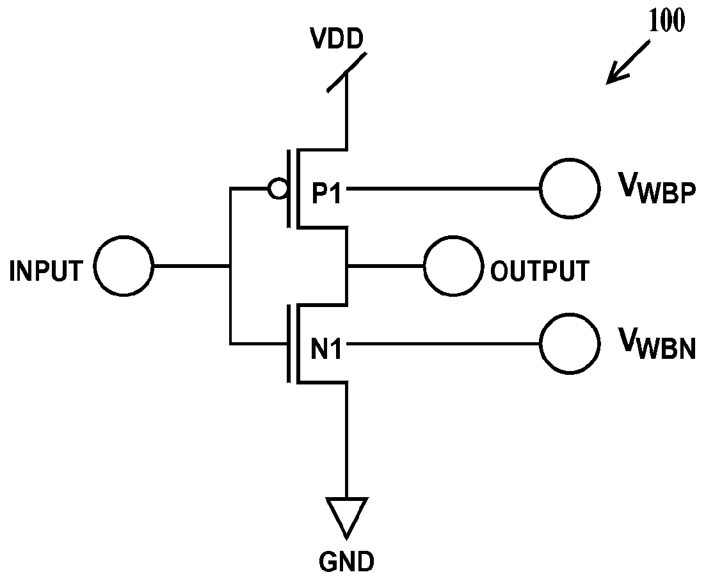

100
VDD
P1
V_{WBP}
INPUT
OUTPUT
N1
V_{WBN}
GND

FIG. 1

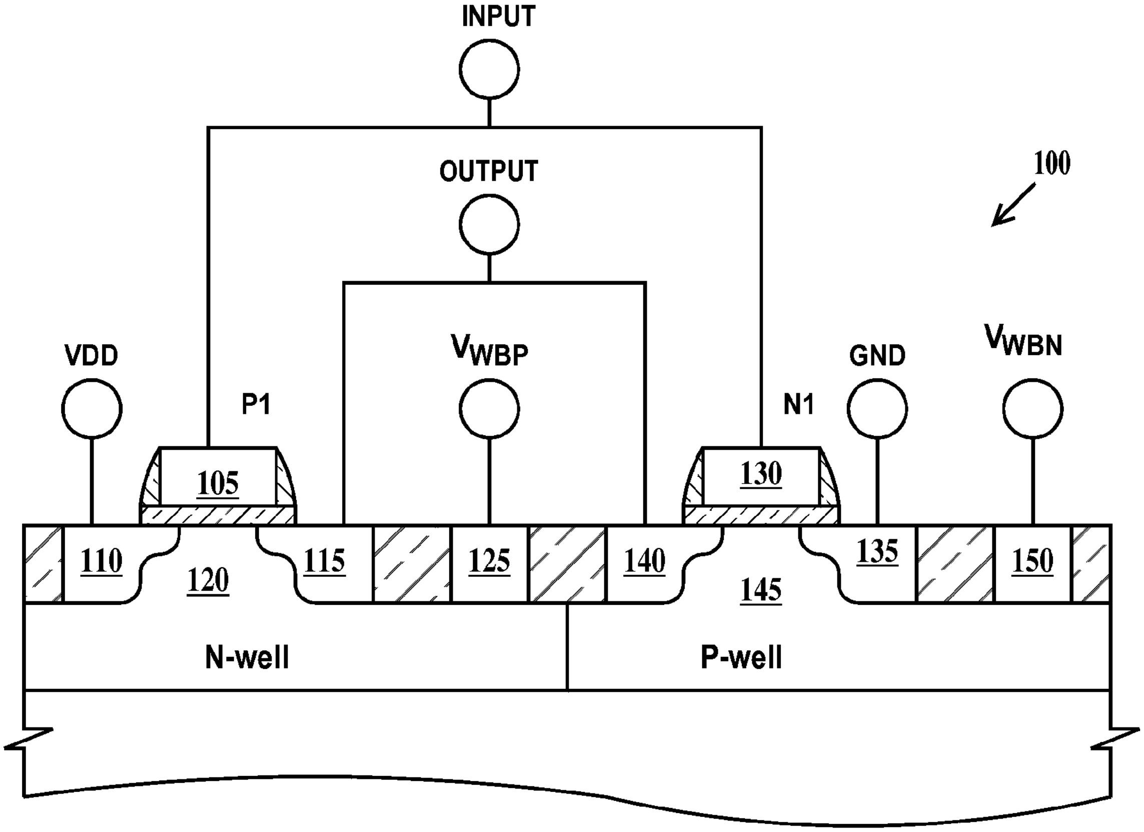

INPUT
OUTPUT
100
VDD
P1
V_{WBP}
N1
GND
V_{WBN}
105
130
110
120
115
125
140
145
135
150
N-well
P-well

FIG. 2

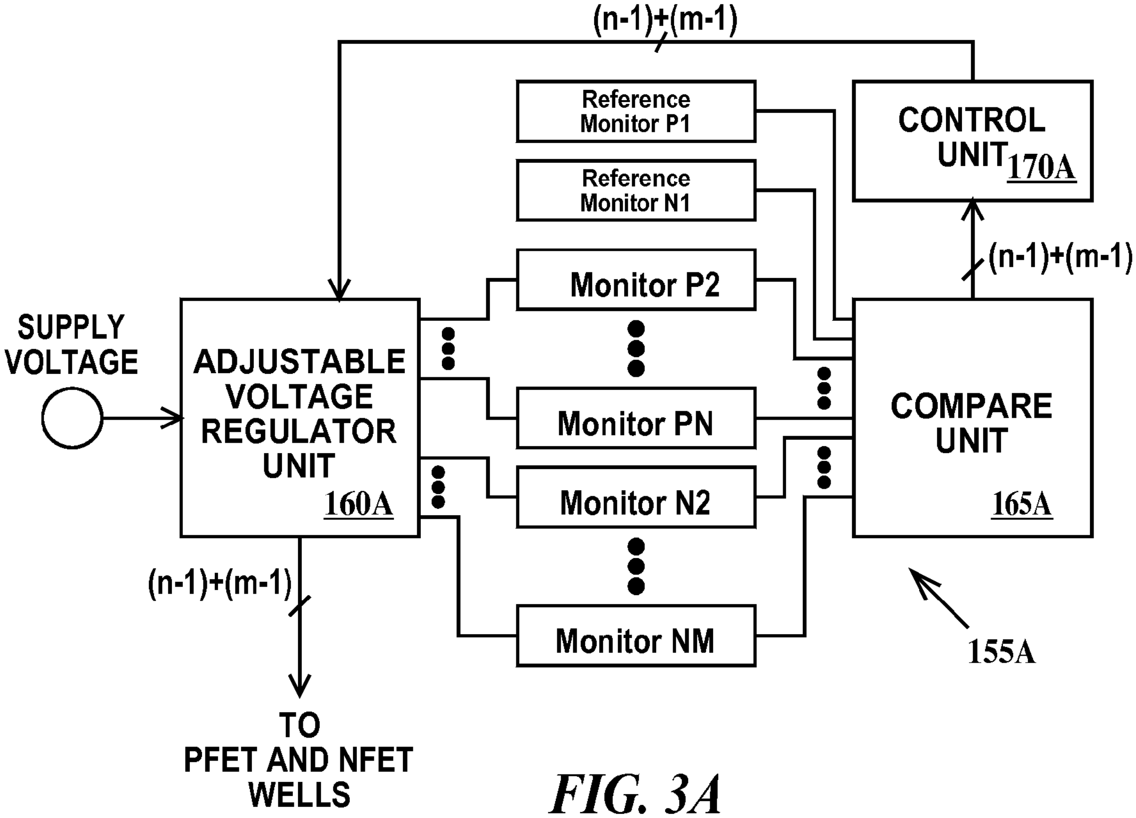

(n-1)+(m-1)
Reference Monitor P1
Reference Monitor N1
CONTROL UNIT 170A
(n-1)+(m-1)
SUPPLY VOLTAGE
ADJUSTABLE VOLTAGE REGULATOR UNIT 160A
Monitor P2
Monitor PN
Monitor N2
Monitor NM
COMPARE UNIT 165A
(n-1)+(m-1)
155A
TO PFET AND NFET WELLS

FIG. 3A

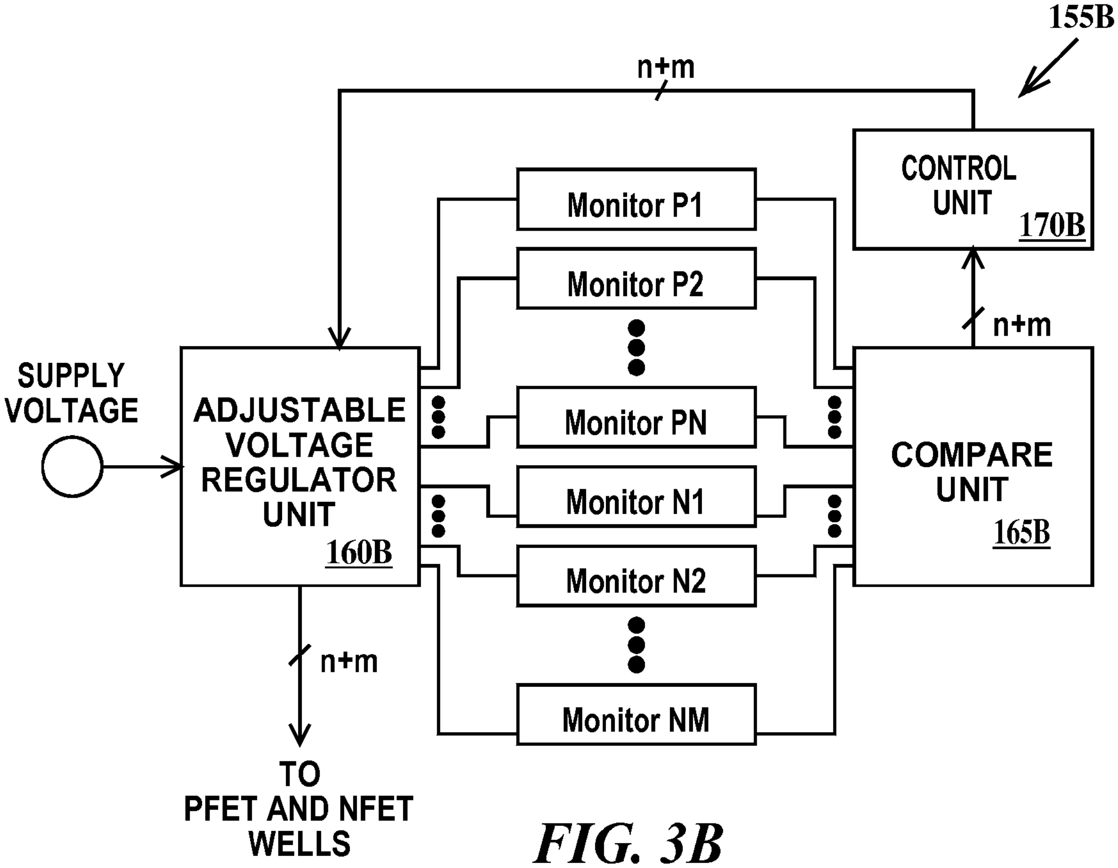

155B
n+m
CONTROL UNIT 170B
Monitor P1
Monitor P2
n+m
SUPPLY VOLTAGE
ADJUSTABLE VOLTAGE REGULATOR UNIT 160B
Monitor PN
Monitor N1
Monitor N2
Monitor NM
COMPARE UNIT 165B
n+m
TO PFET AND NFET WELLS

FIG. 3B

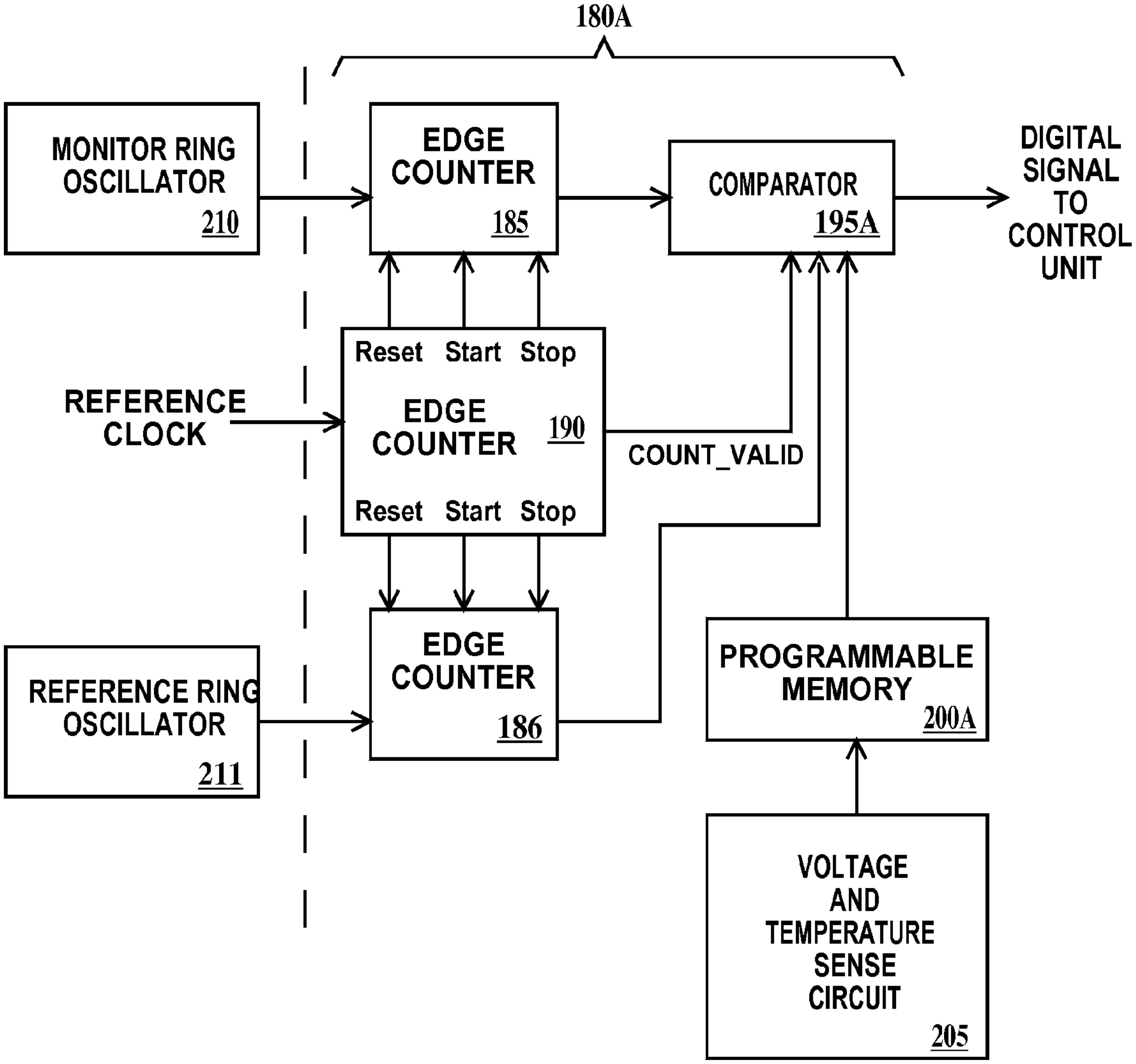

180A
MONITOR RING OSCILLATOR 210
EDGE COUNTER 185
COMPARATOR 195A
DIGITAL SIGNAL TO CONTROL UNIT
Reset Start Stop
REFERENCE CLOCK
EDGE COUNTER 190
COUNT_VALID
Reset Start Stop
EDGE COUNTER 186
REFERENCE RING OSCILLATOR 211
PROGRAMMABLE MEMORY 200A
VOLTAGE AND TEMPERATURE SENSE CIRCUIT 205

FIG. 4A

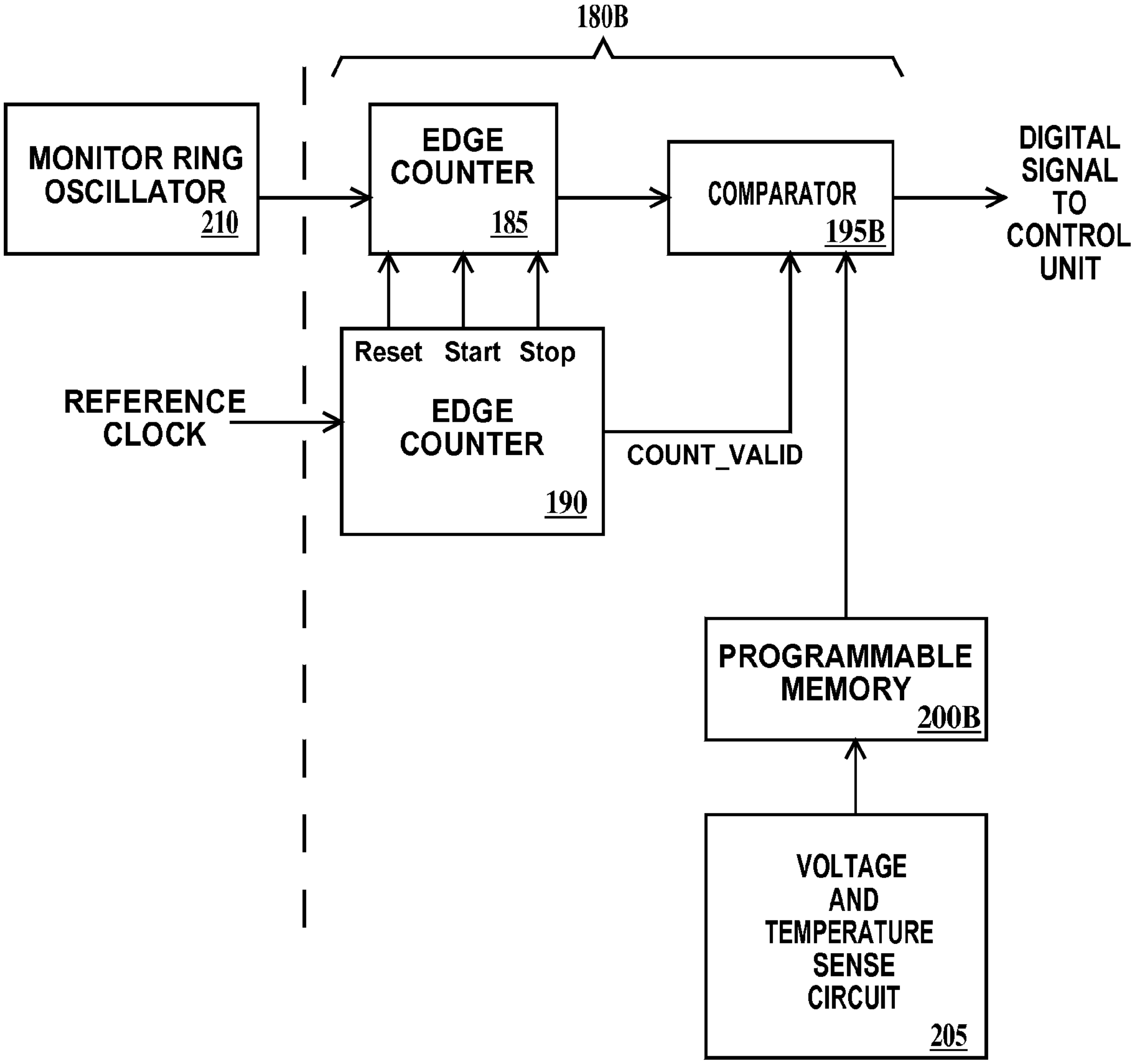

180B
MONITOR RING OSCILLATOR
210
EDGE COUNTER
185
COMPARATOR
195B
DIGITAL SIGNAL TO CONTROL UNIT
Reset
Start
Stop
REFERENCE CLOCK
EDGE COUNTER
190
COUNT_VALID
PROGRAMMABLE MEMORY
200B
VOLTAGE AND TEMPERATURE SENSE CIRCUIT
205

FIG. 4B

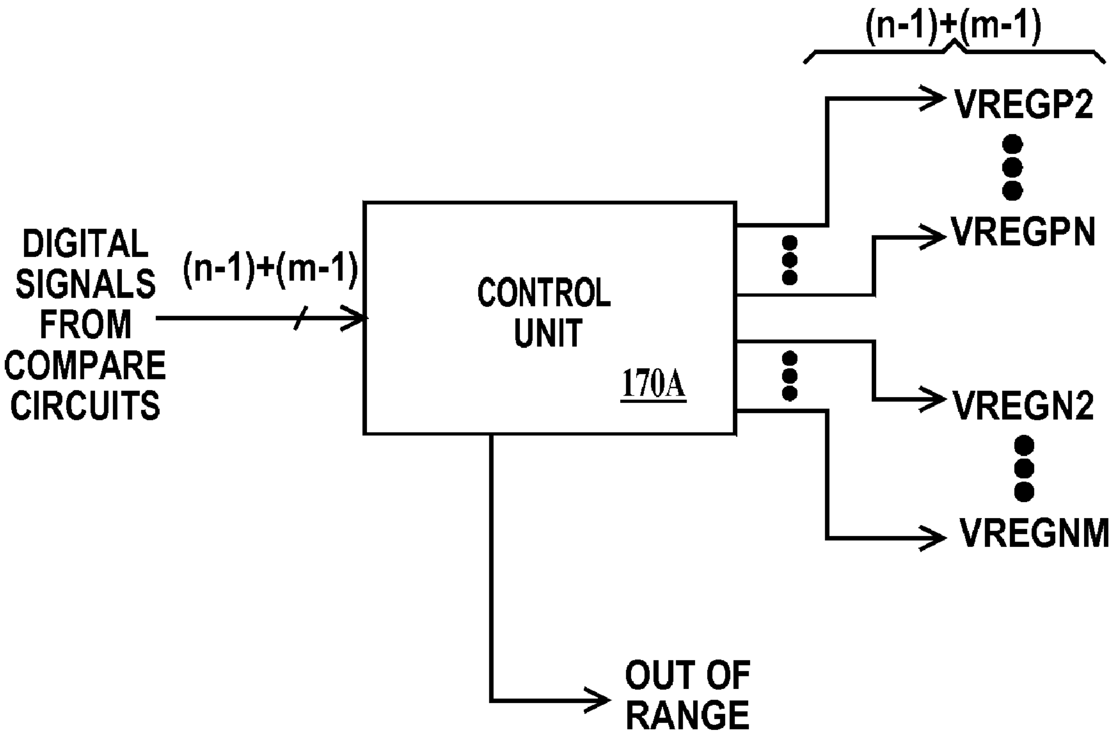

(n-1)+(m-1)
VREGP2
VREGPN
VREGN2
VREGNM
DIGITAL SIGNALS FROM COMPARE CIRCUITS
(n-1)+(m-1)
CONTROL UNIT
170A
OUT OF RANGE

FIG. 5A

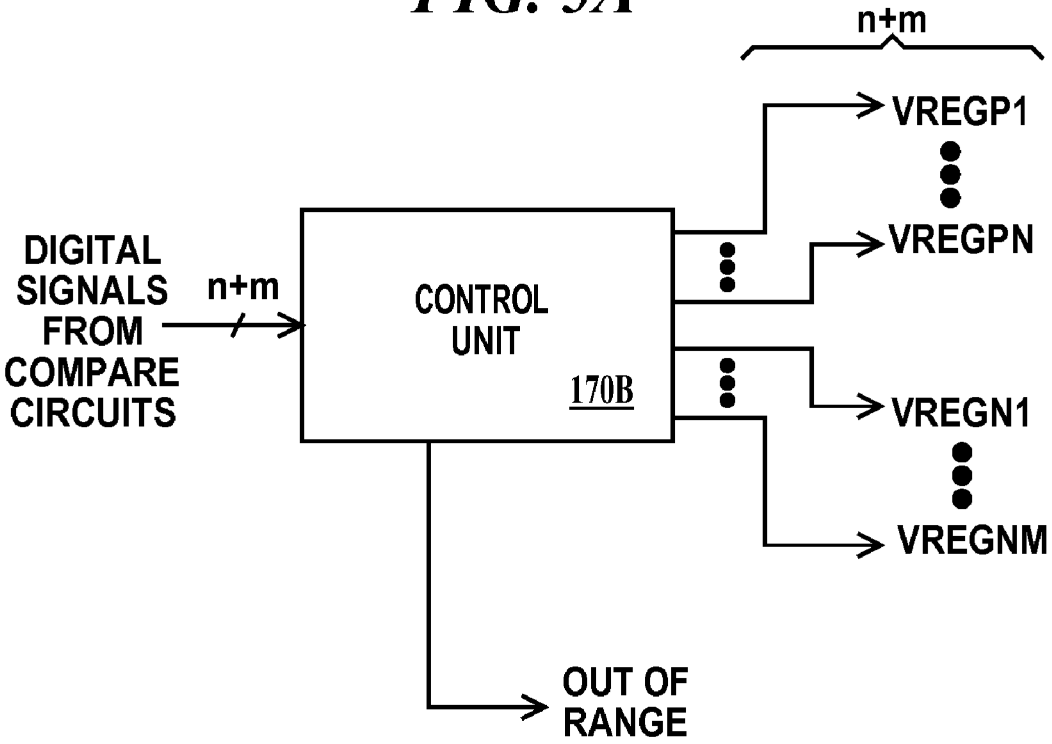

n+m
VREGP1
VREGPN
VREGN1
VREGNM
DIGITAL SIGNALS FROM COMPARE CIRCUITS
n+m
CONTROL UNIT
170B
OUT OF RANGE

FIG. 5B

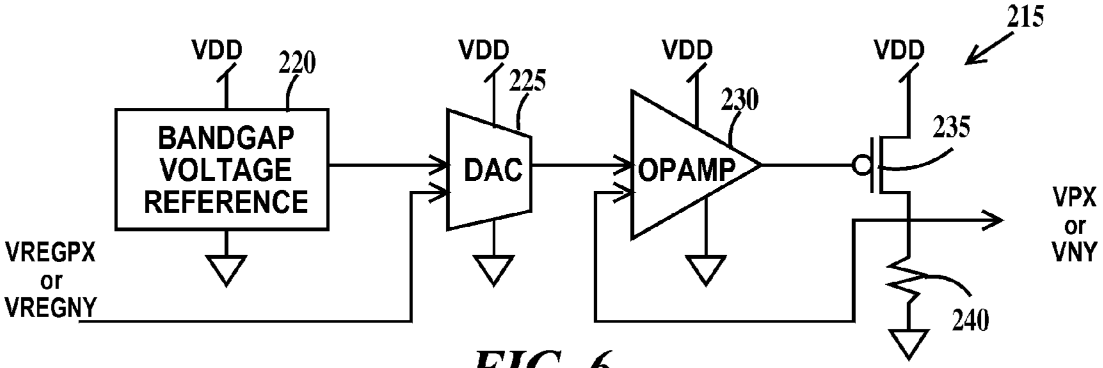


FIG. 6

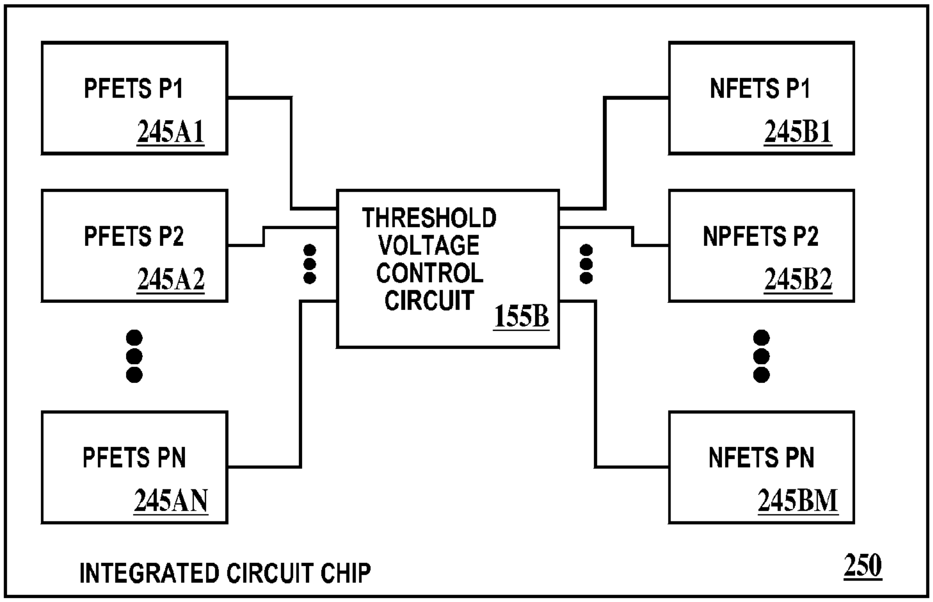


FIG. 7A

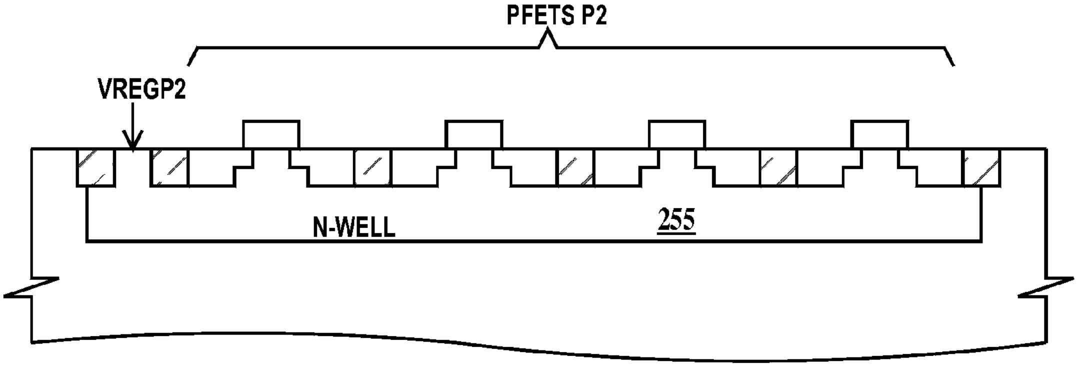


FIG. 7B

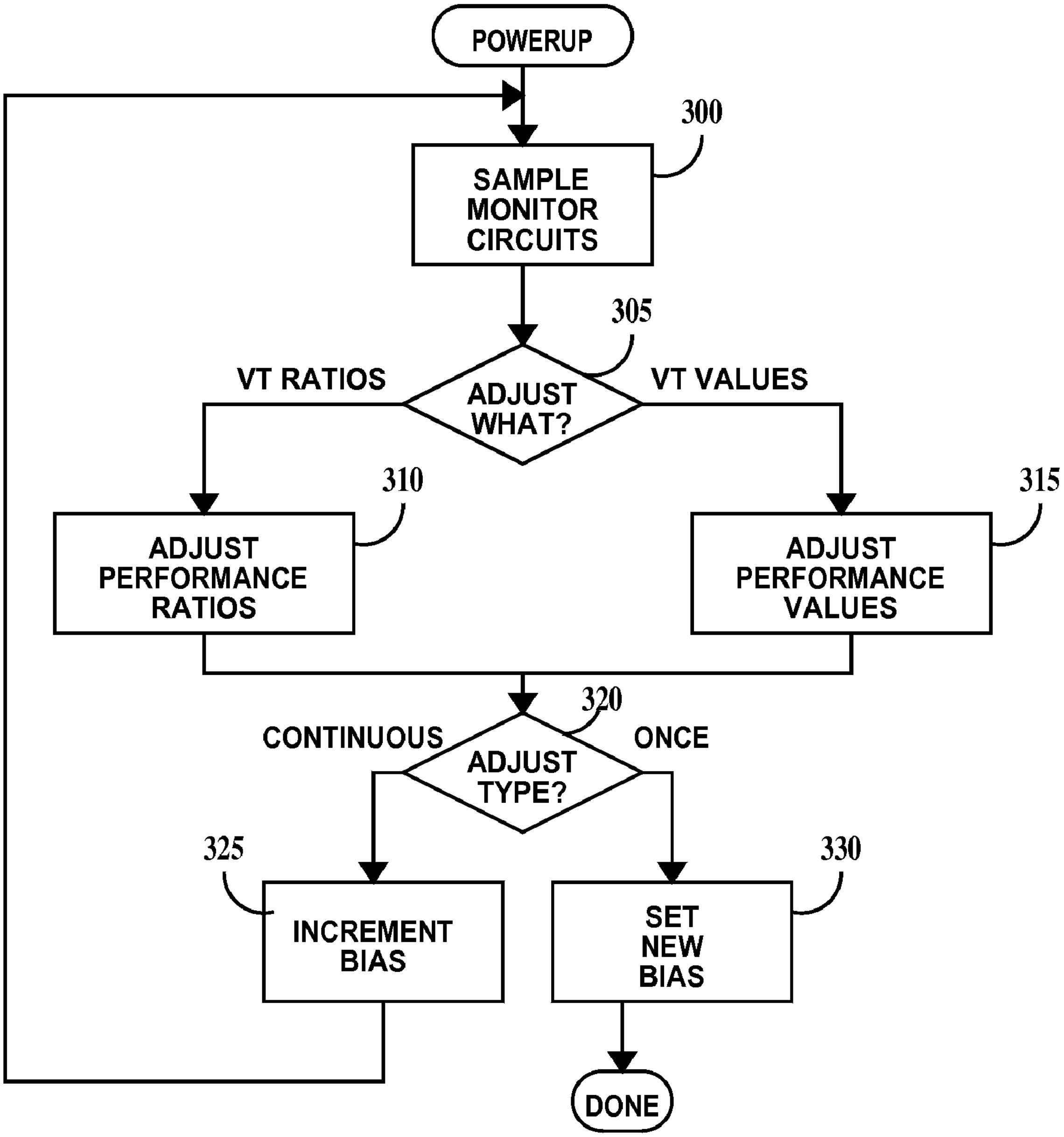

POWERUP
300
SAMPLE MONITOR CIRCUITS
305
VT RATIOS
ADJUST WHAT?
VT VALUES
310
ADJUST PERFORMANCE RATIOS
315
ADJUST PERFORMANCE VALUES
320
CONTINUOUS
ADJUST TYPE?
ONCE
325
INCREMENT BIAS
330
SET NEW BIAS
DONE

FIG. 8

METHODS TO REDUCE THRESHOLD VOLTAGE TOLERANCE AND SKEW IN MULTI-THRESHOLD VOLTAGE APPLICATIONS

This Application is a continuation of U.S. patent application Ser. No. 11/424,961 filed on Jun. 19, 2006.

FIELD OF THE INVENTION

The present invention relates to the field of integrated circuits; more specifically, it relates to methods and circuits to reduce threshold voltage tolerance and skew in integrated circuits utilizing devices having multiple different threshold voltages.

BACKGROUND OF THE INVENTION

In order to reduce power consumption and increase performance, circuits having devices with different threshold voltages have been used in different portions of the integrated circuit. Devices with low threshold voltages are faster, but have greater sub-threshold voltage leakage (consume more power) compared with devices having high threshold voltages but low sub-threshold voltage leakage. Using a mix of high threshold voltage devices on non-performance critical circuit paths and low threshold voltage devices on performance critical circuit paths can result in lower overall power consumption and higher performance than using devices having the same threshold voltages.

However, it is critical that the designed relationship between the different threshold voltage values of different-threshold voltage devices be maintained in the fabricated integrated circuit in order to ease timing closure during design and avoid signal propagation timing issues. Therefore, there is a need for methods and circuits for maintaining the design values and/or relationships between the different threshold voltage values of multiple threshold voltage devices.

SUMMARY OF THE INVENTION

A first aspect of the present invention is a circuit, comprising: a first set of field effect transistors (FETs) having a designed first threshold voltage and a second set of FETs having a designed second threshold voltage, the first threshold voltage different from the second threshold voltage; a first monitor circuit containing at least one FET of the first set of FETs and a second monitor circuit containing at least one FET of the second set of FETs; a compare circuit adapted to generate a compare signal based on a performance measurement of the first monitor circuit and a performance measurement of the second monitor circuit; and a control unit adapted to generate a control signal to a voltage regulator based on the compare signal, the voltage regulator adapted to supply a bias voltage to wells of FETs of the second set of FETs, the value of the bias voltage based on the control signal.

A second aspect of the present invention is the first aspect, wherein the compare circuit includes a first edge counter connected between the first monitor circuit and a first comparator and a second edge counter connected between a reference clock and the first comparator; and further including: an additional compare circuit including a third edge counter connected between the second monitor circuit and a second comparator and a fourth edge counter connected between the reference clock and the second comparator; and a first memory device containing a first performance specification for the first monitor circuit coupled to the first comparator and a second memory device memory containing a second performance specification for the second monitor circuit coupled to the second comparator.

A third aspect of the present invention is a method, comprising: providing a first set of field effect transistors (FETs) having a designed first threshold voltage and a second set of FETs having a designed second threshold voltage, the first threshold voltage different from the second threshold voltage; providing a first monitor circuit containing at least one FET of the first set of FETs and a second monitor circuit containing at least one FET of the second set of FETs; providing a compare circuit adapted to generate a compare signal based on a performance measurement of the first monitor circuit and a performance measurement of the second monitor circuit; and providing a control unit adapted to generate a control signal to a voltage regulator based on the compare signal, the voltage regulator adapted to supply a bias voltage to wells of FETs of the second set of FETs, the value of the bias voltage based on the control signal.

A fourth aspect of the present invention is the third aspect wherein the compare circuit includes a first edge counter connected between the first monitor circuit and a first comparator and a second edge counter connected between a reference clock and the first comparator; and further including: providing an additional compare circuit including a third edge counter connected between the second monitor circuit and a second comparator and a fourth edge counter connected between the reference clock and the second comparator; and providing a first p[device containing a first performance specification for the first monitor circuit coupled to the first comparator and a second memory device containing a second performance specification for the second monitor circuit coupled to the second comparator.

A fifth aspect of the present invention is a method, comprising: (a) measuring the performance of a first monitor circuit having at least one field effect transistor (FET) of a first set of FETs, each FET of the first set of FETs having a designed first threshold voltage; (b) measuring the performance of a second monitor circuit having at least one field effect transistor (FET) of a second set of FETs, each FET of the second set of FETs having a designed second threshold voltage, the second threshold voltage different from the first threshold voltage; and (c) applying a bias voltage to wells of the FETs of the second set of FETs based on comparing a measured performance of the first and second monitor circuits to specified performances of the first and second monitor circuits.

A sixth aspect of the present invention is the fifth aspect further including: (d) applying an additional bias voltage to wells of FETs of the first set of FETs based on the comparing the performances of the first and second monitor circuits measured in steps (a) and (b) to specified performances of the first and second monitor circuits.

BRIEF DESCRIPTION OF DRAWINGS

The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. **1** is an exemplary circuit illustrating the principle for threshold voltage control according to the embodiments of the present invention;

FIG. **2** is a cross-sectional view illustrating the physical structure of the inverter of FIG. **1**;

FIG. **3**A is a schematic block circuit diagram of a circuit for threshold voltage control according to a first embodiment of the present invention;

FIG. **3**B is a schematic block circuit diagram of a circuit for threshold voltage control according to a second embodiment of the present invention

FIG. **4**A is a block circuit diagram of an exemplary individual compare circuit of the compare unit of FIG. **3**A;

FIG. **4**B is a block circuit diagram of an exemplary individual compare circuit of the compare unit of FIG. **3**B;

FIG. **5**A is a diagram illustrating the control signal generated by the control unit of FIG. **3**A according to the first embodiment of the present invention;

FIG. **5**B is a diagram illustrating the control signal generated by the control unit of FIG. **3**B according to the second embodiment of the present invention;

FIG. **6** is a schematic block diagram of a typical voltage regulator used to adjust well bias according to embodiments of the present invention;

FIG. **7**A is a diagram illustrating an exemplary floor plan of an integrated circuit chip according to the embodiments of the present invention;

FIG. **7**B is an exemplary cross-sectional diagram of multiple field effect transistors formed in a common well; and

FIG. **8** is a flowchart of the methods of controlling threshold voltages of multiple-threshold voltage devices according to the embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The performance of a field effect transistor (FET) is defined as the switching speed of the FET and the performance of a circuit is defined as the time delay of a signal propagated from an input to an output of the circuit.

FIG. **1** is an exemplary circuit illustrating the principle for threshold voltage control according to the embodiments of the present invention. In FIG. **1**, an inverter **100** includes a P-channel field effect transistor (PFET) P**1** and an N-channel field effect transistor (NFET) N**1**. The source of PFET P**1** is connected to V_{DD}, the source of NFET N**1** is connected to ground (or V_{SS}), the drains of PFET P**1** and NFET N**1** are connected to the output of the inverter and the gates of PFET P**1** and NFET N**1** are connected to the input of the inverter. PFET P**1** is fabricated in an N-well and NFET N**1** is fabricated in a P-well as is well known in the art. V_{DD} is defined as the most positive voltage level of the power supply and ground (or V_{SS}) is defined as the most negative voltage level of the power supply.

FIG. **2** is a cross-sectional view illustrating the physical structure of the inverter of FIG. **1**. PFET P**1** includes a gate **105**, a source **110**, a drain **115**, an N-well **120** and an N-well contact **125**. NFET N**1** includes a gate **130**, a source **135**, a drain **140**, a P-well **145** and a P-well contact **150**. The electrical connections described supra in reference to FIG. **1** are illustrated in FIG. **2**. The crosshatched regions indicate dielectric material.

The threshold voltages (V_ts) of PFET P**1** and NFET N**1** are determined during fabrication and are a function of the various doping levels of the source/drains, channel region and gate electrode. The V_ts of PFET P**1** and NFET N**1** may be adjusted (after fabrication of the integrated circuit containing PFET P**1** and NFET N**1** is complete) by applying bias voltages V_{WBP} and V_{WBN} respectively to the N-well of PFET P**1** and the P-well of NFET N**1**. Applying a positive (reverse) bias to the N-well of PFET P**1** decreases its V_t (makes its V_t more negative) thus slowing down the PFET, while applying a negative (forward) bias to the N-well of PFET P**1** increases its V_t (makes its V_t less negative) thus speeding up the PFET. Applying a positive (forward) bias to the P-well of NFET N**1** decreases its V_t (makes its V_t less positive) thus speeding up the NFET, while applying a negative (reverse) bias to the P-well of NFET N**1** increases its V_t (makes its V_t more positive) thus slowing down the NFET.

When integrated circuits having multiple V_t FETs are designed, the V_ts of FETs are designed to be positive or negative fractions of V_{DD}. For example, a first FET may be designed to have a $V_t=V_{DD}/3$, a second FET may be designed to have a $V_t=V_{DD}/4$ and a third FET may be designed to have a $V_t=V_{DD}/5$. If $V_{DD}=1.0$ volt, then the V_1s are 0.33, 0.25 and 0.20 volts respectively. All other parameters being equal, a FET with a V_t of 0.20 volt will be faster than FETs having V_ts of 0.25 volt and 0.33 volt. Further, the switching speeds of the different V_t devices are designed to be ratios of each other. However, due to process variations, there is a +/− tolerance on the actual V_t and therefore the switching speed obtained when the FETs are manufactured. This is called V_t tolerance. Further, since each FETs V_t is typically set during independent manufacturing steps, the tolerances of different FET types do not necessarily track. For example, a first V_t FET could be manufactured faster than design while a second V_t FET on the same integrated circuit chip could be manufactured slower than design. This is called V_t skew. Table I illustrates this problem.

TABLE I

THRESHOLD VOLTAGES VERSUS SWITCHING SPEED

Threshold Voltage in volts	Relative Switching Speed	Switching Speed Tolerance	Switching Speed Range
0.20	0.75	+/−0.15	0.90-0.60
0.25	1.00	+/−0.15	1.15-0.85
0.30	1.25	+/−0.15	1.40-1.10

In table I, the middle speed FET ($V_t=0.25$ volt) is the reference FET (Switching Speed=1.0). Thus, the actual switching speed of the fastest device ($V_t=0.20$ volt) can overlap the actual switching speed of the middle speed device ($V_t=0.25$ volt) and the actual switching speed of the middle speed device ($V_t=0.25$ volt) can overlap the actual switching speed of the slowest device ($V_t=0.30$ volt). This can complicate timing closure of the integrated circuit design because all combinations of V_t skew and tolerance must be accounted for, or it could upset the timing of the circuit design if the switching speed ratios are assumed to be the designed values.

In a first embodiment of the present invention, the performance (switching speed) of the different V_t devices is monitored. One V_t device is chosen as a reference and the well bias of the other V_t devices adjusted (which adjusts the V_t which in turn adjusts the switching speed) until the design performance ratio (design switching speed ratio) of the other V_t devices versus the reference V_t device are brought to or near to design values. PFETs and NFETs are monitored and adjusted separately. This removes V_t skew, but does not adjust for V_t tolerance.

In a second embodiment of the present invention the performance (switching speed) of the different V_t devices is monitored. The well bias of all different V_t devices is adjusted (which adjusts the V_t which in turn adjusts the switching speed) of the different V_t devices until the design performance specification (design switching speed specification) of all the V_t devices are brought to or near to design values. PFETs and

NFETs are monitored and adjusted separately. This removes V_t skew and adjusts for V_t tolerance.

FIG. **3**A is a schematic block circuit diagram of a circuit for threshold voltage control according to a first embodiment of the present invention. In FIG. **3**A, a threshold voltage adjustment circuit **155**A includes an adjustable voltage regulator unit **160**A, a set of PFET monitor circuits P**1** through PN, a set of NFET monitor circuits N**1** through NM, a compare unit **165**A and a control unit **170**A. In the example of FIG. **3**A, reference monitor P**1** monitors a reference PFET having a design V_t of P**1** and reference monitor N**1** monitors a reference NFET having a design V_t of N**1**. Adjustable voltage regulator unit **160**A includes a separate N-well bias voltage regulator for each of the other different V_t PFETs having respective design V_ts of P**2** through PN and a different P-well bias voltage regulator for each of the other different V_t NFETs having design V_ts of N**2** through NM. Compare unit **165**A includes a separate compare circuit for each different V_t PFET (V_ts P**2** through PN) and for each different V_t NFET (V_ts N**2** through NM) that compares the performance of the monitored FET to the performance of the reference FET. Adjustable voltage regulator unit **160**A is coupled to a power supply (ultimately to an external power supply).

Each N-well and P-well bias voltage regulator generates a well bias voltage that is distributed throughout the integrated circuit chip to respective V_t devices as well as to respective monitors P**2** through PN. The output of each monitor P**2** through PN is connected to a respective compare circuit within compare unit **165**A as is the output of reference monitor P**1**. The output of each monitor N**2** through NM is connected to a respective compare circuit within compare unit **165**A as is the output of reference monitor N**1**. The output of compare unit **165**A is connected to control unit **170**A Control unit **170**A generates control signals supplied to respective well bias voltage regulators in adjustable voltage regulator unit **160**A.

The number (n) of PFET monitor circuits is the number of different V_t PFETs in the integrated circuit that are to be monitored and there is one monitor for each. The number (m) of NFET monitor circuits is the number of different V_t NFETs in the integrated circuit that are to be monitored and there is one monitor for each. Reference monitor P**1** monitors the performance of first (and reference) V_t PFETs having a reference design threshold voltage of P**1**. Monitor P**2** monitors the performance of second V_t PFETs having a design threshold voltage of P**2**. Monitor circuit PN monitors the performance of n^{th} V_t PFETs having a design threshold voltage of PN. Reference monitor N**1** monitors the performance of first (and reference) V_t NFETs having a reference design threshold voltage of N**1**. Monitor N**2** monitors the performance of second V_t NFETs having a design threshold voltage of N**2**. Monitor NM monitors the performance of m^{th} V_t NFETs having a design threshold voltage of NM.

The value of n need not be the same as the value of m. Not every different V_t NFET or different V_t PFET on the integrated circuit need be monitored or connected to threshold voltage adjustment circuit **155**A. In one example, adjustable voltage regulator unit **160**A, PFET monitor circuits P**1** through PN, NFET monitor circuits N**1** through NM, compare unit **165**A and control unit **170**A are physically located on the integrated circuit chip. In one example, PFET monitor circuits P**1** through PN, NFET monitor circuits N**1** through NM, compare unit **165**A and control unit **170**A are physically located on the integrated circuit chip while adjustable voltage regulator unit **160**A is physically located off chip.

FIG. **3**B is a schematic block circuit diagram of a circuit for threshold voltage control according to a second embodiment of the present invention. FIG. **3**B is similar to FIG. **3**A except as noted. In FIG. **3**B, a threshold voltage adjustment circuit **155**B includes an adjustable voltage regulator unit **160**B, a set of PFET monitor circuits P**1** through PN, a set of NFET monitor circuits N**1** through NM, a compare unit **165**B and a control unit **170**B. Adjustable voltage regulator unit **160**B includes a separate N-well bias voltage regulator for each of the different V_t PFETs (being monitored) and a separate P-well bias voltage regulator for each of the different V_t NFETs (being monitored).

Each voltage regulator unit generates a well bias voltage that is distributed throughout the integrated circuit chip to respective V_t devices as well as to respective monitors P**1** through PN and N**1** through NM. The output of each monitor P**1** through PN and N**1** through NM is connected to its respective compare circuit within compare unit **165**B where it is compared to a performance target for that V_t FET (instead of to a performance of a reference V_t FET as in the first embodiment of the present invention). The output of compare unit **165**B is connected to control unit **170**B. Control unit **170**B generates control signals supplied to respective well bias voltage regulators in adjustable voltage regulator unit **160**B.

In one example, adjustable voltage regulator unit **160**B, PFET monitor circuits P**1** through PN, NFET monitor circuits N**1** through NM, compare unit **165**B and control unit **170**B are physically located on the integrated circuit chip. In one example, PFET monitor circuits P**1** through PN, NFET monitor circuits N**1** through NM, compare unit **165**B and control unit **170**B are physically located on the integrated circuit chip while adjustable voltage regulator unit **160**B is physically located off chip.

FIG. **4**A is a block circuit diagram of an exemplary individual compare circuit of compare unit **165**A of FIG. **3**A. In FIG. **4**A, a compare circuit **180**A includes a first edge counter **185**, a second edge counter **190**, a third edge counter **186**, a comparator **195**A, a programmable memory **200**A and a voltage and temperature sense circuit **205**. The output of a monitor ring oscillator **210** (monitoring an FET having a design V_t=P**2** through PN or N**2** through NM) is connected to the count input of first edge counter **185**. Ring oscillators are well known in the art and comprise an odd number of sequential inverters with the feedback of the output to the input of the first inverter. The output of first edge counter **185** (a signal indicating the latest actual edge count) is connected to first compare input of a comparator **195**A. The output of a reference monitor ring oscillator **211** (monitoring an FET having a design V_t=P**1** or N**1**) is connected to the count input of third edge counter **186**. A precise reference clock (external or internal to the integrated circuit chip) is connected to the count input of second edge counter **190**. Second edge counter **190** supplies three control signals (reset, start and stop) to first and third edge counters **185** and **186**, and a count valid signal to comparator **195**A. A third compare input of comparator **195**A is coupled to programmable memory **200**A, which contains pre-determined target performance monitor ring oscillator **210** to reference monitor oscillators **211** ratios. Voltage and temperature sense circuit **205** is connected to programmable memory **200**A and provides lookup values for selecting the appropriate target performance ratio based the temperature and the voltage supplied to the monitor ring oscillator.

While each compare circuit may include its own programmable memory and a voltage and temperature sense circuit, a common programmable memory may be shared between two or more of the compare circuits, a common voltage and temperature sense circuit may be shared between two or more of the compare circuits, or both a common programmable memory and a common voltage and temperature sense circuit may be shared between two or more of the compare circuits.

Monitor ring oscillator **210** and reference monitor ring oscillator **211** are exemplary monitor circuits. Monitor ring oscillator **210** represents any of PFET monitors P**2** through PN or NFET monitors N**2** through NM. If ring oscillator **210** represents PFET monitor P**2**, then the PFETs in the signal delay path of the ring oscillator are PFETs designed to have threshold voltage P**2**. If ring oscillator **210** represents PFET monitor PN, then the PFETs in the signal delay path of the ring oscillator are PFETs designed to have threshold voltage PN. If ring oscillator **210** represents NFET monitor N**2**, then the NFETs in the signal delay path of the ring oscillator is NFETs designed to have threshold voltage N**2**. If ring oscillator **210** represents NFET monitor NM, then the NFETs in the signal delay path of the ring oscillator are NFETs designed to have threshold voltage NM. If reference ring oscillator **211** represents PFET reference monitor P**1**, then the PFETs in the signal delay path of the ring oscillator are PFETs designed to have threshold voltage P**1**. If reference ring oscillator **211** represents NFET reference monitor circuit N**1**, then the NFETs in the signal delay path of the ring oscillator are NFETs designed to have threshold voltage N**1**. The delays through monitor ring oscillator **210** and reference ring oscillator **211** varies as a function of V_t and well bias voltage (and also temperature and supply voltages as described infra).

In operation, second edge counter **190** issues a reset to first and third edge counters **185** and **186** to reset its count to zero. Then second edge counter **190** issues a start to first and third edge counters **185** and the first edge counter starts counting edges of the signal from monitor ring oscillator **210**, second edge counter starts counting clock edges from the reference clock and third edge counter **186** starts counting edges of the signal from reference ring oscillator **211**. When second edge counter **190** reaches a preset count value it issues a stop signal to first and second edge counters **185** and **186** and a count valid signal to comparator **195**A. Comparator **195**A compares the ratio of the actual count from first and second edge counters **185** and **186** to a value of a design ratio stored in programmable memory **200**A and then issues a digital signal to control unit **170**A (see FIG. **3**A). The digital signal indicates the difference between the actual ratio and the design ratio. For example, if after 100 reference clock edges, the monitor actual count is 80 and the reference actual count is 20 then the ratio is 8:2. However, if the target ratio is 8:3, then the monitored FETs V_t needs to be changed to give 30 actual counts.

Since the design count is influenced by the actual (as opposed to the designed) V_{DD}/V_{SS} voltage levels (which affects the voltages on the source, drain and gates of FETs) and PFET/NFET temperature, programmable memory **200**A includes a lookup table which comprises a two dimensional matrix of count ratios indexed in a first axis by voltage level increments and in a second axis by temperature increments. Voltage and temperature sensor circuit **205** measures the supply voltage to and temperature of the monitor circuit and passes the information to programmable memory **200**A so a temperature and voltage compensated design ratio can be passed on to comparator **195**A. There is some rounding error, dependent upon the granularity of matrix. Ratios of count values in the matrix may be obtained by simulation of the design, for example by using a software program such as SPICE (simulation program for integrated circuits emphasis). SPICE is a circuit simulator that was originally developed at the Electronics Research Laboratory of the University of California, Berkeley (1975) and now has many commercial variations. The user inputs circuit topology in spice netlist format. The simulator calculates and plots nodal voltages and currents in both time and frequency domains.

FIG. **4**B is a block circuit diagram of an exemplary individual compare circuit of compare unit **165**B of FIG. **3**B. In FIG. **4**B, a compare circuit **180**B includes first edge counter **185**, second edge counter **190**, a comparator **195**B, a programmable memory **200**B and voltage and temperature sense circuit **205**. The output of a monitor ring oscillator **210** (monitoring an FET having a design V_t=P**1** through PN or N**1** through NM) is connected to the count input of first edge counter **185**. The output of first edge counter **185** (a signal indicating the latest actual edge count) is connected to first compare input of a comparator **195**B. A precise reference clock (external or internal to the integrated circuit chip) is connected to the count input of second edge counter **190**. Second edge counter **190** supplies three control signals (reset, start and stop) to first edge counter **185** and a count valid signal to comparator **195**B. A second compare input of comparator **195**B is coupled to programmable memory **200**B, which contains pre-determined target performance values for the monitor ring oscillator **210**. Voltage and temperature sense circuit **205** is connected to programmable memory **200**B and provides lookup values for selecting the appropriate performance target based the temperature of monitor ring oscillator **210** and the voltage supplied to the monitor ring oscillator.

While each compare circuit may include its own programmable memory and a voltage and temperature sense circuit, a common programmable memory may be shared between two or more of the compare circuits, a common voltage and temperature sense circuit may be shared between two or more of the compare circuits, or both a common programmable memory and a common voltage and temperature sense circuit may be shared between two or more of the compare circuits.

Monitor ring oscillator **210** has been described supra, however monitor ring oscillator **210** in FIG. **4**B may represent any of PFET monitors P**1** through PN or NFET monitors N**1** through NM. If ring oscillator **210** represents PFET monitor circuit P**1**, then the PFETs in the signal delay path of the ring oscillator are PFETs designed to have threshold voltage P**1**. If ring oscillator **210** represents PFET monitor P**2**, then the PFETs in the signal delay path of the ring oscillator are PFETs designed to have threshold voltage P**2**. If ring oscillator **210** represents PFET monitor circuit PN, then the PFETs in the signal delay path of the ring oscillator are PFETs designed to have threshold voltage PN. If ring oscillator **210** represents NFET monitor circuit N**1**, then the NFETs in the signal delay path of the ring oscillator are NFETs designed to have threshold voltage N**1**. If ring oscillator **210** represents NFET monitor circuit N**2**, then the NFETs in the signal delay path of the ring oscillator are NFETs designed to have threshold voltage N**2**. If ring oscillator **210** represents NFET monitor circuit NM, then the NFETs in the signal delay path of the ring oscillator are NFETs designed to have threshold voltage NM. The delay through ring oscillator **210** varies as a function of V_t and well bias voltage (and also temperature and supply voltages as described infra).

In operation, second edge counter **190** issues a reset to first edge counter **185** to reset its count to zero. Then second edge counter **190** issues a start to first edge counter **185** and the first edge counter starts counting edges of the signal from ring oscillator **210** and second edge counter starts counting clock edges from the reference clock. When second edge counter **190** reaches a preset count value it issues a stop signal to first edge counter **185** and a count valid signal to comparator **195**B. Comparator **195**B compares the value of the actual count from first edge counter **185** to a value of a design count stored in programmable memory **200**B and then issues a digital signal to control unit **170**B (see FIG. **3**B). The digital signal indicates the difference between the actual edge count and the design edge count. For example, if after 100 reference clock edges, the actual count is 95 and the design count is 90 then the difference is 5 counts, indicating the monitored FETs V_t needs to changed to give 90 actual counts.

Since the design count is influenced by the actual (as opposed to the designed) V_{DD}/V_{SS} voltage levels (which affects the voltages on the source, drain and gates of FETs) and PFET/NFET temperature, programmable memory **200**B includes a lookup table which comprises a two dimensional matrix of counts indexed in a first axis by voltage level increments and in a second axis by temperature increments. Voltage and temperature sensor circuit **205** measures the supply voltage to and temperature of the monitor circuit and passes the information to programmable memory **200**B so a temperature and voltage compensated design count can be passed on to comparator **195**B. There is some rounding error, dependent upon the granularity of matrix. Count values in the matrix may be obtained by simulation of the design, for example by using a software program such as SPICE described supra.

It should be understood that in FIGS. **4**A and **4**B, a ring oscillator is only one example of a circuit that may be used to monitor the performance of FETs and other monitor circuits and if appropriate, other types of compare circuits may be employed to compare the actual performance/switching speed of a PFET or and NFET to the designed performance/switching speed of the PFET or NFET.

FIG. **5**A is a diagram illustrating the control signal generated by control unit **170**A of FIG. **3**A according to the first embodiment of the present invention. In FIG. **5**A, control unit **170**A generates control signals VREGP**2** to VREGPN and VREGN**2** to VREGNM that are sent to respective voltage regulators in adjustable voltage regulator unit **160**A. VREGP**2** adjusts N-well bias voltage on PFETs designed to have threshold voltage P**2**. VREGPN adjusts N-well bias voltage on PFETs designed to have threshold voltage PN. VREGN**2** adjusts P-well bias voltage on NFETs designed to have threshold voltage N**2**. VREGNM adjusts P-well bias voltage on NFETs designed to have threshold voltage NM. There is no VREGP**1** or VREGN**1** signal because PFETs designed to have threshold voltage P**1** and NFETs designed to have threshold voltage N**1** are reference devices.

Control unit **170**A includes logic circuits that "calculate" or interface with on-chip stored software instructions to calculate an adjustment of well bias voltage. The adjustments reflect changes (if any) to be made in the actual threshold voltages of PFETs having design threshold voltages P**2** through PN so that, when changed threshold voltages P**2**' through PN' are divided by the actual threshold voltage P**1**', the design threshold ratios discussed supra (if not the actual V_t values) are restored to within an acceptable tolerance range. For example (P**2**'/P**1**')=(P**2**/P**1**). The adjustments reflect changes (if any) to be made in the actual threshold voltages of NFETs having design threshold voltages N**2** through NM so that, when the changed threshold voltages N**2**' through NM' are divided by the actual threshold voltage N**1**', the design threshold ratios discussed supra (if not the actual V_t values) are restored to within an acceptable tolerance range. For example (N**2**'/N**1**')=(N**2**/N**1**).

The signals VREGP**2** to VREGPN and VREGN**2** to VREGNM may be two-bit or multiple-bit words indicating an magnitude of increase, magnitude of decrease or no change in the well bias to be applied voltage regulators of adjustable voltage regulator unit **160**A. Control unit **170**A also generates an out of range signal, when it is not possible to adjust an individual voltage regulators output voltage any further.

FIG. **5**B is a diagram illustrating the control signal generated by control unit **170**B of FIG. **3**B according to the second embodiment of the present invention. In FIG. **5**B, control unit **170**B generates control signals VREGP**1** to VREGPN and VREGN**1** to VREGNM that are sent to respective voltage regulators in adjustable voltage regulator unit **160**B. VREGP**1** adjusts N-well bias voltage on PFETs designed to have threshold voltage P**1**. VREGPN adjusts N-well bias voltage on PFETs designed to have threshold voltage PN. VREGN**1** adjusts P-well bias voltage on NFETs designed to have threshold voltage N**1**. VREGNM adjusts P-well bias voltage on NFETs designed to have threshold voltage NM.

Control unit **170**B includes logic circuits that "calculate" or interface with on-chip stored software instructions to calculate an adjustment of well bias voltage. The adjustments reflect changes (if any) to be made in the actual threshold voltages of PFETs having design threshold voltages P**1** through PN so that, when changed, the changed threshold voltages P**1**' through PN' should result in the performance (switching speeds) of PFETs having the design threshold voltages P**1** through PN being the designed performance values or within an acceptable tolerance range of the designed performance values, although the actual threshold voltages may not be the designed values. The adjustments reflect changes (if any) to be made in the actual threshold voltages of NFETs having design threshold voltages N**1** through NM so that, when changed, the changed threshold voltages N**1**' through NM' should result in the performance (switching speeds) of NFETS having design threshold voltages N**1** through NM being the designed performance values or within an acceptable tolerance range of the designed performance values, although the actual threshold voltages may not be the designed values.

The signals VREGP**1** to VREGPN and VREGN**1** to VREGNM may be two-bit or multiple-bit words indicating a magnitude of increase, magnitude of decrease or no change in the well bias to be applied to voltage regulators of adjustable voltage regulator unit **160**B. Control unit **170**B also generates an out of range signal, when it is not possible to adjust an individual voltage regulators output voltage any further.

FIG. **6** is a schematic block diagram of a typical voltage regulator used to adjust well bias according to embodiments of the present invention. In FIG. **6**, a voltage regulator **215** includes a bandgap voltage reference **220**, a digital to analog converter **225** an operational amplifier **230**, a PFET **235** and a resistor **240**. The output of bandgap voltage reference **220** is connected to an input of digital to analog converter **225** and controls signals VREGPX or VREGNY (where X=1 to N and Y=1 to M) are connected to control pins of the digital to analog converter. The output of digital to analog converter **225** is connected to a first input of operational amplifier **230** and the output of the operational amplifier is connected to the gate of PFET **235**. The source of PFET **235** is connected to V_{DD} and the drain of PFET **235** is connected to ground though resistor **240**, to a second input of operational amplifier **230** and to the output of voltage regulator **215**. The output voltage regulator **215** is connected to well PX or NY corresponding to the VREG signal applied to the input of the voltage regulator.

FIG. **7**A is a diagram illustrating an exemplary floor plan of an integrated circuit chip according to the embodiments of the present invention. While the different V_t NFETs and PFETs may be placed anywhere on the integrated circuit chip this requires extensive wiring to distribute the well bias voltages. In one option, illustrated ion FIG. **7**A, PFETs of the same V_t

are formed in common N wells **245A1** to **245**AN and NFETs of the same V_t are formed in common P wells **245**B**1** to **245**BM on integrated circuit chip **250**. This reduces the amount of well bias wiring from threshold voltage control circuit **155**B. Notice that if threshold voltage control circuit **155**B is replaced by threshold voltage control circuit **155**A (see FIG. **3**A) then there are no wires to P-well **245A1** and N-well **245**B**1** and in fact, those transistors need not be in a common well, but may be dispersed throughout the integrated circuit chip.

FIG. **7**B is an exemplary cross-sectional diagram of multiple field effect transistors formed in a common well. In FIG. **7**B, a group of PFETs P**2** are formed in a common N-well **255**, which is connected to VREGP**2**. The crosshatched regions indicate dielectric material.

FIG. **8** is a flowchart of the methods of controlling threshold voltages of multiple-threshold voltage devices according to the embodiments of the present invention. In FIG. **8**, after power-up, in step **300**, the performance monitor circuits monitor the performance of the various V_t NFETs and PFETs and in step **305** two options are presented. The first option is to adjust performance ratios of different V_t PFETs/INFETs relative to a reference threshold PFET/NFET performance (the reference PFET/NFET is one of the different V_t PFETs/NFETs) and the second option is to adjust the performance of all different V_t PFETs/NFETs to design values. If the first option is chosen, the method proceeds to step **310**, in which the first embodiment of the present invention described supra is employed. If the second option is chosen the method proceeds to step **315**, in which the second embodiment of the present invention described supra is employed. After step **310** or **315** is performed two additional options are presented in step **320**. The first additional option is to perform a one-time performance correction, and the second additional option is to perform continuous performance corrections. If the first additional option is chosen, the well bias voltages are adjusted by a single amount and the method terminates. Of course, the method using the first additional option may be repeated periodically. If the second additional option is chosen, the well bias voltages are adjusted incrementally by small amounts, and the monitors re-sampled and the well bias voltages adjusted incrementally in a continuous loop. If no adjustment is required (the monitor performance is already acceptable), the voltage regulators are not changed.

Thus, the embodiments of the present invention provide methods and circuits for maintaining the design values and/or relationships between the different threshold voltage values of multi-threshold voltage devices.

The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.

What is claimed is:

1. A method, comprising:

providing a first set of field effect transistors (FETs) having a designed first threshold voltage and a second set of FETs having a designed second threshold voltage, said first threshold voltage different from said second threshold voltage;

providing a first monitor circuit containing at least one FET of said first set of FETs and a second monitor circuit containing at least one FET of said second set of FETs;

providing a compare circuit adapted to generate a compare signal based on a performance measurement of said first monitor circuit and a performance measurement of said second monitor circuit, said compare circuit including a first edge counter connected between said first monitor circuit and a first comparator and a second edge counter connected between a reference clock and said first comparator;

providing a control unit adapted to generate a control signal to a voltage regulator based on said compare signal, said voltage regulator adapted to supply a bias voltage to wells of FETs of said second set of FETs, the value of said bias voltage based on said control signal;

providing an additional compare circuit including a third edge counter connected between said second monitor circuit and a second comparator and a fourth edge counter connected between said reference clock and said second comparator;

said control unit is adapted to generate an additional control signal based on an additional compare signal generated by said additional compare circuit;

providing an additional voltage regulator, said additional voltage regulator adapted to supply an additional bias voltage to wells of FETs of said first set of FETs, the value of said additional bias voltage based on said additional control signal; and

providing a first memory device containing a first performance specification for said first monitor circuit coupled to said first comparator and a second memory device memory containing a second performance specification for said second monitor circuit coupled to said second comparator.

2. The method of claim **1**, wherein said compare circuit includes a first edge counter connected between said first monitor circuit and a first comparator, a second edge counter connected between a reference clock and said first comparator and third edge counter connected between said second monitor circuit and said comparator; and further including:

providing a memory device containing a ratio of said first performance specifications of said first monitor circuit to a second performance specification of said second monitor device, said memory device coupled to said comparator.

3. The method of claim **2**, wherein said control unit is adapted to generate said control signal such that a ratio of a performance of FETs of said first set of FETs and a performance of FETs of said second set of FETs is equal to a performance ratio specification or is within an acceptable tolerance range of said performance ratio specification.

4. The method of claim **1**, wherein said control unit is adapted to generate said control signal and said additional control signal such that a performance of FETs of said first set of FETs is equal to a first performance specification or is within an acceptable tolerance range of said first performance specification and such that a performance of FETs of said second set of FETs is equal to a second performance specification or is within an acceptable tolerance range of said second performance specification.

5. The method of claim **1**, further including:

providing means for adjusting expected values of said performance measurements of said first and second monitor circuits based on a temperature of and supply voltage to said first and second monitor circuits.

6. A method comprising:

(a) measuring a performance of a first monitor circuit having at least one field effect transistor (FET) of a first set of FETs, each FET of said first set of FETs having a designed first threshold voltage;

(b) measuring a performance of a second monitor circuit having at least one field effect transistor (FET) of a second set of FETs, each FET of said second set of FETs having a designed second threshold voltage, said second threshold voltage different from said first threshold voltage;

(c) applying a bias voltage to wells of said FETs of said second set of FETs based on comparing said performances of said first and second monitor circuits measured in steps (a) and (b) to specified performances of said first and second monitor circuits; and

(d) applying an additional bias voltage to wells of FETs of said first set of FETs based on said comparing said performances of said first and second monitor circuits measured in steps (a) and (b) to specified performances of said first and second monitor circuits.

7. The method of claim **6**, step (d) further including:

causing a performance of FETs of said first set of FETs to be equal to a first performance specification or within an acceptable tolerance range of said first performance specification and causing a performance of FETs of said second set of FETs to be equal to a second performance specification or within an acceptable tolerance range of said second performance specification by said applying said bias voltage and said additional bias voltage.

8. The method of claim **6**, step (d) further including, incrementally increasing, incrementally decreasing or not incrementing said bias voltage and said additional bias voltage and repeating steps (a) through (d) continuously while power is applied to an integrated circuit containing said first and second monitor circuits.

9. The method of claim **6**, step (d) further including:

causing a ratio of a performance of FETs of said first set of FETs and a performance of FETs of said second set of FETs to be equal to a performance ratio specification or within an acceptable tolerance range of said performance ratio specification by said applying said bias voltage.

10. The method of claim **6**, step (d) further including, incrementally increasing, incrementally decreasing or not incrementing said bias voltage and repeating steps (a) through (d) continuously while power is applied to an integrated circuit containing said first and second monitor circuits.

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