US 20210375910A1

(19) **United States**
(12) **Patent Application Publication**
BARASKAR et al.
(10) **Pub. No.: US 2021/0375910 A1**
(43) **Pub. Date: Dec. 2, 2021**

(54) **THREE-DIMENSIONAL MEMORY DEVICE CONTAINING III-V COMPOUND SEMICONDUCTOR CHANNEL AND CONTACTS AND METHOD OF MAKING THE SAME**

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(21) Appl. No.: **16/887,818**

(22) Filed: **May 29, 2020**

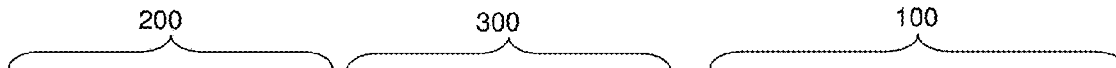
Publication Classification

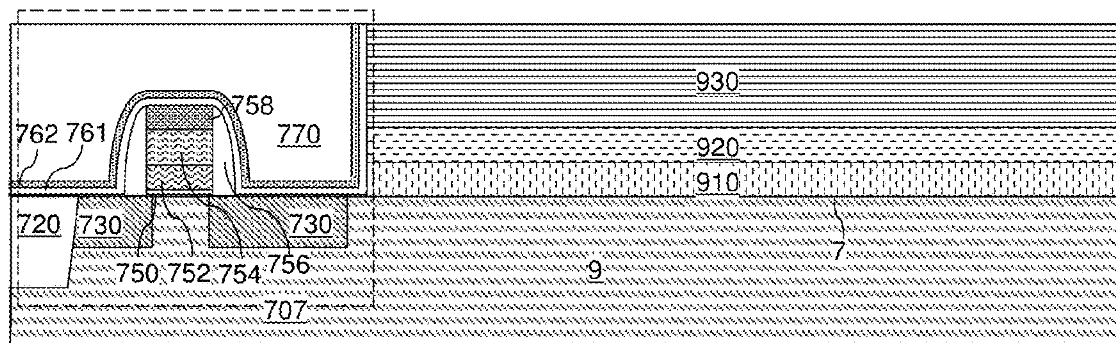
(51) **Int. Cl.**
H01L 27/11582 (2006.01)
H01L 27/11565 (2006.01)
H01L 27/1157 (2006.01)
H01L 27/11519 (2006.01)
H01L 27/11524 (2006.01)
H01L 27/11543 (2006.01)
H01L 27/11556 (2006.01)
H01L 29/207 (2006.01)
H01L 23/522 (2006.01)

(52) **U.S. Cl.**
CPC .. ***H01L 27/11582*** (2013.01); ***H01L 27/11565*** (2013.01); ***H01L 27/1157*** (2013.01); ***H01L 27/11519*** (2013.01); ***H01L 23/5226*** (2013.01); ***H01L 27/11543*** (2013.01); ***H01L 27/11556*** (2013.01); ***H01L 29/207*** (2013.01); ***H01L 27/11524*** (2013.01)

(57) **ABSTRACT**

A three-dimensional memory device includes an alternating stack of insulating layers and electrically conductive layers, and a memory stack structure vertically extending through the alternating stack. The memory stack structure includes a vertical semiconductor channel and a memory film. The vertical semiconductor channel can include a III-V compound semiconductor channel material. A III-V compound substrate semiconductor layer or a III-V compound semiconductor source region can be used to provide low-resistance electrical connection to a bottom end of the vertical semiconductor channel, and a drain region including a graded III-V compound semiconductor material can be used to provide low-resistance electrical connection to a top end of the vertical semiconductor channel.





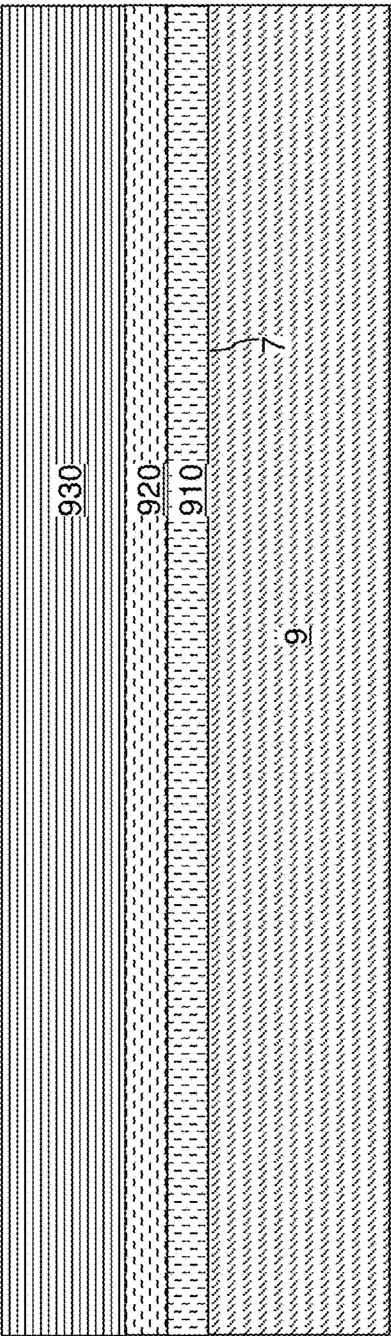


FIG. 1

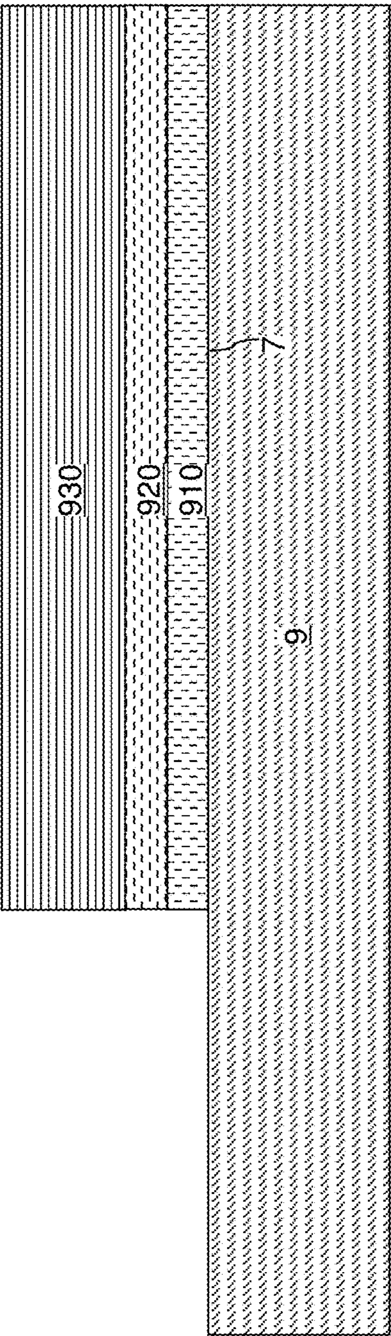
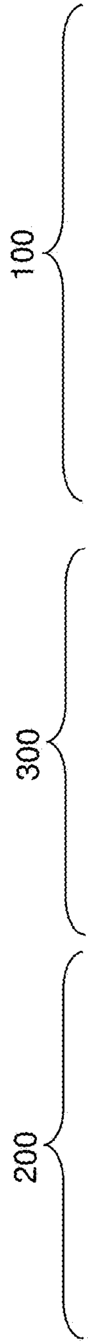


FIG. 2



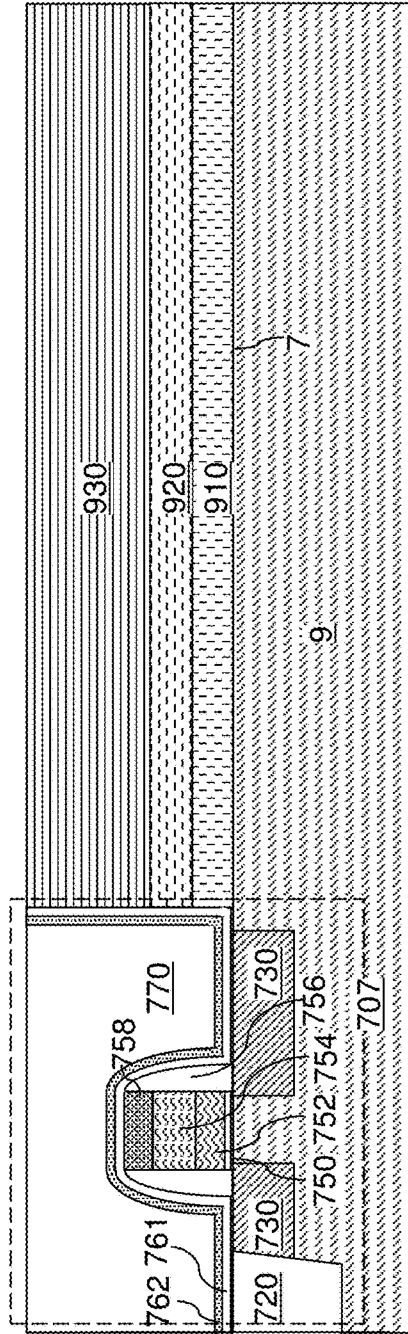


FIG. 3

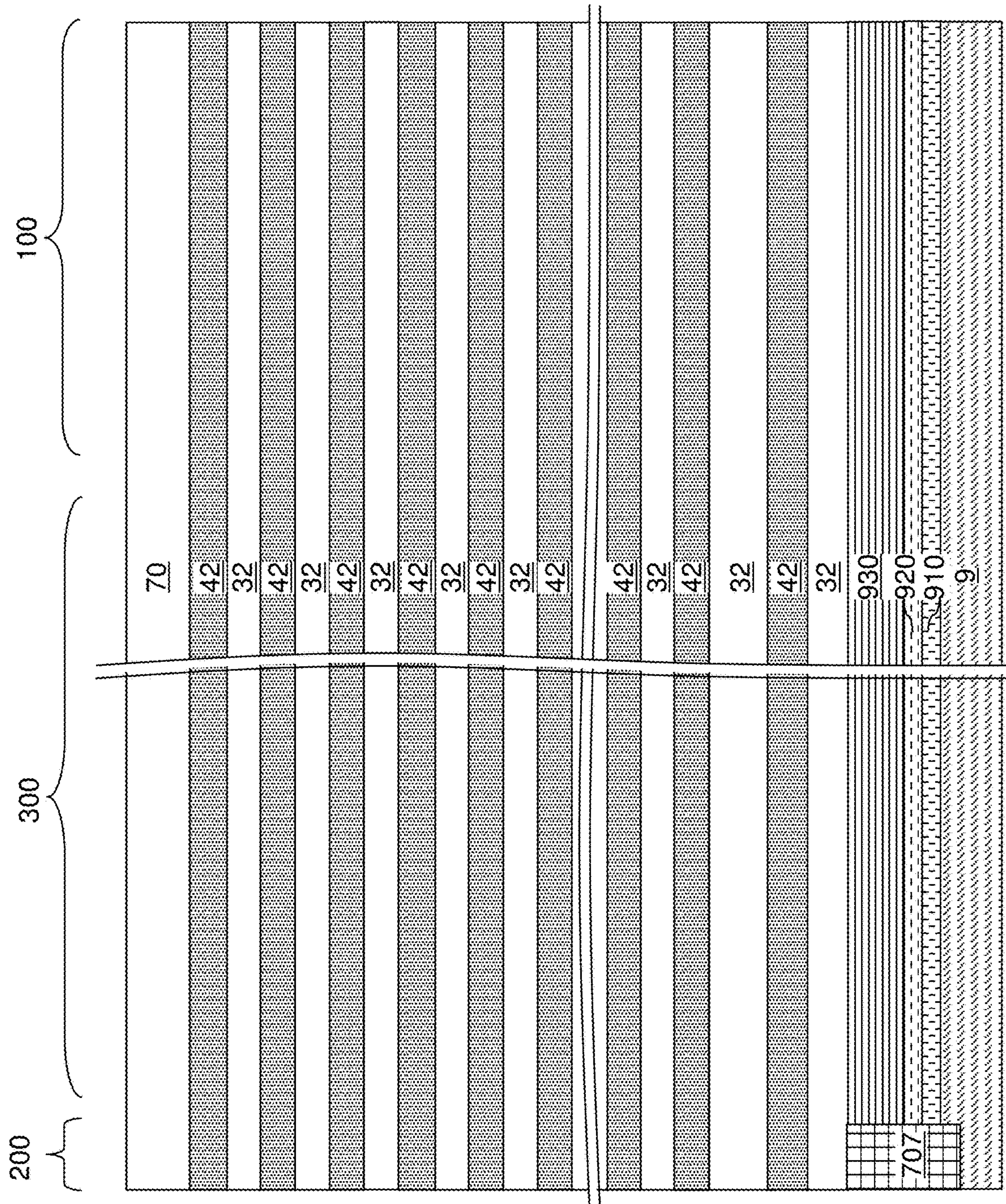


FIG. 4

FIG. 5

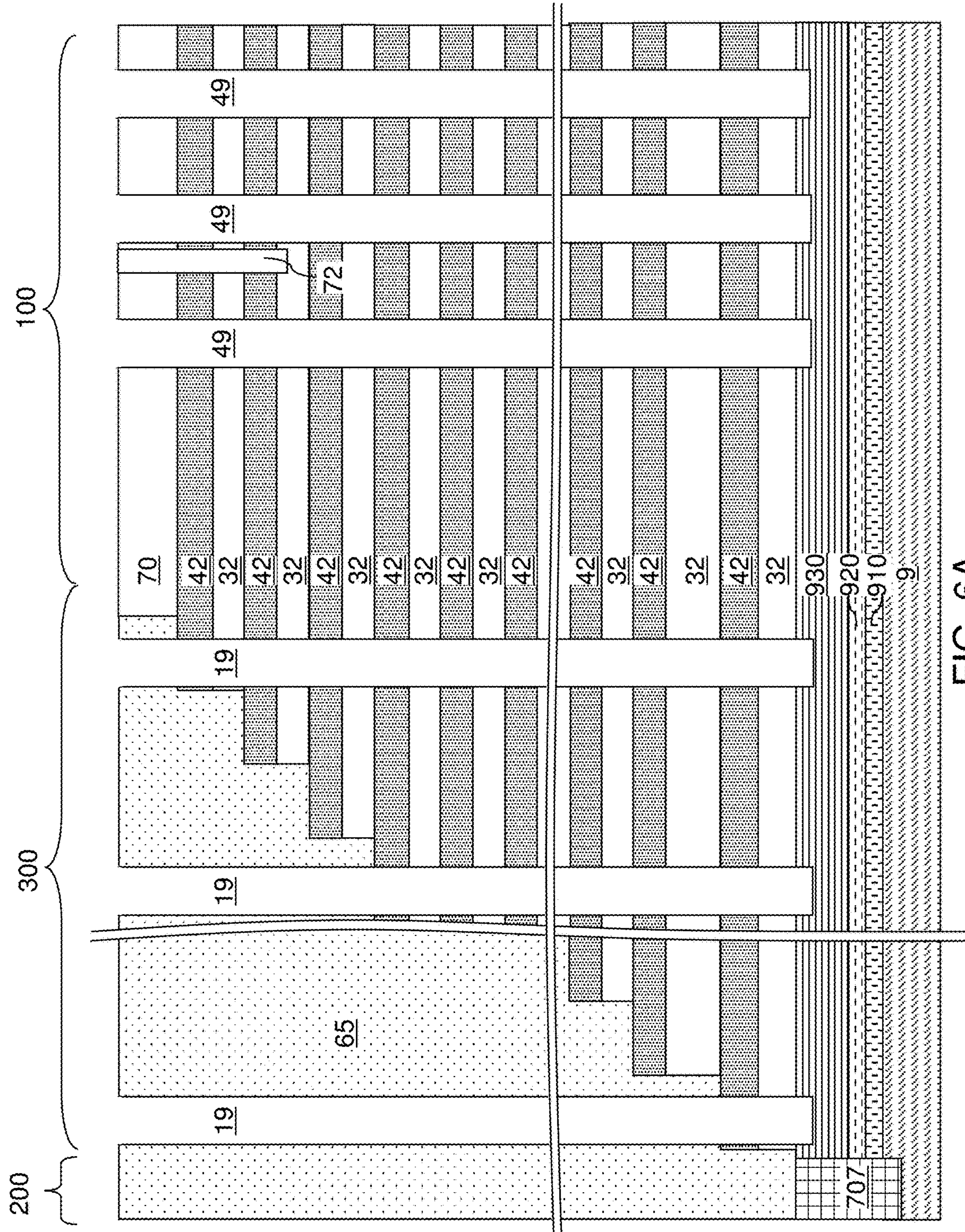


FIG. 6A

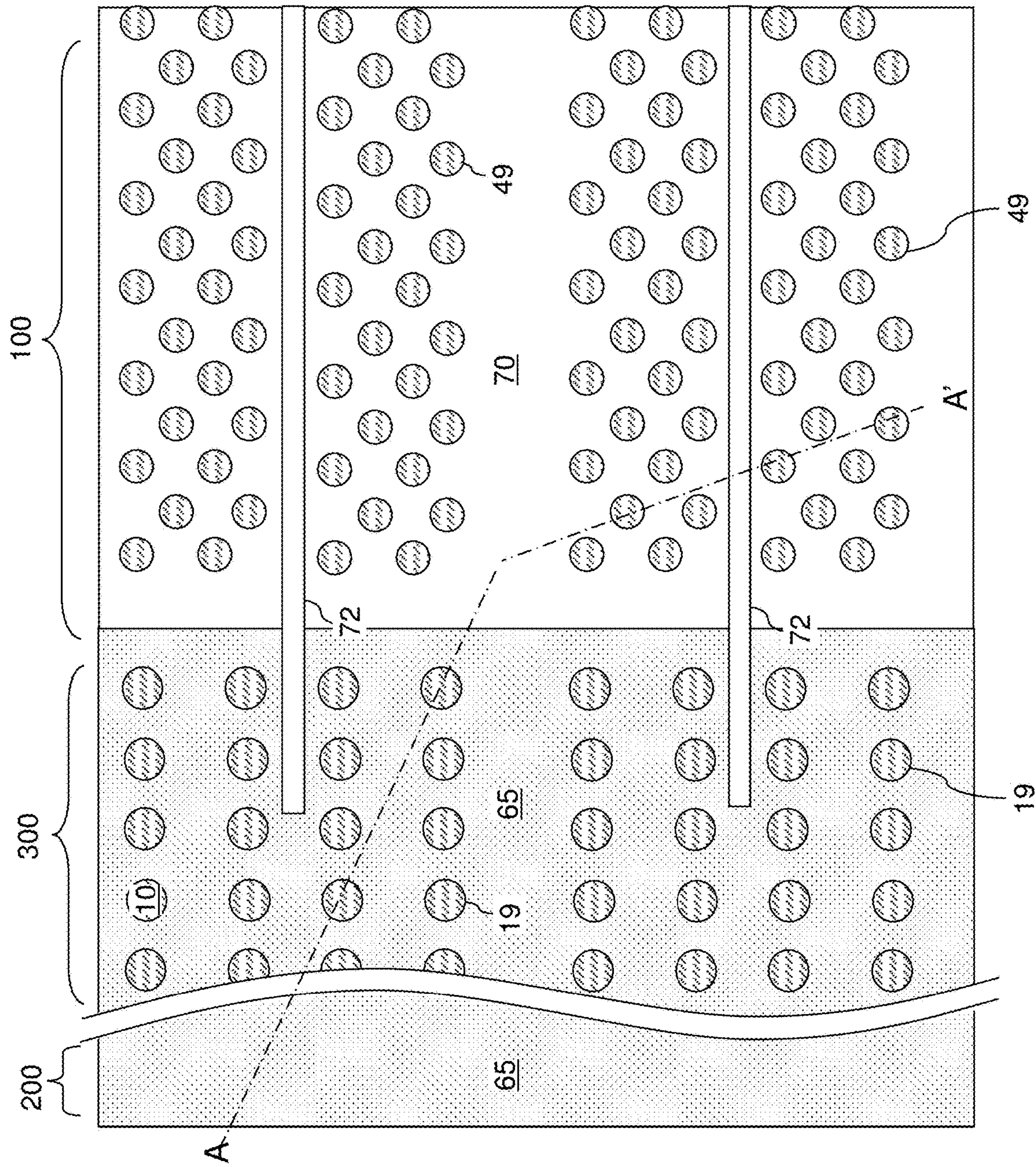


FIG. 6B

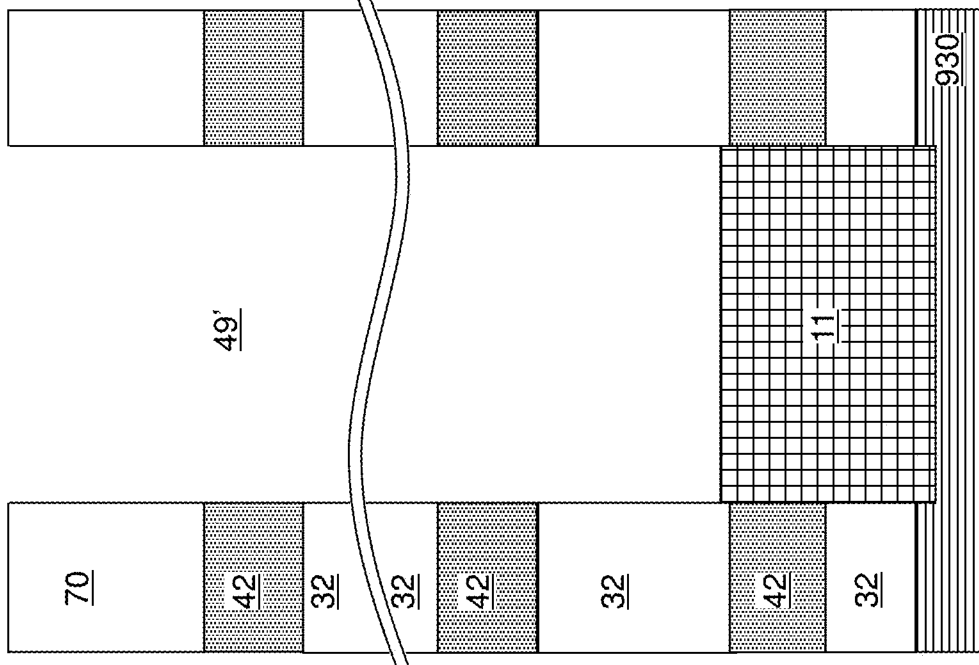


FIG. 7B

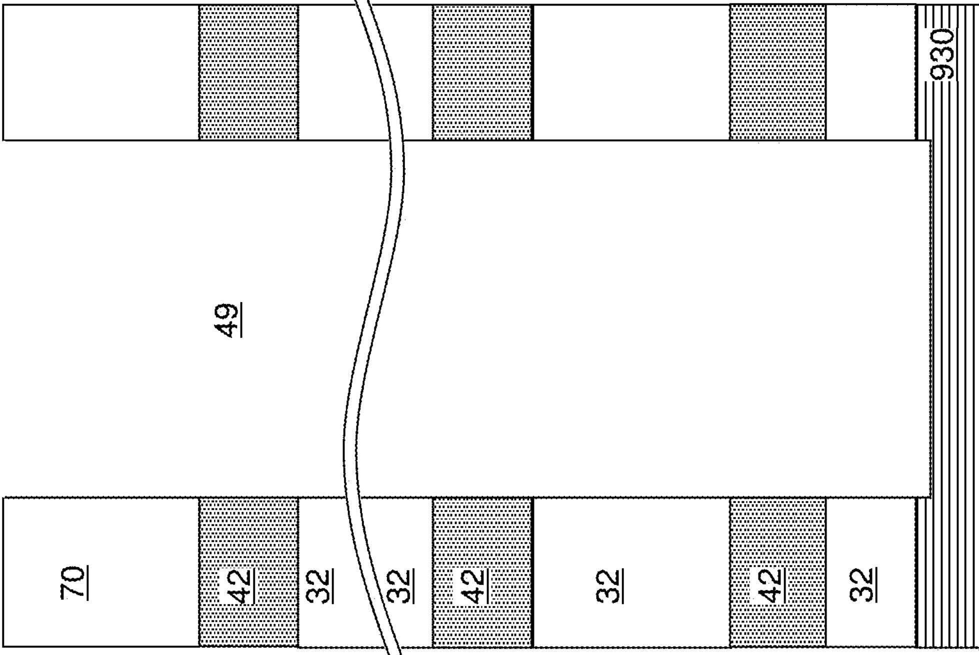


FIG. 7A

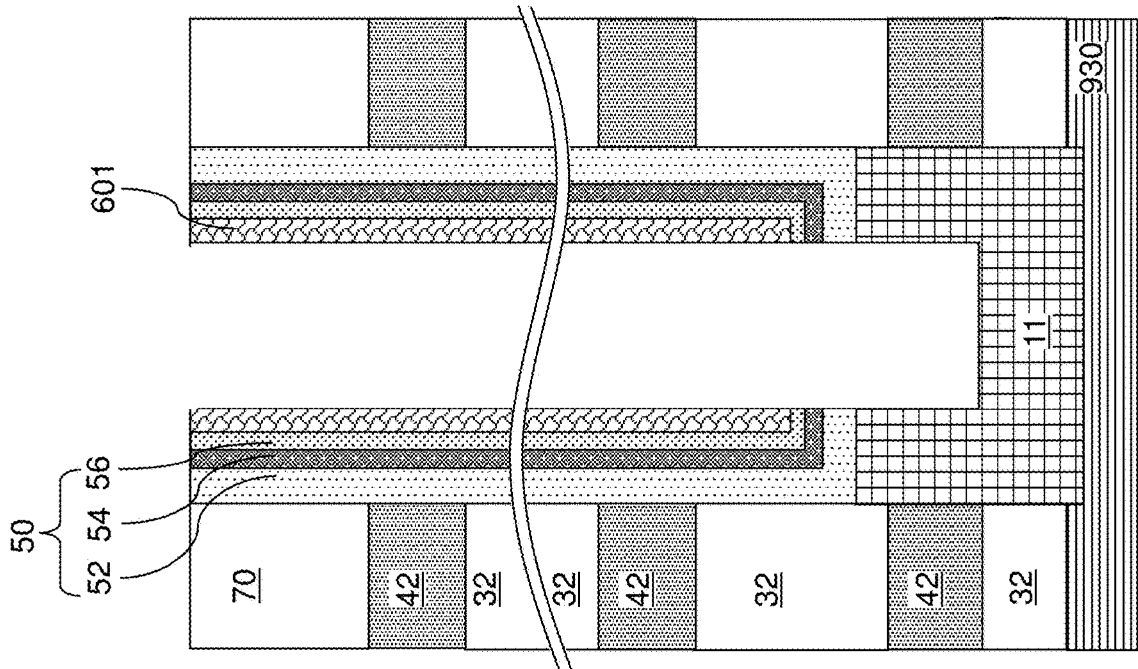


FIG. 7D

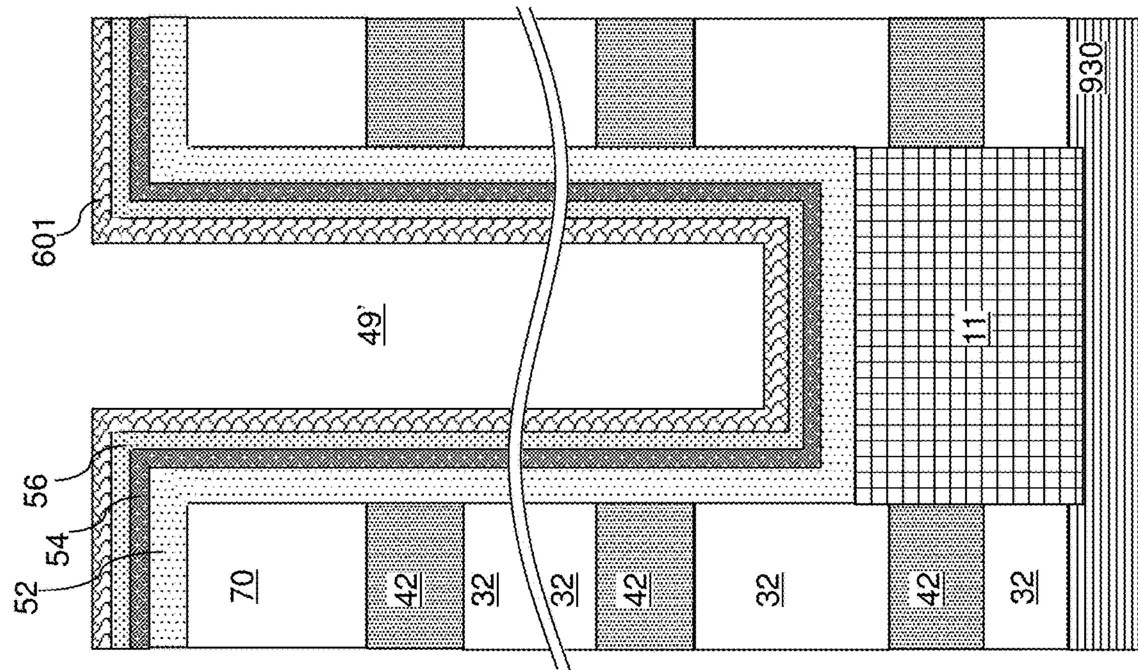


FIG. 7C

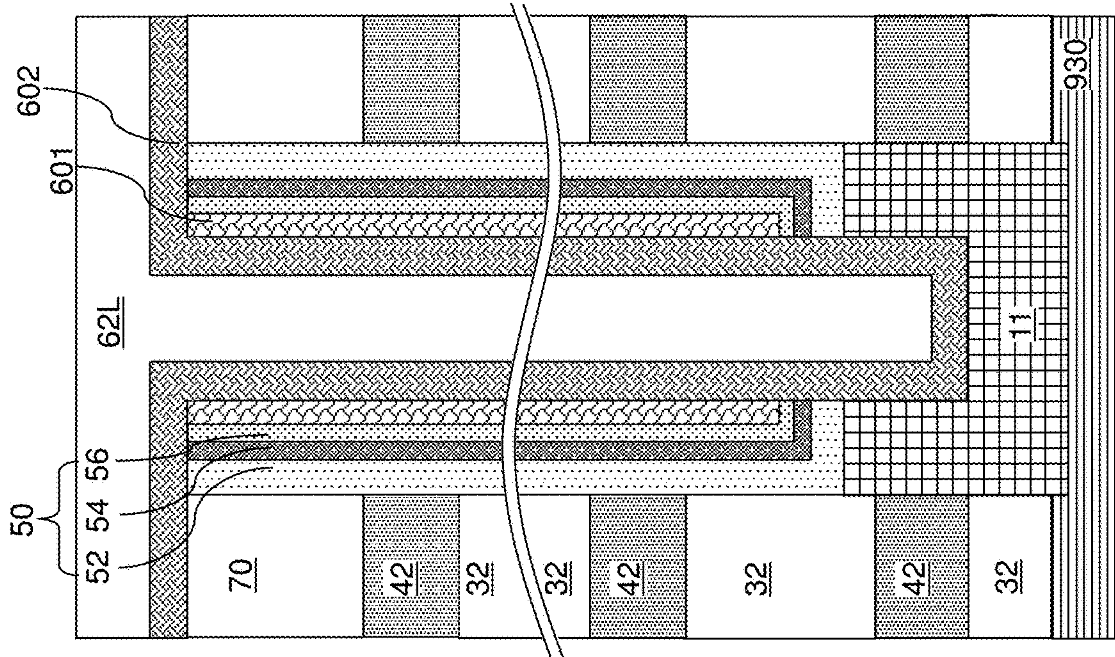


FIG. 7F

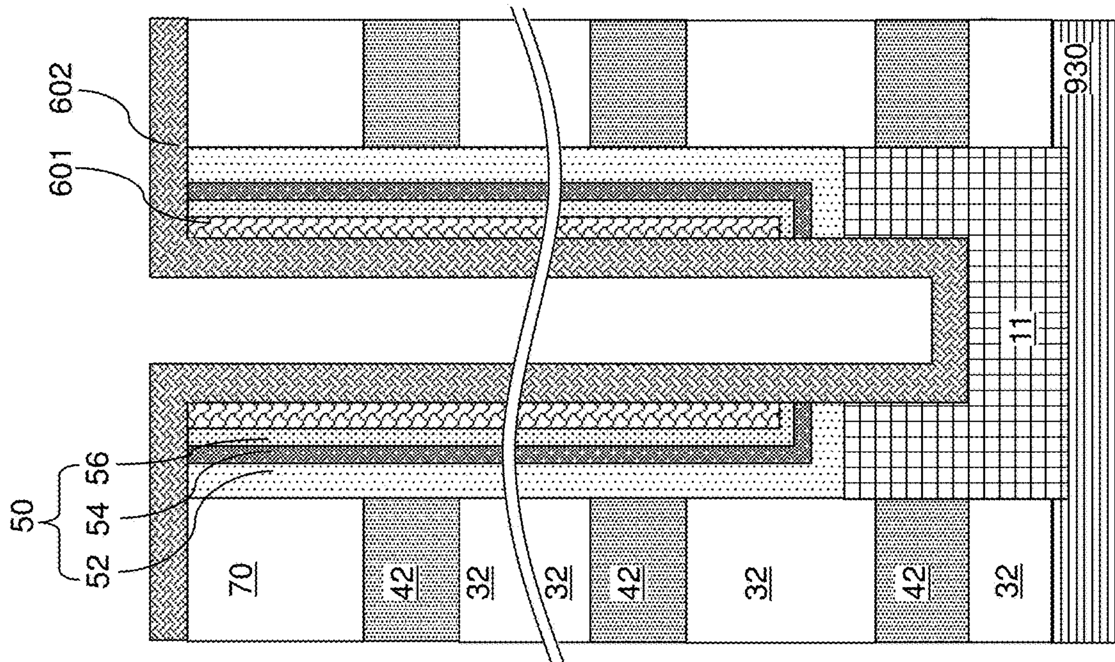


FIG. 7E

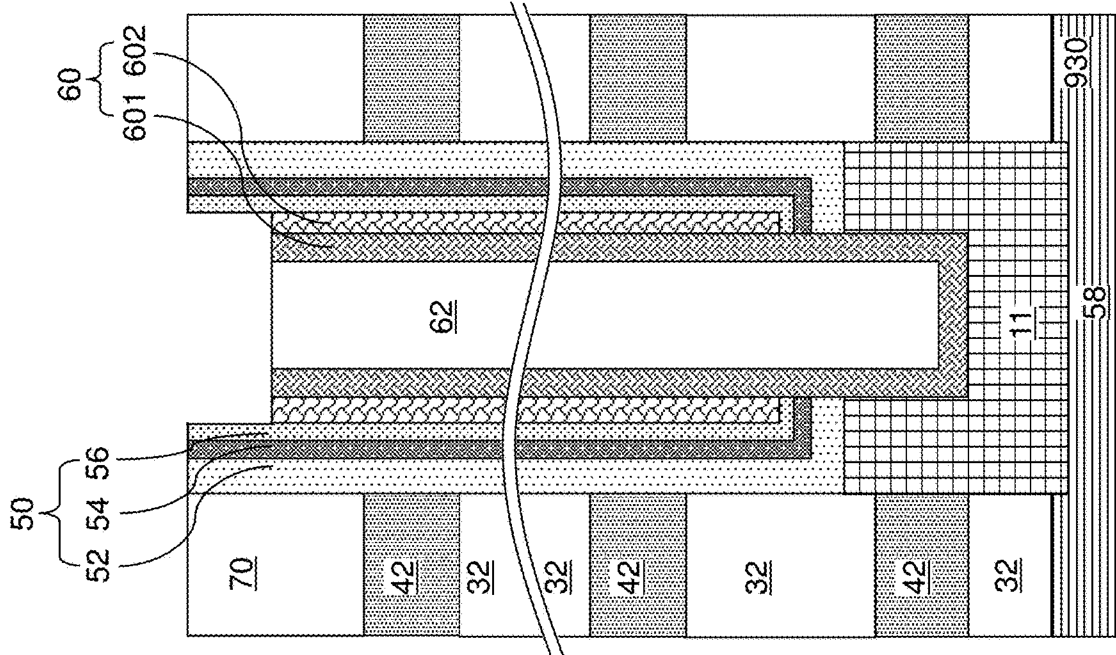


FIG. 7H

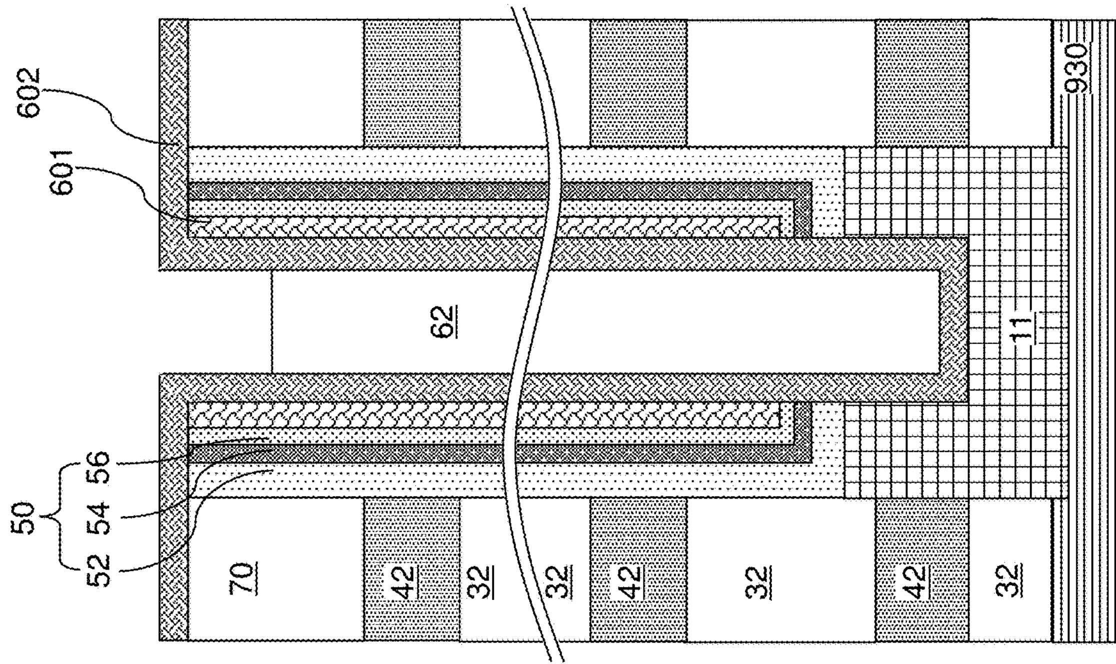


FIG. 7G

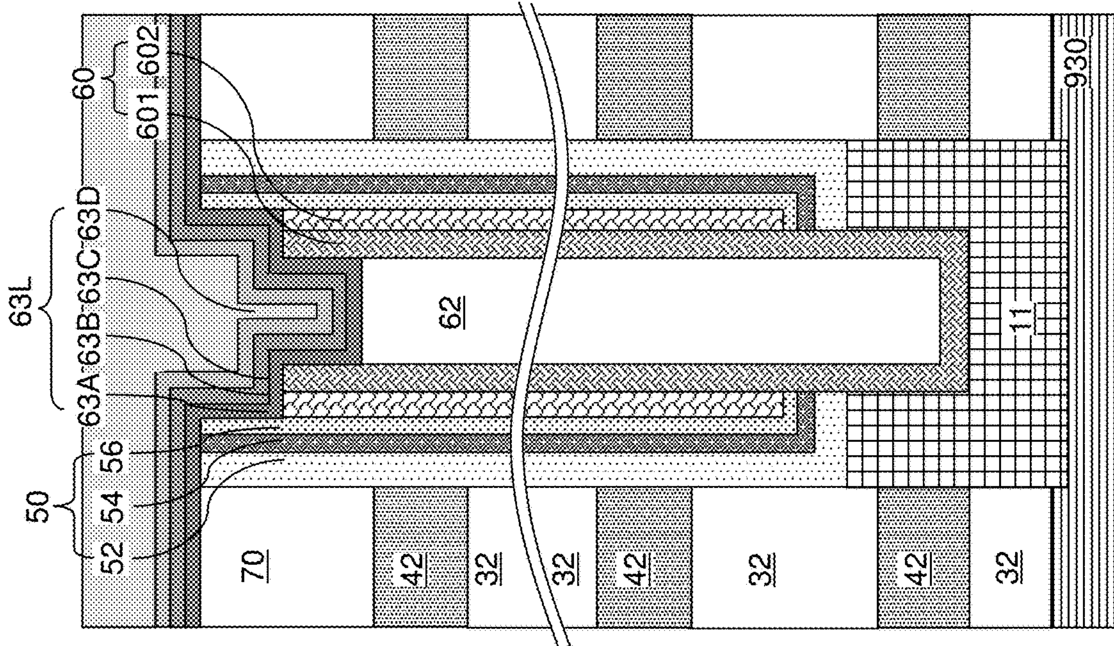


FIG. 7J

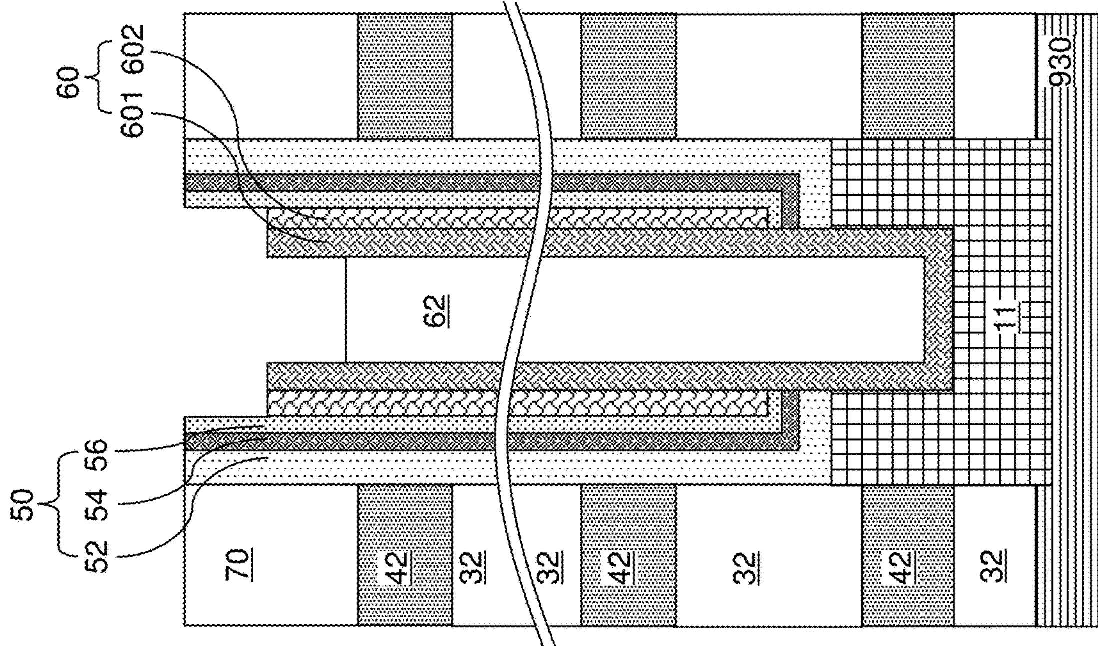


FIG. 7I

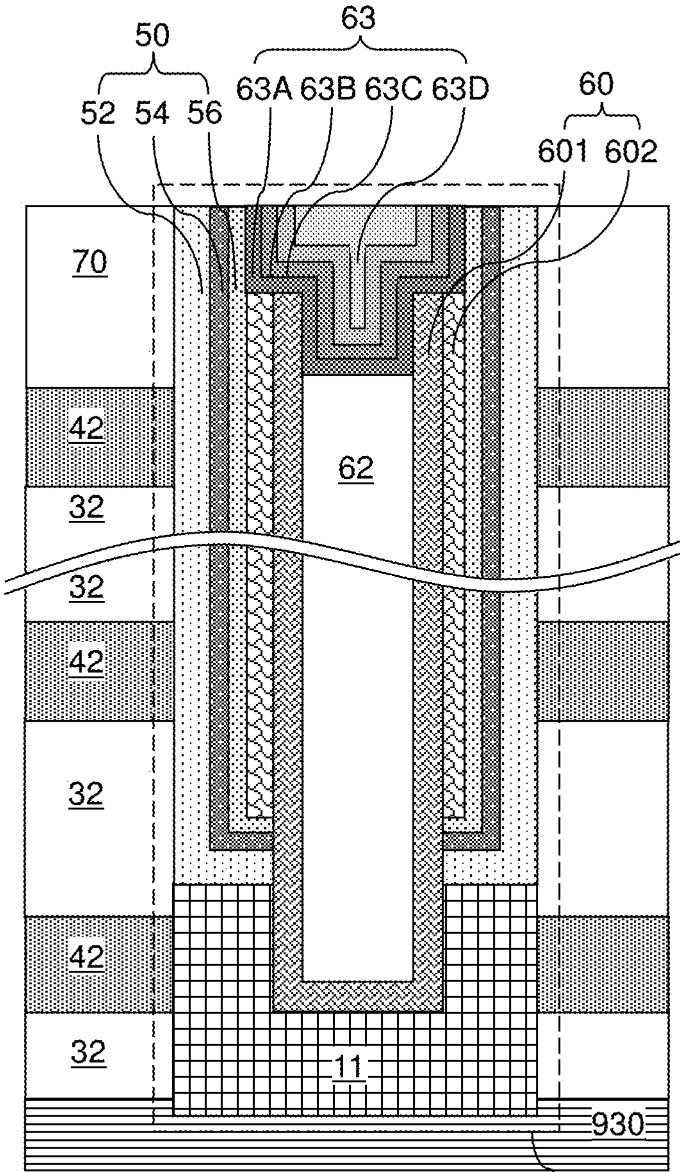


FIG. 7K

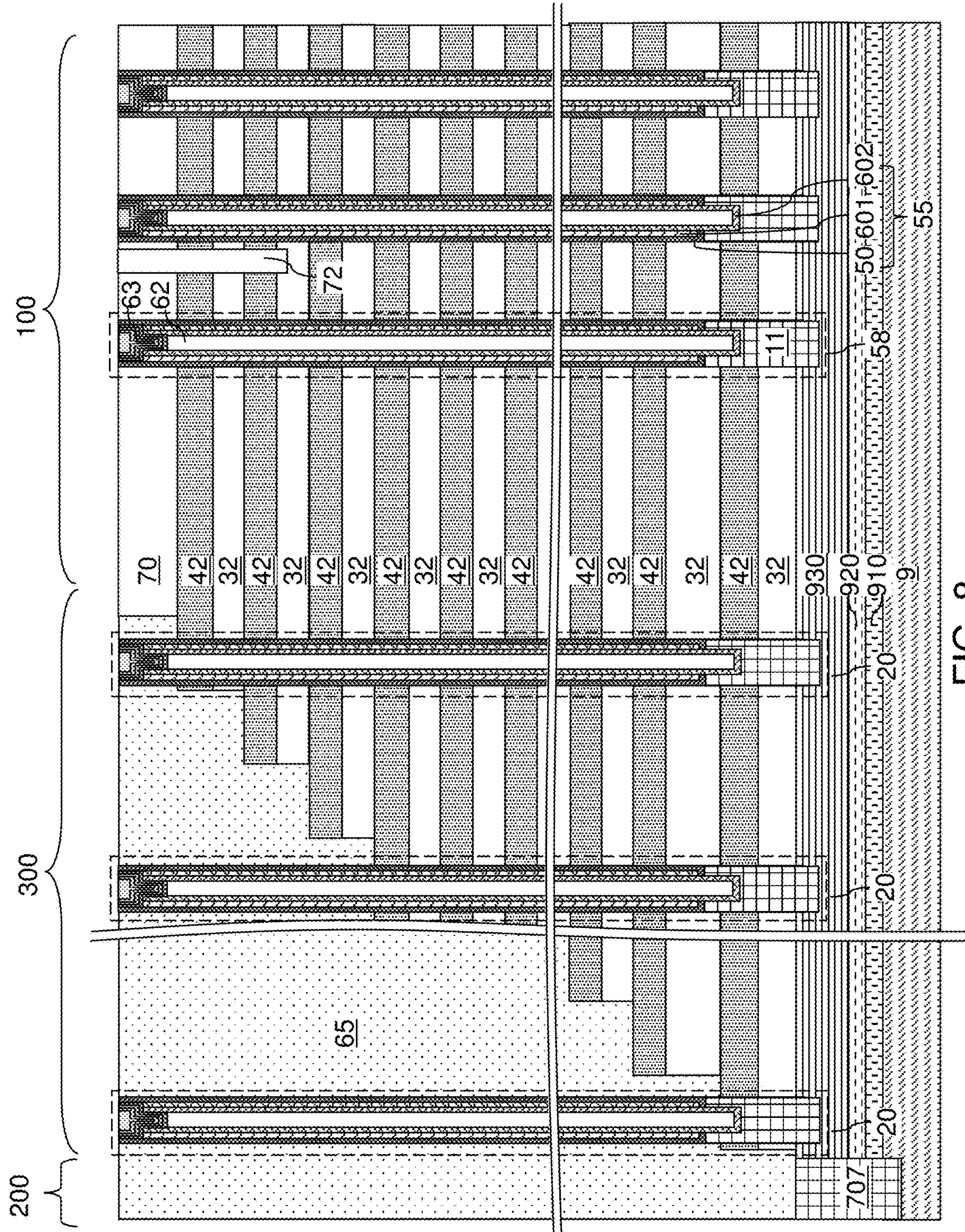


FIG. 8

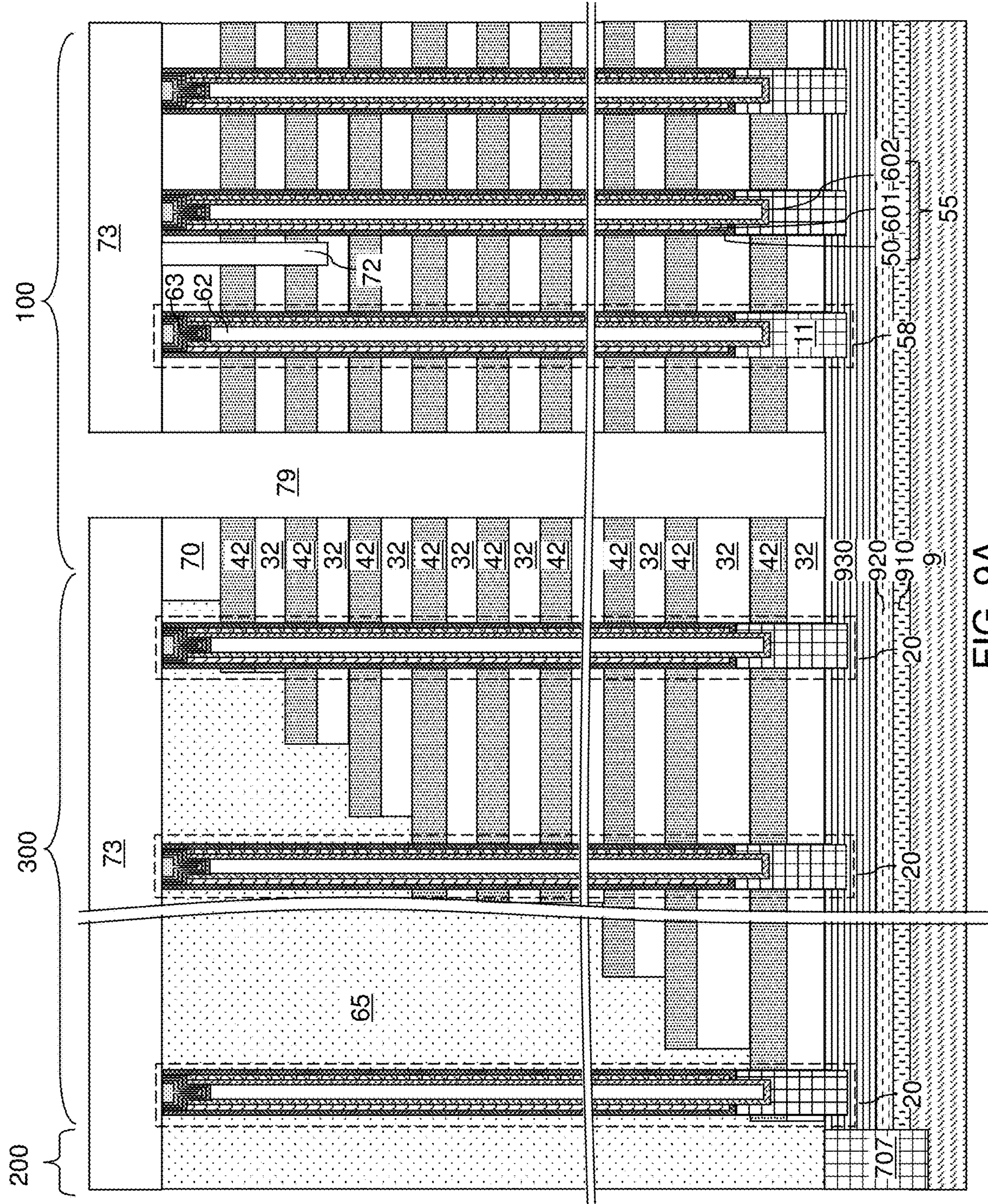


FIG. 9A

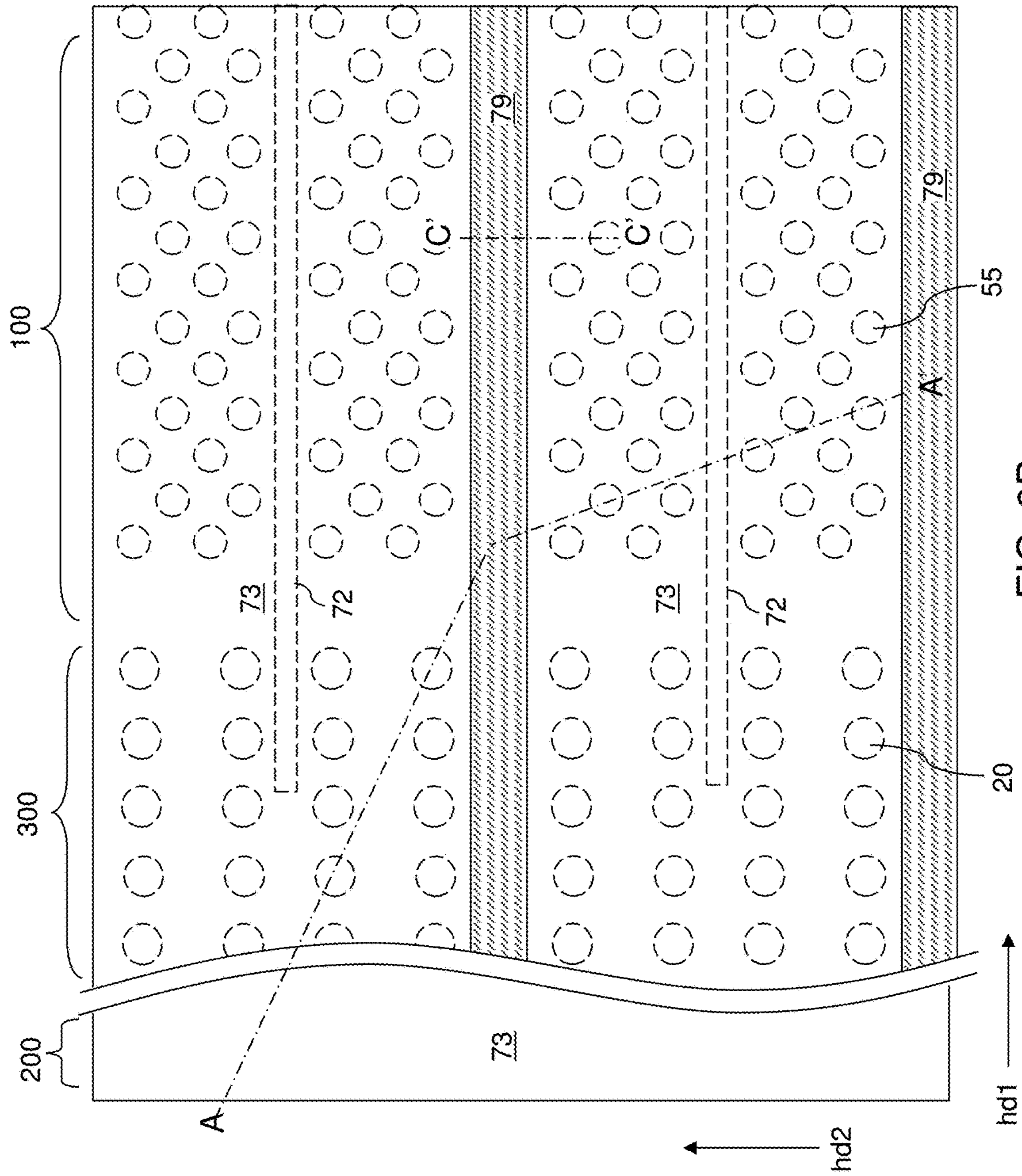


FIG. 9B

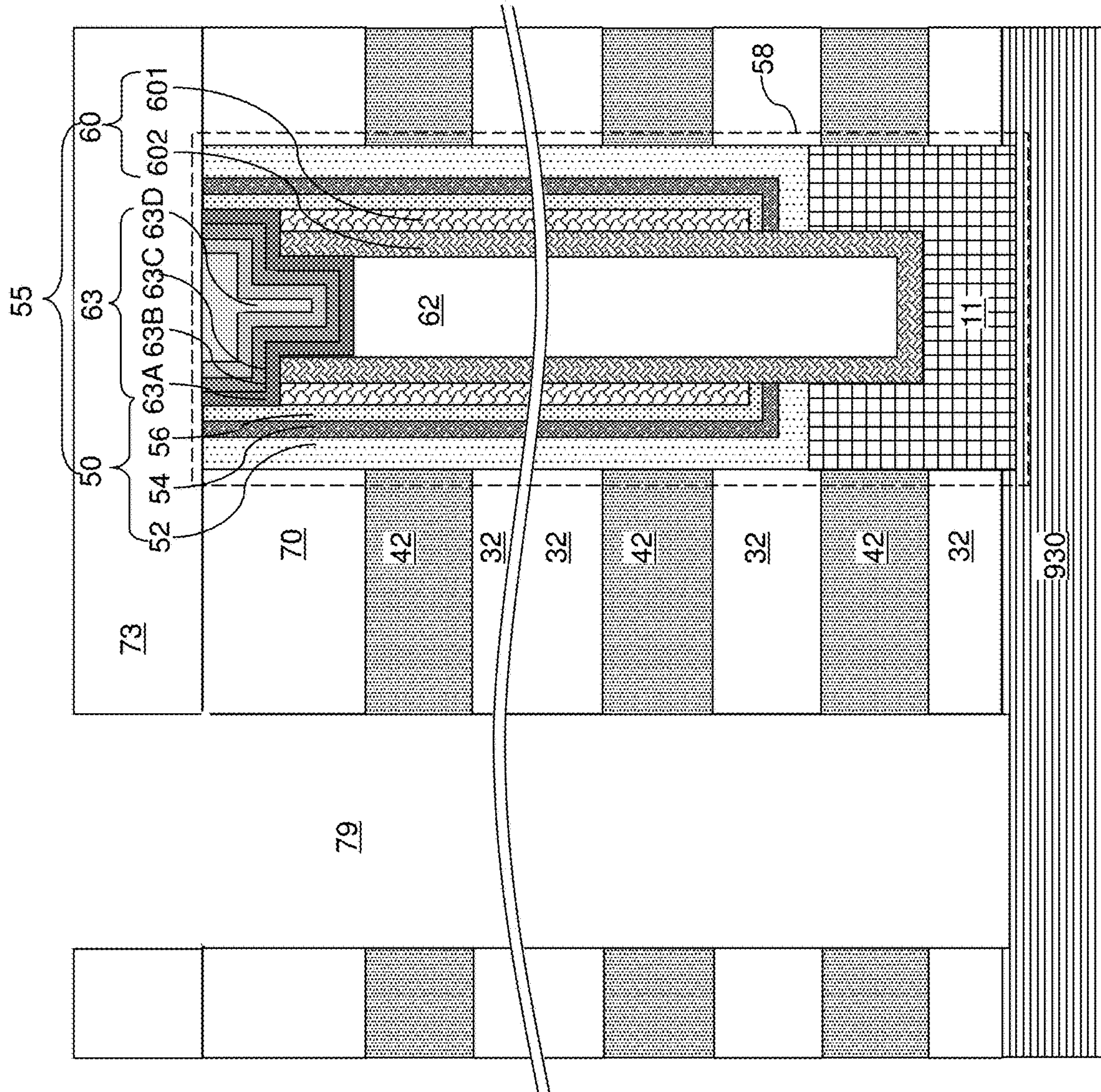


FIG. 9C

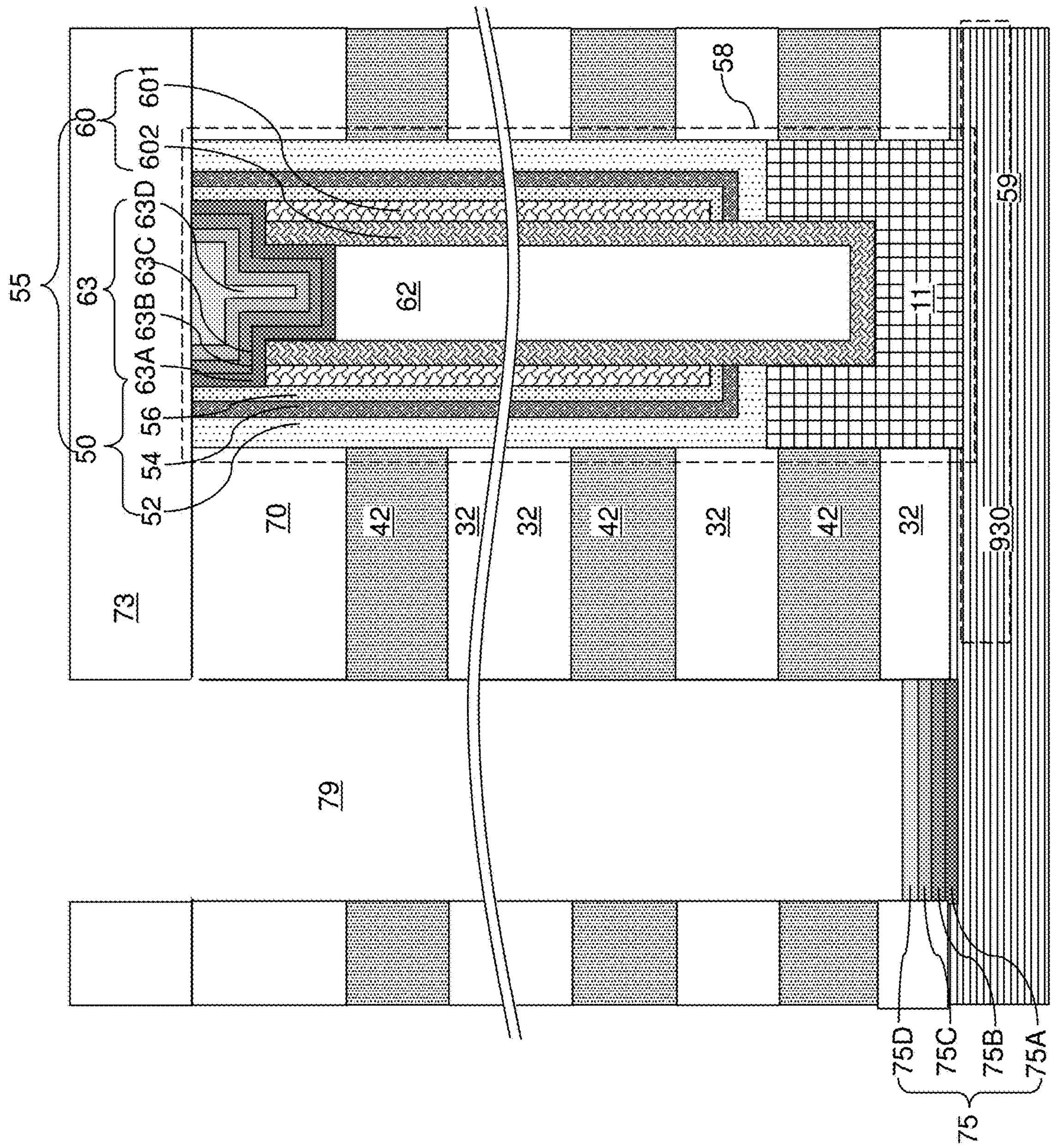


FIG. 10

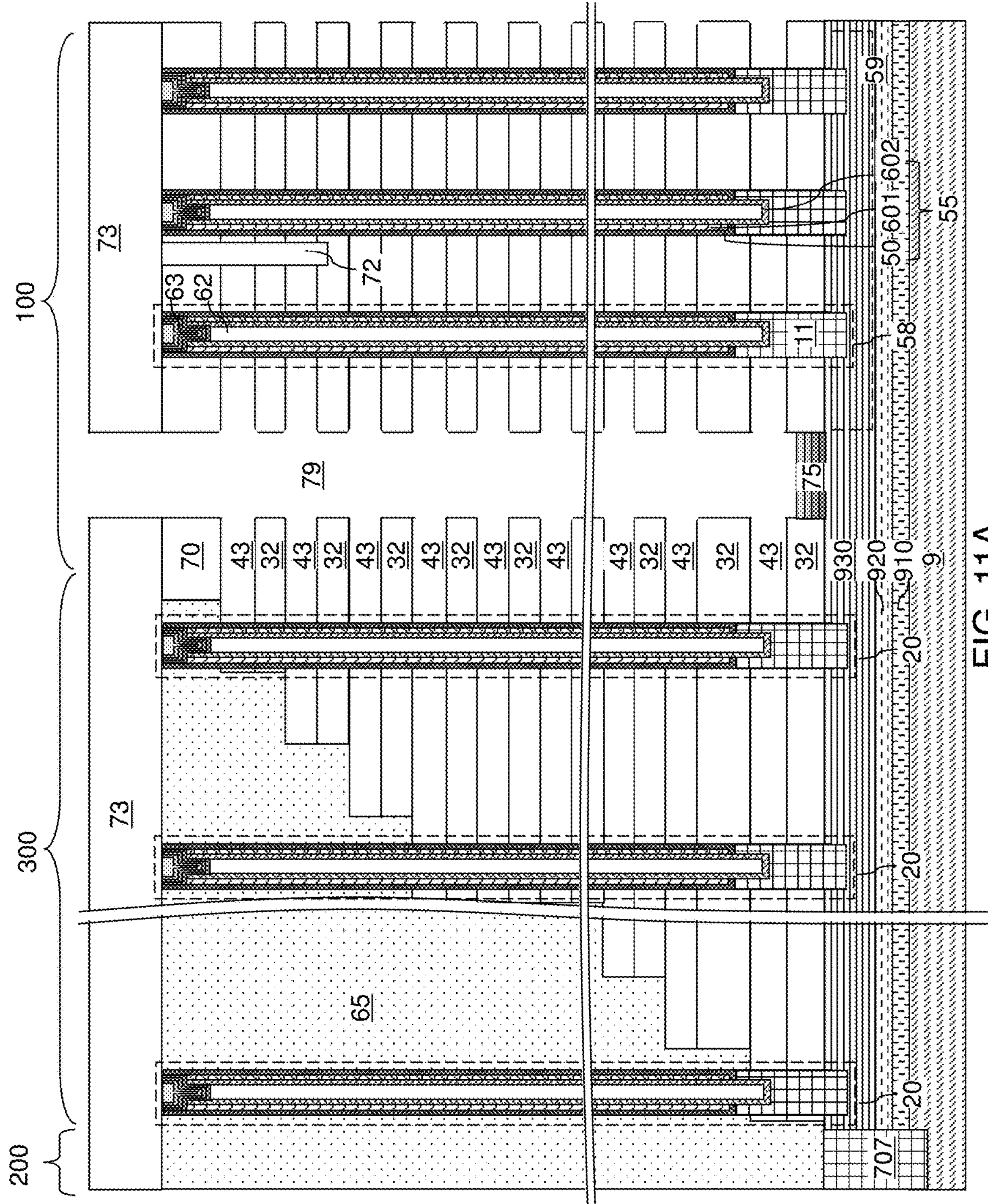


FIG. 11A

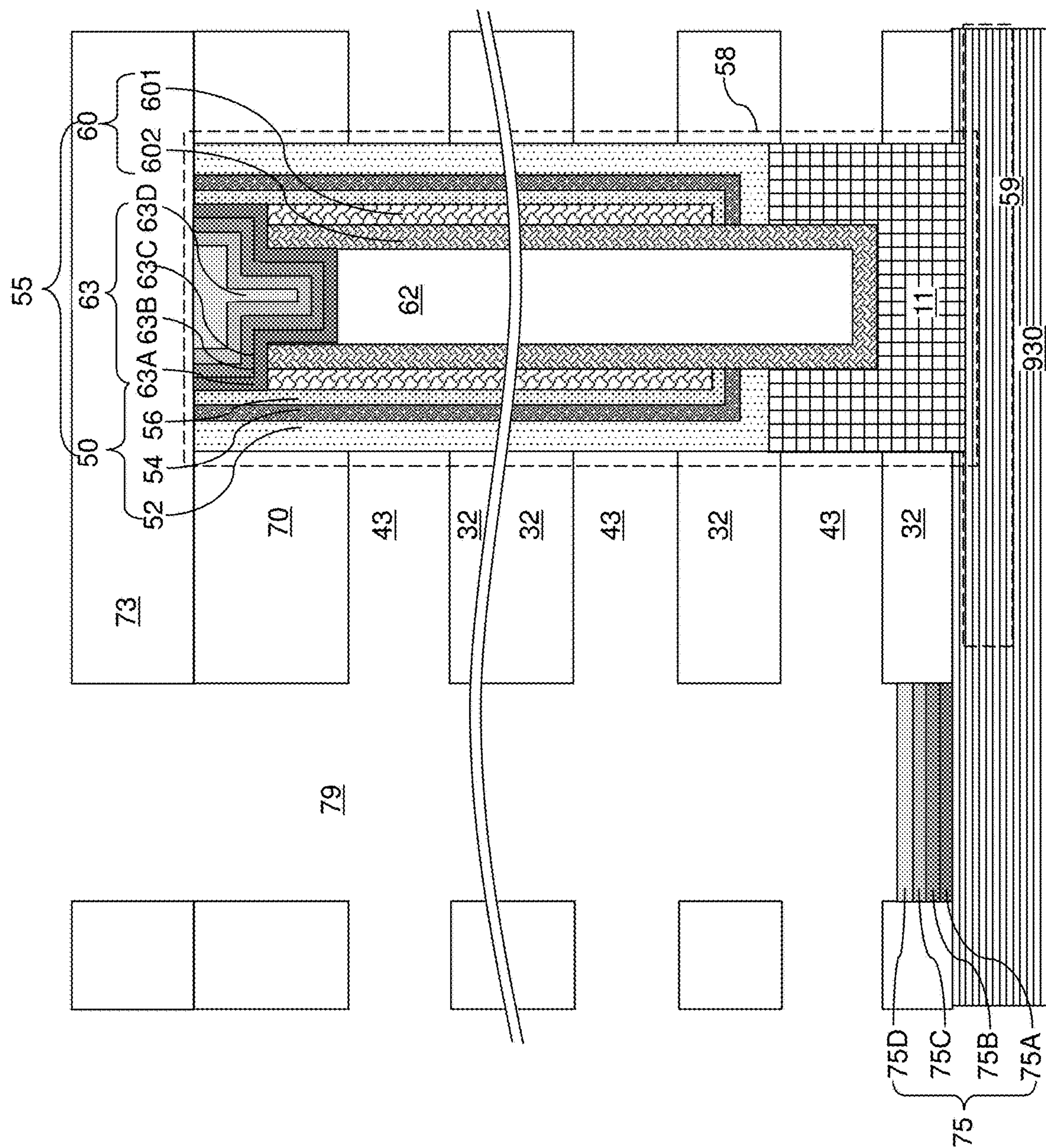


FIG. 11B

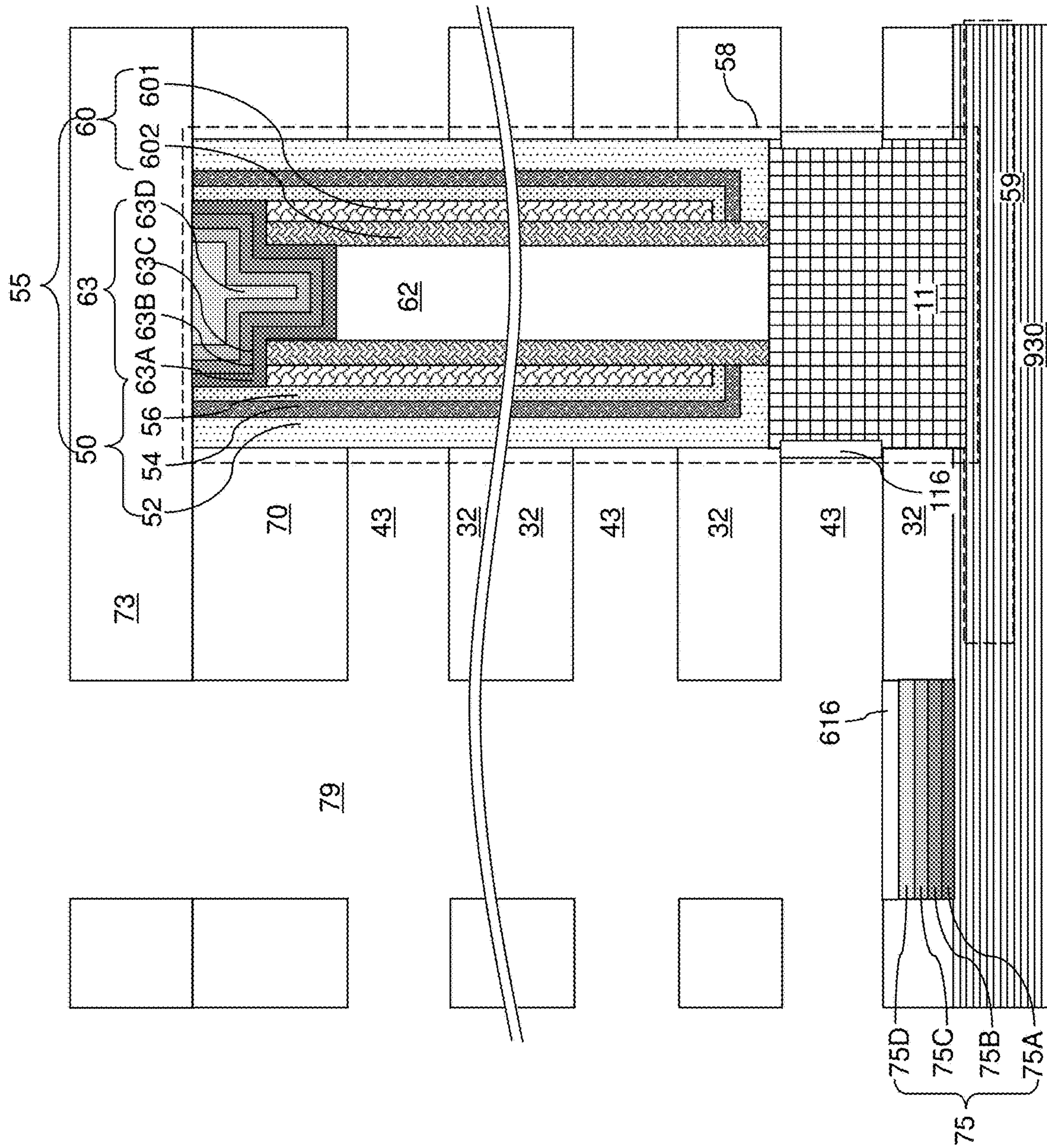


FIG. 12A

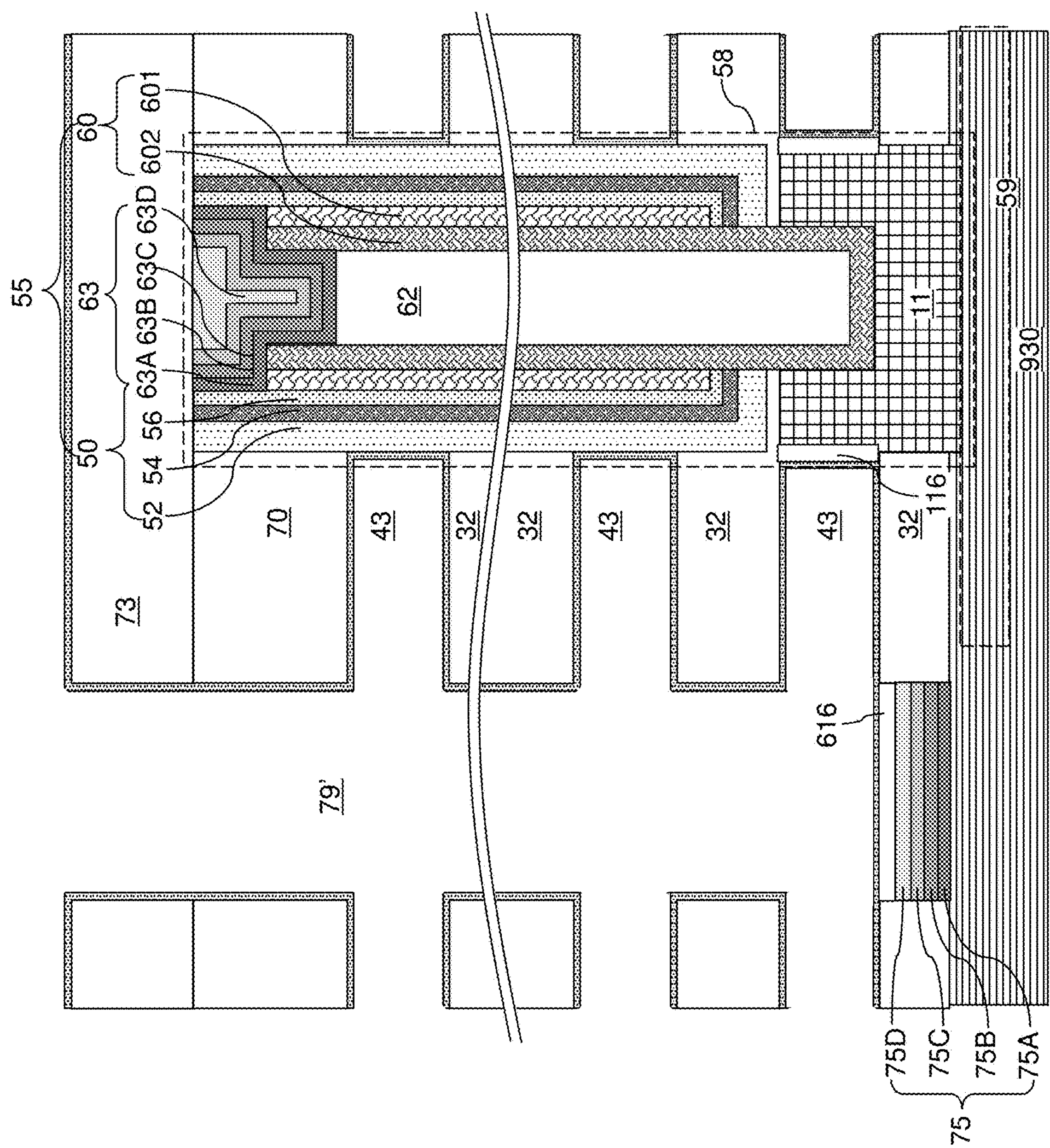


FIG. 12B

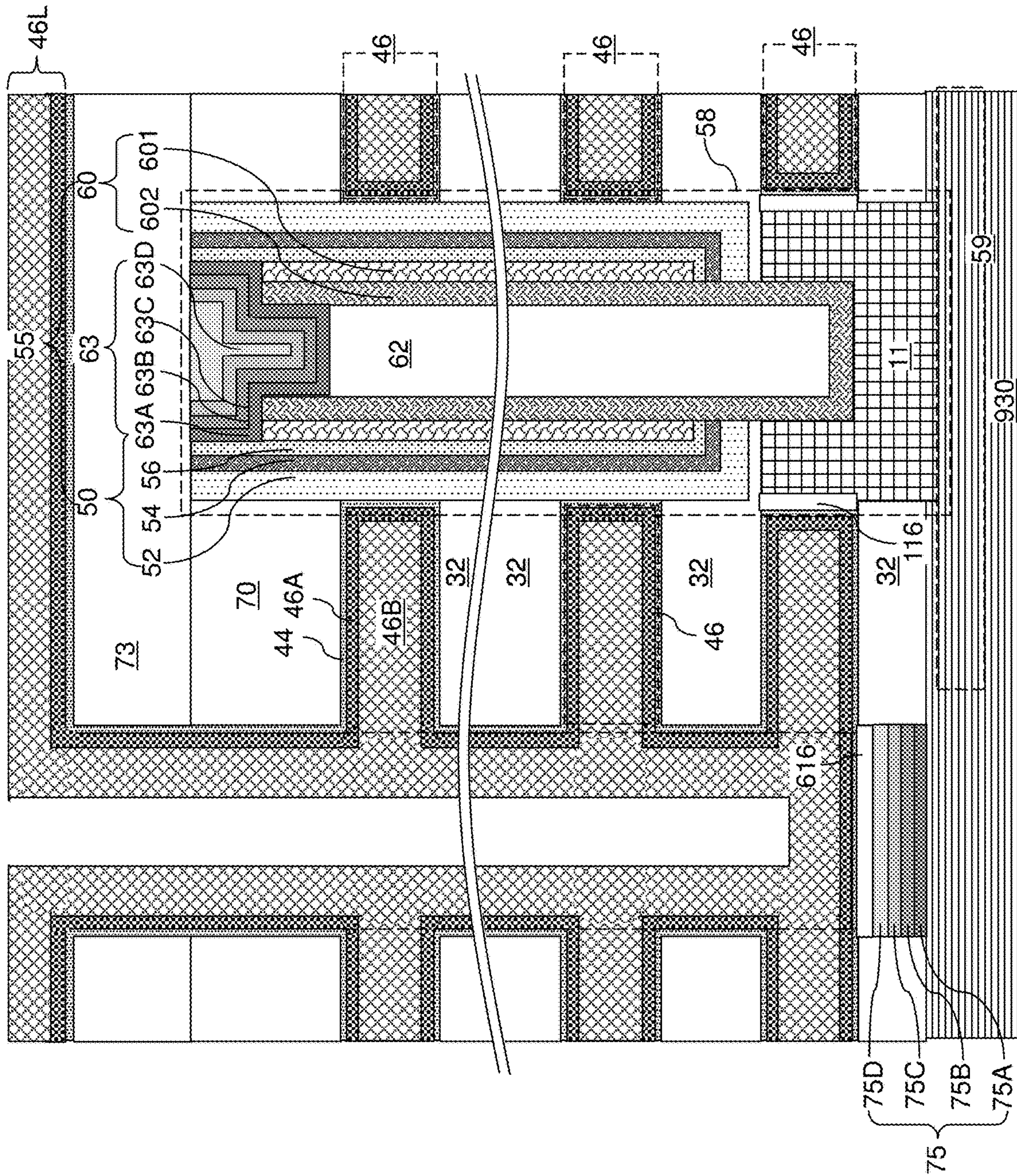


FIG. 13

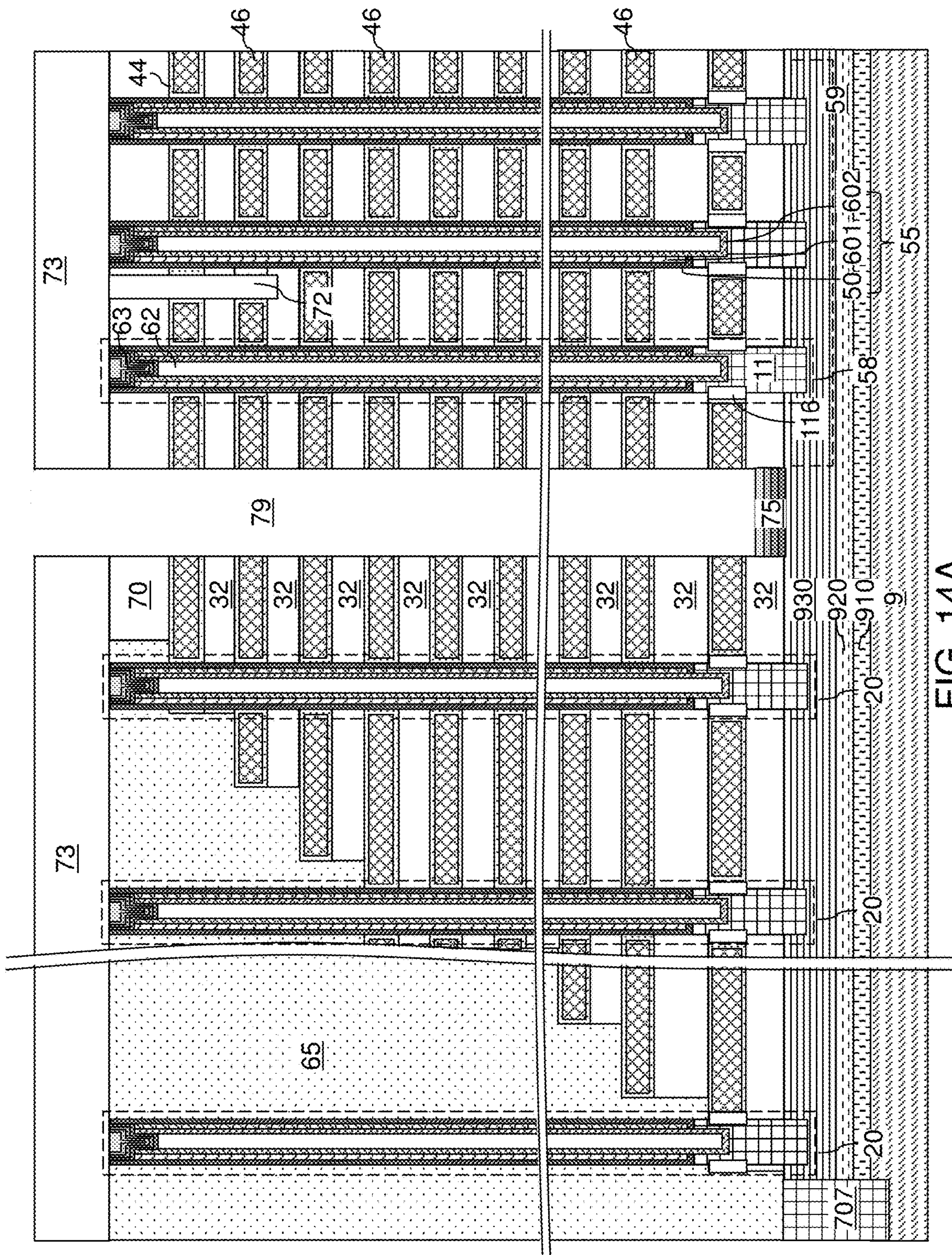


FIG. 14A

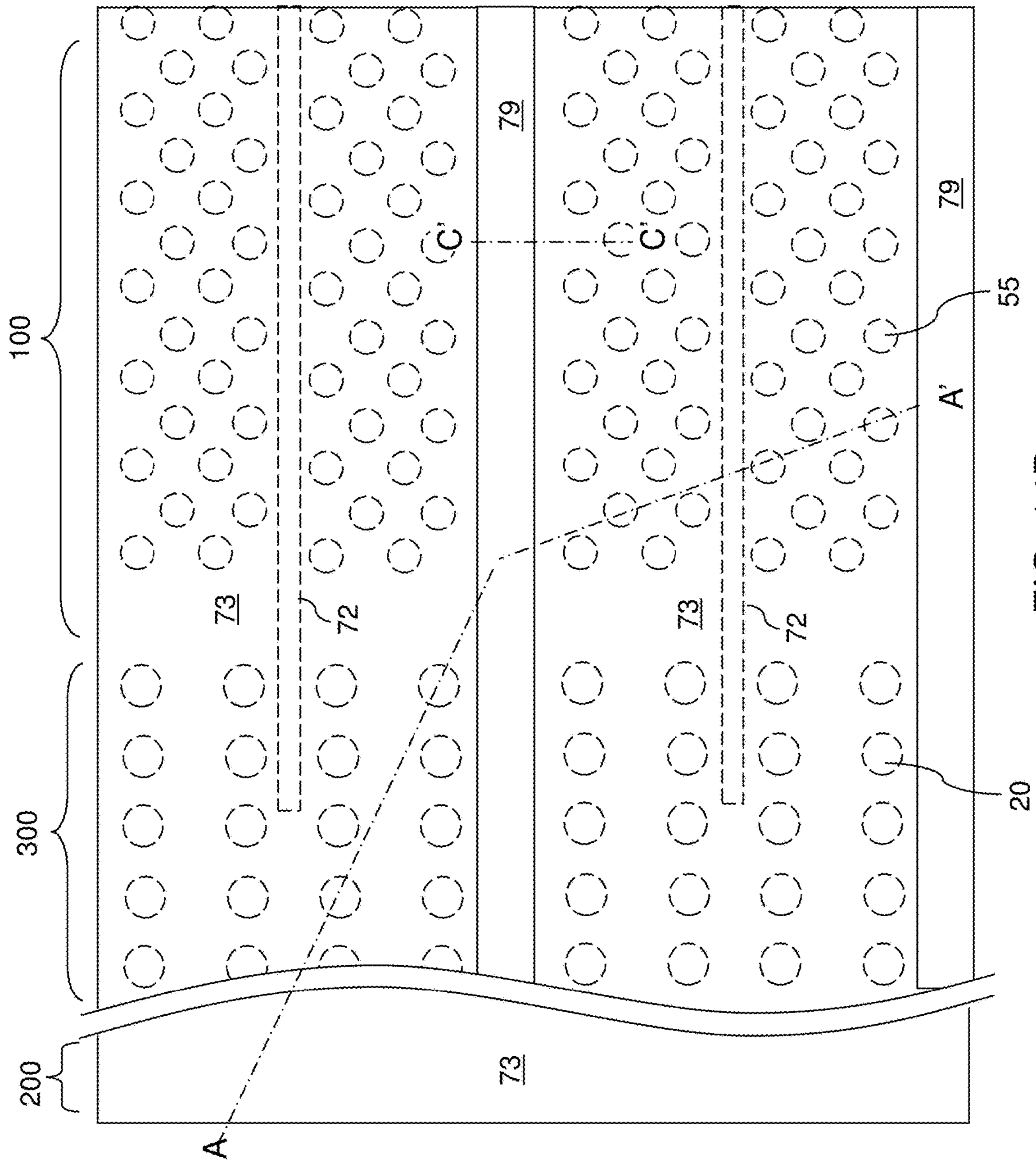


FIG. 14B

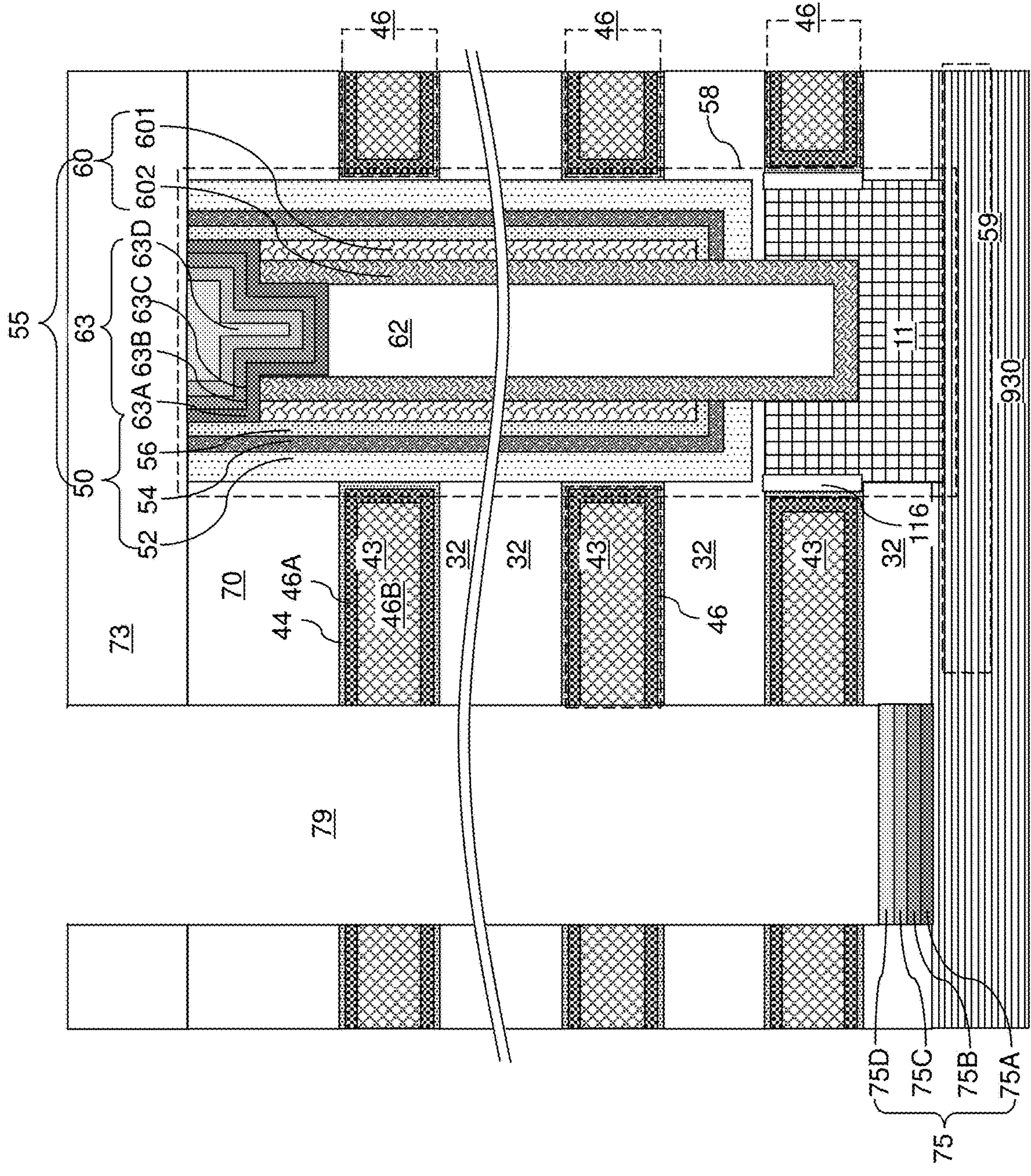


FIG. 14C

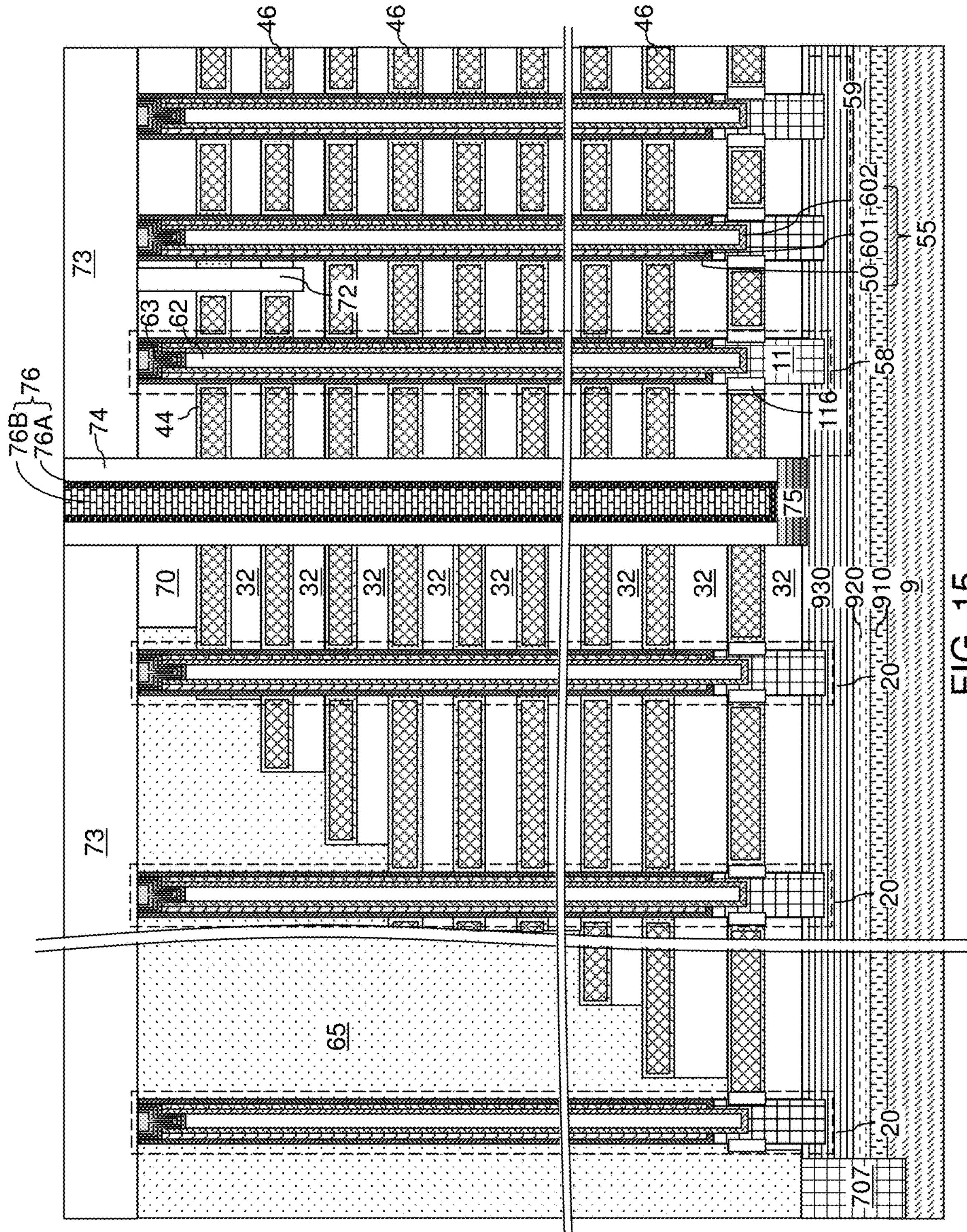


FIG. 15

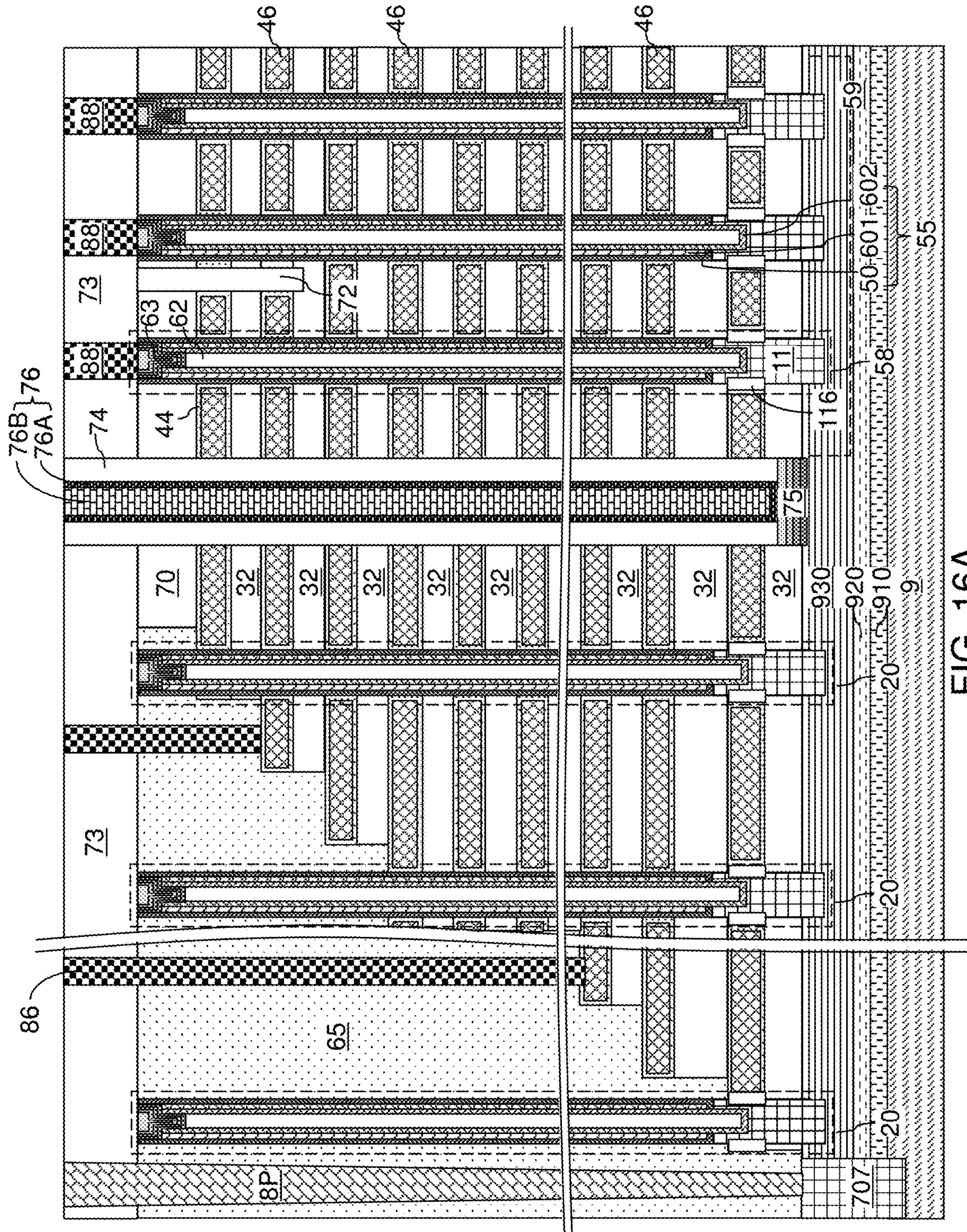


FIG. 16A

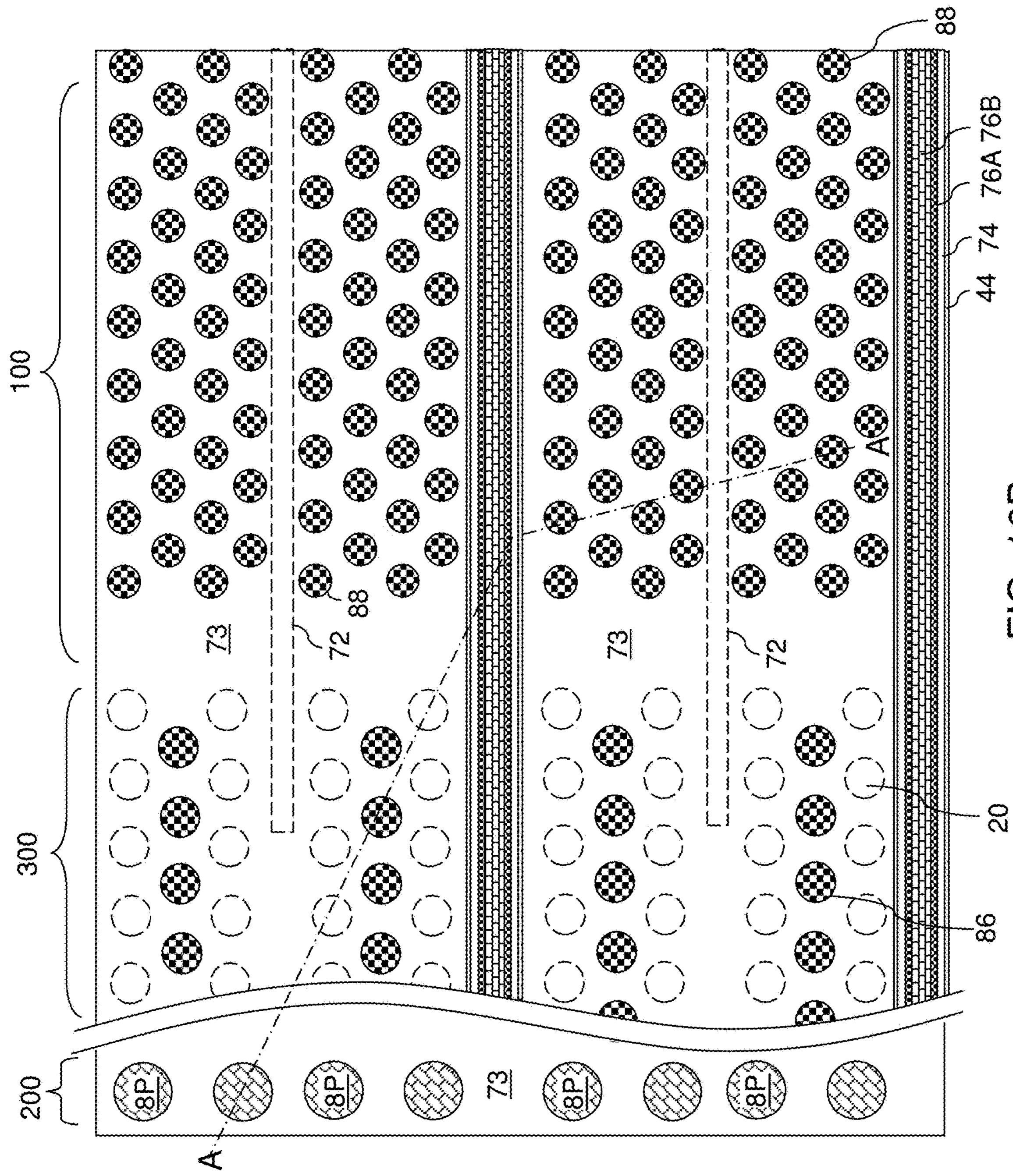


FIG. 16B

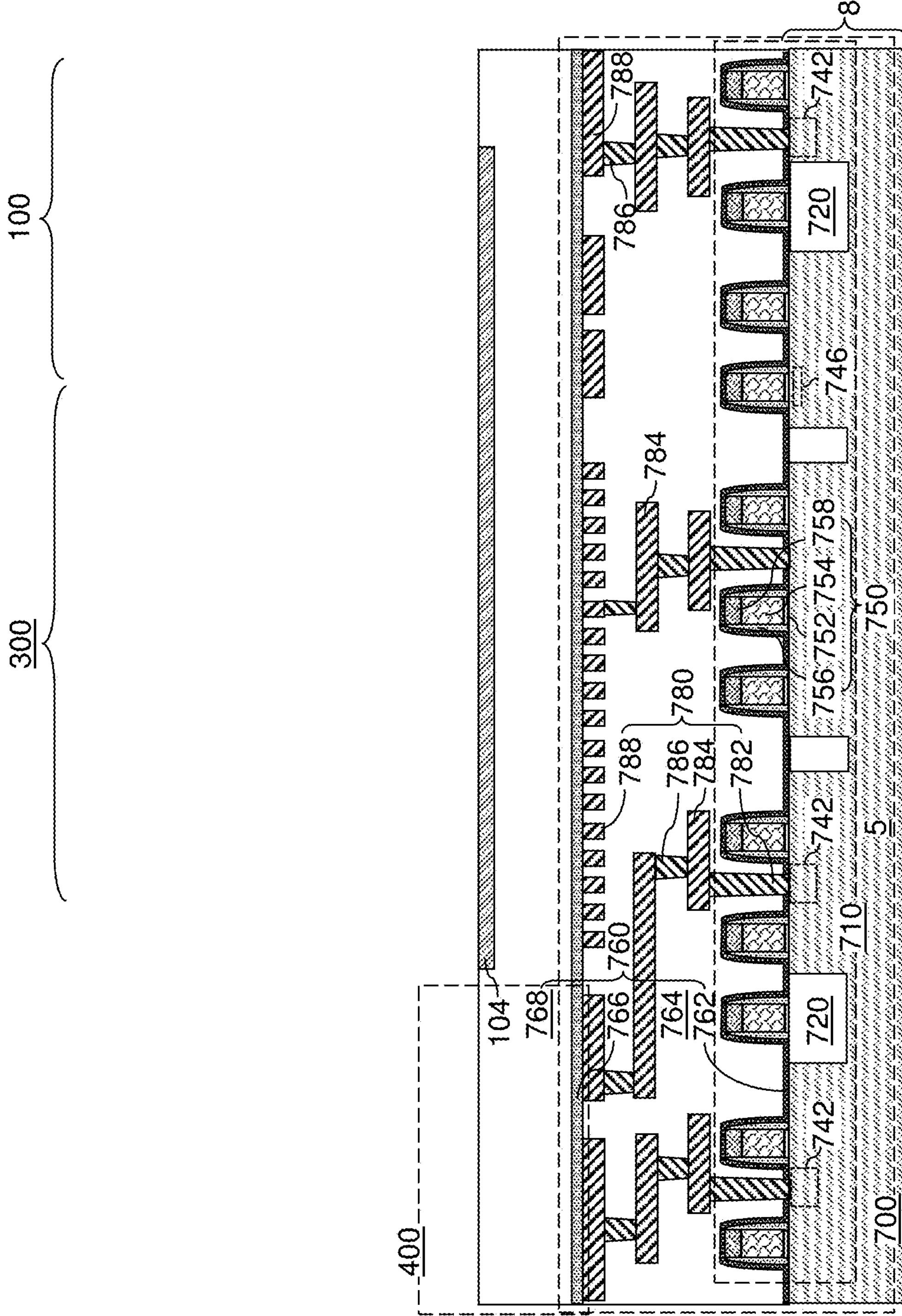


FIG. 17A

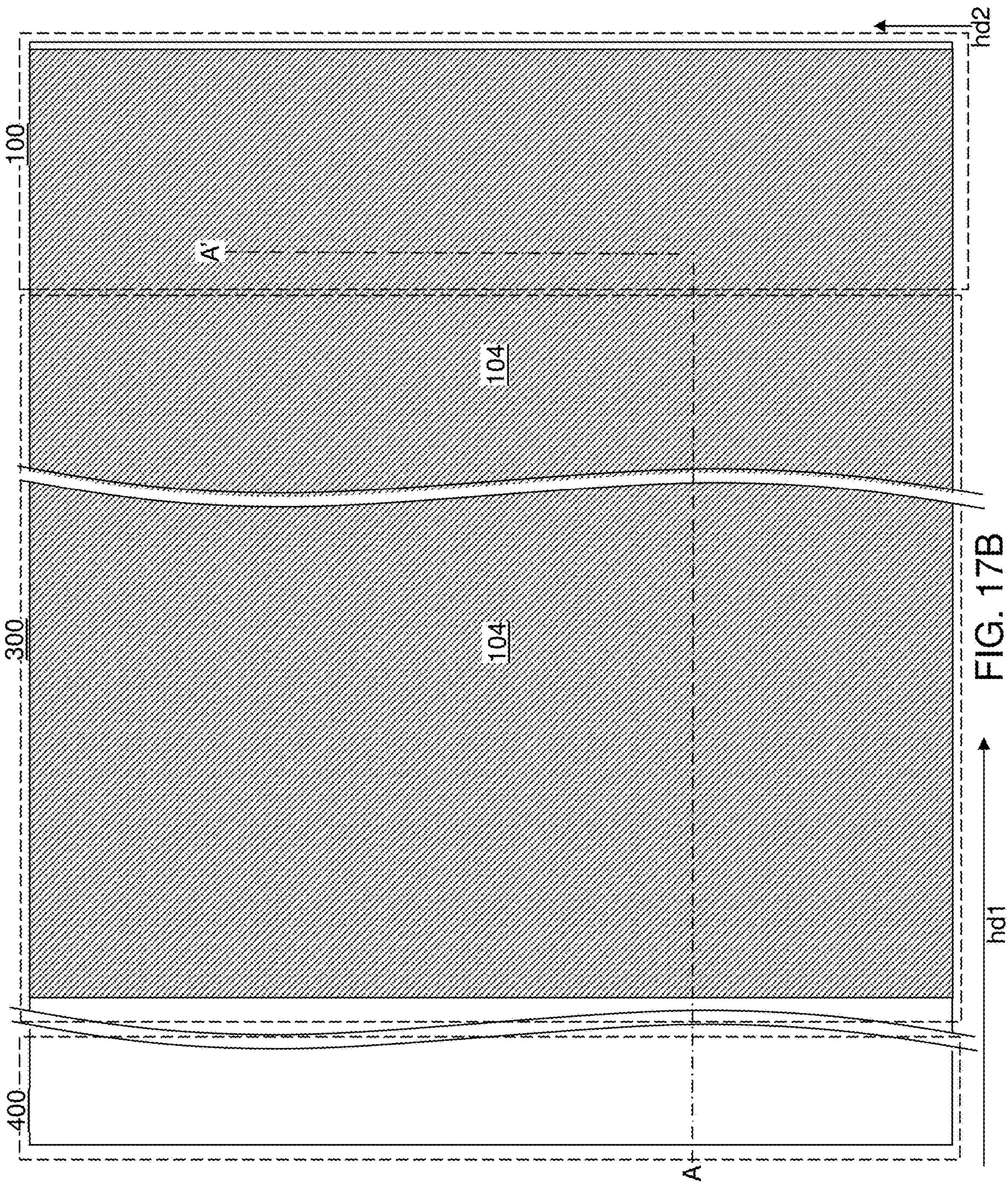


FIG. 17B

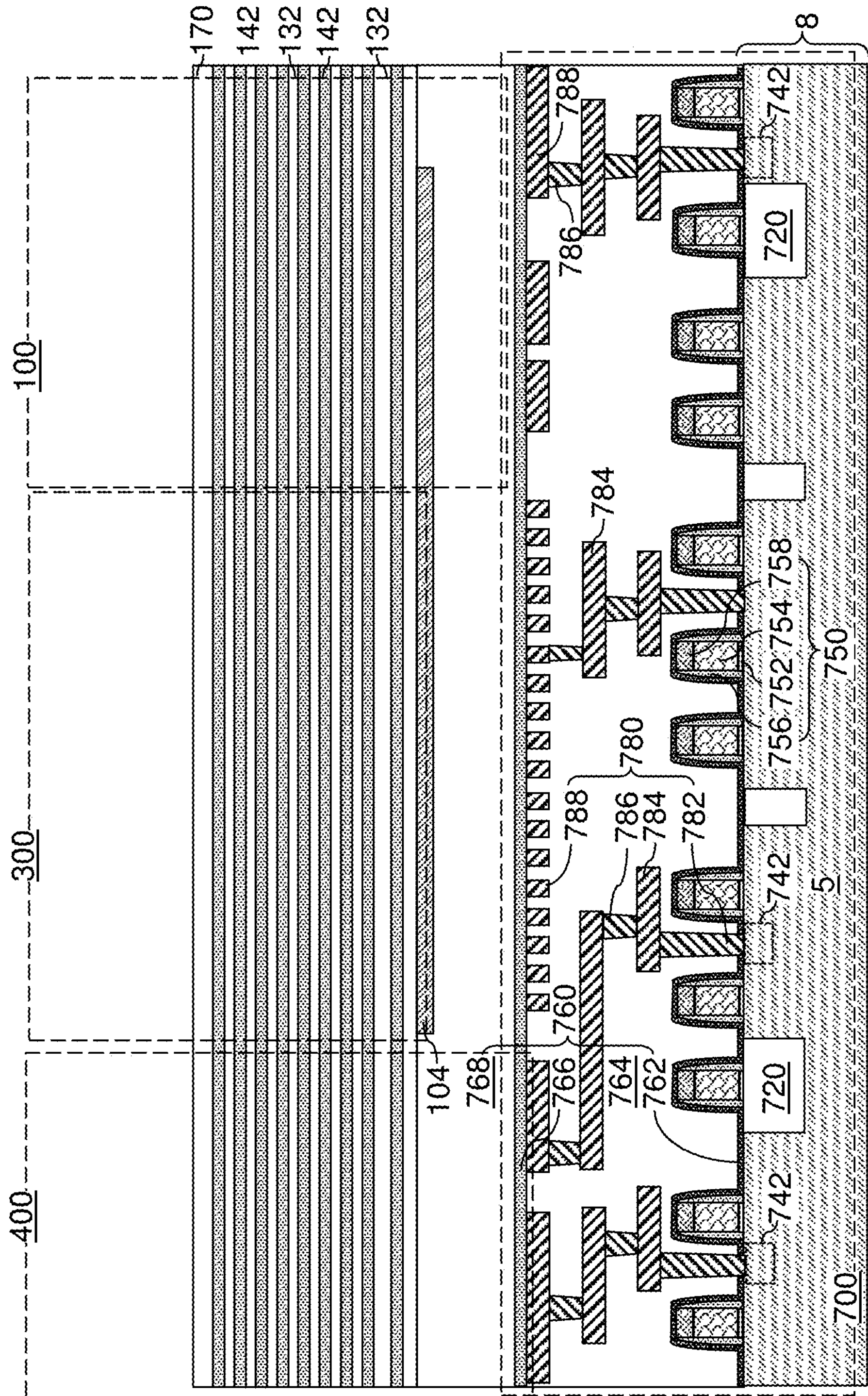


FIG. 18

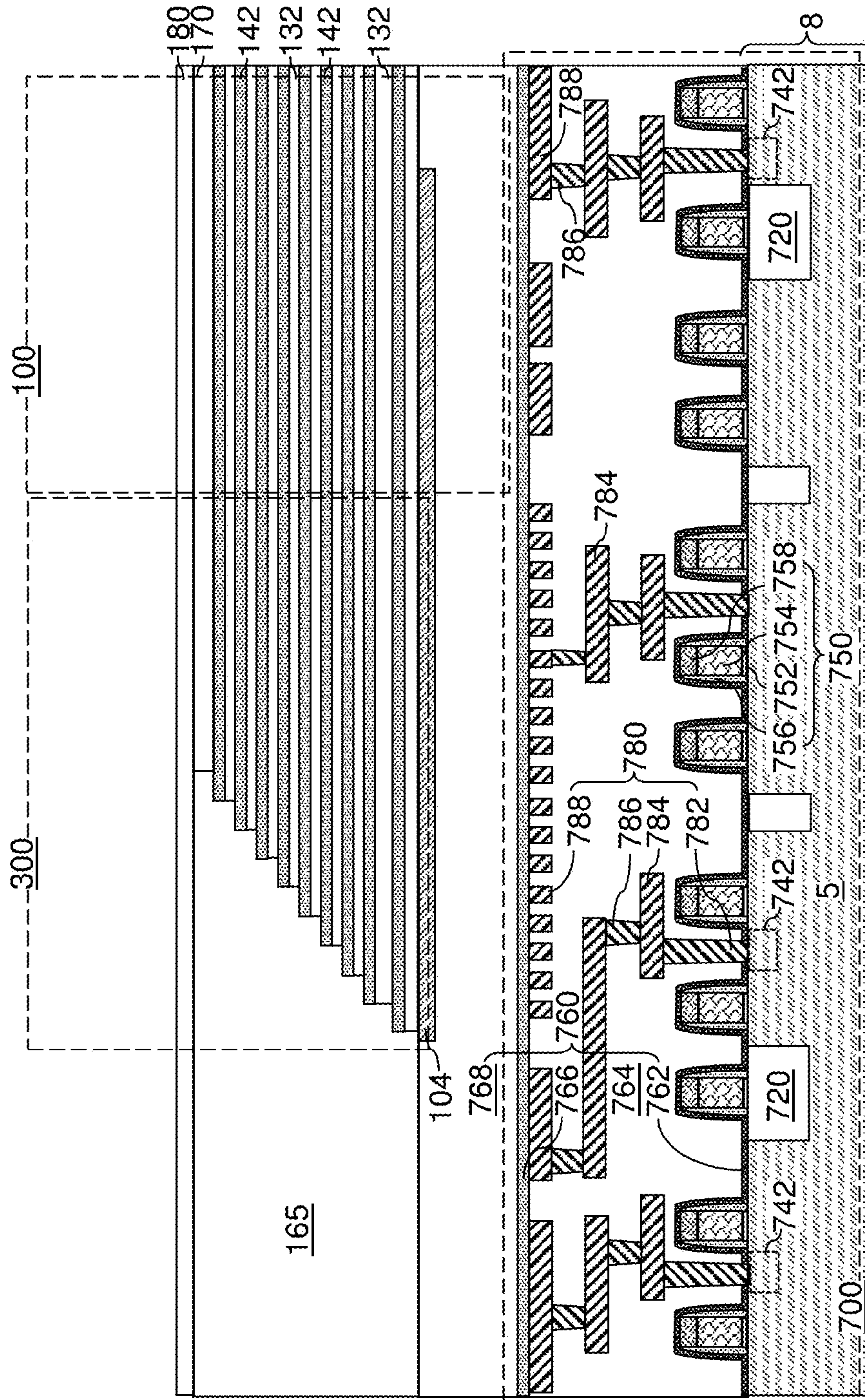


FIG. 19

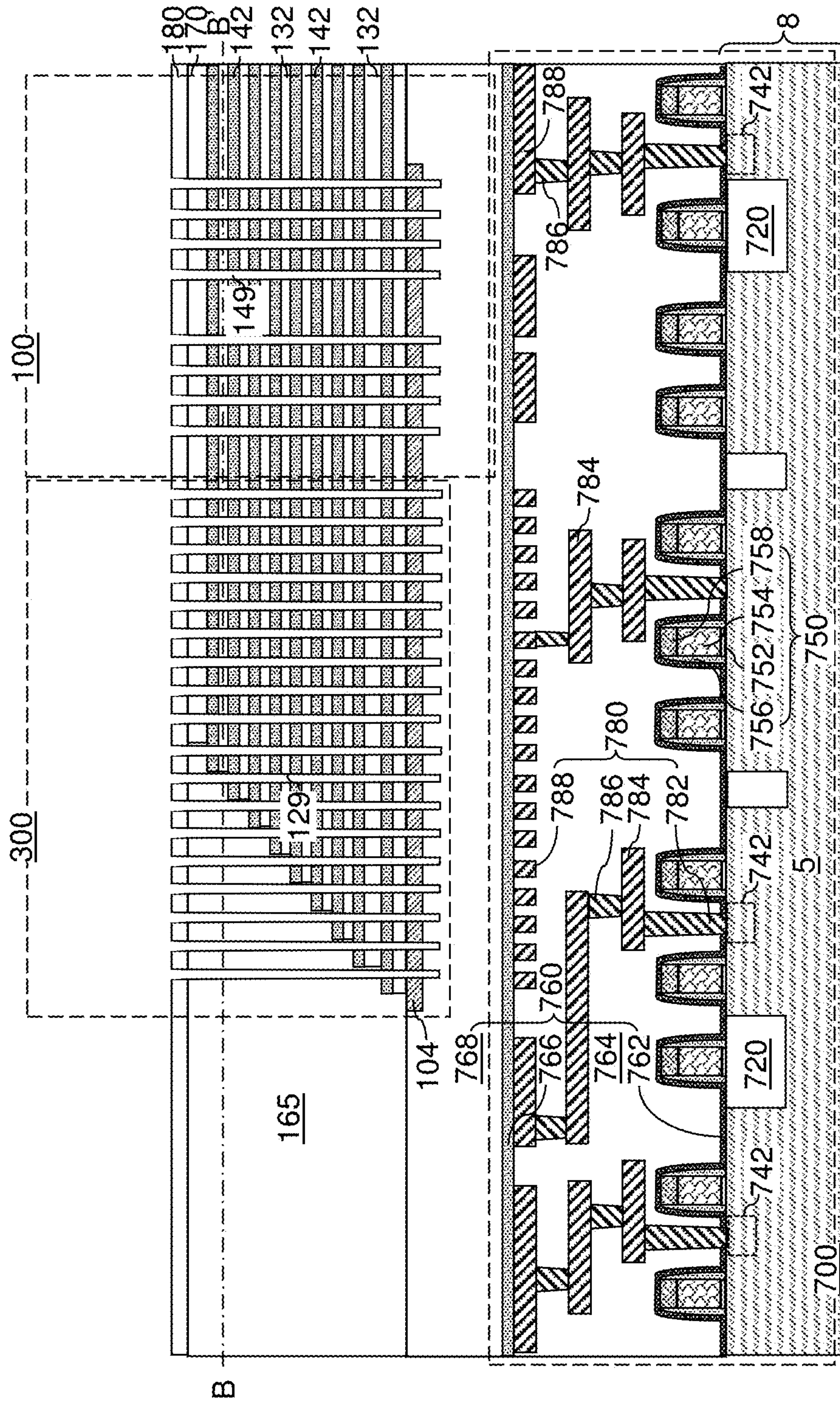


FIG. 20A

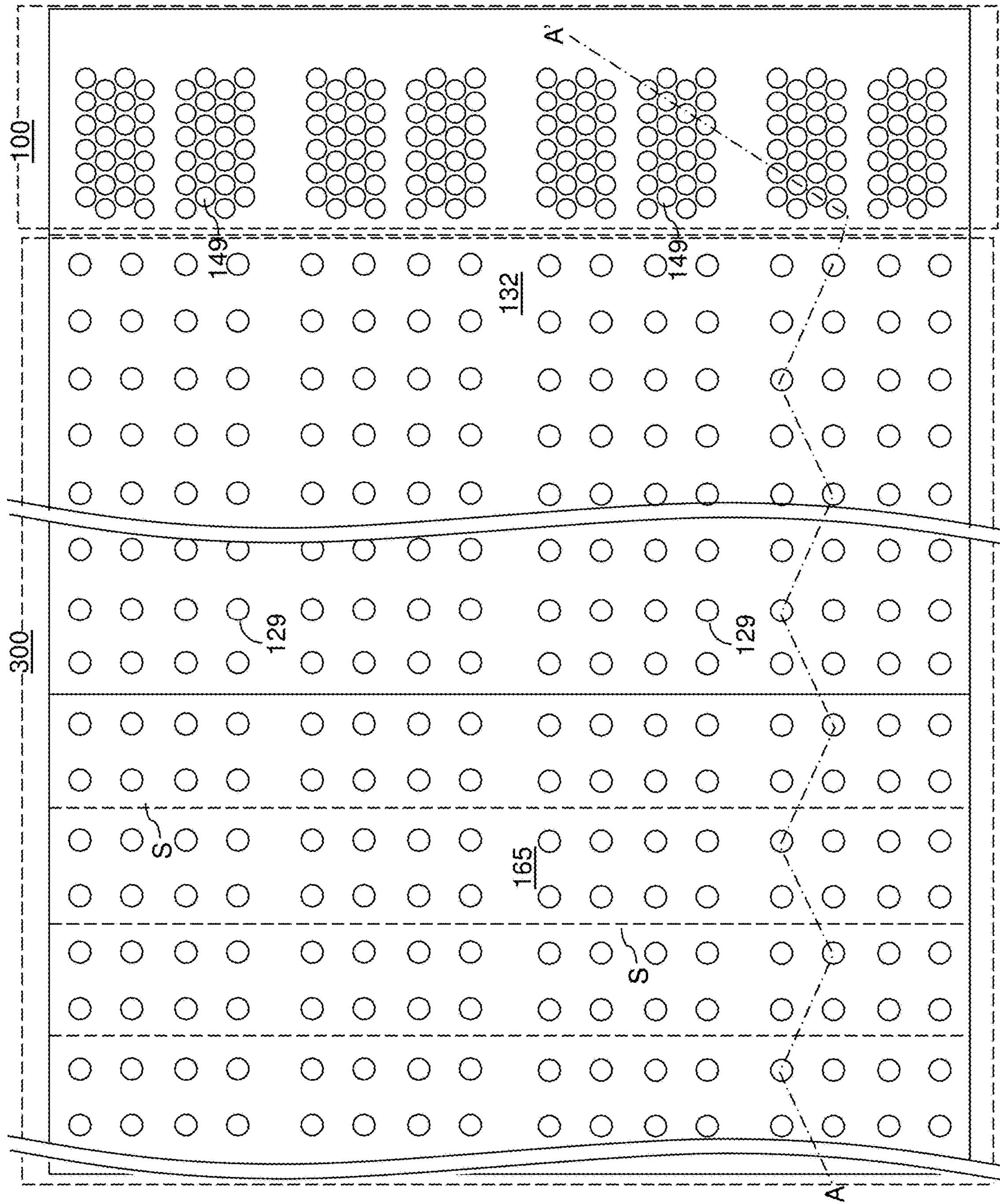


FIG. 20B

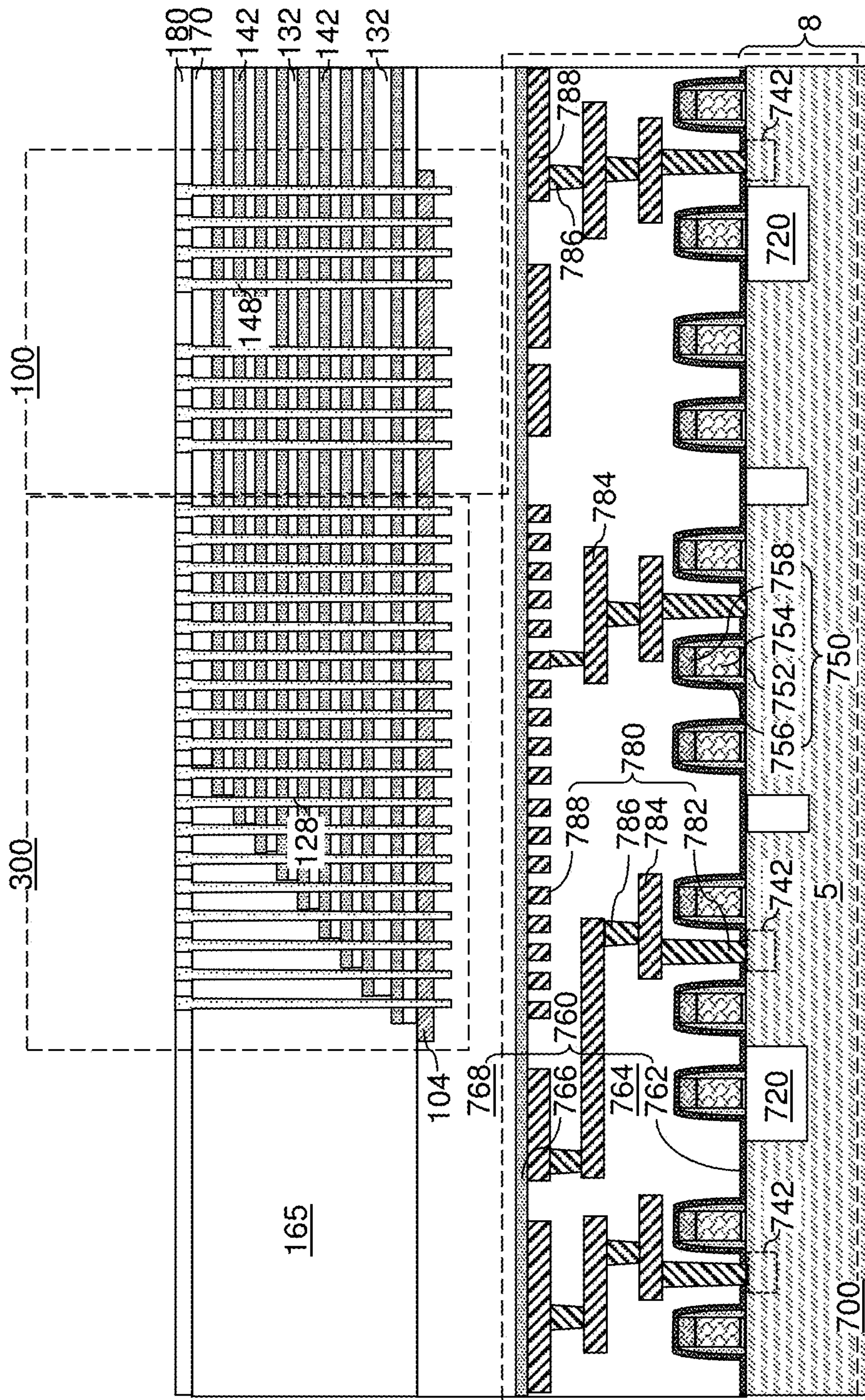


FIG. 21

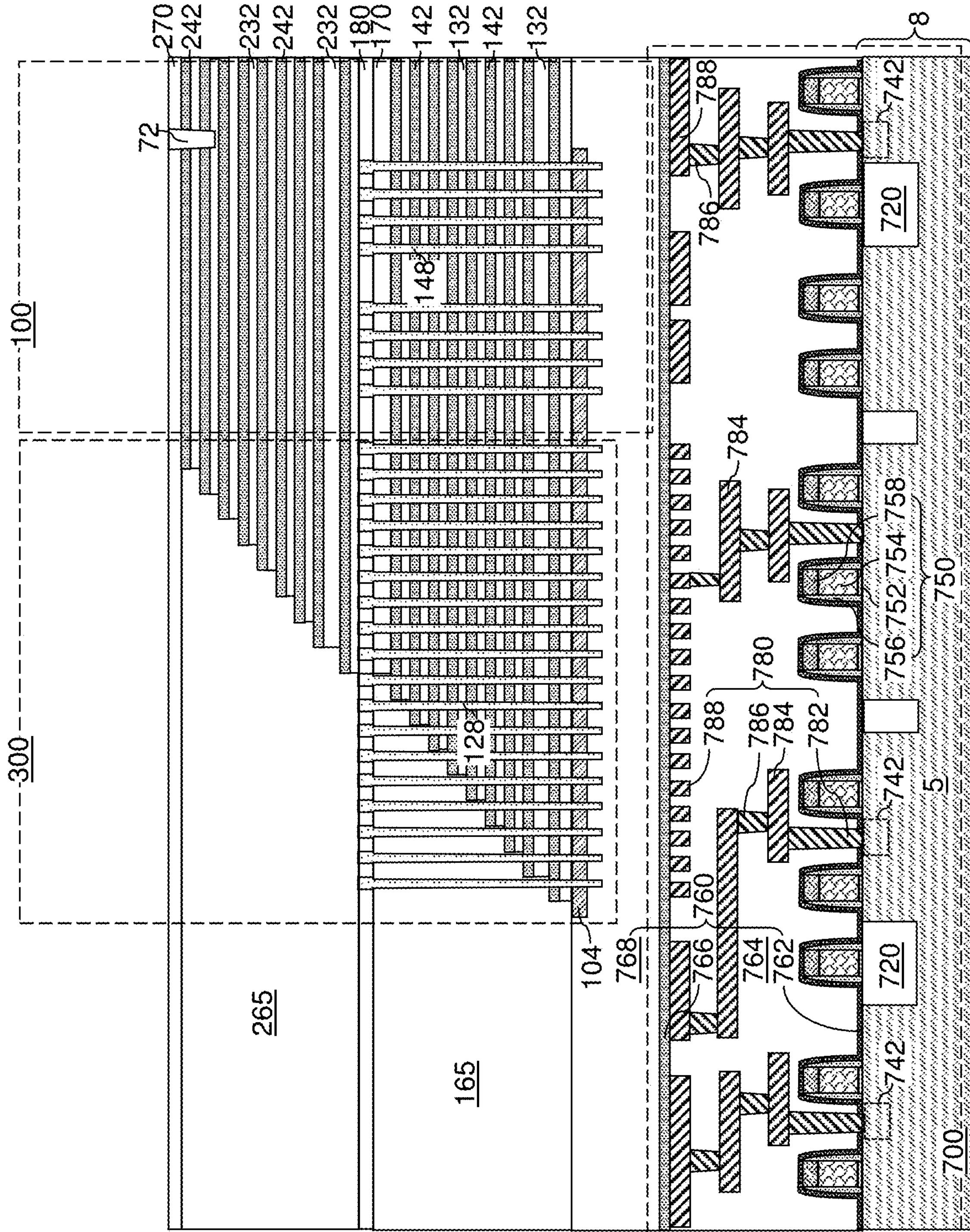


FIG. 22

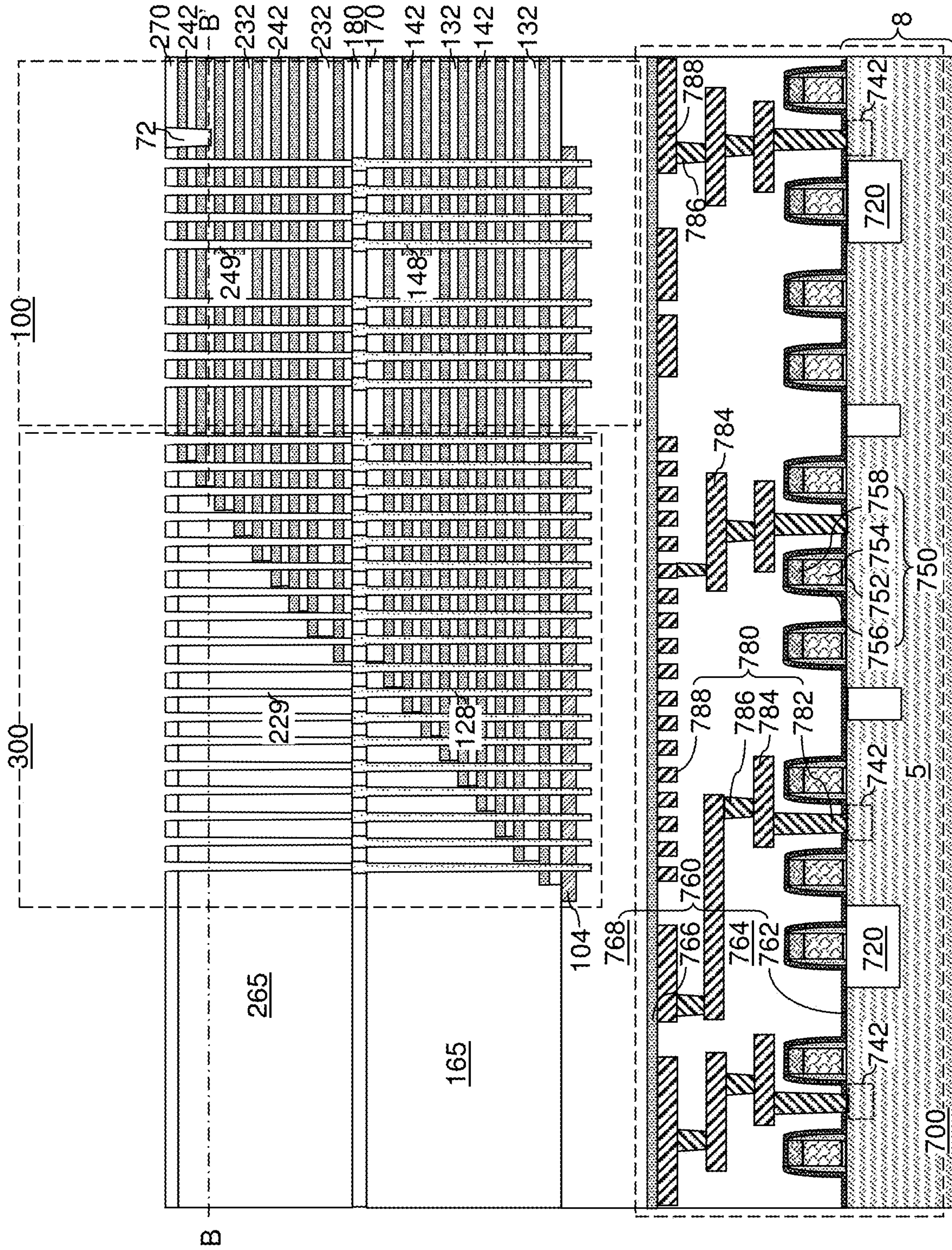


FIG. 23A

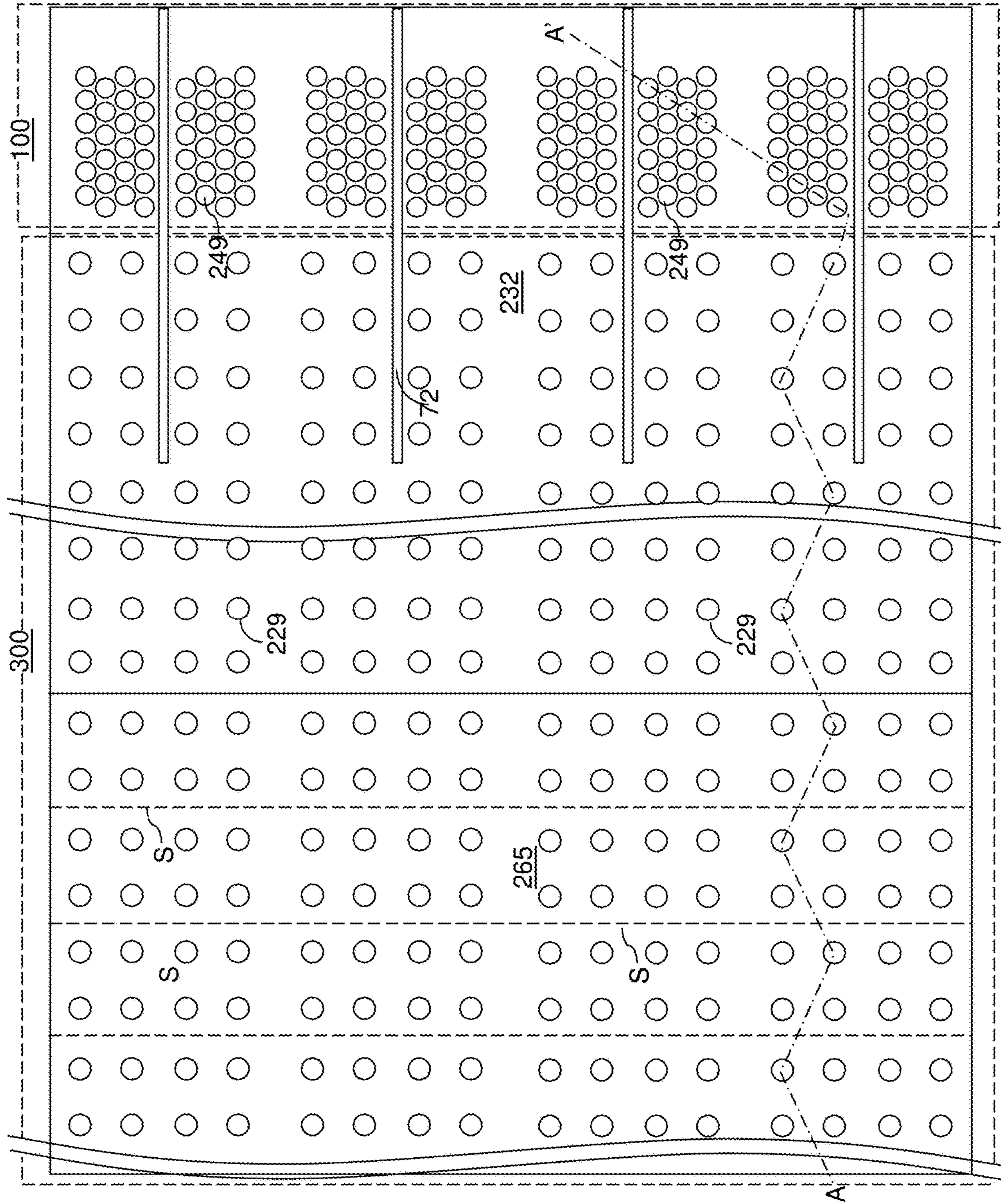


FIG. 23B

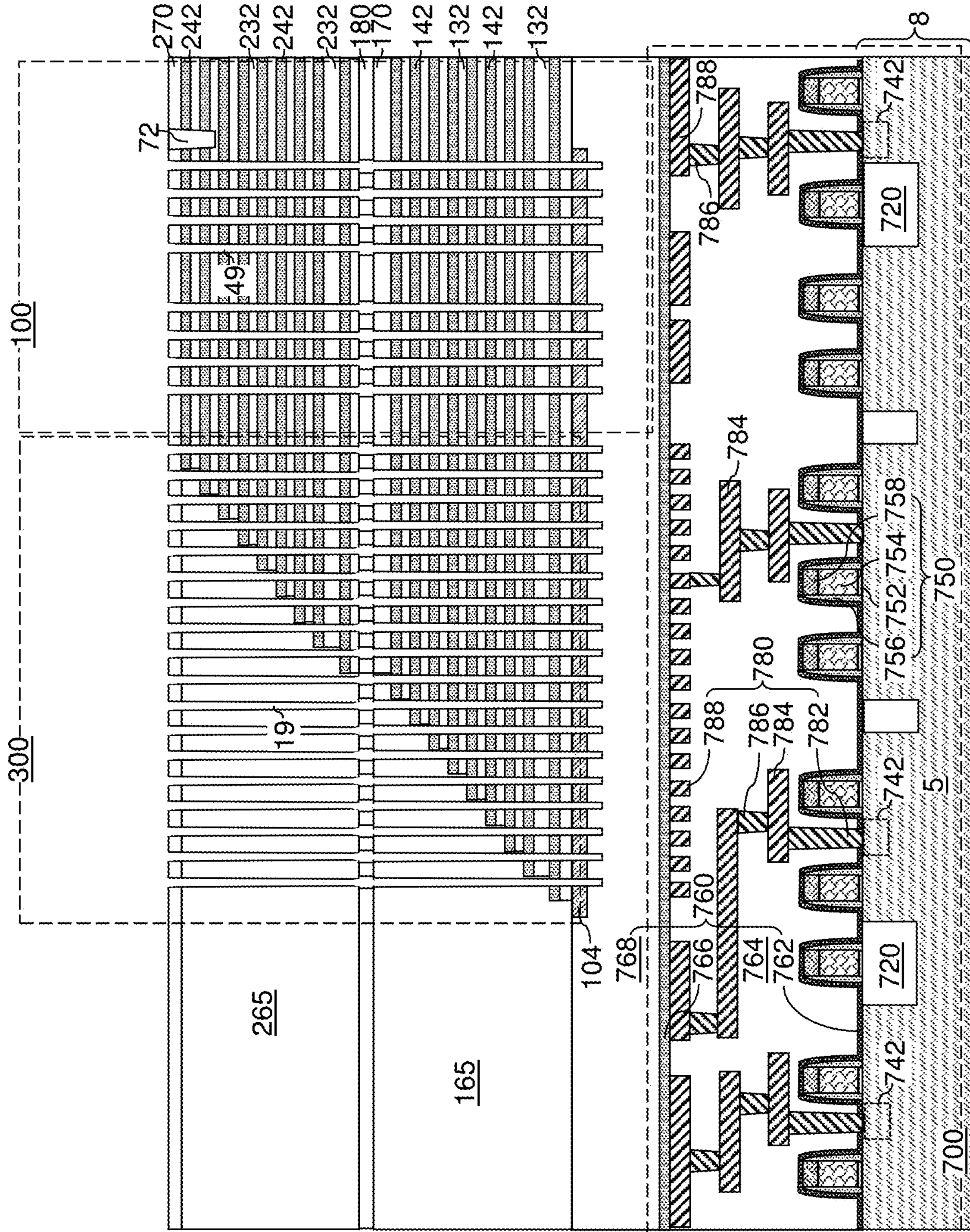


FIG. 24

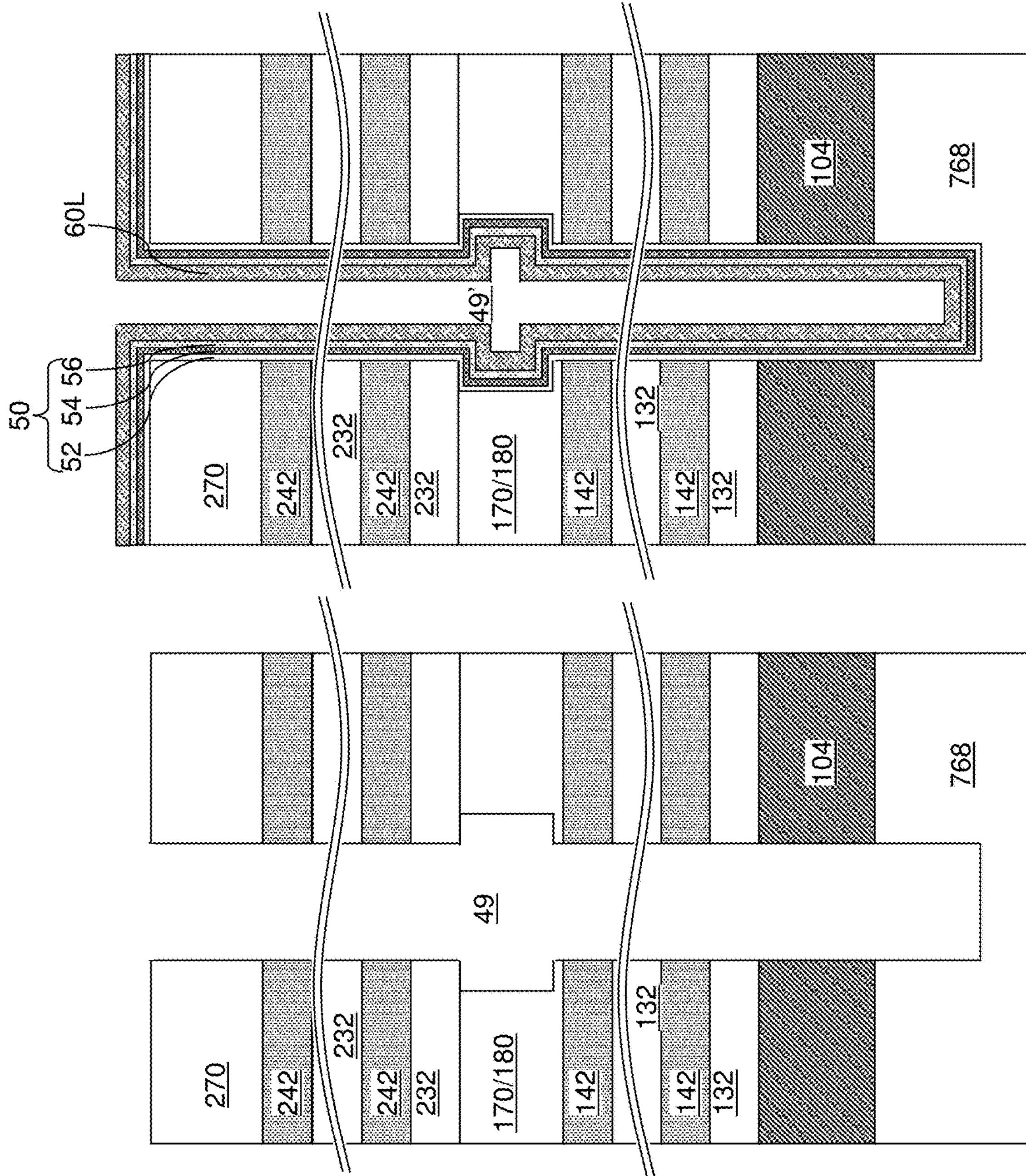


FIG. 25A

FIG. 25B

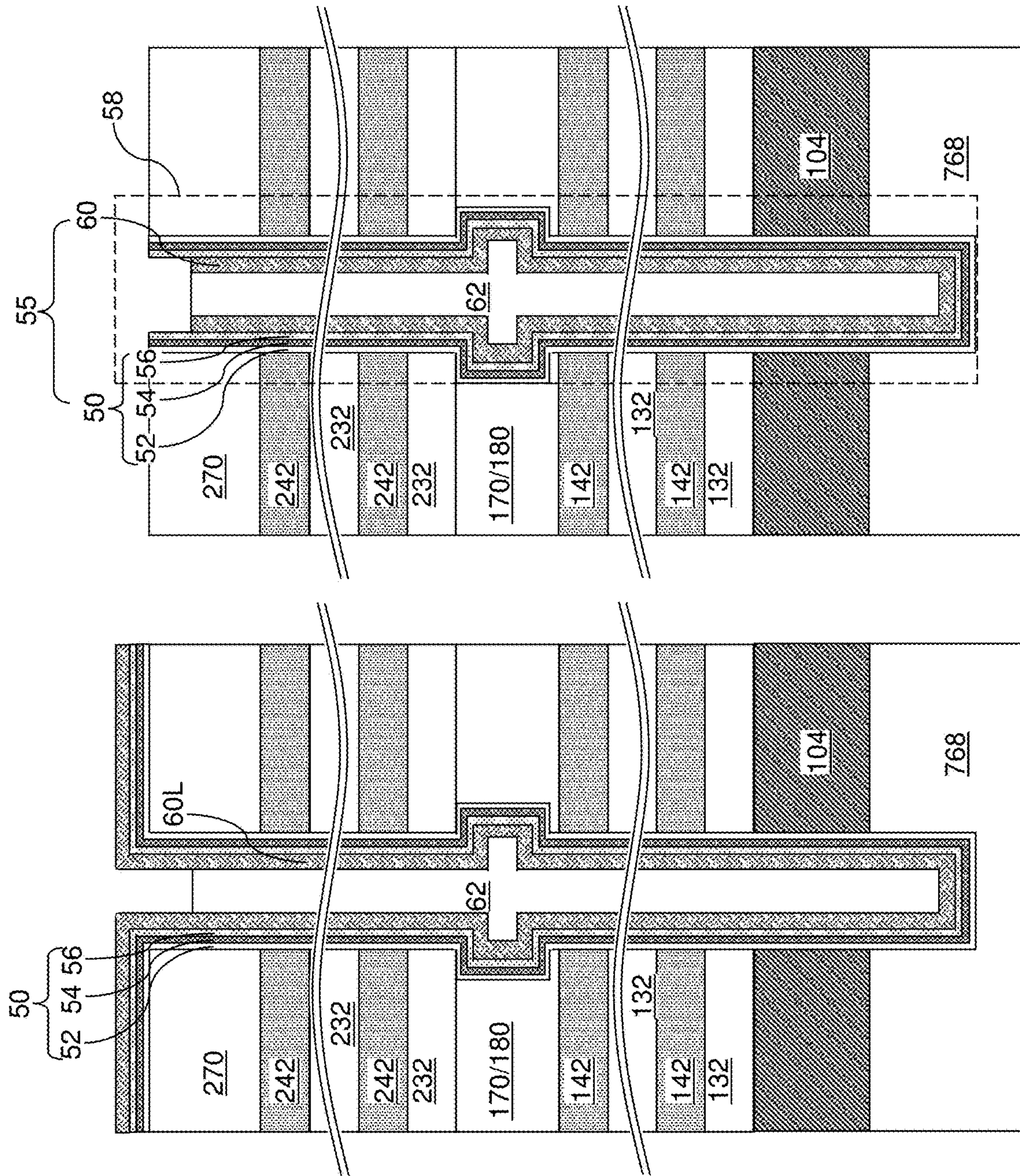


FIG. 25C

FIG. 25D

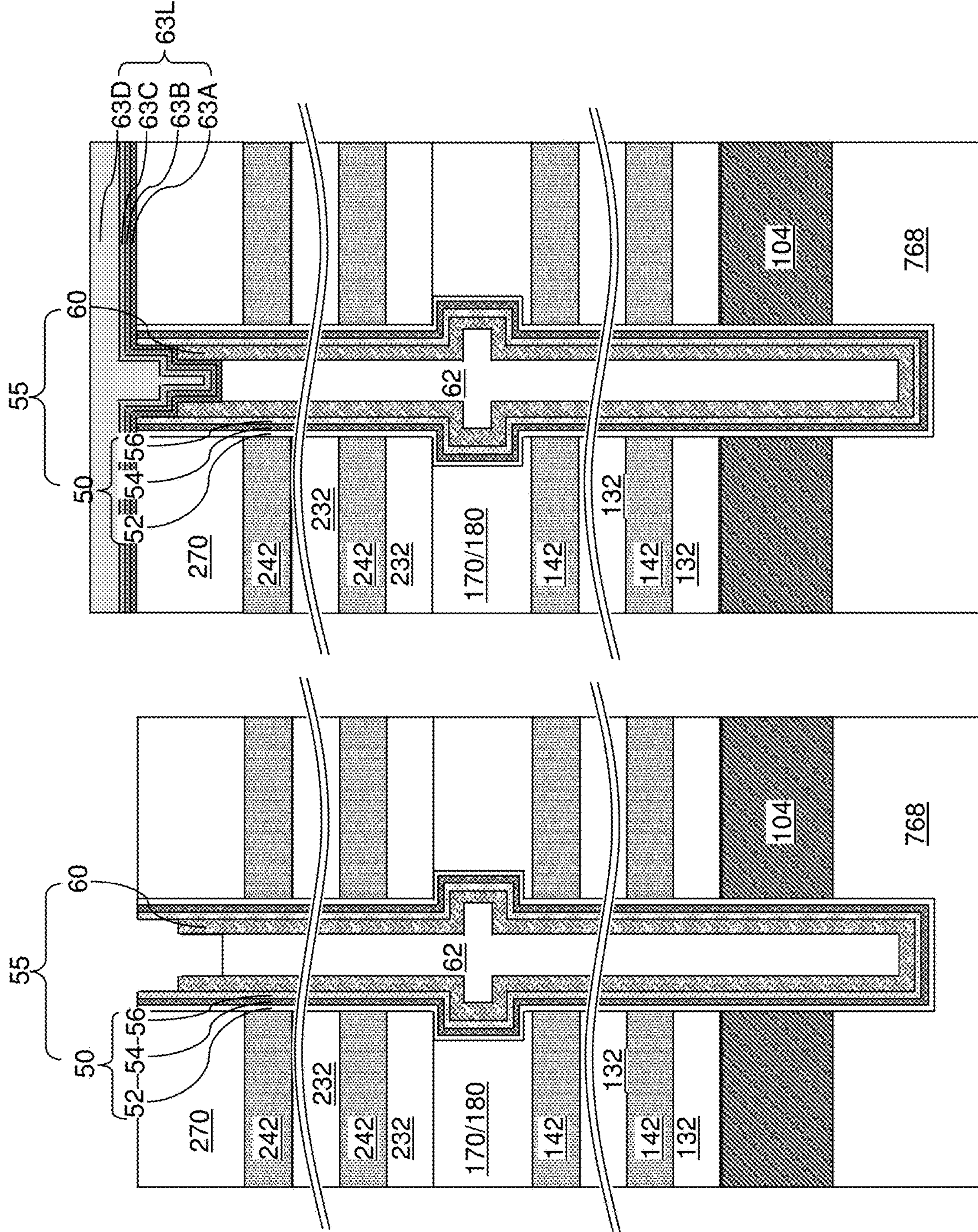


FIG. 25E

FIG. 25F

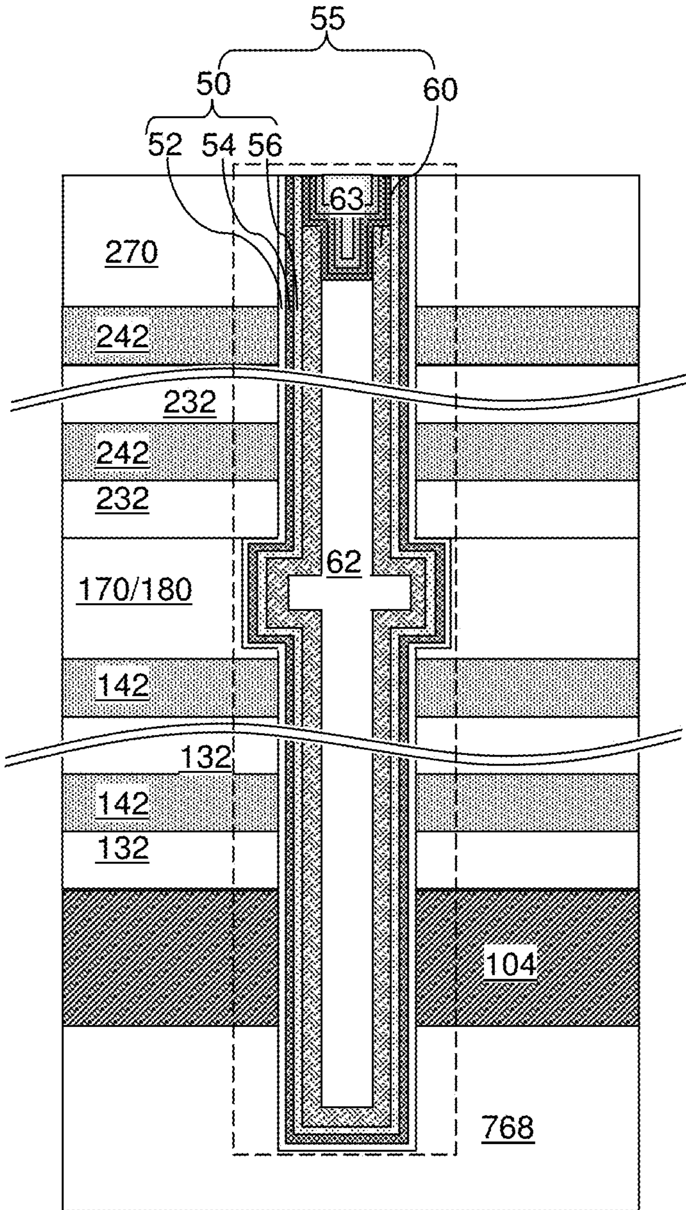


FIG. 25G

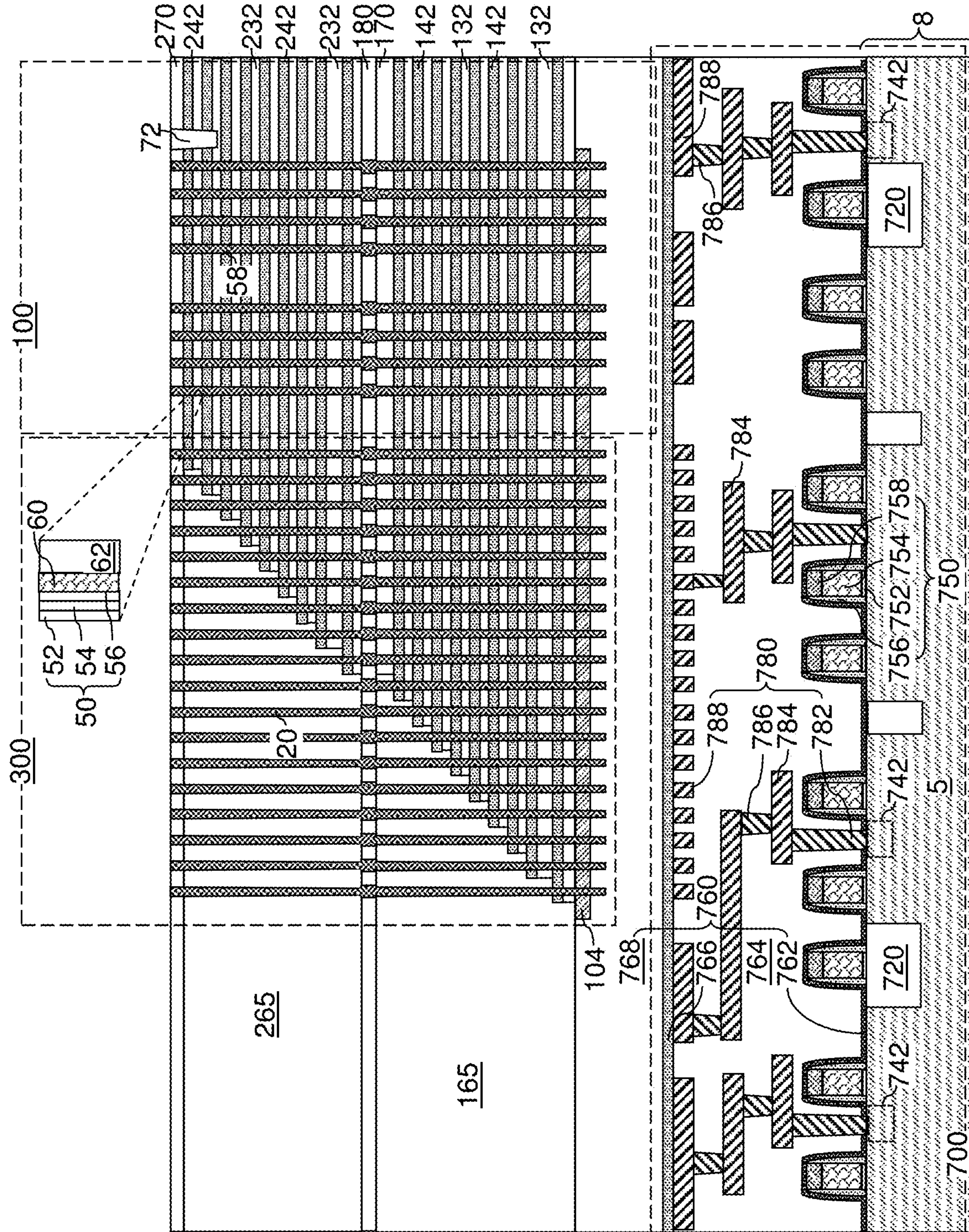


FIG. 26

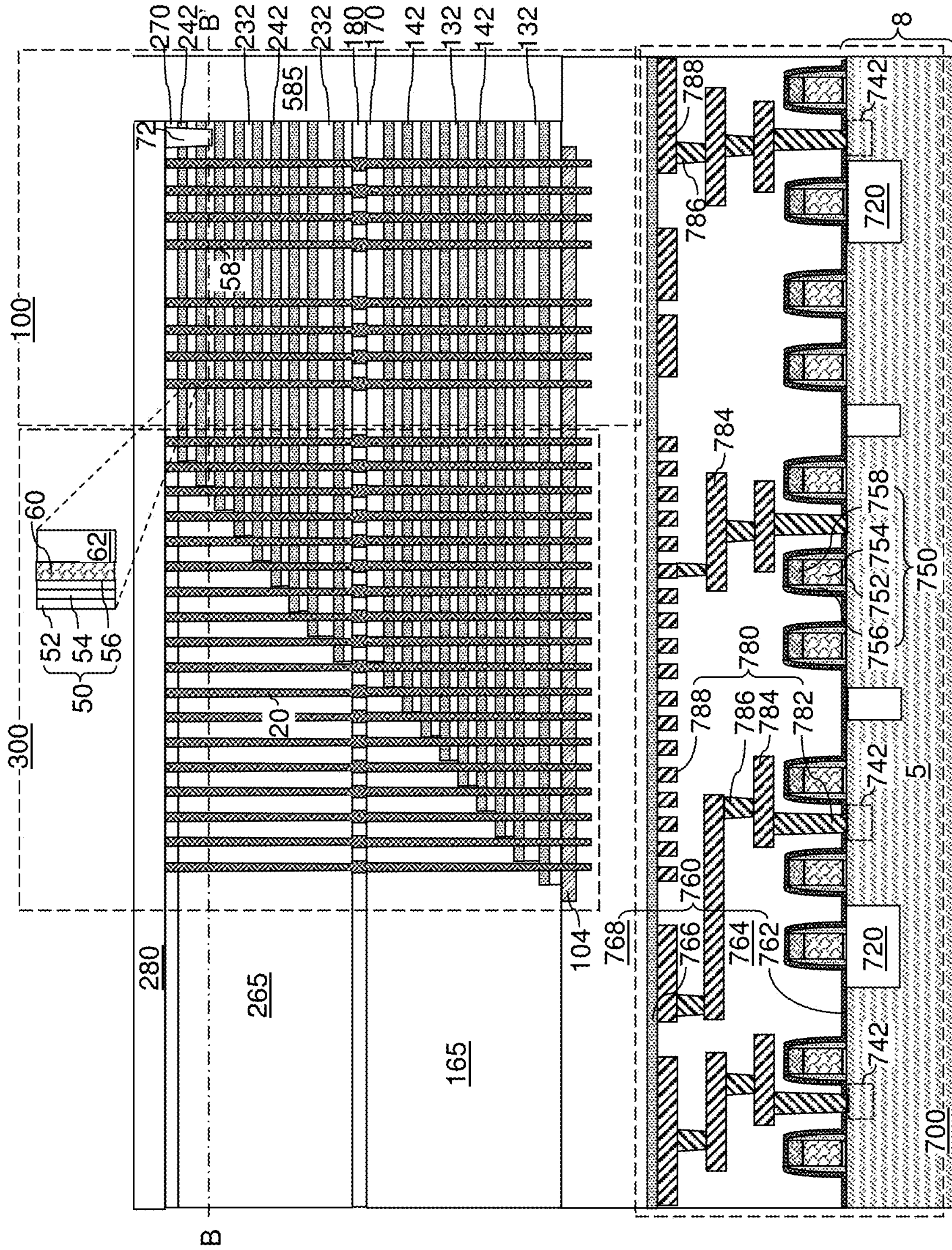


FIG. 27A

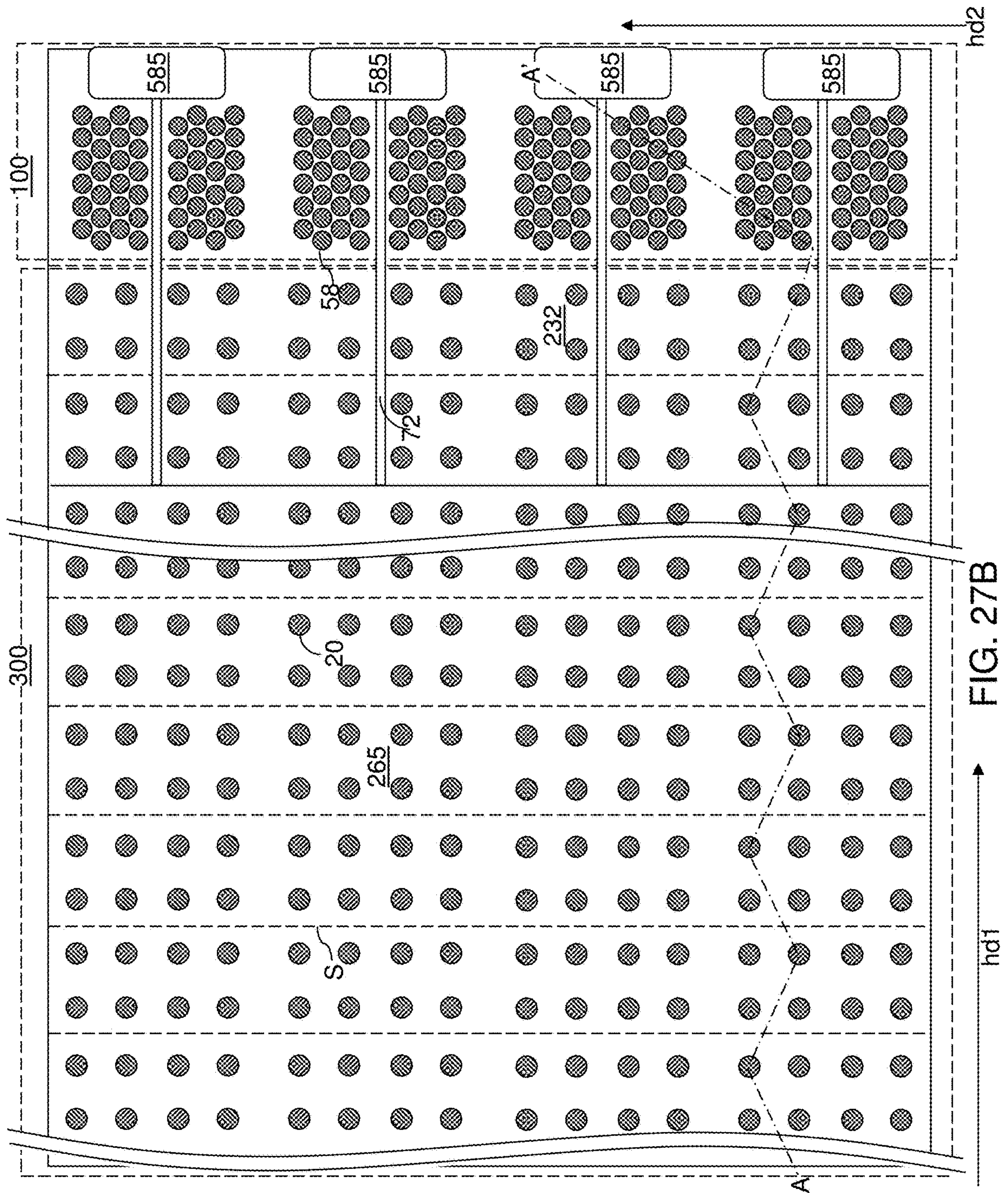


FIG. 27B

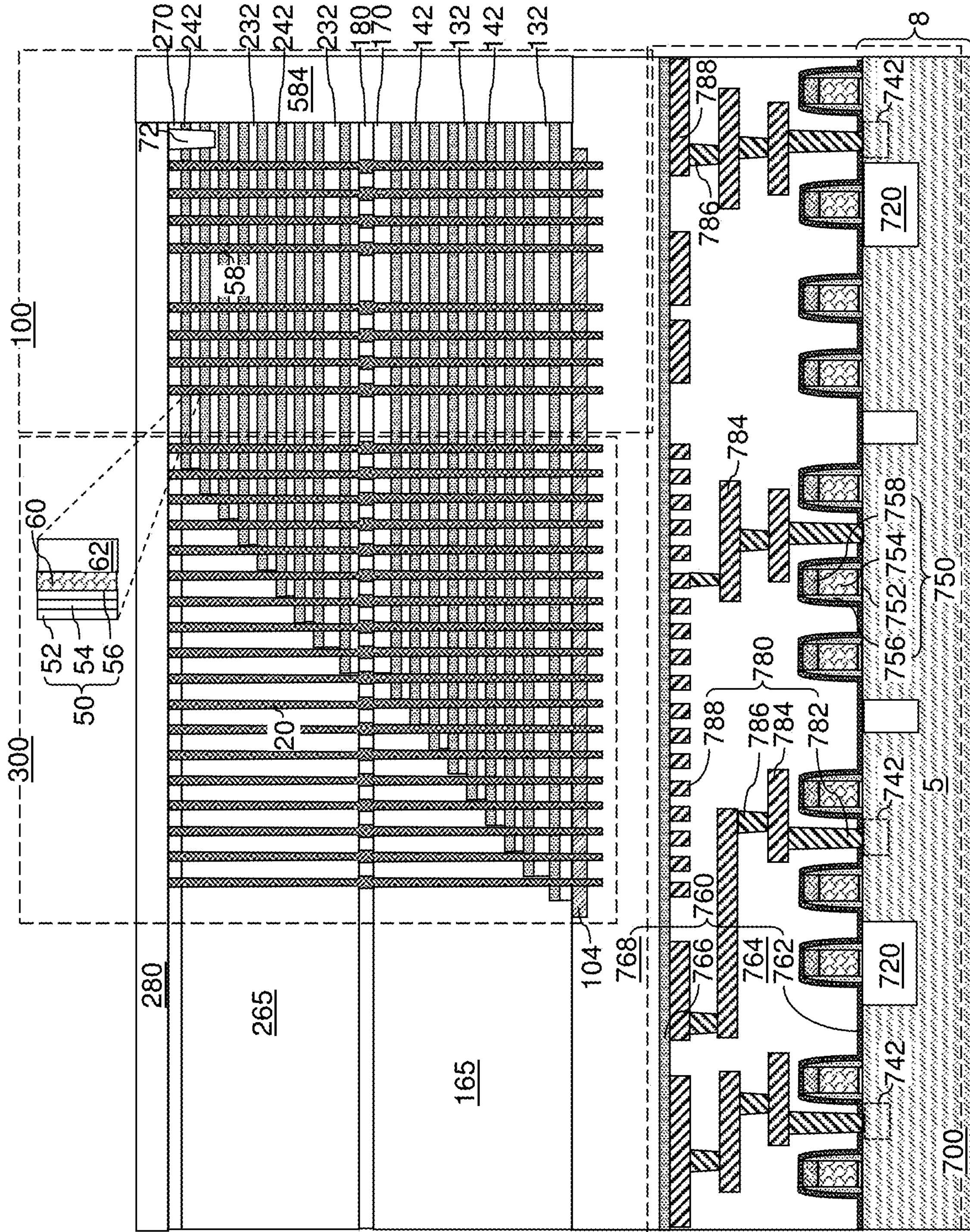


FIG. 28

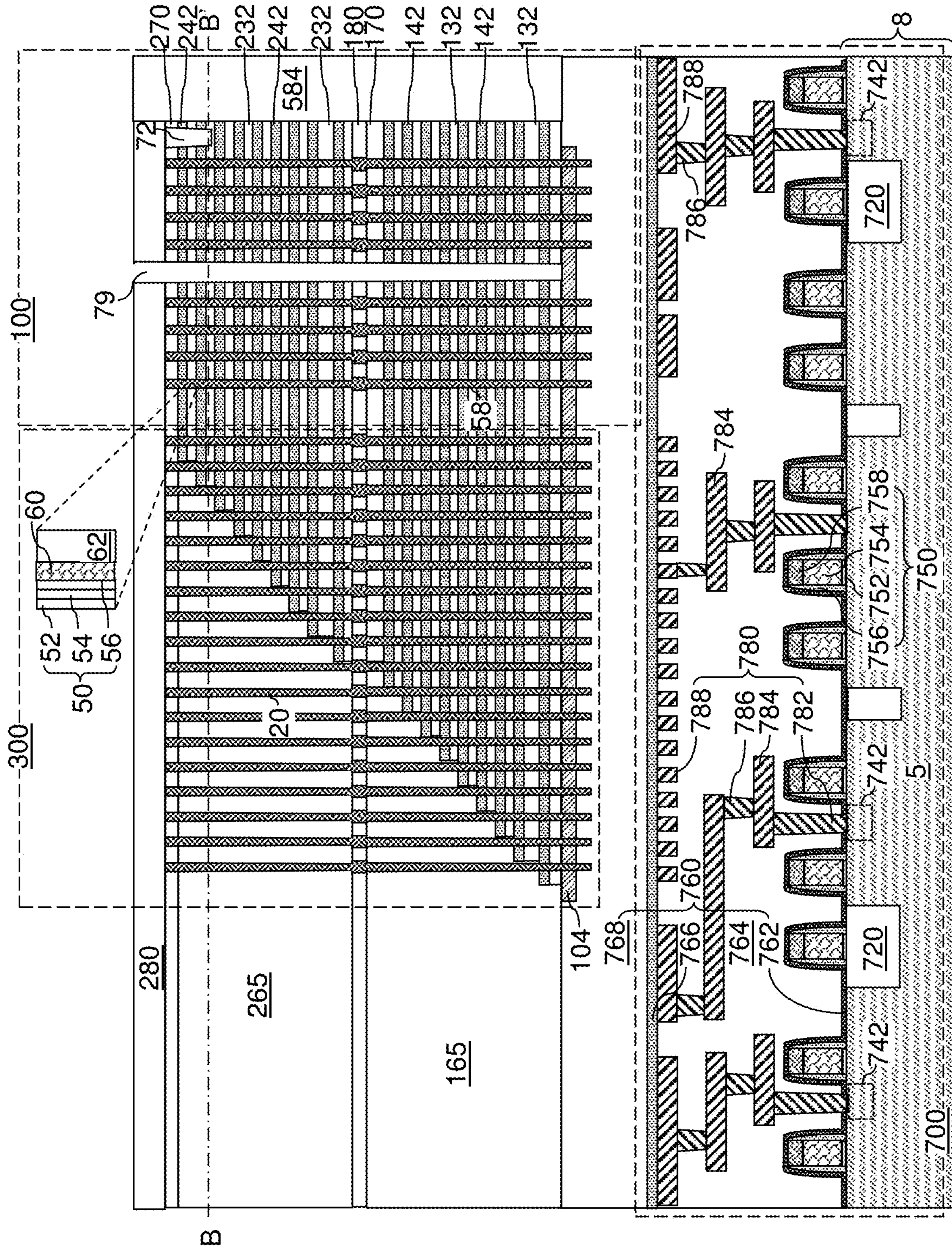


FIG. 29A

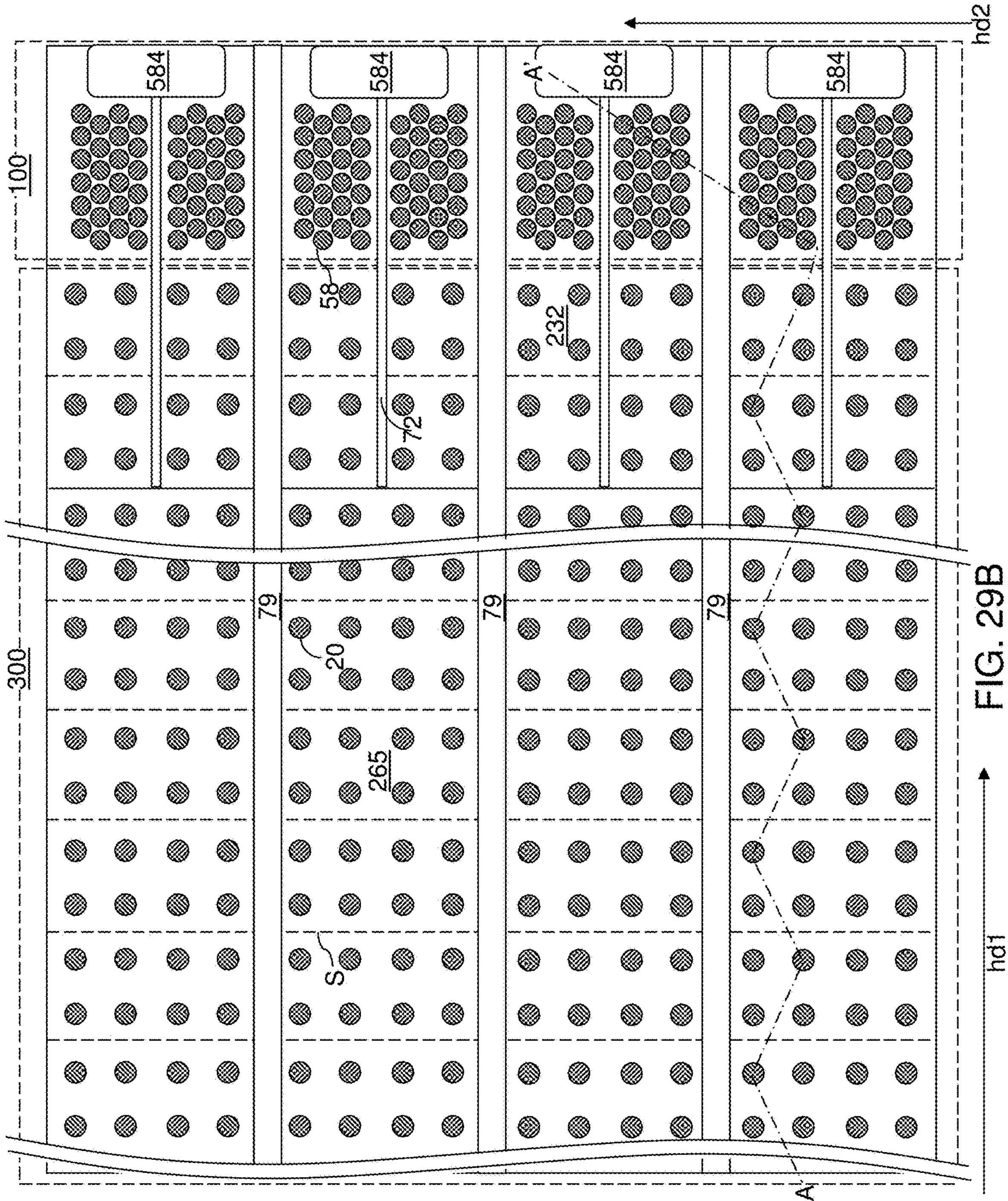


FIG. 29B

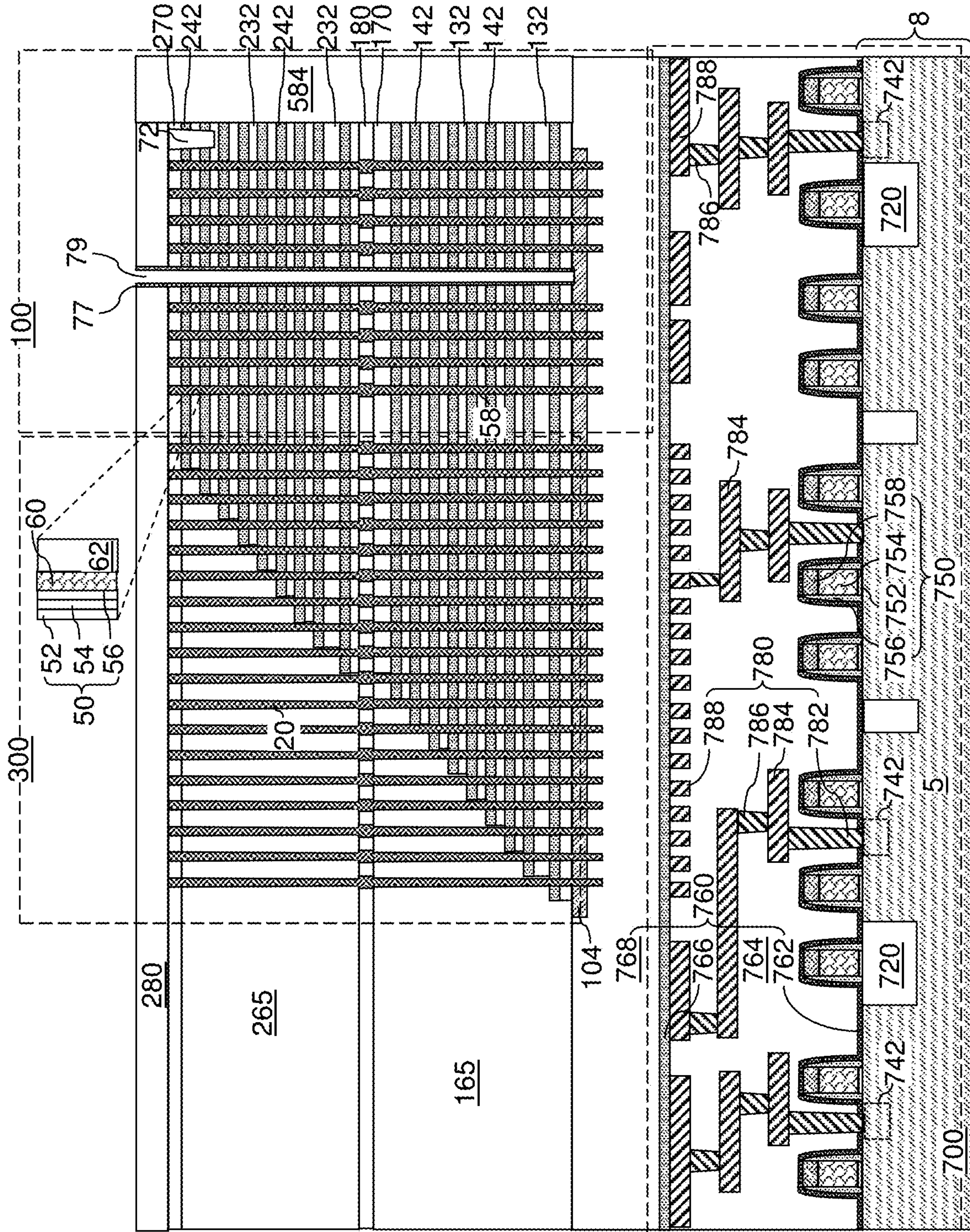


FIG. 30

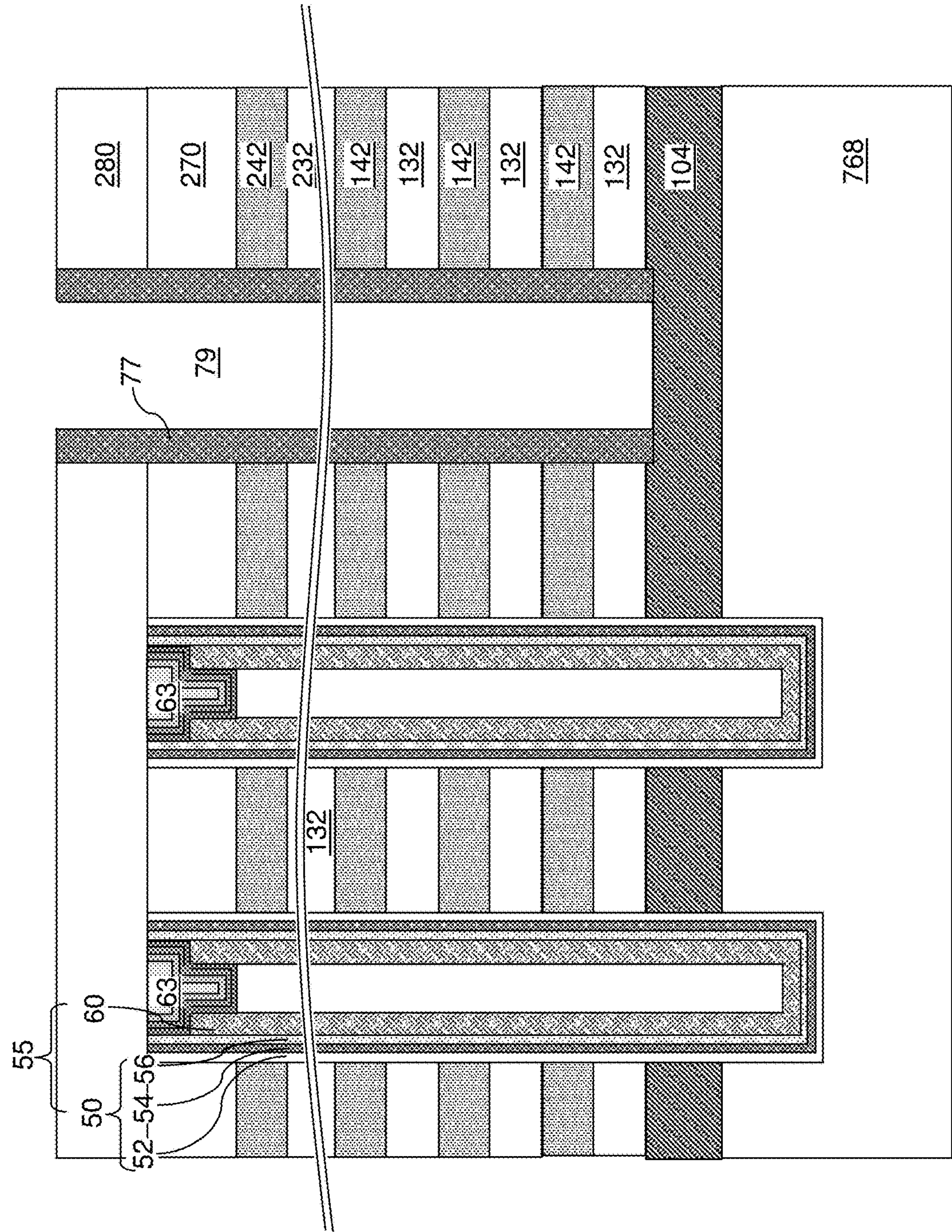


FIG. 31A

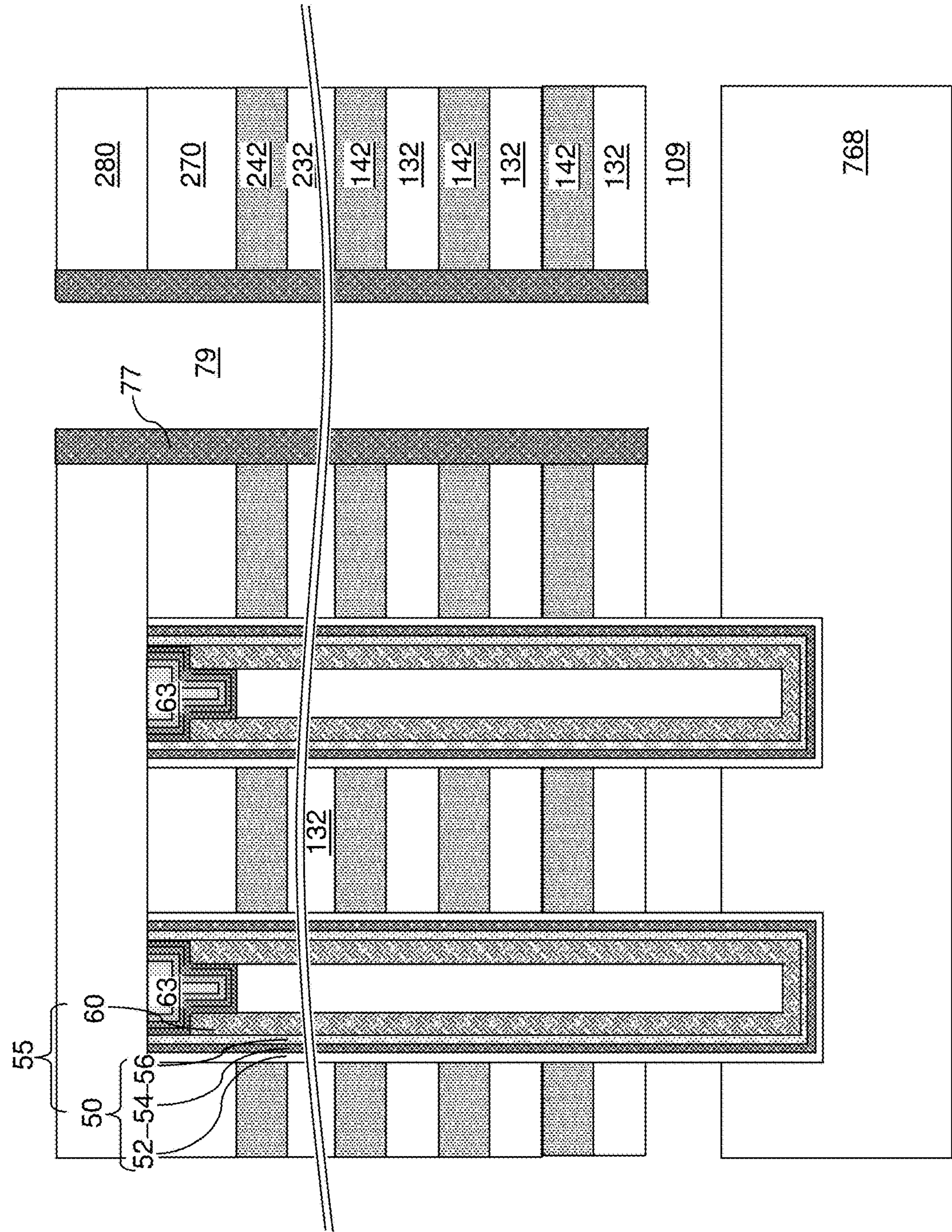


FIG. 31B

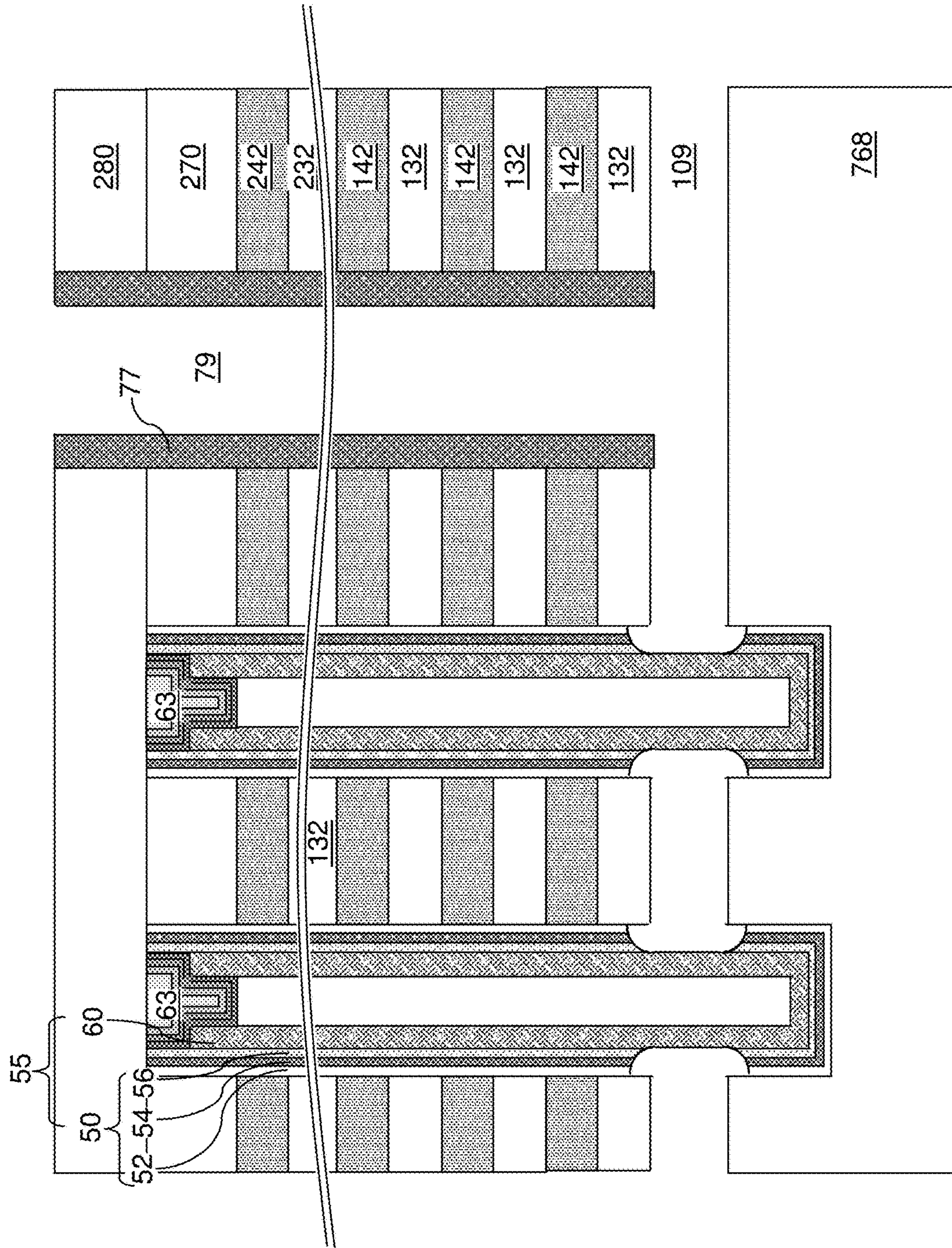


FIG. 31C

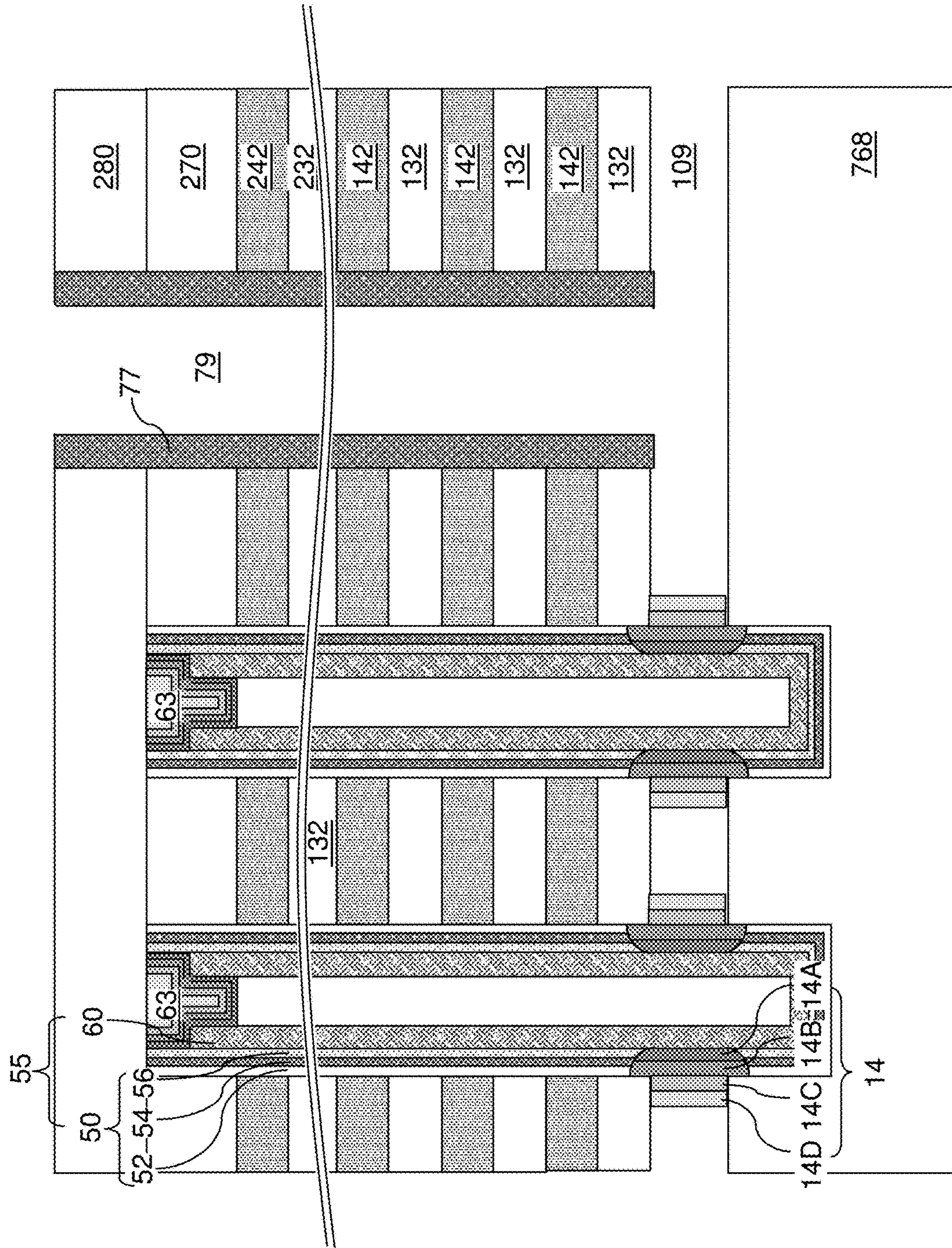


FIG. 31D

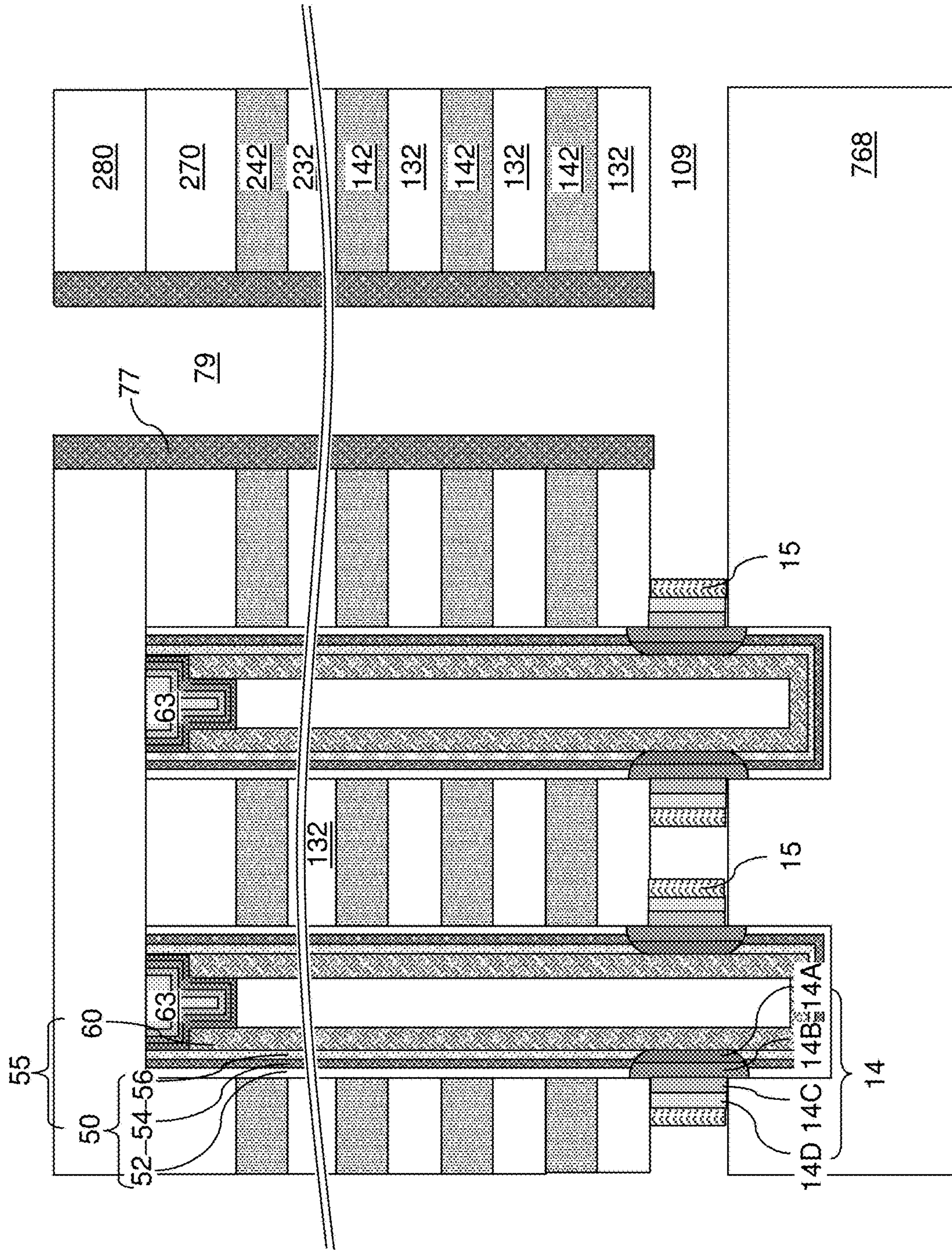


FIG. 31E

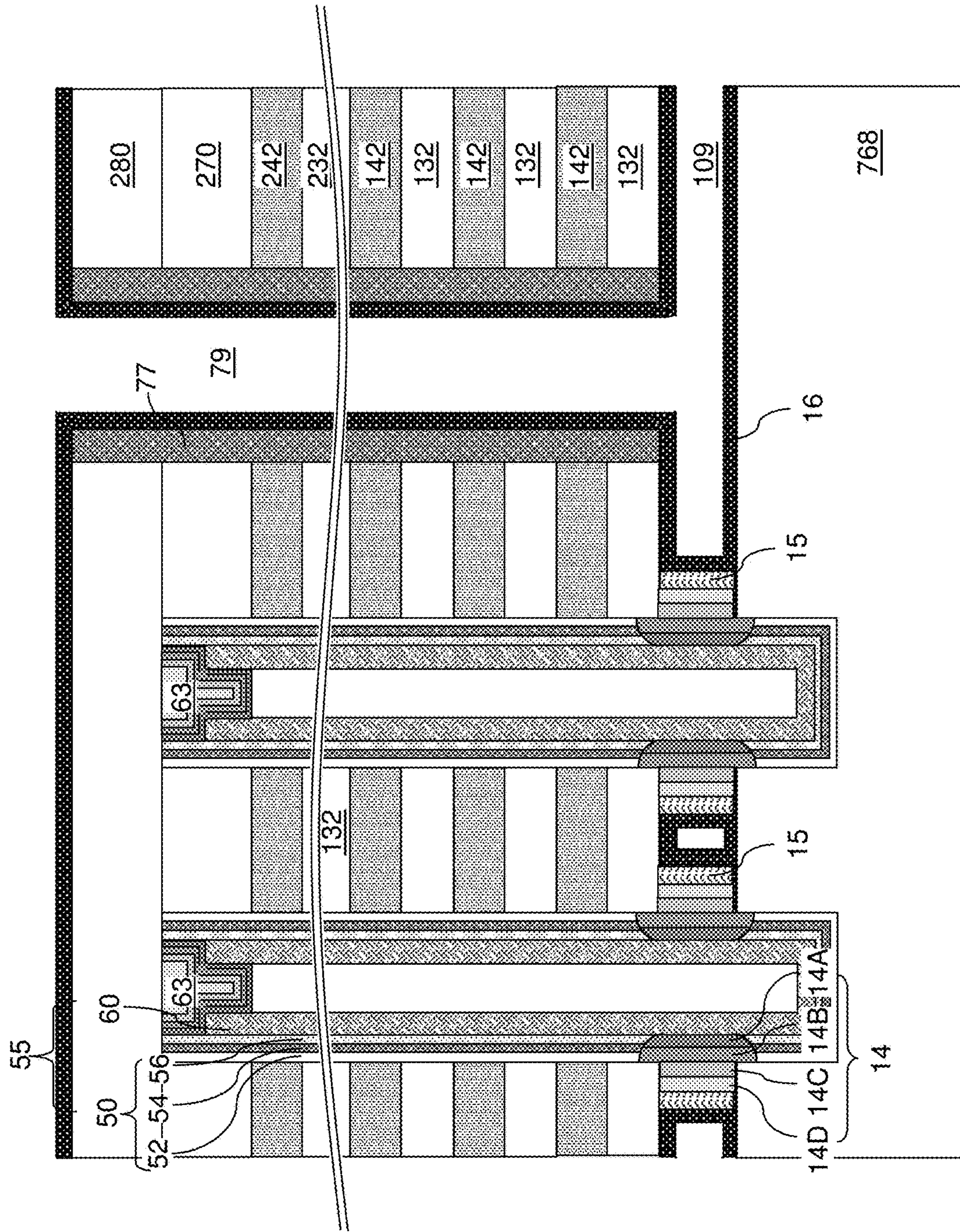


FIG. 31F

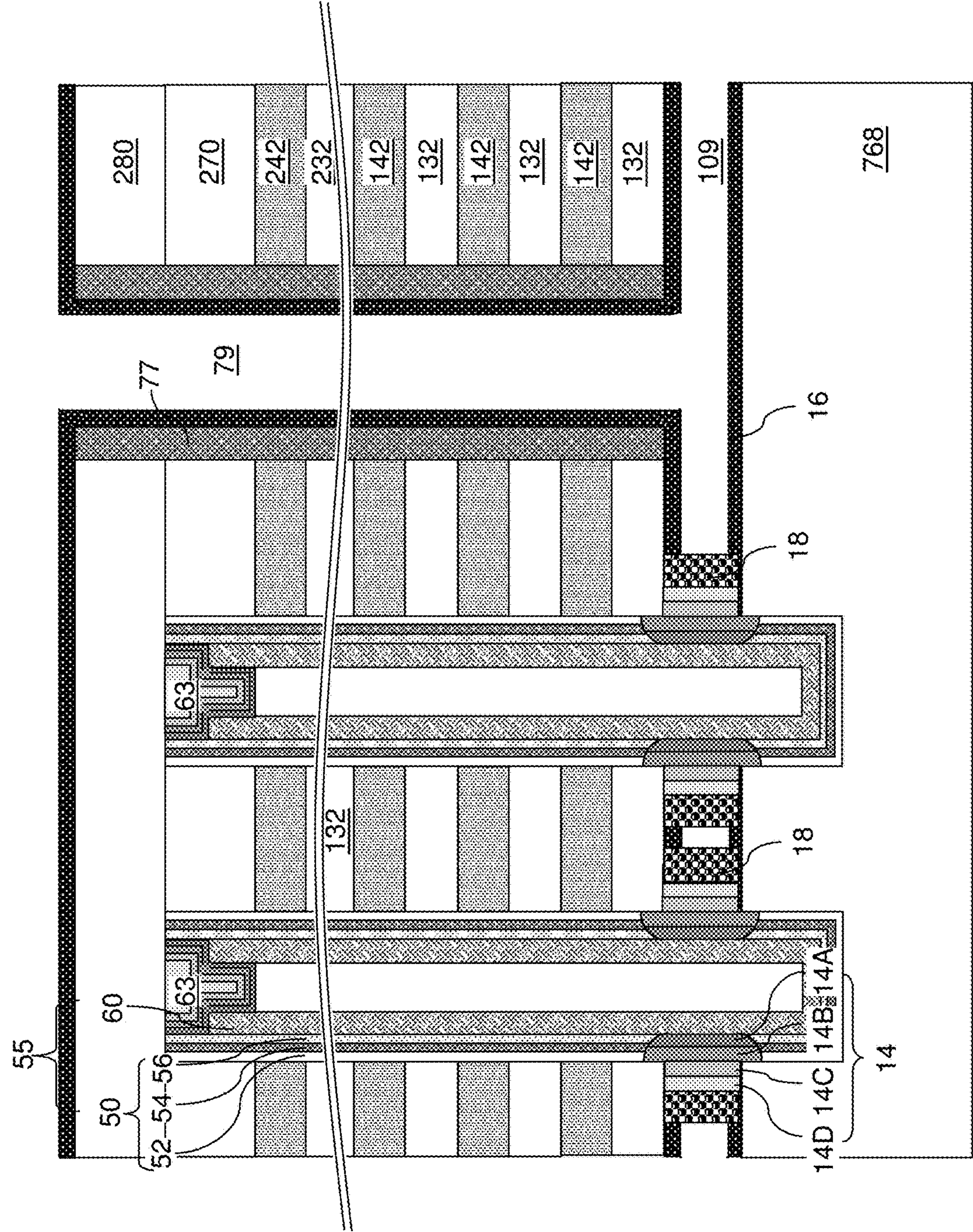


FIG. 31G

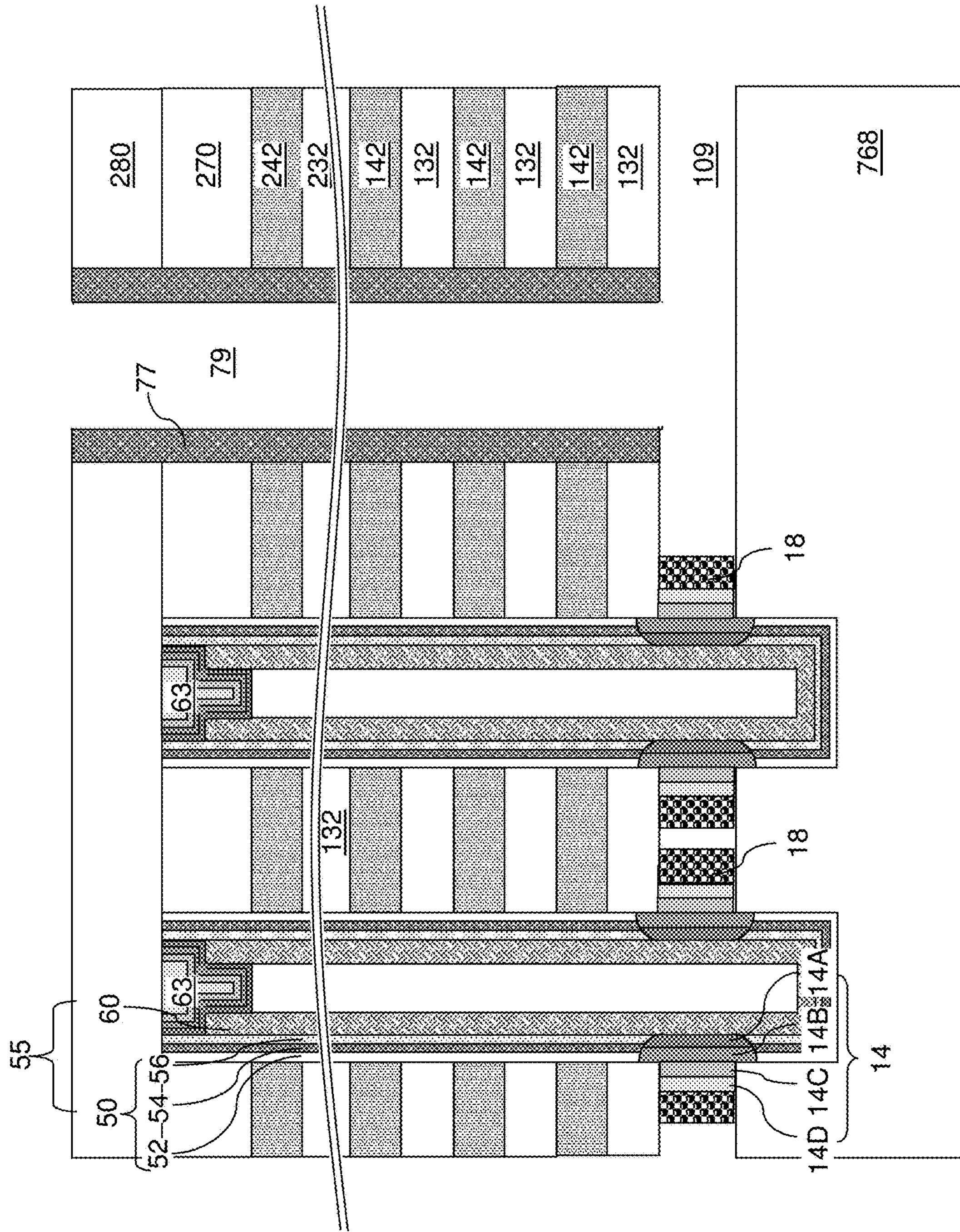


FIG. 31H

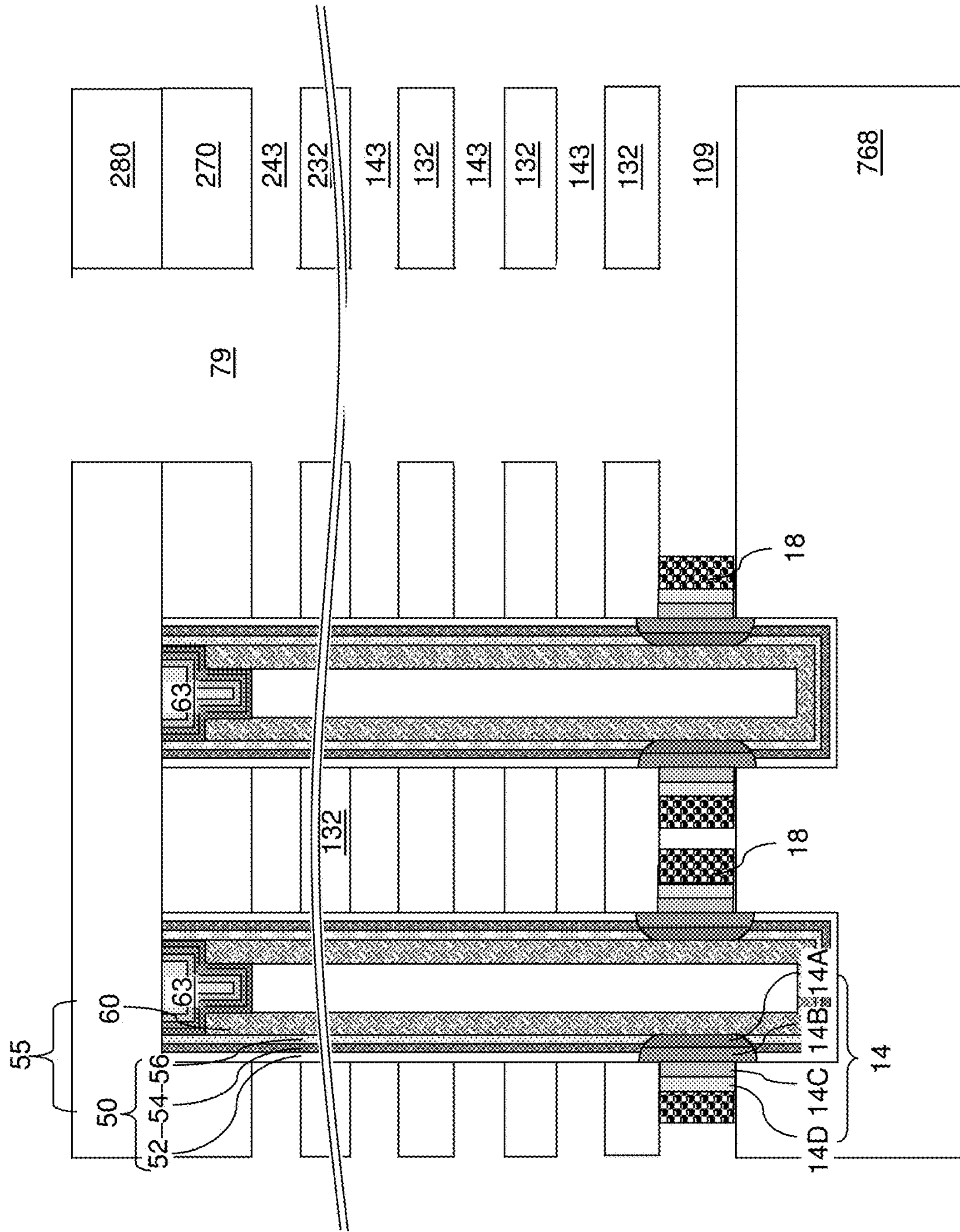


FIG. 32A

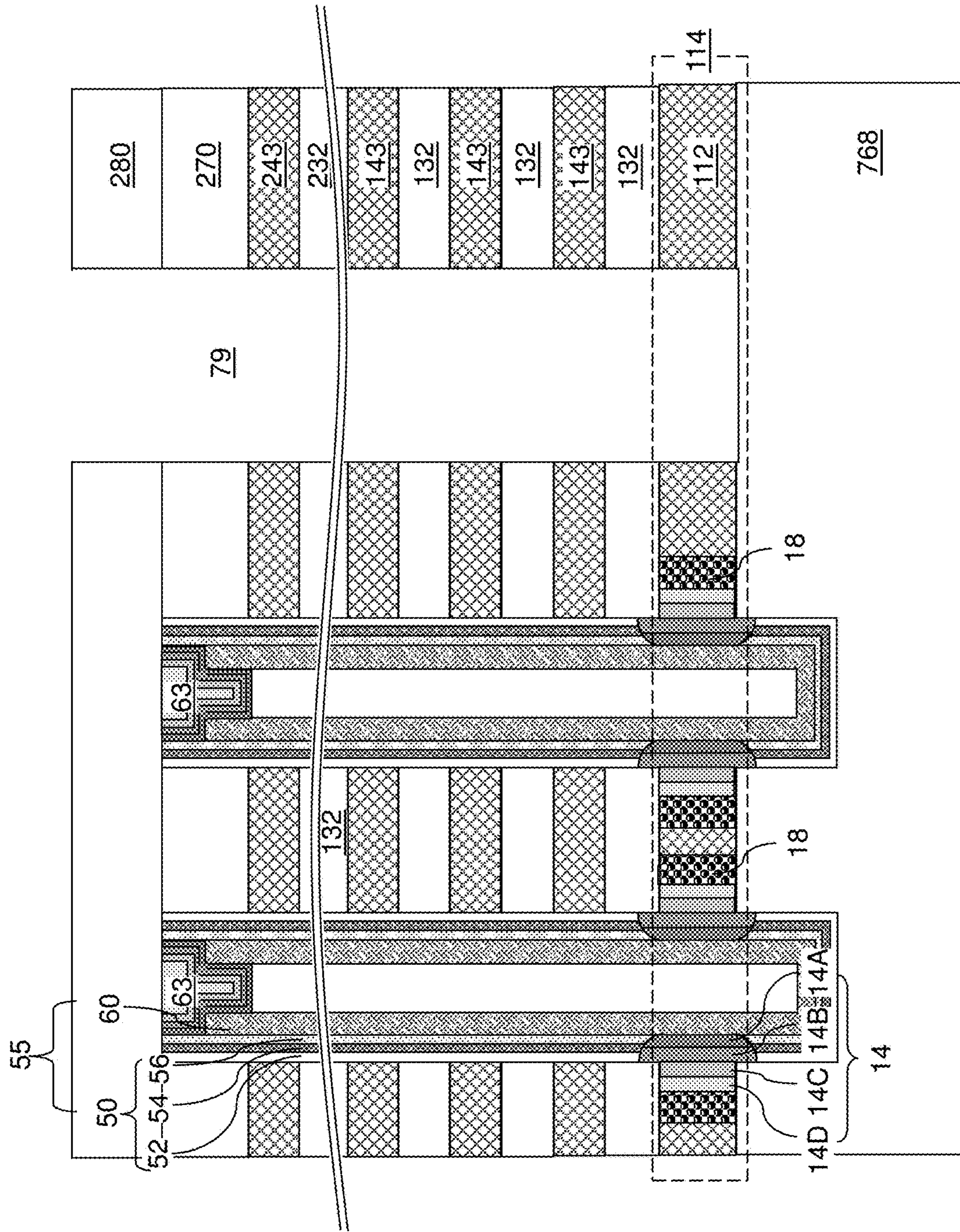


FIG. 32B

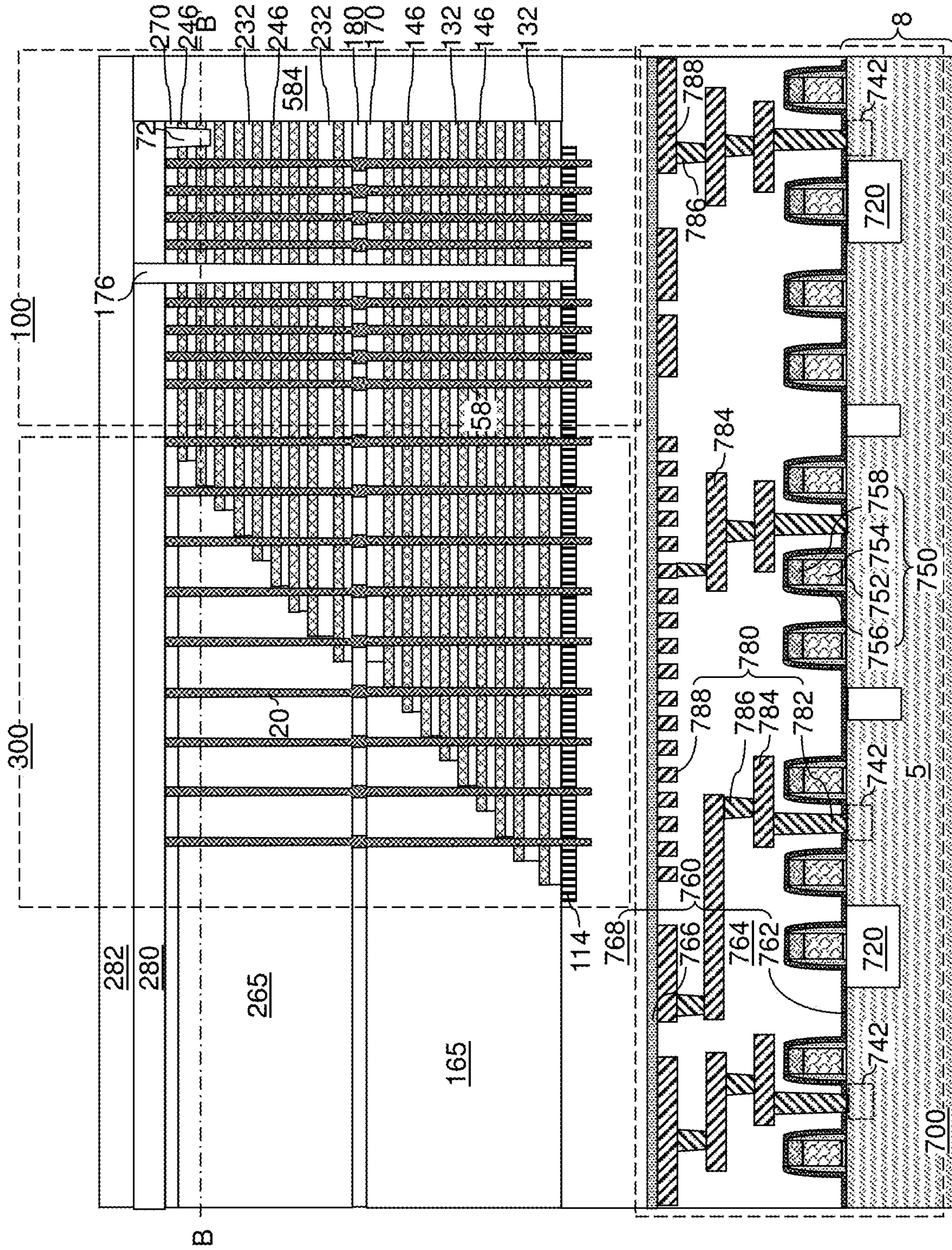


FIG. 33A

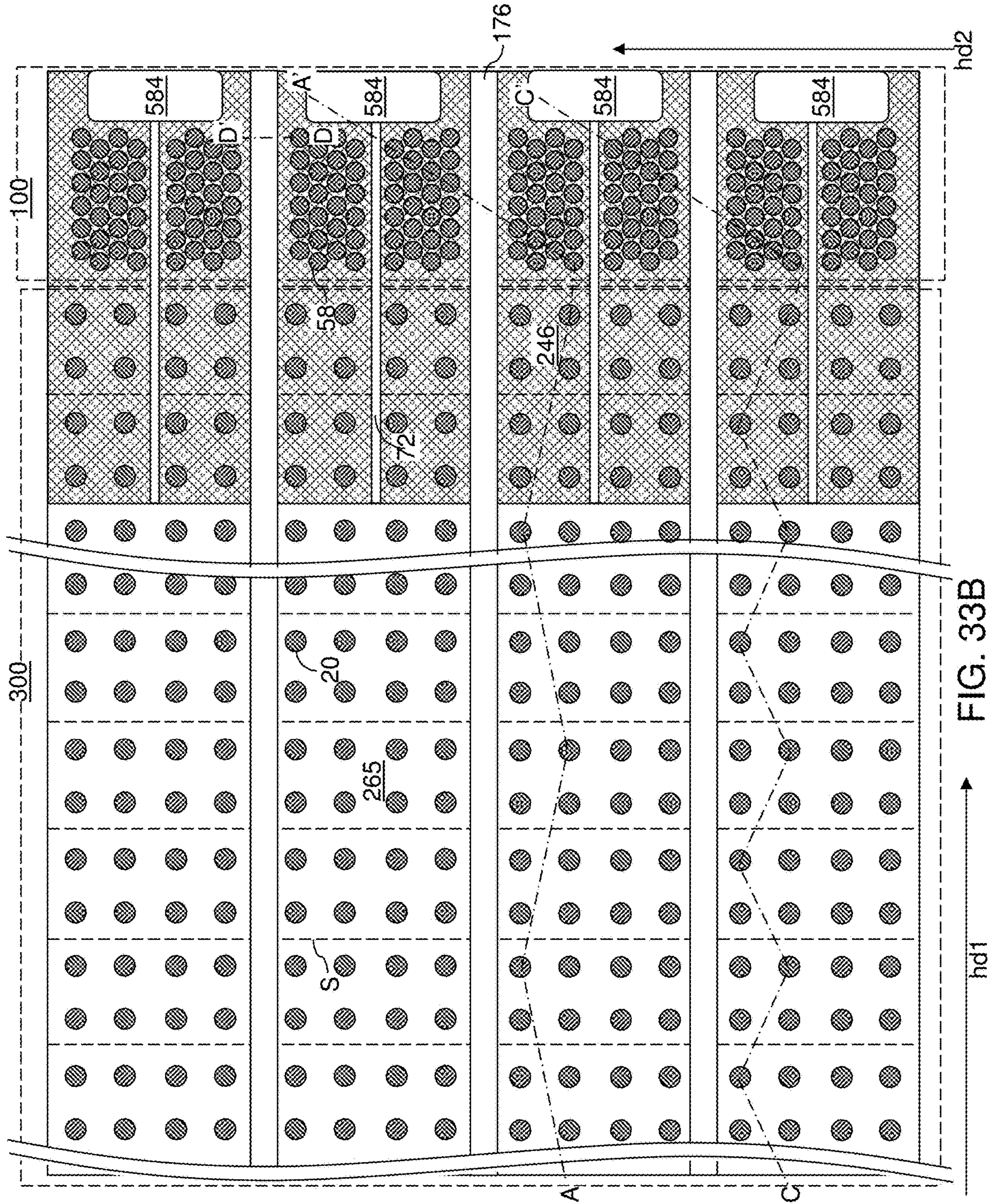


FIG. 33B

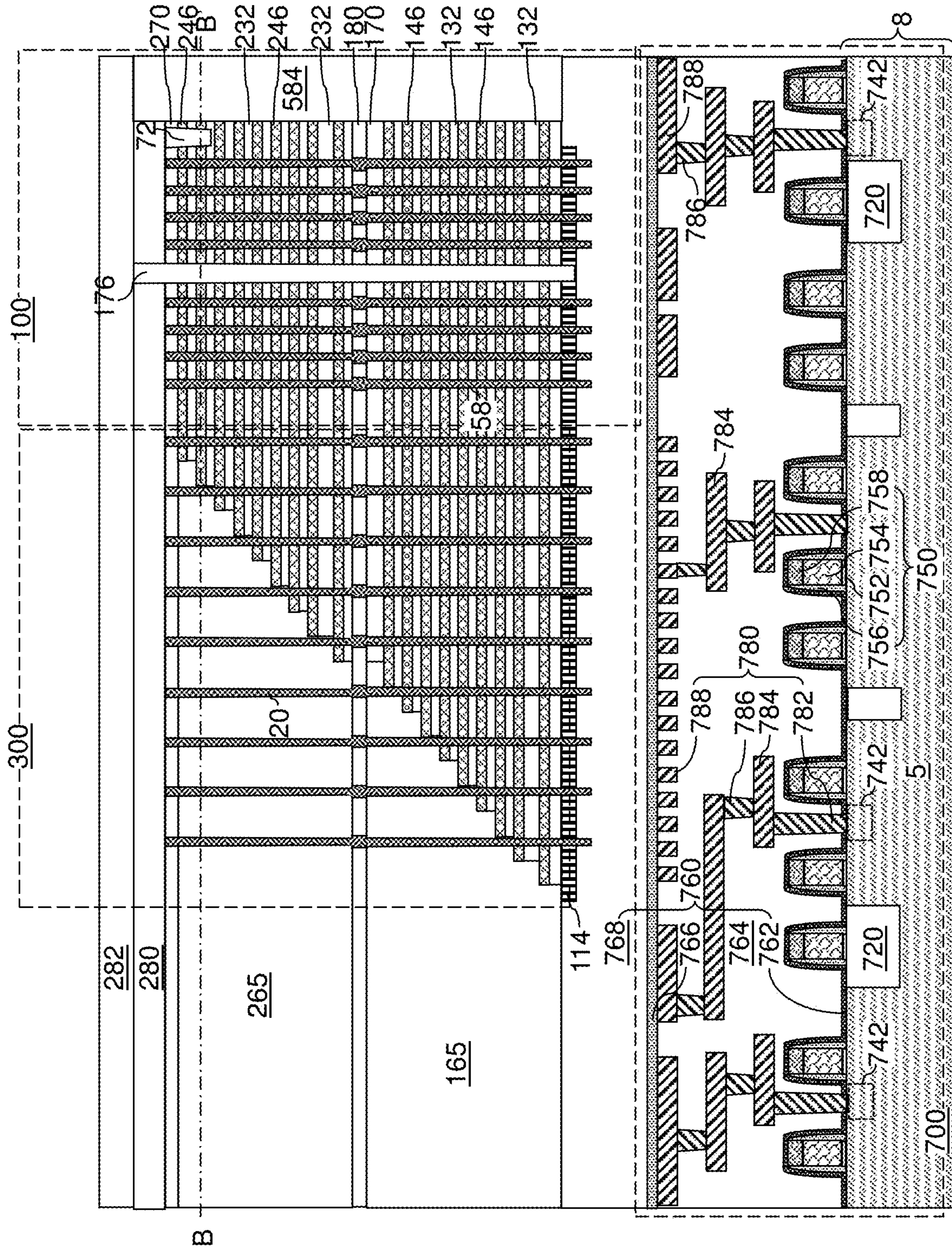


FIG. 33C

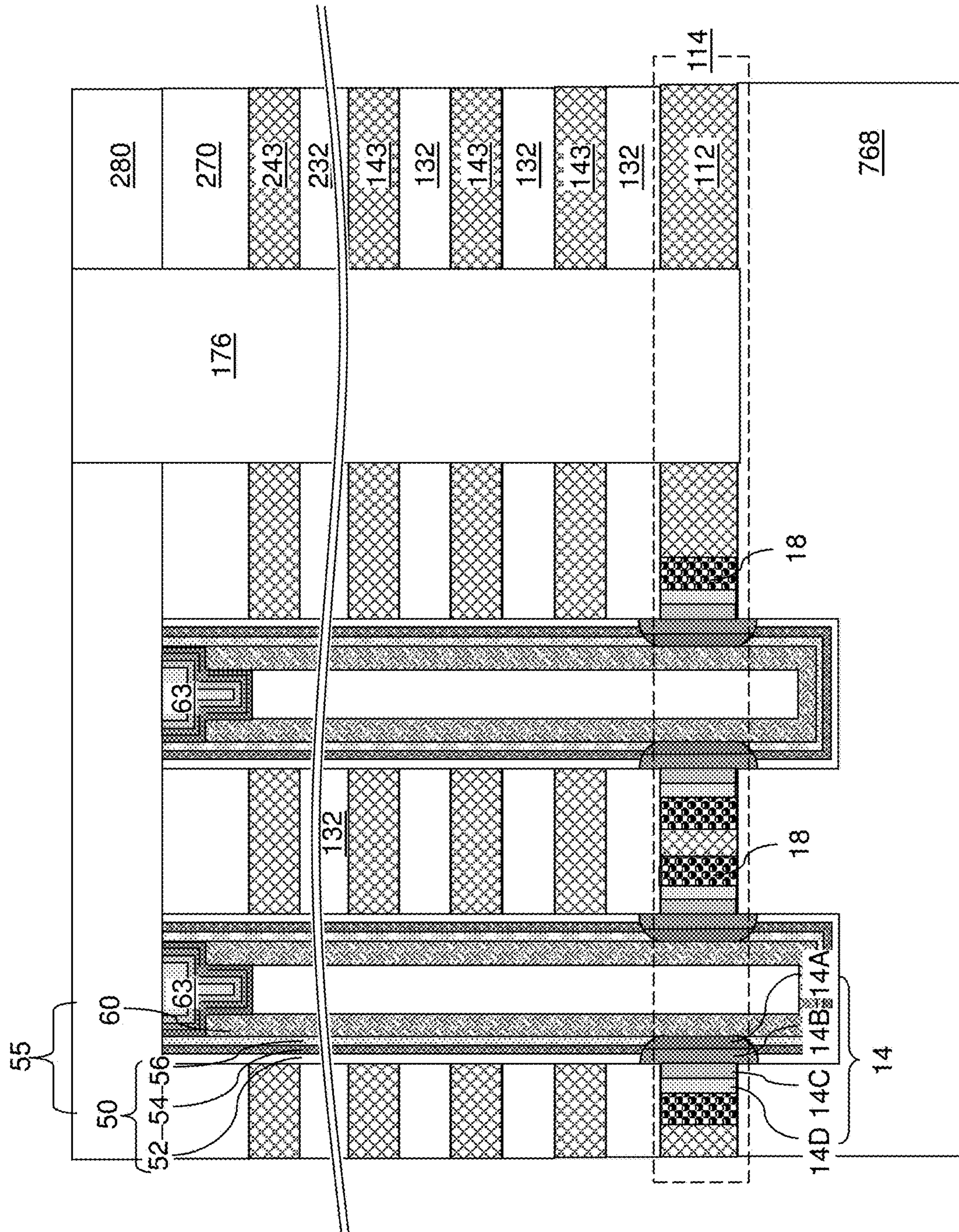


FIG. 33D

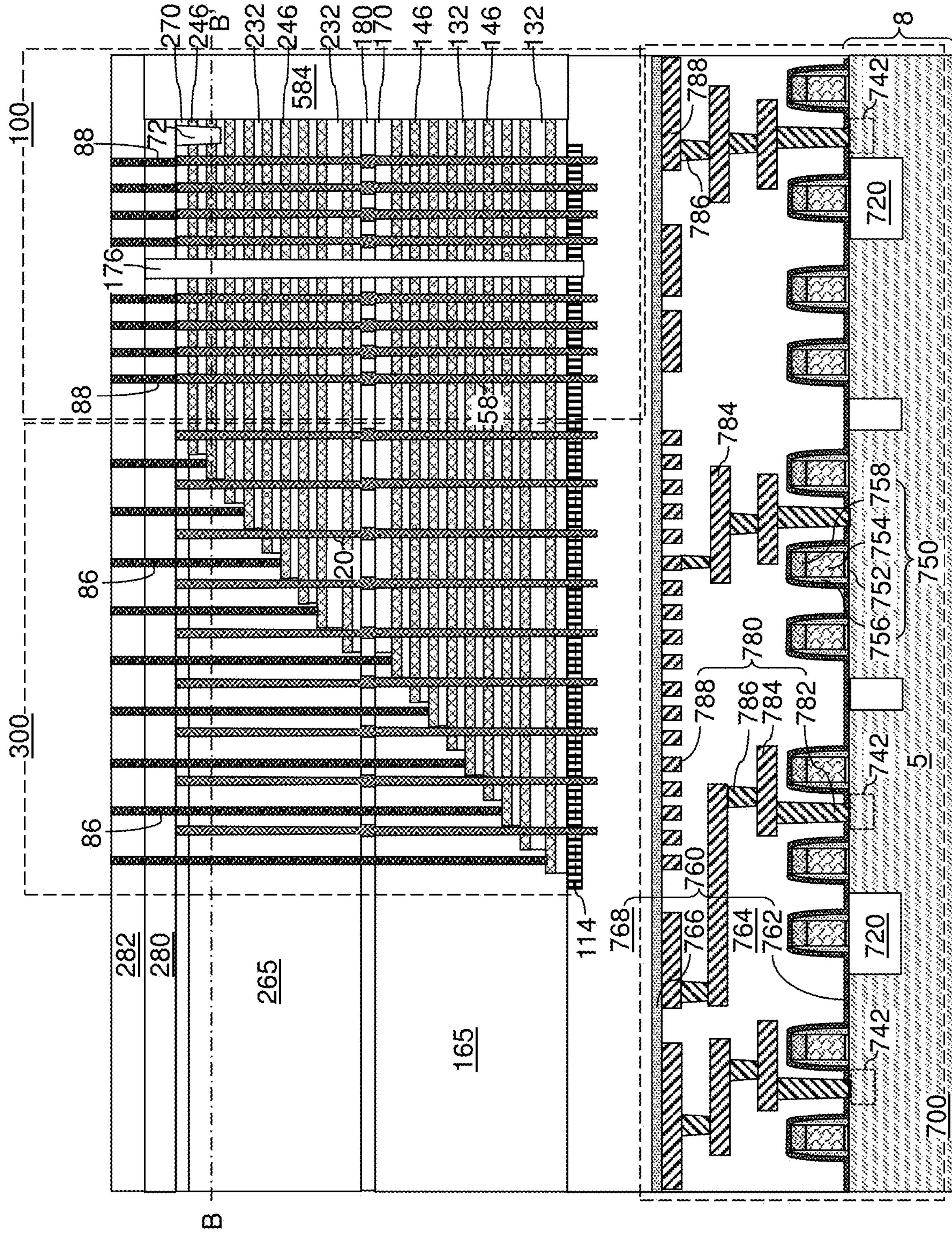


FIG. 34A

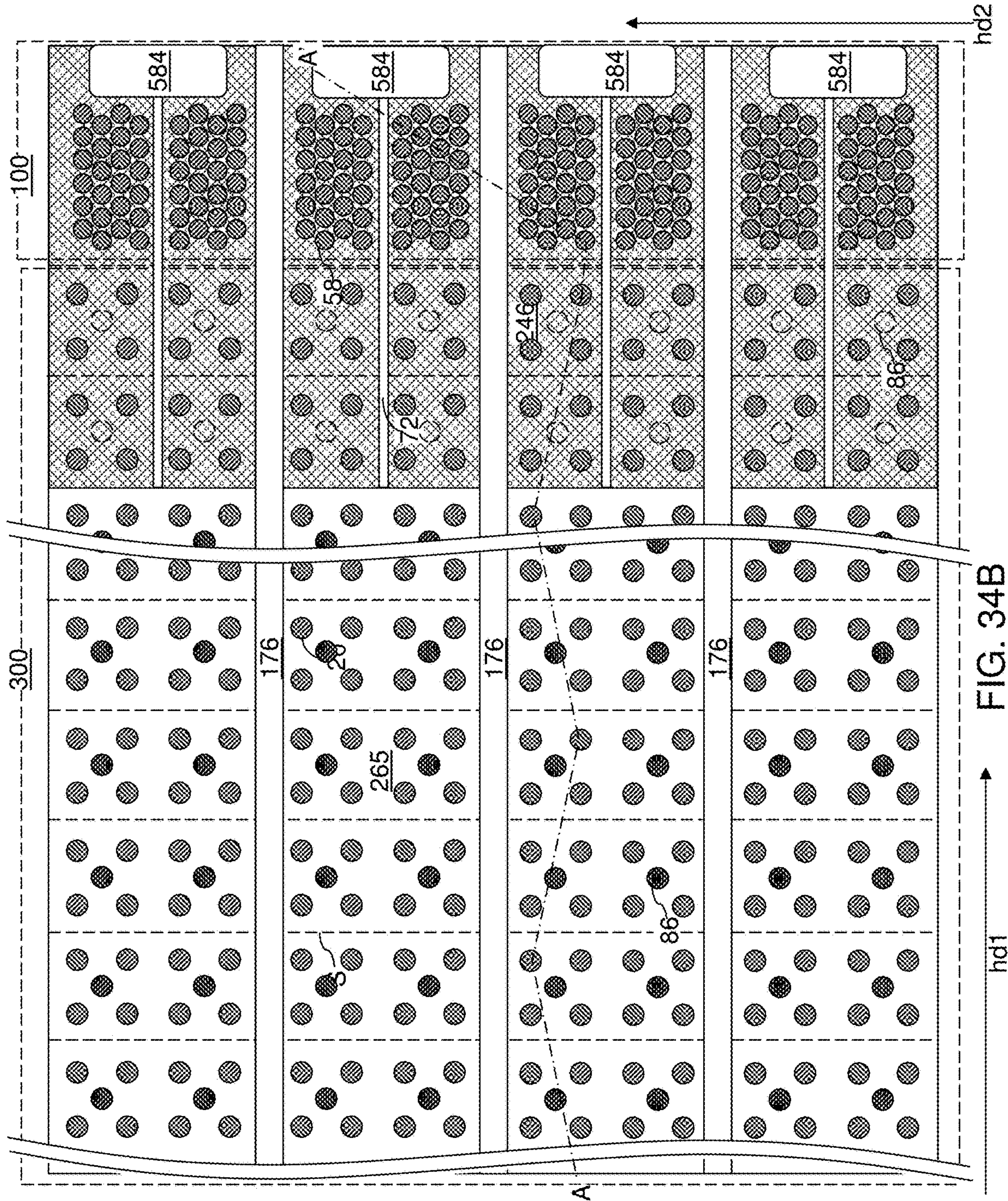


FIG. 34B

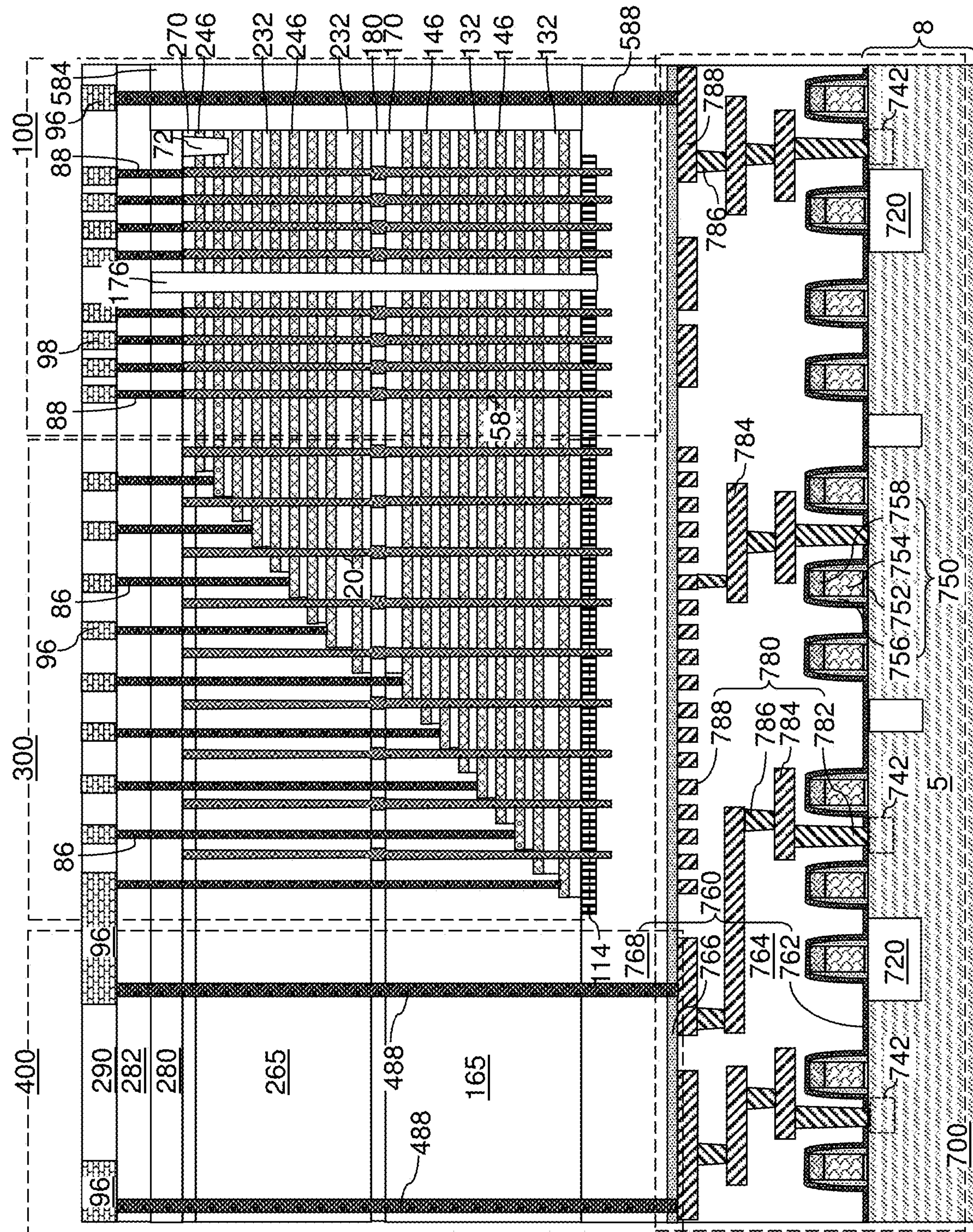


FIG. 35

THREE-DIMENSIONAL MEMORY DEVICE CONTAINING III-V COMPOUND SEMICONDUCTOR CHANNEL AND CONTACTS AND METHOD OF MAKING THE SAME

FIELD

[0001] The present disclosure relates generally to the field of semiconductor devices, and particularly to a three-dimensional memory device including III-V compound semiconductor channel and source and drain contacts, and methods of making the same.

BACKGROUND

[0002] Recently, ultra-high-density storage devices employing three-dimensional (3D) memory stack structures have been proposed. Such memory stack structures can employ an architecture known as Bit Cost Scalable (BiCS) architecture. For example, a 3D NAND stacked memory device can be formed from an array of an alternating stack of insulating materials and spacer material layers that are formed as electrically conductive layer or replaced with electrically conductive layers. Memory openings are formed through the alternating stack, and are filled with memory stack structures, each of which includes a memory film and a vertical semiconductor channel.

SUMMARY

[0003] According to an aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a substrate comprising a III-V compound substrate semiconductor layer; an alternating stack of insulating layers and electrically conductive layers located over the III-V compound substrate semiconductor layer; a memory opening vertically extending through the alternating stack; a memory opening fill structure located in the memory opening and comprising a III-V compound semiconductor pedestal in contact with the III-V compound substrate semiconductor layer, a vertical semiconductor channel, and a memory film located adjacent to the vertical semiconductor channel.

[0004] According to another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a III-V compound substrate semiconductor layer over a substrate; forming an alternating stack of insulating layers and spacer material layers over the III-V compound substrate semiconductor layer, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers; forming a memory opening vertically extending through the alternating stack; forming a memory opening fill structure in the memory opening, wherein the memory opening fill structure is formed by: forming a III-V compound semiconductor pedestal on the III-V compound substrate semiconductor layer; forming a memory film in the memory opening; and forming a vertical III-V compound semiconductor channel on the memory film.

[0005] According to yet another aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: at least one alternating stack of insulating layers and electrically conductive layers located over a substrate; a memory opening vertically extending through the at least one alternating stack; and a memory opening fill structure located in the memory opening and comprising a vertical semiconductor channel comprising a III-V compound semiconductor channel material having a doping of a first conductivity type, a memory film located adjacent to the vertical semiconductor channel, and a drain region including a graded III-V compound semiconductor material having a doping of a second conductivity type that is an opposite of the first conductivity type and having a compositional gradient therein.

[0006] According to still another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming at least one alternating stack of insulating layers and spacer material layers over a substrate, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers; forming a memory opening vertically extending through the alternating stack; forming a memory film in the memory opening; forming a vertical semiconductor channel comprising a III-V compound semiconductor channel material having a doping of a first conductivity type on the memory film; and forming a drain region including a graded III-V compound semiconductor material on the vertical semiconductor channel, wherein the drain region has a doping of a second conductivity type that is an opposite of the first conductivity type and has a compositional gradient therein.

[0007] According to even another aspect of the present disclosure, a three-dimensional memory device is provided, which comprises: a source-level contact layer overlying a substrate and comprising a III-V compound semiconductor source region; at least one alternating stack of insulating layers and electrically conductive layers located over the source-level contact layer; a memory opening vertically extending through the at least one alternating stack; and a memory opening fill structure located in the memory opening and comprising a vertical semiconductor channel comprising a III-V compound semiconductor channel material in contact with an inner sidewall of the III-V compound semiconductor source region, and a memory film located adjacent to the vertical semiconductor channel.

[0008] According to further another aspect of the present disclosure, a method of forming a three-dimensional memory device is provided, which comprises: forming a sacrificial source-level material layer overlying a substrate; forming at least one alternating stack of insulating layers and spacer material layers located over the sacrificial source-level material layer, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers; forming a memory opening through the at least one alternating stack; forming a memory opening fill structure in the memory opening, wherein the memory opening fill structure comprises a vertical semiconductor channel including a III-V compound semiconductor channel material, and a memory film located adjacent to the vertical semiconductor channel; and replacing the sacrificial source-level material layer with a source-level contact layer, wherein the source-level contact layer comprises a III-V compound semiconductor source region that contacts an outer cylindrical sidewall of the vertical semiconductor channel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a schematic vertical cross-sectional view of a first exemplary structure after formation of a germa-

nium-containing buffer layer and a III-V compound substrate semiconductor layer over a top surface of single crystalline silicon layer according to a first embodiment of the present disclosure.

[0010] FIG. **2** is a schematic vertical cross-sectional view of the first exemplary structure after patterning the III-V compound substrate semiconductor layer and the germanium-containing buffer layer according to an embodiment of the present disclosure.

[0011] FIG. **3** is a schematic vertical cross-sectional view of the first exemplary structure after formation of semiconductor devices on the single crystalline silicon layer according to the first embodiment of the present disclosure.

[0012] FIG. **4** is a schematic vertical cross-sectional view of the first exemplary structure after formation of an alternating stack of insulating layers and sacrificial material layers according to the first embodiment of the present disclosure.

[0013] FIG. **5** is a schematic vertical cross-sectional view of the first exemplary structure after formation of stepped terraces and a retro-stepped dielectric material portion according to the first embodiment of the present disclosure.

[0014] FIG. **6**A is a schematic vertical cross-sectional view of the first exemplary structure after formation of memory openings and support openings according to the first embodiment of the present disclosure.

[0015] FIG. **6**B is a top-down view of the first exemplary structure of FIG. **6**A. The vertical plane A-A' is the plane of the cross-section for FIG. **6**A.

[0016] FIGS. **7**A-**7**K are sequential schematic vertical cross-sectional views of a memory opening within the first exemplary structure during formation of a memory opening fill structure therein according to the first embodiment of the present disclosure.

[0017] FIG. **8** is a schematic vertical cross-sectional view of the first exemplary structure after formation of memory stack structures and support pillar structures according to the first embodiment of the present disclosure.

[0018] FIG. **9**A is a schematic vertical cross-sectional view of the first exemplary structure after formation of backside trenches according to the first embodiment of the present disclosure.

[0019] FIG. **9**B is a partial see-through top-down view of the first exemplary structure of FIG. **9**A. The vertical plane A-A' is the plane of the schematic vertical cross-sectional view of FIG. **9**A.

[0020] FIG. **9**C is a vertical cross-sectional view of the first exemplary structure along the vertical plane C-C' of FIG. **9**B.

[0021] FIG. **10** is a schematic vertical cross-sectional view of the first exemplary structure after formation of a III-V compound semiconductor source region in each backside trench according to the first embodiment of the present disclosure.

[0022] FIG. **11**A is a schematic vertical cross-sectional view of the first exemplary structure after formation of backside recesses according to the first embodiment of the present disclosure.

[0023] FIG. **11**B is a magnified view of the first exemplary structure of FIG. **11**A around a memory opening fill structure and a backside trench according to the first embodiment of the present disclosure.

[0024] FIG. **12**A is a schematic vertical cross-sectional view of the first exemplary structure after formation of semiconductor oxide material portions according to the first embodiment of the present disclosure.

[0025] FIG. **12**B is a schematic vertical cross-sectional view of the first exemplary structure after formation of a backside blocking dielectric layer according to the first embodiment of the present disclosure.

[0026] FIG. **13** is a schematic vertical cross-sectional view of the first exemplary structure after formation of electrically conductive layers according to the first embodiment of the present disclosure.

[0027] FIG. **14**A is a schematic vertical cross-sectional view of the first exemplary structure after removal of an electrically conductive material from within the backside trenches according to the first embodiment of the present disclosure.

[0028] FIG. **14**B is a partial see-through top-down view of the first exemplary structure of FIG. **14**A. The vertical plane A-A' is the plane of the schematic vertical cross-sectional view of FIG. **14**A.

[0029] FIG. **14**C is a vertical cross-sectional view of the first exemplary structure along the vertical plane C-C' of FIG. **13**B.

[0030] FIG. **15** is a schematic vertical cross-sectional view of the first exemplary structure after formation of an insulating spacer and a backside contact structure according to the first embodiment of the present disclosure.

[0031] FIG. **16**A is a schematic vertical cross-sectional view of the first exemplary structure after formation of additional contact via structures according to the first embodiment of the present disclosure.

[0032] FIG. **16**B is a top-down view of the first exemplary structure of FIG. **16**A. The vertical plane A-A' is the plane of the schematic vertical cross-sectional view of FIG. **16**A.

[0033] FIG. **17**A is a vertical cross-sectional view of a second exemplary semiconductor structure after formation of semiconductor devices, lower level dielectric layers, lower metal interconnect structures, and a sacrificial source-level material layer on a semiconductor substrate according to a second embodiment of the present disclosure.

[0034] FIG. **17**B is a top-down view of the second exemplary structure of FIG. **17**A. The hinged vertical plane A-A' is the plane of the vertical cross-sectional view of FIG. **17**A.

[0035] FIG. **18** is a vertical cross-sectional view of the second exemplary structure after formation of a first alternating stack of first insulting layers and first spacer material layers according to the second embodiment of the present disclosure.

[0036] FIG. **19** is a vertical cross-sectional view of the second exemplary structure after patterning of first stepped surfaces on the second alternating stack and formation of a first retro-stepped dielectric material portion according to the second embodiment of the present disclosure.

[0037] FIG. **20**A is a vertical cross-sectional view of the second exemplary structure after formation of second-tier memory openings and second-tier support openings according to the second embodiment of the present disclosure.

[0038] FIG. **20**B is a horizontal cross-sectional view of the second exemplary structure along the horizontal plane B-B' in FIG. **20**A. The zig-zag vertical plane A-A' corresponds to the plane of the vertical cross-sectional view of FIG. **20**A.

[0039] FIG. **21** is a vertical cross-sectional view of the second exemplary structure after formation of sacrificial

memory opening fill portions and sacrificial support opening fill portions according to the second embodiment of the present disclosure.

[0040] FIG. **22** is a vertical cross-sectional view of the second exemplary structure after formation of a second-tier alternating stack of second insulating layers and second spacer material layers, second stepped surfaces, and a second retro-stepped dielectric material portion according to the second embodiment of the present disclosure.

[0041] FIG. **23**A is a vertical cross-sectional view of the second exemplary structure after formation of second-tier memory openings and second-tier support openings according to the second embodiment of the present disclosure.

[0042] FIG. **23**B is a horizontal cross-sectional view of the second exemplary structure along the horizontal plane B-B' of FIG. **23**A. The hinged vertical plane A-A' corresponds to the plane of the vertical cross-sectional view of FIG. **23**A.

[0043] FIG. **24** is a vertical cross-sectional view of the second exemplary structure after formation of inter-tier memory openings and inter-tier support openings according to the second embodiment of the present disclosure.

[0044] FIGS. **25**A-**25**G illustrate sequential vertical cross-sectional views of a memory opening during formation of a memory opening fill structure according to the second embodiment of the present disclosure.

[0045] FIG. **26** is a vertical cross-sectional view of the second exemplary structure after formation of memory opening fill structures and support pillar structures according to the second embodiment of the present disclosure.

[0046] FIG. **27**A is a vertical cross-sectional view of the second exemplary structure after formation of pillar cavities according to the second embodiment of the present disclosure.

[0047] FIG. **27**B is a horizontal cross-sectional view of the second exemplary structure along the horizontal plane B-B' of FIG. **27**A. The hinged vertical plane A-A' corresponds to the plane of the vertical cross-sectional view of FIG. **27**A.

[0048] FIG. **28** is a vertical cross-sectional view of the second exemplary structure after formation of dielectric pillar structures according to the second embodiment of the present disclosure.

[0049] FIG. **29**A is a vertical cross-sectional view of the second exemplary structure after formation of a second contact-level dielectric layer and backside trenches according to the second embodiment of the present disclosure.

[0050] FIG. **29**B is a horizontal cross-sectional view of the second exemplary structure along the horizontal plane B-B' of FIG. **29**A. The hinged vertical plane A-A' corresponds to the plane of the vertical cross-sectional view of FIG. **29**A.

[0051] FIG. **30** is a vertical cross-sectional view of the second exemplary structure after formation of backside trench spacers according to the second embodiment of the present disclosure.

[0052] FIGS. **31**A-**31**H illustrate sequential vertical cross-sectional views of memory opening fill structures and a backside trench during formation of a source cavity, a III-V compound semiconductor source region, and an annular metal germanosilicide portion according to the second embodiment of the present disclosure.

[0053] FIGS. **32**A and **32**B illustrate sequential vertical cross-sectional views of memory opening fill structures and a backside trench during formation of backside recesses and electrically conductive layers according to the second embodiment of the present disclosure.

[0054] FIG. **33**A is a vertical cross-sectional view of the second exemplary structure after formation of backside trench fill structures in the backside trenches according to the second embodiment of the present disclosure.

[0055] FIG. **33**B is a horizontal cross-sectional view of the second exemplary structure along the horizontal plane B-B' of FIG. **33**A. The hinged vertical plane A-A' corresponds to the plane of the vertical cross-sectional view of FIG. **33**A.

[0056] FIG. **33**C is a vertical cross-sectional view of the second exemplary structure along the vertical plane C-C' of FIG. **33**B.

[0057] FIG. **33**D is a vertical cross-sectional view of the second exemplary structure along the vertical plane D-D' of FIG. **33**B.

[0058] FIG. **34**A is a vertical cross-sectional view of the second exemplary structure after formation of a second contact-level dielectric layer and various contact via structures according to the second embodiment of the present disclosure.

[0059] FIG. **34**B is a horizontal cross-sectional view of the second exemplary structure along the vertical plane B-B' of FIG. **34**A. The hinged vertical plane A-A' corresponds to the plane of the vertical cross-sectional view of FIG. **34**A.

[0060] FIG. **35** is a vertical cross-sectional view of the second exemplary structure after formation of through-memory-level via structures and upper metal line structures according to the second embodiment of the present disclosure.

DETAILED DESCRIPTION

[0061] As discussed above, the present disclosure is directed to a three-dimensional memory device including III-V compound semiconductor channel and source and drain contacts, and methods of making the same, the various aspects of which are discussed herein in detail.

[0062] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. The term "at least one" element refers to all possibilities including the possibility of a single element and the possibility of multiple elements.

[0063] The same reference numerals refer to the same element or similar element. Unless otherwise indicated, elements having the same reference numerals are presumed to have the same composition and the same function. Unless otherwise indicated, a "contact" between elements refers to a direct contact between elements that provides an edge or a surface shared by the elements. If two or more elements are not in direct contact with each other or among one another, the two elements are "disjoined from" each other or "disjoined among" one another. As used herein, a first element located "on" a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located "directly on" a second element if there exist a physical contact between a surface of the first element and a surface of the second element. As used herein, a first element is "electrically connected to" a second element if there exists a conductive path consisting of at least one

conductive material between the first element and the second element. As used herein, a “prototype” structure or an “in-process” structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0064] As used herein, a “layer” refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, or may have one or more layer thereupon, thereabove, and/or therebelow.

[0065] As used herein, a first surface and a second surface are “vertically coincident” with each other if the second surface overlies or underlies the first surface and there exists a vertical plane or a substantially vertical plane that includes the first surface and the second surface. A substantially vertical plane is a plane that extends straight along a direction that deviates from a vertical direction by an angle less than 5 degrees. A vertical plane or a substantially vertical plane is straight along a vertical direction or a substantially vertical direction, and may, or may not, include a curvature along a direction that is perpendicular to the vertical direction or the substantially vertical direction.

[0066] A monolithic three-dimensional memory array is a memory array in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term “monolithic” means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Pat. No. 5,915,167 titled “Three-dimensional Structure Memory.” The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three-dimensional memory arrays.

[0067] Generally, a semiconductor package (or a “package”) refers to a unit semiconductor device that can be attached to a circuit board through a set of pins or solder balls. A semiconductor package may include a semiconductor chip (or a “chip”) or a plurality of semiconductor chips that are bonded thereamongst, for example, by flip-chip bonding or another chip-to-chip bonding. A package or a chip may include a single semiconductor die (or a “die”) or a plurality of semiconductor dies. A die is the smallest unit that can independently execute external commands or report status. Typically, a package or a chip with multiple dies is capable of simultaneously executing as many number of external commands as the total number of planes therein. Each die includes one or more planes. Identical concurrent operations can be executed in each plane within a same die, although there may be some restrictions. In case a die is a memory die, i.e., a die including memory elements, concurrent read operations, concurrent write operations, or concurrent erase operations can be performed in each plane within a same memory die. In a memory die, each plane contains a number of memory blocks (or “blocks”), which are the smallest unit that can be erased by in a single erase operation. Each memory block contains a number of pages, which are the smallest units that can be selected for programming. A page is also the smallest unit that can be selected to a read operation.

[0068] Referring to FIG. **1**, a first exemplary structure according to a first embodiment of the present disclosure is illustrated, which includes a substrate containing a single crystalline silicon layer **9**. The single crystalline silicon layer **9** can have a major surface **7**, i.e., a surface that occupies more than 25% of the entire area of the single crystalline silicon layer **9**. The major surface may be a planar surface located within a horizontal plane. In one embodiment, the single crystalline silicon layer **9** may be provided within a semiconductor substrate such as a commercially available bulk single crystal silicon wafer or a silicon-on-insulator substrate. The single crystalline silicon layer **9** may comprise an upper portion of a bulk silicon wafer, a doped well in a bulk silicon wafer, a single crystal silicon film deposited on the silicon wafer, the silicon portion of a silicon on insulator substrate or any other underlying single crystal silicon surface.

[0069] An optional graded silicon-germanium-containing buffer layer **910** may be grown on the major surface **7** (which may be a top surface) of the single crystalline silicon layer **9** by an epitaxial deposition process. The optional graded silicon-germanium-containing buffer layer **910** includes a graded epitaxial silicon-germanium alloy material in which the atomic concentration of germanium increases gradually within a vertical distance from the single crystalline silicon layer **9**. If present, the graded silicon-germanium-containing buffer layer **910** can include a vertically increasing atomic percentage of germanium that may include, for example, from 0% to 100%, such as from 10% to 90%, and/or from 20% to 80%. The thickness of the graded silicon-germanium-containing buffer layer **910** can be selected such that the graded silicon-germanium-containing buffer layer **910** remains single crystalline throughout the growth process. The average lattice constant may gradually change from the lattice constant of silicon to the lattice constant of germanium from the bottom portion of the graded silicon-germanium-containing buffer layer **910** to the top portion of the graded silicon-germanium-containing buffer layer **910**. The thickness of the graded silicon-germanium-containing buffer layer **910** may be in a range from 50 nm to 1,000 nm, such as from 100 nm to 500 nm, although lesser and greater thicknesses may also be employed. Alternatively, the graded silicon-germanium-containing buffer layer **910** may be omitted.

[0070] A germanium-containing buffer layer **920** can be grown directly on the single crystalline silicon layer **9** (in case a graded silicon-germanium-containing buffer layer **910** is omitted) or directly on a top surface of the graded silicon-germanium-containing buffer layer **910**. The germanium-containing buffer layer **920** can include single crystalline germanium and/or a single crystalline silicon-germanium alloy in which the atomic concentration of germanium is at least 80%. An epitaxy process employing a germanium-containing precursor (such as digermane) can be performed

to form the germanium-containing buffer layer **920**. The germanium-containing buffer layer **920** can be epitaxially aligned to the single crystalline silicon layer **9**. The thickness of the germanium-containing buffer layer **920** may be in a range from 50 nm to 600 nm, such as from 100 nm to 300 nm, although lesser and greater thicknesses may also be employed.

[0071] A III-V compound substrate semiconductor layer **930** can be grown over the top surface of single crystalline silicon layer **9**. The III-V compound substrate semiconductor layer **930** includes a III-V compound semiconductor material such as AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InGaAs, InSb, AlGaN, AlGaP, AlGaAs, AlGaSb, GaInN, GaInP, GaInAs, GaInSb, etc. In one embodiment, the III-V compound substrate semiconductor layer **930** comprises GaAs. The III-V compound substrate semiconductor layer **930** can be grown directly on the top surface of the germanium-containing buffer layer **920** by an epitaxial deposition process, which may employ a chemical vapor deposition process. The III-V compound substrate semiconductor layer **930** can be epitaxially aligned to the single crystalline material of the germanium-containing buffer layer **920**. The III-V compound substrate semiconductor layer **930** may be intrinsic or may have a doping of a first conductivity type, which may be p-type or n-type. The atomic concentration of dopants of the first conductivity type in the III-V compound substrate semiconductor layer **930** may be in a range from $1.0\times10^{15}/cm^3$ to $1.0\times10^{18}/cm^3$, m, such as from $1.0\times10^{16}/cm^3$ to $1.0\times10^{17}/cm^3$, although lesser and greater atomic concentrations can also be employed. In one embodiment, the first conductivity type may be p-type, and the III-V compound substrate semiconductor layer **930** can include p-doped GaAs.

[0072] The first exemplary structure may include a memory array region **100** in which a memory array is to be subsequently formed, a staircase region **300** in which contact via structures to word lines are to be subsequently formed, and an optional peripheral device region **200** in which peripheral semiconductor devices are to be subsequently formed. If present, the peripheral device region **200** may be employed to provide a logic (i.e., driver) circuit including field effect transistors and configured to control operation of memory elements in the memory array to be subsequently formed. Alternatively, the driver circuit may be formed below the memory array region **100** or on a separate substrate from the memory array region **100** and then bonded to the memory array region **100**.

[0073] Referring to FIG. **2**, a photoresist layer (not shown) can be applied over the top surface of the first exemplary structure, and can be lithographically patterned to cover the memory array region **100** and the staircase region **300**. An etch process can be performed to physically expose the single crystalline silicon layer **9** in the peripheral device region **200**. The photoresist layer can be subsequently removed, for example, by ashing.

[0074] Referring to FIG. **3**, at least one semiconductor device **707** for a peripheral circuitry can be formed in the peripheral device region **200**. The at least one semiconductor device can include, for example, field effect transistors. For example, at least one shallow trench isolation structure **720** can be formed by etching portions of the single crystalline silicon layer **9** and depositing a dielectric material therein. A gate dielectric layer, at least one gate conductor layer, and a gate cap dielectric layer can be formed over the single crystalline silicon layer **9**, and can be subsequently patterned to form at least one gate structure (**750**, **752**, **754**, **758**), each of which can include a gate dielectric **750**, a gate electrode (**752**, **754**), and a gate cap dielectric **758**. The gate electrode (**752**, **754**) may include a stack of a first gate electrode portion **752** and a second gate electrode portion **754**. At least one gate spacer **756** can be formed around the at least one gate structure (**750**, **752**, **754**, **758**) by depositing and anisotropically etching a dielectric liner. Active regions **730** can be formed in upper portions of the single crystalline silicon layer **9**, for example, by introducing electrical dopants employing the at least one gate structure (**750**, **752**, **754**, **758**) as masking structures. Additional masks may be employed as needed. The active region **730** can include source regions and drain regions of field effect transistors. A first dielectric liner **761** and a second dielectric liner **762** can be optionally formed. Each of the first and second dielectric liners (**761**, **762**) can comprise a silicon oxide layer, a silicon nitride layer, and/or a dielectric metal oxide layer. As used herein, silicon oxide includes silicon dioxide as well as non-stoichiometric silicon oxides having more or less than two oxygen atoms for each silicon atoms. Silicon dioxide is preferred. In an illustrative example, the first dielectric liner **761** can be a silicon oxide layer, and the second dielectric liner **762** can be a silicon nitride layer. The least one semiconductor device for the peripheral circuitry can contain a driver circuit for memory devices to be subsequently formed, which can include at least one NAND device. Alternatively, as described above the peripheral region **200** containing the driver circuit may be formed under the memory array region **100** or on a separate substrate from the memory array region **100**.

[0075] A dielectric material such as silicon oxide can be deposited over the at least one semiconductor device, and can be subsequently planarized to form a planarization dielectric layer **770**. The planarization dielectric layer **770** and the dielectric liners (**761**, **762**) can be removed from the memory array region **100** and the staircase region **300**, for example, by performing a chemical mechanical planarization process. In one embodiment, the top surface of the planarization dielectric layer **770** may be within the same horizontal plane as the top surface of the III-V compound substrate semiconductor layer **930**.

[0076] Referring to FIG. **4**, a stack of an alternating plurality of insulating layers **32** and spacer material layers can be formed over the top surface of the III-V compound substrate semiconductor layer **930**. The spacer material layers may be formed as electrically conductive layers, or may be formed as sacrificial material layers **42** and may be subsequently replaced with electrically conductive layers. While the present disclosure is described employing an embodiment in which the spacer material layers are sacrificial material layers **42** that are subsequently replaced with electrically conductive layers, embodiments are expressly contemplated herein in which electrically conductive layers are formed instead of sacrificial material layers **42**. In this case, steps for replacing the sacrificial material layers **42** with electrically conductive layers can be omitted.

[0077] The stack of the alternating plurality is herein referred to as an alternating stack (**32**, **42**). The insulating layers **32** include a first material, which is an insulating material. Insulating materials that can be employed for the insulating layers **32** include, but are not limited to, silicon oxide (including doped or undoped silicate glass), silicon

nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the insulating layers **32** comprise, and/or consists essentially of, silicon oxide.

[0078] The spacer material layers include a second material that is different from the first material. In case the spacer material layers are formed as the sacrificial material layers **42**, the sacrificial material layers **42** include a sacrificial material that can be subsequently removed selective to the material of the insulating layers **32**. As used herein, a removal of a first material is "selective to" a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a "selectivity" of the removal process for the first material with respect to the second material. The sacrificial material layers **42** comprise, and/or consist essentially of, an insulating material, a semiconductor material, or a conductive material. The sacrificial material layers **42** can be subsequently replaced with electrically conductive electrodes which can function, for example, as control gate electrodes of a vertical NAND device. Non-limiting examples of the sacrificial material that can be employed for the sacrificial material include silicon nitride, an amorphous semiconductor material (such as amorphous silicon), and a polycrystalline semiconductor material (such as polysilicon). In one embodiment, the sacrificial material layers **42** can include silicon nitride.

[0079] In one embodiment, the insulating layers **32** can include silicon oxide, and sacrificial material layers can include silicon nitride sacrificial material layers. The insulating layers **32** can be deposited, for example, by chemical vapor deposition (CVD). For example, if silicon oxide is employed for the insulating layers **32**, tetraethyl orthosilicate (TEOS) can be employed as the precursor material for the CVD process. The sacrificial material layers **42** can be formed, for example, CVD or atomic layer deposition (ALD). The thicknesses of the insulating layers **32**) and the sacrificial material layers **42** can be in a range from 10 nm to 60 nm, such as from 20 nm to 40 nm, although lesser and greater thicknesses can be employed for each insulating layer **32** and for each sacrificial material layer **42**. In some embodiments, the bottommost sacrificial material layer **42** may be subsequently replaced with an electrically conductive layer that functions as a source-side electrode that turns on or turns off a horizontal semiconductor channel that is formed in the top surface portions of the III-V compound substrate semiconductor layer **930**.

[0080] The number of repetitions of the pairs of an insulating layer **32** and a sacrificial material layer (e.g., a control gate electrode or a sacrificial material layer) **42** can be in a range from 2 to 1,024, and typically from 8 to 256, although a greater number of repetitions can also be employed. The top and bottom gate electrodes in the stack may function as the select gate electrodes. In one embodiment, each sacrificial material layer **42** in the alternating stack (**32**, **42**) can have a uniform thickness that is substantially invariant within each respective sacrificial material layer **42**.

[0081] Optionally, an insulating cap layer **70** can be formed over the alternating stack (**32**, **42**). The insulating cap layer **70** includes a dielectric material that is different from the material of the sacrificial material layers **42**. In one embodiment, the insulating cap layer **70** can include a dielectric material that can be employed for the insulating layers **32** as described above. The insulating cap layer **70** can have a greater thickness than each of the insulating layers **32**. The insulating cap layer **70** can be deposited, for example, by chemical vapor deposition. In one embodiment, the insulating cap layer **70** can be a silicon oxide layer.

[0082] Referring to FIG. **5**, stepped surfaces are formed at a peripheral device region of the alternating stack (**32**, **42**), which is herein referred to as a terrace region. As used herein, "stepped surfaces" refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. A stepped cavity is formed within the volume from which portions of the alternating stack (**32**, **42**) are removed through formation of the stepped surfaces. A "stepped cavity" refers to a cavity having stepped surfaces. The terrace region is formed in the staircase region **300**, which is located between the memory array region **100** and the peripheral device region **200** containing the at least one semiconductor device for the peripheral circuitry.

[0083] The stepped cavity can have various stepped surfaces such that the horizontal cross-sectional shape of the stepped cavity changes in steps as a function of the vertical distance from the top surface of the substrate (**9**, **10**). In one embodiment, the stepped cavity can be formed by repetitively performing a set of processing steps. The set of processing steps can include, for example, an etch process of a first type that vertically increases the depth of a cavity by one or more levels, and an etch process of a second type that laterally expands the area to be vertically etched in a subsequent etch process of the first type. As used herein, a "level" of a structure including alternating plurality is defined as the relative position of a pair of a first material layer and a second material layer within the structure. Each sacrificial material layer **42** other than a topmost sacrificial material layer **42** within the alternating stack (**32**, **42**) laterally extends farther than any overlying sacrificial material layer **42** within the alternating stack (**32**, **42**) in the terrace region. The terrace region includes stepped surfaces of the alternating stack (**32**, **42**) that continuously extend from a bottommost layer within the alternating stack (**32**, **42**) to a topmost layer within the alternating stack (**32**, **42**).

[0084] A retro-stepped dielectric material portion **65** (i.e., an insulating fill material portion) can be formed in the stepped cavity by deposition of a dielectric material therein. For example, a dielectric material such as silicon oxide can be deposited in the stepped cavity. Excess portions of the deposited dielectric material can be removed from above the top surface of the insulating cap layer **70**, for example, by chemical mechanical planarization (CMP). The remaining portion of the deposited dielectric material filling the stepped cavity constitutes the retro-stepped dielectric material portion **65**. As used herein, a "retro-stepped" element refers to an element that has stepped surfaces and a horizontal cross-sectional area that increases monotonically as a

function of a vertical distance from a top surface of a substrate on which the element is present. If silicon oxide is employed for the retro-stepped dielectric material portion **65**, the silicon oxide of the retro-stepped dielectric material portion **65** may, or may not, be doped with dopants such as B, P, and/or F.

[0085] Optionally, drain select level isolation structures **72** can be formed through the insulating cap layer **70** and a subset of the sacrificial material layers **42** located at drain select levels. The drain select level isolation structures **72** can be formed, for example, by forming drain select level isolation trenches and filling the drain select level isolation trenches with a dielectric material such as silicon oxide. Excess portions of the dielectric material can be removed from above the top surface of the insulating cap layer **70**.

[0086] Referring to FIGS. **6**A and **6**B, a lithographic material stack (not shown) including at least a photoresist layer can be formed over the insulating cap layer **70** and the retro-stepped dielectric material portion **65**, and can be lithographically patterned to form openings therein. The openings include a first set of openings formed over the memory array region **100** and a second set of openings formed over the staircase region **300**. The pattern in the lithographic material stack can be transferred through the insulating cap layer **70** or the retro-stepped dielectric material portion **65**, and through the alternating stack (**32**, **42**) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the alternating stack (**32**, **42**) underlying the openings in the patterned lithographic material stack are etched to form memory openings **49** and support openings **19**. As used herein, a "memory opening" refers to a structure in which memory elements, such as a memory stack structure, is subsequently formed. As used herein, a "support opening" refers to a structure in which a support structure (such as a support pillar structure) that mechanically supports other elements is subsequently formed. The memory openings **49** are formed through the insulating cap layer **70** and the entirety of the alternating stack (**32**, **42**) in the memory array region **100**. The support openings **19** are formed through the retro-stepped dielectric material portion **65** and the portion of the alternating stack (**32**, **42**) that underlie the stepped surfaces in the staircase region **300**.

[0087] The memory openings **49** extend through the entirety of the alternating stack (**32**, **42**). The support openings **19** extend through a subset of layers within the alternating stack (**32**, **42**). The chemistry of the anisotropic etch process employed to etch through the materials of the alternating stack (**32**, **42**) can alternate to optimize etching of the materials in the alternating stack (**32**, **42**). The anisotropic etch can be, for example, a series of reactive ion etches. The sidewalls of the memory openings **49** and the support openings **19** can be substantially vertical, or can be tapered. The patterned lithographic material stack can be subsequently removed, for example, by ashing.

[0088] The memory openings **49** and the support openings **19** can extend from the top surface of the alternating stack (**32**, **42**) to at least the horizontal plane including the topmost surface of the III-V compound substrate semiconductor layer **930**. In one embodiment, an overetch into the III-V compound substrate semiconductor layer **930** may be optionally performed after the top surface of the III-V compound substrate semiconductor layer **930** is physically exposed at a bottom of each memory opening **49** and each support opening **19**. The overetch may be performed prior to, or after, removal of the lithographic material stack. In other words, the recessed surfaces of the III-V compound substrate semiconductor layer **930** may be vertically offset from the un-recessed top surfaces of the III-V compound substrate semiconductor layer **930** by a recess depth. The recess depth can be, for example, in a range from 1 nm to 50 nm, although lesser and greater recess depths can also be employed. The overetch is optional, and may be omitted. If the overetch is not performed, the bottom surfaces of the memory openings **49** and the support openings **19** can be coplanar with the topmost surface of the III-V compound substrate semiconductor layer **930**.

[0089] Each of the memory openings **49** and the support openings **19** may include a sidewall (or a plurality of sidewalls) that extends substantially perpendicular to the topmost surface of the single crystalline silicon layer **9**. A two-dimensional array of memory openings **49** can be formed in the memory array region **100**. A two-dimensional array of support openings **19** can be formed in the staircase region **300**.

[0090] FIGS. **7**A-**7**K illustrate structural changes in a memory opening **49**, which is one of the memory openings **49** in the exemplary structure of FIGS. **6**A and **6**B. The same structural change occurs simultaneously in each of the other memory openings **49** and in each of the support openings **19**.

[0091] Referring to FIG. **7**A, a memory opening **49** in the exemplary device structure of FIGS. **6**A and **6**B is illustrated. The memory opening **49** extends through the insulating cap layer **70**, the alternating stack (**32**, **42**), and optionally into an upper portion of the III-V compound substrate semiconductor layer **930**. At this processing step, each support opening **19** can extend through the retro-stepped dielectric material portion **65**, a subset of layers in the alternating stack (**32**, **42**), and optionally through the upper portion of the III-V compound substrate semiconductor layer **930**. The recess depth of the bottom surface of each memory opening with respect to the top surface of the III-V compound substrate semiconductor layer **930** can be in a range from 0 nm to 30 nm, although greater recess depths can also be employed. Optionally, the sacrificial material layers **42** can be laterally recessed partially to form lateral recesses (not shown), for example, by an isotropic etch.

[0092] Referring to FIG. **7**B, an optional III-V compound semiconductor pedestal (e.g., an epitaxial pedestal) **11** can be formed at the bottom portion of each memory opening **49** and each support openings **19**, for example, by selective epitaxy. Each III-V compound semiconductor pedestal **11** comprises a single crystalline III-V compound semiconductor material in epitaxial alignment with the single crystalline semiconductor material of the III-V compound substrate semiconductor layer **930**. The III-V compound semiconductor pedestal **11** can be formed by selectively growing a single crystalline III-V compound semiconductor material from a physically exposed portion of a top surface of the III-V compound substrate semiconductor layer **930** at the bottom of the memory opening **49**. Each III-V compound semiconductor pedestal **11** can include any of the III-V compound semiconductor materials that may be employed for the III-V compound substrate semiconductor layer **930**. The single crystalline III-V compound semiconductor material of the III-V compound semiconductor pedestals **11** may be the same as, or may be different from, the III-V compound semiconductor material of the III-V compound substrate

semiconductor layer **930**. In one embodiment, the top surface of each III-V compound semiconductor pedestal **11** can be formed above a horizontal plane including the top surface of a bottommost sacrificial material layer **42**. In this case, a source select gate electrode can be subsequently formed by replacing the bottommost sacrificial material layer **42** with a conductive material layer. The III-V compound semiconductor pedestal **11** can be a portion of a transistor channel. The transistor channel extends between a source region to be subsequently formed on the III-V compound substrate semiconductor layer **930** and a drain region to be subsequently formed in an upper portion of the memory opening **49**. A memory cavity **49'** is present in the unfilled portion of the memory opening **49** above the III-V compound semiconductor pedestal **11**. In one embodiment, the III-V compound semiconductor pedestal **11** can have a doping of the first conductivity type, which is the same as the conductivity type of the III-V compound substrate semiconductor layer **930** that the III-V compound semiconductor pedestal **11** contacts. In one embodiment, the single crystalline III-V compound semiconductor material of the III-V compound semiconductor pedestals **11** may include p-type doped ("p-doped") GaAs or InGaAs.

[0093] Referring to FIG. **7**C, a stack of layers including a blocking dielectric layer **52**, a charge storage layer **54**, a tunneling dielectric layer **56**, and an optional first semiconductor channel layer **601** can be sequentially deposited in the memory openings **49**.

[0094] The blocking dielectric layer **52** can include a single dielectric material layer or a stack of a plurality of dielectric material layers. In one embodiment, the blocking dielectric layer can include a dielectric metal oxide layer consisting essentially of a dielectric metal oxide. As used herein, a dielectric metal oxide refers to a dielectric material that includes at least one metallic element and at least oxygen. The dielectric metal oxide may consist essentially of the at least one metallic element and oxygen, or may consist essentially of the at least one metallic element, oxygen, and at least one non-metallic element such as nitrogen. In one embodiment, the blocking dielectric layer **52** can include a dielectric metal oxide having a dielectric constant greater than 7.9, i.e., having a dielectric constant greater than the dielectric constant of silicon nitride. The thickness of the dielectric metal oxide layer can be in a range from 1 nm to 20 nm, although lesser and greater thicknesses can also be employed. The dielectric metal oxide layer can subsequently function as a dielectric material portion that blocks leakage of stored electrical charges to control gate electrodes. In one embodiment, the blocking dielectric layer **52** includes aluminum oxide. In one embodiment, the blocking dielectric layer **52** can include multiple dielectric metal oxide layers having different material compositions. Alternatively or additionally, the blocking dielectric layer **52** can include a dielectric semiconductor compound such as silicon oxide, silicon oxynitride, silicon nitride, or a combination thereof.

[0095] Subsequently, the charge storage layer **54** can be formed. In one embodiment, the charge storage layer **54** can be a continuous layer or patterned discrete portions of a charge trapping material including a dielectric charge trapping material, which can be, for example, silicon nitride. Alternatively, the charge storage layer **54** can include a continuous layer or patterned discrete portions of a conductive material such as doped polysilicon or a metallic material that is patterned into multiple electrically isolated portions (e.g., floating gates), for example, by being formed within lateral recesses into sacrificial material layers **42**. In one embodiment, the charge storage layer **54** includes a silicon nitride layer. In one embodiment, the sacrificial material layers **42** and the insulating layers **32** can have vertically coincident sidewalls, and the charge storage layer **54** can be formed as a single continuous layer.

[0096] In another embodiment, the sacrificial material layers **42** can be laterally recessed with respect to the sidewalls of the insulating layers **32**, and a combination of a deposition process and an anisotropic etch process can be employed to form the charge storage layer **54** as a plurality of memory material portions that are vertically spaced apart. While the present disclosure is described employing an embodiment in which the charge storage layer **54** is a single continuous layer, embodiments are expressly contemplated herein in which the charge storage layer **54** is replaced with a plurality of memory material portions (which can be charge trapping material portions or electrically isolated conductive material portions) that are vertically spaced apart. The charge storage layer **54** can be formed as a single charge storage layer of homogeneous composition, or can include a stack of multiple charge storage layers. The multiple charge storage layers, if employed, may, or may not, comprise a plurality of spaced-apart floating gate material layers that contain conductive materials and/or semiconductor materials. Alternatively or additionally, the charge storage layer **54** may comprise an insulating charge trapping material, such as one or more silicon nitride segments. Alternatively, the charge storage layer **54** may comprise conductive nanoparticles such as metal nanoparticles, which can be, for example, ruthenium nanoparticles. The charge storage layer **54** can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for storing electrical charges therein. The thickness of the charge storage layer **54** can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0097] The tunneling dielectric layer **56** includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The tunneling dielectric layer **56** can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the tunneling dielectric layer **56** can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO stack. In one embodiment, the tunneling dielectric layer **56** can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the tunneling dielectric layer **56** can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0098] The optional first semiconductor channel layer **601** includes a semiconductor material such as at least one III-V compound semiconductor material. The at least one III-V

compound semiconductor material has a doping of the first conductivity type, i.e., the same conductivity type as the conductivity type of the III-V compound substrate semiconductor layer **930** and the III-V compound semiconductor pedestals **11**. In one embodiment, the first semiconductor channel layer **601** includes p-doped GaAs or InGaAs. The first semiconductor channel layer **601** can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the first semiconductor channel layer **601** can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. A memory cavity **49'** is formed in the volume of each memory opening **49** that is not filled with the deposited material layers (**52**, **54**, **56**, **601**).

[0099] Referring to FIG. **7**D, the optional first semiconductor channel layer **601**, the tunneling dielectric layer **56**, the charge storage layer **54**, and the blocking dielectric layer **52** are sequentially anisotropically etched employing at least one anisotropic etch process. The portions of the first semiconductor channel layer **601**, the tunneling dielectric layer **56**, the charge storage layer **54**, and the blocking dielectric layer **52** located above the top surface of the insulating cap layer **70** can be removed by the at least one anisotropic etch process. Further, the horizontal portions of the first semiconductor channel layer **601**, the tunneling dielectric layer **56**, the charge storage layer **54**, and the blocking dielectric layer **52** at a bottom of each memory cavity **49'** can be removed to form openings in remaining portions thereof. Each of the first semiconductor channel layer **601**, the tunneling dielectric layer **56**, the charge storage layer **54**, and the blocking dielectric layer **52** can be etched by a respective anisotropic etch process employing a respective etch chemistry, which may, or may not, be the same for the various material layers.

[0100] Each remaining portion of the first semiconductor channel layer **601** can have a tubular configuration. The charge storage layer **54** can comprise a charge trapping material or a floating gate material. In one embodiment, each charge storage layer **54** can include a vertical stack of charge storage regions that store electrical charges upon programming. In one embodiment, the charge storage layer **54** can be a charge storage layer in which each portion adjacent to the sacrificial material layers **42** constitutes a charge storage region.

[0101] A surface of the III-V compound semiconductor pedestal **11** (or a surface of the III-V compound substrate semiconductor layer **930** in case the III-V compound semiconductor pedestals **11** are not employed) can be physically exposed underneath the opening through the first semiconductor channel layer **601**, the tunneling dielectric layer **56**, the charge storage layer **54**, and the blocking dielectric layer **52**. Optionally, the physically exposed semiconductor surface at the bottom of each memory cavity **49'** can be vertically recessed so that the recessed semiconductor surface underneath the memory cavity **49'** is vertically offset from the topmost surface of the III-V compound semiconductor pedestal **11** (or of the III-V compound substrate semiconductor layer **930** in case III-V compound semiconductor pedestals **11** are not employed) by a recess distance. A tunneling dielectric layer **56** is located over the charge storage layer **54**. A set of a blocking dielectric layer **52**, a charge storage layer **54**, and a tunneling dielectric layer **56** in a memory opening **49** constitutes a memory film **50**, which includes a plurality of charge storage regions (comprising the charge storage layer **54**) that are insulated from surrounding materials by the blocking dielectric layer **52** and the tunneling dielectric layer **56**. In one embodiment, the first semiconductor channel layer **601**, the tunneling dielectric layer **56**, the charge storage layer **54**, and the blocking dielectric layer **52** can have vertically coincident sidewalls.

[0102] Referring to FIG. **7**E, a second semiconductor channel layer **602** can be deposited directly on the semiconductor surfaces of the III-V compound semiconductor pedestal **11** (or the III-V compound substrate semiconductor layer **930** if the III-V compound semiconductor pedestal **11** is omitted), and directly on the first semiconductor channel layer **601**. The second semiconductor channel layer **602** includes at least one III-V compound semiconductor material. In one embodiment, the second semiconductor channel layer **602** includes the same III-V compound semiconductor material as the first semiconductor channel layer **601**. The second semiconductor channel layer **602** can have a doping of the first conductivity type. For example, the second semiconductor channel layer **602** can include p-doped GaAs or InGaAs. The second semiconductor channel layer **602** can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the second semiconductor channel layer **602** can be in a range from 2 nm to 10 nm, although lesser and greater thicknesses can also be employed. The second semiconductor channel layer **602** may partially fill the memory cavity **49'** in each memory opening, or may fully fill the cavity in each memory opening.

[0103] The materials of the first semiconductor channel layer **601** and the second semiconductor channel layer **602** are collectively referred to as a semiconductor channel material, which may be a polycrystalline III-V compound semiconductor material. In other words, the semiconductor channel material is a set of all semiconductor material in the first semiconductor channel layer **601** and the second semiconductor channel layer **602**.

[0104] Referring to FIG. **7**F, in case the memory cavity **49'** in each memory opening is not completely filled by the second semiconductor channel layer **602**, a dielectric core layer **62**L can be deposited in the memory cavity **49'** to fill any remaining portion of the memory cavity **49'** within each memory opening. The dielectric core layer **62**L includes a dielectric material such as silicon oxide or organosilicate glass. The dielectric core layer **62**L can be deposited by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD), or by a self-planarizing deposition process such as spin coating.

[0105] Referring to FIG. **7**G, the horizontal portion of the dielectric core layer **62**L can be removed, for example, by a recess etch from above the top surface of the second semiconductor channel layer **602**. Further, the material of the dielectric core layer **62**L can be vertically recessed selective to the semiconductor material of the second semiconductor channel layer **602** into each memory opening **49** down to a depth between a first horizontal plane including the top surface of the insulating cap layer **70** and a second horizontal plane including the bottom surface of the insulating cap layer **70**. Each remaining portion of the dielectric core layer **62**L constitutes a dielectric core **62**.

[0106] Referring to FIG. **7**H, portions of the first semiconductor channel layer **601** and the second semiconductor channel layer **602** that are located above the horizontal plane including the top surface of the dielectric core **62** can be

removed, for example, by performing a selective isotropic etch process that etches the semiconductor materials of the semiconductor channel layers (**601**, **602**) selective to the dielectric materials of the insulating cap layer **70** and the memory film **50**. Each remaining portion of the semiconductor channel layers (**601**, **602**) comprises a vertical semiconductor channel **60**. The III-V compound material of the vertical semiconductor channel **60** is herein referred to as a III-V compound semiconductor channel material. In one embodiment, the first semiconductor channel layer **601** and the second semiconductor channel layer **602** may have a same material composition. In another embodiment, an anneal process can be formed at this processing step or at a later processing step to homogenize the material composition in the vertical semiconductor channel **60**. In this case, the III-V compound semiconductor channel material of the vertical semiconductor channel **60** can have a fixed band gap, which is the band gap of the III-V compound semiconductor material of the vertical semiconductor channel **60**.

[0107] Referring to FIG. 7I, the dielectric core **62** can be vertically recess below the horizontal top surfaces of the vertical semiconductor channel **60**. The top surface of the dielectric core **62** may be recessed down to, or below, the horizontal plane including the top surface of the topmost sacrificial material layer **42**. Top portions of the inner sidewall of the second semiconductor channel layer **602** can be physically exposed to the recess region that is formed over the dielectric core **62**. The recess region can have an upper portion that is laterally bounded by the memory film **50** and a lower portion that is laterally bounded by the inner sidewall of the second semiconductor channel layer **602**.

[0108] Referring to FIG. 7J, a graded III-V compound semiconductor material layer **63**L can be deposited over the dielectric core **62**, the vertical semiconductor channel **60**, and the insulating cap layer **70**. In one embodiment, the graded III-V compound semiconductor material layer **63**L includes a layer stack of at least two discrete III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) having different material compositions and having a doping of a second conductivity type that is the opposite of the first conductivity type. Specifically, the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) may include at least two III-V compound semiconductor material layers such as three or more III-V compound semiconductor material layers having a respective band gap. The band gaps of the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) are selected such that the band gap of the first III-V compound semiconductor material layer **63**A that is deposited directly on the vertical semiconductor channel **60** may substantially match or be slightly greater than the band gap of the vertical semiconductor channel **60**. Subsequently deposited III-V compound semiconductor material layers (**63**B, **63**C, **63**D) have a respective band gap that is less than the band gap of any previously deposited III-V compound semiconductor material layer.

[0109] In an illustrative example, the III-V compound semiconductor channel material of the vertical semiconductor channel **60** can include p-doped GaAs or InGaAs, and the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) can include a first III-V compound semiconductor material layer **63**A including n-doped GaAs or InGaAs and having the same band gap or substantially the same band gap as the vertical semiconductor channel **60**. For example, if the vertical semiconductor layer **60** comprises p-doped GaAs, then the first III-V compound semiconductor material layer **63**A comprises n-doped GaAs or n-doped InGaAs having a formula $In_xGa_{1-x}As$, where $0<x<0.1$. If the vertical semiconductor layer **60** comprises p-doped InGaAs having a formula $In_yGa_{1-y}As$, then the first III-V compound semiconductor material layer **63**A comprises n-doped InGaAs having a formula $In_xGa_{1-x}As$, where $x>y$. The second III-V compound semiconductor material layer **63**B is deposited on the first III-V compound semiconductor material layer **63**A. The second III-V compound semiconductor material layer **63**B comprises a n-doped InGaAs which contains more indium than the vertical semiconductor layer **60** and the first III-V compound semiconductor material layer **63**A. For example, if the vertical semiconductor layer **60** comprises p-doped GaAs, then the second III-V compound semiconductor material layer **63**B comprises n-doped InGaAs having a formula $In_zGa_{1-z}As$, where $z>0.1$, such as $0.1<z<0.3$. If the vertical semiconductor layer **60** comprises p-doped InGaAs having a formula $In_yGa_{1-y}As$, then the second III-V compound semiconductor material layer **63**B comprises n-doped InGaAs having a formula $In_zGa_{1-z}As$, where $z>x>y$. The third III-V compound semiconductor material layer **63**C may be deposited on the second III-V compound semiconductor material layer **63**B. The third III-V compound semiconductor material layer **63**C comprises a n-doped InGaAs which contains more indium than the second III-V compound semiconductor material layer **63**B. The third III-V compound semiconductor material layer **63**C may have a formula $In_pGa_{1-p}As$, where $p>z$, for example $0.3<p<0.5$. The fourth III-V compound semiconductor material layer **63**D may be deposited on the third III-V compound semiconductor material layer **63**C. The fourth III-V compound semiconductor material layer **63**D comprises a n-doped InGaAs which contains more indium than the third III-V compound semiconductor material layer **63**C. The fourth III-V compound semiconductor material layer **63**D may have a formula $In_qGa_{1-q}As$, where $q>p$, for example $0.5<q<0.7$. Generally, the III-V compound semiconductor material of each successive III-V compound semiconductor material layer can be selected such that the band gap of each subsequently deposited III-V compound semiconductor material layer decreases relative to the band gap of an immediately preceding III-V compound semiconductor material layer.

[0110] While the present disclosure is described employing an embodiment in which the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) include four III-V compound semiconductor material layers, two, three, four, or more layers can be included in the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D). Further, while an example in which the vertical semiconductor channel **60** includes n-doped GaAs or InGaAs, embodiments are expressly contemplated herein in which the vertical semiconductor channel **60** includes any III-V compound semiconductor material having a doping of a first conductivity type and having a fixed band gap. The III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) include any number of III-V compound semiconductor material layers. The III-V compound semiconductor material layer **63**L may be deposited by non-selective III-V compound semiconductor deposition processes (such as chemical vapor deposition processes without concurrent flow of an etchant gas such as HCl), or by selective III-V compound semiconductor deposition process (such as

chemical vapor deposition processes employing concurrent or alternating flow of an etchant gas).

[0111] The first III-V compound semiconductor material layer **63**A that contacts the vertical semiconductor channel **60** has the same band gap as, or has substantially the same band gap as, the vertical semiconductor channel **60**. Each subsequently deposited layer within the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) has a lesser band gaps relative to the band gap of a respective preceding III-V compound semiconductor material layer. The layers in the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) can have a doping of a second conductivity type that is the opposite of the first conductivity type. The thickness of each layer within the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) can be selected such that each interface between layers within the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) extends below the horizontal plane including the top surface of the vertical semiconductor channel **60**. The total thickness of the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) can be selected that the entire volume of the recess region overlying the vertical semiconductor channel **60** is filled with the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D).

[0112] While the present disclosure is described employing an embodiment in which the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) are formed as discrete material layers, embodiments are expressly contemplated herein in which a single continuously graded III-V compound semiconductor material layer **63**L replaces the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D). In this case, the continuously graded III-V compound semiconductor material layer has a composition gradient that provides a continuously decreasing band gap as a function of a distance from the interface with the vertical semiconductor channel **60**. For example, the continuously graded III-V compound semiconductor material layer may include an InGaAs layer in which the atomic concentration of indium continuously increases as a function of a distance from the interface with the vertical semiconductor channel. The atomic concentration of indium in the continuously graded III-V compound semiconductor material layer may increase, for example, from 0% to 10% at the interface to a range from 50% to 100% at a distal portion of the continuously graded III-V compound semiconductor material layer. The graded III-V compound semiconductor material layer **63**L includes a continuously decreasing band gap from the vertical semiconductor channel **60** to the top of the layer **63**L. Thus, in this embodiment, layer **63**L may be an InGaAs layer of a second conductivity type (e.g., n-doped InGaAs layer) having a continuously increasing indium content and a continuously decreasing gallium content starting from the interface with the vertical semiconductor channel and ending at the top surface of layer **63**L. In one embodiment, the bottom surface of layer **63**L may comprise a gallium rich InGaAs material or a GaAs material which contains essentially no indium. In one embodiment, the top surface of layer **63**L may comprise an indium rich InGaAs material which has a higher indium content than the gallium rich InGaAs material, or an InAs material which contains essentially no gallium.

[0113] Referring to FIG. **7**K, portions of the III-V compound semiconductor material layer **63**L located above the horizontal plane including the top surface of the insulating cap layer **70** can be removed by performing a planarization process. For example, a chemical mechanical planarization process can be performed to remove portions of the III-V compound semiconductor material layer **63**L located above the horizontal plane including the top surface of the insulating cap layer **70**. Each remaining portion of the III-V compound semiconductor material layer **63**L that fills a recess region and contacts a respective one of the vertical semiconductor channels **60** comprises a drain region **63**. Each drain region **63** can include either plural layers of the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) or one single continuously graded III-V compound semiconductor material layer.

[0114] Each drain region **63** is formed at an upper end of a respective vertical semiconductor channel **60**. The III-V compound semiconductor pedestals **11**, the vertical semiconductor channels **60**, and the III-V compound substrate semiconductor layer **930** have a doping of the first conductivity type, and each drain region **63** has a doping of the second conductivity type that is the opposite of the first conductivity type. Each drain region has a compositional gradient therein. The III-V compound semiconductor material layer(s) within each drain region **63** incudes a variable band gap (e.g., different discrete band gaps or a continuously graded band gap) that decrease with a distance from an interface between the drain region **63** and the vertical semiconductor channel **60**.

[0115] According to an aspect of the present disclosure, the vertical semiconductor channel **60** within each memory opening **49** comprises a III-V compound semiconductor channel material. In one embodiment, the III-V compound semiconductor channel material has a fixed band gap that is uniform throughout the vertical semiconductor channel **60**. The drain region **63** within each memory opening **49** has a variable band gap that varies within the drain region **63**. In one embodiment, the variable band gap of the drain region **63** can monotonically decrease within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. The distance may be measured vertically from a horizontal interface, or may be measured horizontally from a vertical interface. As used herein, a quantity "monotonically decreases" with a parament if the value of the quantity does not increase for any increase in the parameter. In one embodiment, the variable band gap of the drain region **63** can decrease continuously or stepwise within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. As used herein, a quantity "decreases stepwise" with a parament if the value of the quantity decreases in steps as the value of the parameter increases.

[0116] In one embodiment, the III-V compound semiconductor channel material comprises a doped gallium arsenide channel material, and the drain region **63** comprises a layer stack including a doped gallium arsenide drain layer (which may comprise a first III-V compound semiconductor material layer **63**A) and at least one doped indium gallium arsenide layer (which may be comprise one or more additional III-V compound semiconductor material layers (**63**B, **63**C, **63**D). In one embodiment, the drain region **63** comprises a plurality of doped indium gallium arsenide layers including indium atoms at different atomic indium percentages. In one embodiment, the difference between the variable band gap of the drain region **63** and the fixed band gap of the vertical semiconductor channel **60** monotonically

increases within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. In one embodiment, the vertical semiconductor channel **60** comprises a cylindrical inner sidewall, a cylindrical outer sidewall, and an annular top surface extending between the cylindrical inner sidewall and the cylindrical outer sidewall. The drain region **63** contacts the annular top surface and an upper portion of the cylindrical inner sidewall of the vertical semiconductor channel **60**. The dopant concentration of dopants of the second conductivity type in the drain region **63** can be in a range from $5.0\times10^{18}/cm^3$ to $2.0\times10^{21}/cm^3$, although lesser and greater dopant concentrations can also be employed.

[0117] Each adjoining pair of a first semiconductor channel layer **601** and a second semiconductor channel layer **602** can collectively form a vertical semiconductor channel **60** through which electrical current can flow when a vertical NAND device including the vertical semiconductor channel **60** is turned on. A tunneling dielectric layer **56** is surrounded by a charge storage layer **54**, and laterally surrounds a portion of the vertical semiconductor channel **60**. Each adjoining set of a tunneling dielectric layer **56**, a charge storage layer **54**, and a blocking dielectric layer **52** collectively constitute a memory film **50**, which includes a vertical stack of memory elements that can store a respective data bit with a macroscopic retention time. As used herein, a macroscopic retention time refers to a retention time suitable for operation of a memory device as a permanent memory device such as a retention time in excess of 24 hours. In alternative embodiments, a blocking dielectric layer **52** may not be formed in each memory opening **49**, and may be subsequently formed in backside recesses that are formed by removal of the sacrificial material layers **42** at a subsequent processing step.

[0118] Each combination of a memory film **50** and a vertical semiconductor channel **60** within a memory opening **49** constitutes a memory stack structure **55**. The memory stack structure **55** is a combination of a semiconductor channel **60**, a tunneling dielectric layer **56**, a plurality of memory elements as embodied as portions of the charge storage layer **54**, and a blocking dielectric layer **52**. Each combination of a III-V compound semiconductor pedestal **11** (if present), a memory stack structure **55**, a dielectric core **62**, and a drain region **63** within a memory opening **49** is herein referred to as a memory opening fill structure **58**. Each combination of a III-V compound semiconductor pedestal **11** (if present), a memory film **50**, a vertical semiconductor channel **60**, a dielectric core **62**, and a drain region **63** within each support opening **19** fills the respective support openings **19**, and constitutes a support pillar structure.

[0119] Referring to FIG. **8**, the exemplary structure is illustrated after formation of memory opening fill structures **58** and support pillar structure **20** within the memory openings **49** and the support openings **19**, respectively. An instance of a memory opening fill structure **58** can be formed within each memory opening **49** of the structure of FIGS. **6**A and **6**B. An instance of the support pillar structure **20** can be formed within each support opening **19** of the structure of FIGS. **6**A and **6**B.

[0120] Each memory stack structure **55** includes a vertical semiconductor channel **60**, which may comprise multiple semiconductor channel layers (**601**, **602**), and a memory film **50**. The memory film **50** may comprise a tunneling dielectric layer **56** laterally surrounding the vertical semiconductor channel **60**, a vertical stack of charge storage regions (comprising charge storage layer **54**) laterally surrounding the tunneling dielectric layer **56**, and an optional blocking dielectric layer **52**. While the present disclosure is described employing the illustrated configuration for the memory stack structure, the methods of the present disclosure can be applied to alternative memory stack structures including different layer stacks or structures for the memory film **50** and/or for the vertical semiconductor channel **60**.

[0121] Referring to FIGS. **9**A-**9**C, a contact level dielectric layer **73** can be formed over the alternating stack (**32**, **42**) of insulating layer **32** and sacrificial material layers **42**, and over the memory stack structures **55** and the support pillar structures **20**. The contact level dielectric layer **73** includes a dielectric material that is different from the dielectric material of the sacrificial material layers **42**. For example, the contact level dielectric layer **73** can include silicon oxide. The contact level dielectric layer **73** can have a thickness in a range from 50 nm to 500 nm, although lesser and greater thicknesses can also be employed.

[0122] A photoresist layer (not shown) can be applied over the contact level dielectric layer **73**, and is lithographically patterned to form openings in areas between clusters of memory stack structures **55**. The pattern in the photoresist layer can be transferred through the contact level dielectric layer **73**, the alternating stack (**32**, **42**) and/or the retro-stepped dielectric material portion **65** employing an anisotropic etch to form backside trenches **79**, which vertically extend from the top surface of the contact level dielectric layer **73** at least to the top surface of the substrate (**9**, **10**), and laterally extend through the memory array region **100** and the staircase region **300**.

[0123] In one embodiment, the backside trenches **79** can laterally extend along a first horizontal direction hd**1** and can be laterally spaced apart among one another along a second horizontal direction hd**2** that is perpendicular to the first horizontal direction hd**1**. The memory stack structures **55** can be arranged in rows that extend along the first horizontal direction hd**1**. The drain select level isolation structures **72** can laterally extend along the first horizontal direction hd**1**. Each backside trench **79** can have a uniform width that is invariant along the lengthwise direction (i.e., along the first horizontal direction hd**1**). Each drain select level isolation structure **72** can have a uniform vertical cross-sectional profile along vertical planes that are perpendicular to the first horizontal direction hd**1** that is invariant with translation along the first horizontal direction hd**1**. Multiple rows of memory stack structures **55** can be located between a neighboring pair of a backside trench **79** and a drain select level isolation structure **72**, or between a neighboring pair of drain select level isolation structures **72**. In one embodiment, the backside trenches **79** can include a source contact opening in which a source contact via structure can be subsequently formed. A top surface of the III-V compound substrate semiconductor layer **930** is physically exposed at the bottom of each backside trench **79**. The photoresist layer can be removed, for example, by ashing.

[0124] Referring to FIG. **10**, a III-V compound semiconductor source region **75** can be formed in each backside trench **79** by performing a series of selective III-V compound deposition processes. Each III-V compound semiconductor source region **75** includes a graded III-V compound semiconductor material layer, which may comprise a single

continuously graded III-V compound semiconductor material layer or a layer stack including at least two discrete III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) having different material compositions and having a doping of the second conductivity type that is the opposite of the first conductivity type. Specifically, the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) may include at least two III-V compound semiconductor material layers such as three or more III-V compound semiconductor material layers having a respective band gap. The band gaps of the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) are selected that the band gap of a first III-V compound semiconductor material layer **75**A that is deposited directly on the III-V compound substrate semiconductor layer **930** substantially matches or is slightly smaller than the band gap of the III-V compound substrate semiconductor layer **930**. Subsequently deposited III-V compound semiconductor material layers (**75**B, **75**C, **75**D) have a respective band gap that is less than the band gap of any previously deposited III-V compound semiconductor material layer. The III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) may be deposited by selective III-V compound semiconductor deposition processes (such as chemical vapor deposition processes employing concurrent or alternating flow of an etchant gas).

[0125] In an illustrative example, the III-V compound semiconductor channel material of the substrate semiconductor layer **930** can include p-doped GaAs or InGaAs, and the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) can include a first III-V compound semiconductor material layer **75**A including n-doped GaAs or InGaAs and having the same band gap or substantially the same band gap as the substrate semiconductor layer **930**. For example, if the substrate semiconductor layer **930** comprises p-doped GaAs, then the first III-V compound semiconductor material layer **75**A comprises n-doped GaAs or n-doped InGaAs having a formula $In_xGa_{1-x}As$, where $0<x<0.1$. If the substrate semiconductor layer **930** comprises p-doped InGaAs having a formula $In_yGa_{1-y}As$, then the first III-V compound semiconductor material layer **75**A comprises n-doped InGaAs having a formula $In_xGa_{1-x}As$, where $x>y$. The second III-V compound semiconductor material layer **75**B is deposited on the first III-V compound semiconductor material layer **75**A. The second III-V compound semiconductor material layer **75**B comprises a n-doped InGaAs which contains more indium than the substrate semiconductor layer **930** and the first III-V compound semiconductor material layer **75**A. For example, if the substrate semiconductor layer **930** comprises p-doped GaAs, then the second III-V compound semiconductor material layer **75**B comprises n-doped InGaAs having a formula $In_zGa_{1-z}As$, where $z>0.1$, such as $0.1<z<0.3$. If the substrate semiconductor layer **930** comprises p-doped InGaAs having a formula $In_yGa_{1-y}As$, then the second III-V compound semiconductor material layer **75**B comprises n-doped InGaAs having a formula $In_zGa_{1-z}As$, where $z>x>y$. The third III-V compound semiconductor material layer **75**C may be deposited on the second III-V compound semiconductor material layer **75**B. The third III-V compound semiconductor material layer **75**C comprises a n-doped InGaAs which contains more indium than the second III-V compound semiconductor material layer **75**B. The third III-V compound semiconductor material layer **75**C may have a formula $In_pGa_{1-p}As$, where $p>z$, for example $0.3<p<0.5$. The fourth III-V compound semiconductor material layer **75**D may be deposited on the third III-V compound semiconductor material layer **75**C. The fourth III-V compound semiconductor material layer **75**D comprises a n-doped InGaAs which contains more indium than the third III-V compound semiconductor material layer **75**C. The fourth III-V compound semiconductor material layer **75**D may have a formula $In_qGa_{1-q}As$, where $q>p$, for example $0.5<q<0.7$. Generally, the III-V compound semiconductor material of each successive III-V compound semiconductor material layer can be selected such that the band gap of each subsequently deposited III-V compound semiconductor material layer decreases relative to the band gap of an immediately preceding III-V compound semiconductor material layer.

[0126] While the present disclosure is described employing an embodiment in which the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) include four III-V compound semiconductor material layers, two, three, four, or more layers can be included in the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D). Further, while an example in which each source region **75** includes n-doped GaAs or InGaAs, embodiments are expressly contemplated herein in which each source region **75** includes any III-V compound semiconductor material having a doping of the second conductivity type and having a variable band gap that increases stepwise or continuously with a vertical distance from an interface with the III-V compound substrate semiconductor layer **930**. Generally, the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) include any number of III-V compound semiconductor material layers. The first III-V compound semiconductor material layer **75**A that contacts the vertical semiconductor channel **60** has the same band gap as, or has substantially the same band gap as, the vertical semiconductor channel **60**. Each subsequently deposited layer within the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) has a lesser band gaps relative to the band gap of a respective preceding III-V compound semiconductor material layer. The layers in the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) can have a doping of the second conductivity type. The thickness of each source region **75** can be in a range from 20 nm to 60 nm, and top surface of each source region **75** can be at, or below, the top surface of the bottommost insulating layer **32**.

[0127] While an embodiment in which the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D) are formed as discrete material layers is described above, embodiments are expressly contemplated herein in which a single continuously graded III-V compound semiconductor material layer replaces the III-V compound semiconductor material layers (**75**A, **75**B, **75**C, **75**D). In this case, the continuously graded III-V compound semiconductor material layer has a composition gradient that provides a continuously decreasing band gap as a function of a distance from the interface with the III-V compound substrate semiconductor layer **930**. For example, the continuously graded III-V compound semiconductor material layer may include an InGaAs layer in which the atomic concentration of indium continuously increases as a function of a distance from the interface with the III-V compound substrate semiconductor layer **930**. The atomic concentration of indium in the continuously graded III-V compound semiconductor material layer may increase, for example, from 0% to 10%

at the interface to a range from 50% to 100% at a distal portion of the continuously graded III-V compound semiconductor material layer.

[0128] Generally, each source region **75** can be formed as a III-V compound semiconductor source region comprising a doped III-V compound material, and can be formed on the top surface of the III-V compound substrate semiconductor layer **930**. The III-V compound semiconductor source region comprises a graded III-V compound semiconductor material having a vertical compositional gradient that provides a variable band gap (e.g., varying continuously or step wise) that decreases with a vertical distance from an interface with the III-V compound substrate semiconductor layer **930**. The vertical composition gradient may be stepwise (i.e., including stepwise changes in composition) or may be gradual (i.e., including a continuous change in composition).

[0129] An upper portion of the III-V compound substrate semiconductor layer **930** that extends between the source region **75** and the plurality of III-V compound semiconductor pedestals **11** constitutes a horizontal semiconductor channel **59** for a plurality of field effect transistors. The horizontal semiconductor channel **59** is connected to multiple vertical semiconductor channels **60** through respective III-V compound semiconductor pedestals **11**. The horizontal semiconductor channel **59** contacts the source region **75** and the plurality of III-V compound semiconductor pedestals **11**.

[0130] Referring to FIGS. **11**A and **11**B, an etchant that selectively etches the second material of the sacrificial material layers **42** with respect to the first material of the insulating layers **32** can be introduced into the backside trenches **79**, for example, employing an etch process. Backside recesses **43** are formed in volumes from which the sacrificial material layers **42** are removed. The removal of the second material of the sacrificial material layers **42** can be selective to the first material of the insulating layers **32**, the material of the retro-stepped dielectric material portion **65**, the semiconductor material of the III-V compound substrate semiconductor layer **930**, and the material of the outermost layer of the memory films **50**. In one embodiment, the sacrificial material layers **42** can include silicon nitride, and the materials of the insulating layers **32** and the retro-stepped dielectric material portion **65** can be selected from silicon oxide and dielectric metal oxides.

[0131] The etch process that removes the second material (i.e., the spacer material such as the material of the sacrificial material layers **42**) selective to the first material and the outermost layer of the memory films **50** can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside trenches **79**. For example, if the sacrificial material layers **42** include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The support pillar structures **20**, the retro-stepped dielectric material portion **65**, and the memory stack structures **55** provide structural support while the backside recesses **43** are present within volumes previously occupied by the sacrificial material layers **42**.

[0132] Each backside recess **43** can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each backside recess **43** can be greater than the height of the backside recess **43**. A plurality of backside recesses **43** can be formed in the volumes from which the second material of the sacrificial material layers **42** is removed. The memory openings in which the memory stack structures **55** are formed are herein referred to as front side openings or front side cavities in contrast with the backside recesses **43**. In one embodiment, the memory array region **100** comprises an array of monolithic three-dimensional NAND strings having a plurality of device levels disposed above the III-V compound substrate semiconductor layer **930**. In this case, each backside recess **43** can define a space for receiving a respective word line of the array of monolithic three-dimensional NAND strings.

[0133] Each of the plurality of backside recesses **43** can extend substantially parallel to the top surface of the III-V compound substrate semiconductor layer **930**. A backside recess **43** can be vertically bounded by a top surface of an underlying insulating layer **32** and a bottom surface of an overlying insulating layer **32**. In one embodiment, each backside recess **43** can have a uniform height throughout.

[0134] Referring to FIG. **12**A, physically exposed surface portions of the optional III-V compound semiconductor pedestals **11** and the III-V compound substrate semiconductor layer **930** can be converted into dielectric material portions by thermal conversion and/or plasma conversion of the semiconductor materials into dielectric materials. For example, thermal conversion and/or plasma conversion can be employed to convert a surface portion of each III-V compound semiconductor pedestal **11** into a tubular dielectric spacer **116**, and to convert each physically exposed surface portion of the III-V compound substrate semiconductor layer **930** into a planar dielectric portion **616**. In one embodiment, each tubular dielectric spacer **116** can be topologically homeomorphic to a torus, i.e., generally ring-shaped. As used herein, an element is topologically homeomorphic to a torus if the shape of the element can be continuously stretched without destroying a hole or forming a new hole into the shape of a torus. The tubular dielectric spacers **116** include a dielectric material that includes the same semiconductor element as the III-V compound semiconductor pedestals **11** and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the tubular dielectric spacers **116** is a dielectric material. In one embodiment, the tubular dielectric spacers **116** can include a dielectric oxide derived from the semiconductor material of the III-V compound semiconductor pedestals **11**. For example, the tubular dielectric spacers **116** can comprise, and/or can consist essentially of, gallium oxide. In one embodiment, the planar dielectric portions **616** can include a dielectric oxide derived from the semiconductor material of the III-V compound substrate semiconductor layer **930**. For example, the planar dielectric portions **616** can comprise, and/or can consist essentially of, indium oxide or indium gallium oxide. Dopants in the drain regions **63**, the source regions **75**, and the semiconductor channels **60** can be activated during the anneal process that forms the planar dielectric portions **616** and the tubular dielectric spacers **116**. Alternatively, an additional anneal process may be performed to active the electrical dopants in the drain regions **63**, the source regions **75**, and the semiconductor channels **60**.

[0135] Referring to FIG. **12**B, a backside blocking dielectric layer **44** can be optionally formed. The backside blocking dielectric layer **44**, if present, comprises a dielectric

material that functions as a control gate dielectric for the control gates to be subsequently formed in the backside recesses **43**. In case the blocking dielectric layer **52** is present within each memory opening, the backside blocking dielectric layer **44** is optional. In case the blocking dielectric layer **52** is omitted, the backside blocking dielectric layer **44** is present.

[0136] The backside blocking dielectric layer **44** can be formed in the backside recesses **43** and on a sidewall of the backside trench **79**. The backside blocking dielectric layer **44** can be formed directly on horizontal surfaces of the insulating layers **32** and sidewalls of the memory stack structures **55** within the backside recesses **43**. If the backside blocking dielectric layer **44** is formed, formation of the tubular dielectric spacers **116** and the planar dielectric portion **616** prior to formation of the backside blocking dielectric layer **44** is optional. In one embodiment, the backside blocking dielectric layer **44** can be formed by a conformal deposition process such as atomic layer deposition (ALD). The backside blocking dielectric layer **44** can consist essentially of aluminum oxide. The thickness of the backside blocking dielectric layer **44** can be in a range from 1 nm to 15 nm, such as 2 to 6 nm, although lesser and greater thicknesses can also be employed.

[0137] The dielectric material of the backside blocking dielectric layer **44** can be a dielectric metal oxide such as aluminum oxide, a dielectric oxide of at least one transition metal element, a dielectric oxide of at least one Lanthanide element, a dielectric oxide of a combination of aluminum, at least one transition metal element, and/or at least one Lanthanide element. Alternatively or additionally, the backside blocking dielectric layer **44** can include a silicon oxide layer. The backside blocking dielectric layer **44** can be deposited by a conformal deposition method such as chemical vapor deposition or atomic layer deposition. The backside blocking dielectric layer **44** is formed on the sidewalls of the backside trenches **79**, horizontal surfaces and sidewalls of the insulating layers **32**, the portions of the sidewall surfaces of the memory stack structures **55** that are physically exposed to the backside recesses **43**, and a top surface of the planar dielectric portion **616**. A backside cavity **79'** is present within the portion of each backside trench **79** that is not filled with the backside blocking dielectric layer **44**.

[0138] Referring to FIG. **13**, a metallic barrier layer **46**A can be deposited in the backside recesses **43**. The metallic barrier layer **46**A includes an electrically conductive metallic material that can function as a diffusion barrier layer and/or adhesion promotion layer for a metallic fill material to be subsequently deposited. The metallic barrier layer **46**A can include a conductive metallic nitride material such as TiN, TaN, WN, or a stack thereof, or can include a conductive metallic carbide material such as TiC, TaC, WC, or a stack thereof. In one embodiment, the metallic barrier layer **46**A can be deposited by a conformal deposition process such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). The thickness of the metallic barrier layer **46**A can be in a range from 2 nm to 8 nm, such as from 3 nm to 6 nm, although lesser and greater thicknesses can also be employed. In one embodiment, the metallic barrier layer **46**A can consist essentially of a conductive metal nitride such as TiN.

[0139] A metal fill material is deposited in the plurality of backside recesses **43**, on the sidewalls of the at least one the backside trench **79**, and over the top surface of the contact level dielectric layer **73** to form a metallic fill material layer **46**B. The metallic fill material can be deposited by a conformal deposition method, which can be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, or a combination thereof. In one embodiment, the metallic fill material layer **46**B can consist essentially of at least one elemental metal. The at least one elemental metal of the metallic fill material layer **46**B can be selected, for example, from tungsten, cobalt, ruthenium, titanium, and tantalum. In one embodiment, the metallic fill material layer **46**B can consist essentially of a single elemental metal. In one embodiment, the metallic fill material layer **46**B can be deposited employing a fluorine-containing precursor gas such as WF_6. In one embodiment, the metallic fill material layer **46**B can be a tungsten layer including a residual level of fluorine atoms as impurities. The metallic fill material layer **46**B is spaced from the insulating layers **32** and the memory stack structures **55** by the metallic barrier layer **46**A, which can block diffusion of fluorine atoms therethrough.

[0140] A plurality of electrically conductive layers **46** can be formed in the plurality of backside recesses **43**, and a continuous electrically conductive material layer **46**L can be formed on the sidewalls of each backside trench **79** and over the contact level dielectric layer **73**. Each electrically conductive layer **46** includes a portion of the metallic barrier layer **46**A and a portion of the metallic fill material layer **46**B that are located between a vertically neighboring pair of dielectric material layers such as a pair of insulating layers **32**. The continuous electrically conductive material layer **46**L includes a continuous portion of the metallic barrier layer **46**A and a continuous portion of the metallic fill material layer **46**B that are located in the backside trenches **79** or above the contact level dielectric layer **73**.

[0141] Each sacrificial material layer **42** can be replaced with an electrically conductive layer **46**. A backside cavity **79'** is present in the portion of each backside trench **79** that is not filled with the backside blocking dielectric layer **44** and the continuous electrically conductive material layer **46**L. A tubular dielectric spacer **116** laterally surrounds a III-V compound semiconductor pedestal **11**. A bottommost electrically conductive layer **46** laterally surrounds each tubular dielectric spacer **116** upon formation of the electrically conductive layers **46**.

[0142] Referring to FIGS. **14A-14**C, the deposited metallic material of the continuous electrically conductive material layer **46**L is etched back from the sidewalls of each backside trench **79** and from above the contact level dielectric layer **73**, for example, by an isotropic wet etch, an anisotropic dry etch, or a combination thereof. Each remaining portion of the deposited metallic material in the backside recesses **43** constitutes an electrically conductive layer **46**. Each electrically conductive layer **46** can be a conductive line structure. Thus, the sacrificial material layers **42** are replaced with the electrically conductive layers **46**.

[0143] Each electrically conductive layer **46** can function as a combination of a plurality of control gate electrodes located at a same level and a word line electrically interconnecting, i.e., electrically shorting, the plurality of control gate electrodes located at the same level. The plurality of control gate electrodes within each electrically conductive layer **46** are the control gate electrodes for the vertical memory devices including the memory stack structures **55**. In other words, each electrically conductive layer **46** can be

a word line that functions as a common control gate electrode for the plurality of vertical memory devices.

[0144] In one embodiment, the removal of the continuous electrically conductive material layer **46**L can be selective to the material of the backside blocking dielectric layer **44**. In this case, a horizontal portion of the backside blocking dielectric layer **44** can be present at the bottom of each backside trench **79**. In another embodiment, the removal of the continuous electrically conductive material layer **46**L may not be selective to the material of the backside blocking dielectric layer **44** or, the backside blocking dielectric layer **44** may not be employed. The planar dielectric portions **616** can be removed during removal of the continuous electrically conductive material layer **46**L. A backside cavity **79'** is present within each backside trench **79**.

[0145] Referring to FIG. **15**, an insulating material layer can be formed in the backside trenches **79** and over the contact level dielectric layer **73** by a conformal deposition process. Exemplary conformal deposition processes include, but are not limited to, chemical vapor deposition and atomic layer deposition. The insulating material layer includes an insulating material such as silicon oxide, silicon nitride, a dielectric metal oxide, an organosilicate glass, or a combination thereof. In one embodiment, the insulating material layer can include silicon oxide. The insulating material layer can be formed, for example, by low pressure chemical vapor deposition (LPCVD) or atomic layer deposition (ALD). The thickness of the insulating material layer can be in a range from 1.5 nm to 60 nm, although lesser and greater thicknesses can also be employed.

[0146] If a backside blocking dielectric layer **44** is present, the insulating material layer can be formed directly on surfaces of the backside blocking dielectric layer **44** and directly on the sidewalls of the electrically conductive layers **46**. If a backside blocking dielectric layer **44** is not employed, the insulating material layer can be formed directly on sidewalls of the insulating layers **32** and directly on sidewalls of the electrically conductive layers **46**.

[0147] An anisotropic etch is performed to remove horizontal portions of the insulating material layer from above the contact level dielectric layer **73** and at the bottom of each backside trench **79**. Each remaining portion of the insulating material layer constitutes an insulating spacer **74**. A backside cavity **79'** is present within a volume surrounded by each insulating spacer **74**. A top surface of the III-V compound substrate semiconductor layer **930** can be physically exposed at the bottom of each backside trench **79**.

[0148] A bottommost electrically conductive layer **46** provided upon formation of the electrically conductive layers **46** within the alternating stack (**32**, **46**) can comprise a select gate electrode for the field effect transistors. Each source region **75** is formed in an upper portion of the III-V compound substrate semiconductor layer **930**. Semiconductor channels (**59**, **11**, **60**) extend between each source region **75** and a respective set of drain regions **63**. The semiconductor channels (**59**, **11**, **60**) include the vertical semiconductor channels **60** of the memory stack structures **55**.

[0149] A backside contact via structure **76** can be formed within each backside cavity **79'**. Each backside contact via structure **76** can fill a respective backside cavity **79'**. The contact via structures **76** can be formed by depositing at least one conductive material in the remaining unfilled volume (i.e., the backside cavity **79'**) of the backside trench **79**. For example, the at least one conductive material can include a conductive liner **76**A and a conductive fill material portion **76**B. The conductive liner **76**A can include a conductive metal silicide and/or germanide, such as nickel germanosilicide, and/or a conductive metallic liner such as TiN, TaN, WN, TiC, TaC, WC, an alloy thereof, or a stack thereof. The thickness of the conductive liner **76**A can be in a range from 3 nm to 30 nm, although lesser and greater thicknesses can also be employed. The conductive fill material portion **76**B can include a metal or a metallic alloy. For example, the conductive fill material portion **76**B can include W, Cu, Al, Co, Ru, Ni, an alloy thereof, or a stack thereof.

[0150] The at least one conductive material can be planarized employing the contact level dielectric layer **73** overlying the alternating stack (**32**, **46**) as a stopping layer. If chemical mechanical planarization (CMP) process is employed, the contact level dielectric layer **73** can be employed as a CMP stopping layer. Each remaining continuous portion of the at least one conductive material in the backside trenches **79** constitutes a backside contact via structure **76**.

[0151] The backside contact via structure **76** extends through the alternating stack (**32**, **46**), and contacts a top surface of the source region **75**. If a backside blocking dielectric layer **44** is employed, the backside contact via structure **76** can contact a sidewall of the backside blocking dielectric layer **44**.

[0152] Referring to FIGS. **16**A and **16**B, additional contact via structures (**88**, **86**, **8**P) can be formed through the contact level dielectric layer **73**, and optionally through the retro-stepped dielectric material portion **65**. For example, drain contact via structures **88** can be formed through the contact level dielectric layer **73** on each drain region **63**. The drain contact via structures **88** may comprise a nickel germanosilicide layer which contacts the drain region **63** and a tungsten fill layer located on the nickel germanosilicide layer. Word line contact via structures **86** can be formed on the electrically conductive layers **46** through the contact level dielectric layer **73**, and through the retro-stepped dielectric material portion **65**. Peripheral device contact via structures **8**P can be formed through the retro-stepped dielectric material portion **65** directly on respective nodes of the peripheral devices.

[0153] Referring to FIGS. **1**-**16**B and according to various embodiments of the present disclosure, a three-dimensional memory device is provided, which comprises: a substrate comprising a III-V compound substrate semiconductor layer **930**; an alternating stack of insulating layers **32** and electrically conductive layers **46** located over the III-V compound substrate semiconductor layer **930**; a memory opening **49** vertically extending through the alternating stack (**32**, **46**); a memory opening fill structure **58** located in the memory opening **49** and comprising a III-V compound semiconductor pedestal **11** in contact with the III-V compound substrate semiconductor layer **930**, a vertical semiconductor channel **60**, and a memory film **50** located adjacent to the vertical semiconductor channel **60**.

[0154] In one embodiment, the substrate comprises a single crystalline silicon layer **9**; and a germanium-containing buffer layer **920** located on top of the single crystalline silicon layer **9**, wherein the III-V compound substrate semiconductor layer **930** is located over the germanium-containing buffer layer **920**. In one embodiment, the germanium-containing buffer layer **920** is epitaxially aligned to the single crystalline silicon layer **9**; and the III-V compound

substrate semiconductor layer **930** is epitaxially aligned to the germanium-containing buffer layer **920**. In one embodiment, the vertical semiconductor channel **60** comprises a III-V compound semiconductor channel material. In one embodiment, the III-V compound substrate semiconductor layer **930** is single crystalline; and the III-V compound semiconductor pedestal **11** is epitaxially aligned to the III-V compound substrate semiconductor layer **930**.

[0155] In one embodiment, a drain region **63** can be located at an upper end of the vertical semiconductor channel **60**. The III-V compound semiconductor pedestal **11** and the III-V compound substrate semiconductor layer **930** have a doping of a first conductivity type; and the drain region **63** has a doping of a second conductivity type that is an opposite of the first conductivity type.

[0156] In one embodiment, the III-V compound semiconductor channel material comprises polycrystalline gallium arsenide or indium gallium arsenide; and the drain region **63** comprises a graded III-V compound semiconductor material having a compositional gradient that provides a variable band gap that decreases with a distance from an interface with the vertical semiconductor channel **60**.

[0157] In one embodiment, a top surface of the III-V compound semiconductor pedestal **11** is located above a horizontal plane including a top surface of a bottommost one of the electrically conductive layers **46**. A tubular dielectric spacer **116** can laterally surround, and can contact, the III-V compound semiconductor pedestal **11**. The tubular dielectric spacer **116** can comprise, and/or can consist essentially of, an oxide of a III-V compound material of the III-V compound semiconductor pedestal **11**.

[0158] In one embodiment, the three-dimensional memory device comprises: a III-V compound semiconductor source region **75** comprising a doped III-V compound material and contacting a top surface of the III-V compound substrate semiconductor layer **930**; an insulating spacer **74** contacting sidewalls of the alternating stack (**32**, **46**); and a backside contact via structure **76** laterally surrounded by the insulating spacer **74** and contacting a top surface of the III-V compound semiconductor source region **75**. In one embodiment, a bottom surface of the insulating spacer **74** contacts a peripheral portion of a top surface of the III-V compound semiconductor source region **75**. In one embodiment, the III-V compound substrate semiconductor layer **930** comprises gallium arsenide; and the graded III-V compound semiconductor material of the drain **63** comprises a continuously or step wise graded indium gallium arsenide.

[0159] In one embodiment, the memory film **50** include a tunneling dielectric layer **56** contacting the vertical semiconductor channel **60**; a charge storage layer **54** in contact with the tunneling dielectric layer **56**; and a blocking dielectric layer **52** located between the charge storage layer **54** and the electrically conductive layers **46**.

[0160] In one embodiment, the alternating stack comprises a terrace region in which each electrically conductive layer **46** other than a topmost electrically conductive layer **46** within the alternating stack (**32**, **46**) laterally extends farther than any overlying electrically conductive layer **46** within the alternating stack (**32**, **46**). The terrace region comprises stepped surfaces of the alternating stack (**32**, **46**) that continuously extend from a bottommost layer within the alternating stack (**32**, **46**) to a topmost layer within the alternating stack (**32**, **46**). A retro-stepped dielectric material portion **65** can overlie the stepped surfaces. Contact via structures **86** can vertically extend through the retro-stepped dielectric material portion **65**, and can contact a top surface of a respective one of the electrically conductive layers **46**.

[0161] Referring to FIGS. **17**A and **17**B, a second exemplary structure according to a second embodiment of the present disclosure is illustrated. The second exemplary structure includes a substrate **8** and semiconductor devices **710** formed thereupon. The substrate **8** includes a substrate semiconductor layer **5** at least at an upper portion thereof. Shallow trench isolation structures **720** may be formed in an upper portion of the substrate semiconductor layer **5** to provide electrical isolation from other semiconductor devices. The semiconductor devices **710** may include, for example, field effect transistors including respective transistor active regions **742** (i.e., source regions and drain regions), channel regions **746**, and gate structures **750**. The field effect transistors may be arranged in a CMOS configuration. Each gate structure **750** may include, for example, a gate dielectric **752**, a gate electrode **754**, a dielectric gate spacer **756** and a gate cap dielectric **758**. The semiconductor devices **710** may include any semiconductor circuitry to support operation of a memory structure to be subsequently formed, which is typically referred to as a driver circuitry, which is also known as peripheral circuitry. As used herein, a peripheral circuitry refers to any, each, or all, of word line decoder circuitry, word line switching circuitry, bit line decoder circuitry, bit line sensing and/or switching circuitry, power supply/distribution circuitry, data buffer and/or latch, or any other semiconductor circuitry that may be implemented outside a memory array structure for a memory device. For example, the semiconductor devices may include word line switching devices for electrically biasing word lines of three-dimensional memory structures to be subsequently formed.

[0162] Dielectric material layers are formed over the semiconductor devices, which are herein referred to as lower-level dielectric material layers **760**. The lower-level dielectric material layers **760** may include, for example, a dielectric liner **762** (such as a silicon nitride liner that blocks diffusion of mobile ions and/or apply appropriate stress to underlying structures), first dielectric material layers **764** that overlie the dielectric liner **762**, a silicon nitride layer (e.g., hydrogen diffusion barrier) **766** that overlies the first dielectric material layers **764**, and at least one second dielectric material layer **768**.

[0163] The dielectric layer stack including the lower-level dielectric material layers **760** functions as a matrix for lower-level metal interconnect structures **780** that provide electrical wiring to and from the various nodes of the semiconductor devices and landing pads for through-memory-level contact via structures to be subsequently formed. The lower-level metal interconnect structures **780** are formed within the dielectric layer stack of the lower-level dielectric material layers **760**, and comprise a lower-level metal line structure located under and optionally contacting a bottom surface of the silicon nitride layer **766**.

[0164] For example, the lower-level metal interconnect structures **780** may be formed within the first dielectric material layers **764**. The first dielectric material layers **764** may be a plurality of dielectric material layers in which various elements of the lower-level metal interconnect structures **780** are sequentially formed. Each dielectric material layer selected from the first dielectric material layers **764** may include any of doped silicate glass, undoped silicate

glass, organosilicate glass, silicon nitride, silicon oxynitride, and dielectric metal oxides (such as aluminum oxide). In one embodiment, the first dielectric material layers **764** may comprise, or consist essentially of, dielectric material layers having dielectric constants that do not exceed the dielectric constant of undoped silicate glass (silicon oxide) of 3.9. The lower-level metal interconnect structures **780** may include various device contact via structures **782** (e.g., source and drain electrodes which contact the respective source and drain nodes of the device or gate electrode contacts), intermediate lower-level metal line structures **784**, lower-level metal via structures **786**, and landing-pad-level metal line structures **788** that are configured to function as landing pads for through-memory-level contact via structures to be subsequently formed.

[0165] The landing-pad-level metal line structures **788** may be formed within a topmost dielectric material layer of the first dielectric material layers **764** (which may be a plurality of dielectric material layers). Each of the lower-level metal interconnect structures **780** may include a metallic nitride liner and a metal fill structure. Top surfaces of the landing-pad-level metal line structures **788** and the topmost surface of the first dielectric material layers **764** may be planarized by a planarization process, such as chemical mechanical planarization. The silicon nitride layer **766** may be formed directly on the top surfaces of the landing-pad-level metal line structures **788** and the topmost surface of the first dielectric material layers **764**.

[0166] The at least one second dielectric material layer **768** may include a single dielectric material layer or a plurality of dielectric material layers. Each dielectric material layer selected from the at least one second dielectric material layer **768** may include any of doped silicate glass, undoped silicate glass, and organosilicate glass. In one embodiment, the at least one second dielectric material layer **768** may comprise, or consist essentially of, dielectric material layers having dielectric constants that do not exceed the dielectric constant of undoped silicate glass (silicon oxide) of 3.9.

[0167] The lower-level metal interconnect structures **780** may be electrically connected to active nodes (e.g., transistor active regions **742** or gate electrodes **754**) of the semiconductor devices **710** (e.g., CMOS devices), and are located at the level of the lower-level dielectric material layers **760**. Through-memory-level contact via structures may be subsequently formed directly on the lower-level metal interconnect structures **780** to provide electrical connection to memory devices to be subsequently formed. In one embodiment, the pattern of the lower-level metal interconnect structures **780** may be selected such that the landing-pad-level metal line structures **788** (which are a subset of the lower-level metal interconnect structures **780** located at the topmost portion of the lower-level metal interconnect structures **780**) may provide landing pad structures for the through-memory-level contact via structures to be subsequently formed.

[0168] A sacrificial source-level material layer **104** can be formed over the at least one second dielectric material layer **768**. The sacrificial source-level material layer **104** includes a sacrificial material that may be removed selective to the at least one second dielectric material layer **768**, which includes at least one dielectric material layer overlying the lower-level metal interconnect structures **780**. In one embodiment, the sacrificial source-level material layer **104** may include a semiconductor material such as undoped amorphous silicon or polysilicon. The thickness of the sacrificial source-level material layer **104** may be in a range from 30 nm to 400 nm, such as from 60 nm to 200 nm, although lesser and greater thicknesses may also be used.

[0169] The region of the semiconductor devices **710** and the combination of the lower-level dielectric material layers **760** and the lower-level metal interconnect structures **780** is herein referred to an underlying peripheral device region **700**, which is located underneath a memory-level assembly to be subsequently formed and includes peripheral devices for the memory-level assembly. The lower-level metal interconnect structures **780** are formed in the lower-level dielectric material layers **760**.

[0170] Referring to FIG. **18**, an alternating stack of first material layers and second material layers is subsequently formed. Each first material layer may include a first material, and each second material layer may include a second material that is different from the first material. In case at least another alternating stack of material layers is subsequently formed over the alternating stack of the first material layers and the second material layers, the alternating stack is herein referred to as a first-tier alternating stack. The level of the first-tier alternating stack is herein referred to as a first-tier level, and the level of the alternating stack to be subsequently formed immediately above the first-tier level is herein referred to as a second-tier level, etc.

[0171] The first-tier alternating stack may include first insulting layers **132** as the first material layers, and first spacer material layers as the second material layers. In one embodiment, the first spacer material layers may be sacrificial material layers that are subsequently replaced with electrically conductive layers. In another embodiment, the first spacer material layers may be electrically conductive layers that are not subsequently replaced with other layers. While the present disclosure is described using embodiments in which sacrificial material layers are replaced with electrically conductive layers, embodiments in which the spacer material layers are formed as electrically conductive layers (thereby obviating the need to perform replacement processes) are expressly contemplated herein.

[0172] In one embodiment, the first material layers and the second material layers may be first insulating layers **132** and first sacrificial material layers **142**, respectively. In one embodiment, each first insulating layer **132** may include a first insulating material, and each first sacrificial material layer **142** may include a first sacrificial material. An alternating plurality of first insulating layers **132** and first sacrificial material layers **142** is formed over the sacrificial source-level material layer **104**.

[0173] As used herein, an alternating stack of first elements and second elements refers to a structure in which instances of the first elements and instances of the second elements alternate. Each instance of the first elements that is not an end element of the alternating plurality is adjoined by two instances of the second elements on both sides, and each instance of the second elements that is not an end element of the alternating plurality is adjoined by two instances of the first elements on both ends. The first elements may have the same thickness throughout, or may have different thicknesses. The second elements may have the same thickness throughout, or may have different thicknesses. The alternating plurality of first material layers and second material layers may begin with an instance of the first material layers

or with an instance of the second material layers, and may end with an instance of the first material layers or with an instance of the second material layers. In one embodiment, an instance of the first elements and an instance of the second elements may form a unit that is repeated with periodicity within the alternating plurality.

[0174] The first-tier alternating stack (**132**, **142**) may include first insulating layers **132** composed of the first material, and first sacrificial material layers **142** composed of the second material, which is different from the first material. The first material of the first insulating layers **132** may be at least one insulating material. Insulating materials that may be used for the first insulating layers **132** include, but are not limited to silicon oxide (including doped or undoped silicate glass), silicon nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the first material of the first insulating layers **132** may be silicon oxide.

[0175] The second material of the first sacrificial material layers **142** is a sacrificial material that may be removed selective to the first material of the first insulating layers **132**. As used herein, a removal of a first material is "selective to" a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a "selectivity" of the removal process for the first material with respect to the second material.

[0176] The first sacrificial material layers **142** may comprise an insulating material, a semiconductor material, or a conductive material. The second material of the first sacrificial material layers **142** may be subsequently replaced with electrically conductive electrodes which may function, for example, as control gate electrodes of a vertical NAND device. In one embodiment, the first sacrificial material layers **142** may be material layers that comprise silicon nitride.

[0177] In one embodiment, the first insulating layers **132** may include silicon oxide, and sacrificial material layers may include silicon nitride sacrificial material layers. The first material of the first insulating layers **132** may be deposited, for example, by chemical vapor deposition (CVD). For example, if silicon oxide is used for the first insulating layers **132**, tetraethylorthosilicate (TEOS) may be used as the precursor material for the CVD process. The second material of the first sacrificial material layers **142** may be formed, for example, CVD or atomic layer deposition (ALD).

[0178] The thicknesses of the first insulating layers **132** and the first sacrificial material layers **142** may be in a range from 20 nm to 50 nm, although lesser and greater thicknesses may be used for each first insulating layer **132** and for each first sacrificial material layer **142**. The number of repetitions of the pairs of a first insulating layer **132** and a first sacrificial material layer **142** may be in a range from 2 to 1,024, and typically from 8 to 256, although a greater number of repetitions may also be used. In one embodiment, each first sacrificial material layer **142** in the first-tier alternating stack (**132**, **142**) may have a uniform thickness that is substantially invariant within each respective first sacrificial material layer **142**.

[0179] A first insulating cap layer **170** is subsequently formed over the first alternating stack (**132**, **142**). The first insulating cap layer **170** includes a dielectric material, which may be any dielectric material that may be used for the first insulating layers **132**. In one embodiment, the first insulating cap layer **170** includes the same dielectric material as the first insulating layers **132**. The thickness of the first insulating cap layer **170** may be in a range from 20 nm to 300 nm, although lesser and greater thicknesses may also be used.

[0180] Referring to FIG. **19**, the first insulating cap layer **170** and the first-tier alternating stack (**132**, **142**) may be patterned to form first stepped surfaces in the staircase region **300**. The staircase region **300** may include a respective first stepped area in which the first stepped surfaces are formed, and a second stepped area in which additional stepped surfaces are to be subsequently formed in a second-tier structure (to be subsequently formed over a first-tier structure) and/or additional tier structures. The first stepped surfaces may be formed, for example, by forming a mask layer (not shown) with an opening therein, etching a cavity within the levels of the first insulating cap layer **170**, and iteratively expanding the etched area and vertically recessing the cavity by etching each pair of a first insulating layer **132** and a first sacrificial material layer **142** located directly underneath the bottom surface of the etched cavity within the etched area. In one embodiment, top surfaces of the first sacrificial material layers **142** may be physically exposed at the first stepped surfaces. The cavity overlying the first stepped surfaces is herein referred to as a first stepped cavity.

[0181] A dielectric fill material (such as undoped silicate glass or doped silicate glass) may be deposited to fill the first stepped cavity. Excess portions of the dielectric fill material may be removed from above the horizontal plane including the top surface of the first insulating cap layer **170**. A remaining portion of the dielectric fill material that fills the region overlying the first stepped surfaces constitute a first retro-stepped dielectric material portion **165**. As used herein, a "retro-stepped" element refers to an element that has stepped surfaces and a horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. The first-tier alternating stack (**132**, **142**) and the first retro-stepped dielectric material portion **165** collectively constitute a first-tier structure, which is an in-process structure that is subsequently modified.

[0182] An inter-tier dielectric layer **180** may be optionally deposited over the first-tier structure (**132**, **142**, **170**, **165**). The inter-tier dielectric layer **180** includes a dielectric material such as silicon oxide. In one embodiment, the inter-tier dielectric layer **180** may include a doped silicate glass having a greater etch rate than the material of the first insulating layers **132** (which may include an undoped silicate glass). For example, the inter-tier dielectric layer **180** may include phosphosilicate glass. The thickness of the inter-tier dielectric layer **180** may be in a range from 30 nm to 300 nm, although lesser and greater thicknesses may also be used.

[0183] Referring to FIGS. **20**A and **20**B, various first-tier openings (**149**, **129**) may be formed through the inter-tier dielectric layer **180** and the first-tier structure (**132**, **142**, **170**,

165) and the sacrificial source-level material layer **104** and into an upper portion of the lower-level dielectric material layers **760**. A photoresist layer (not shown) may be applied over the inter-tier dielectric layer **180**, and may be lithographically patterned to form various openings therethrough. The pattern of openings in the photoresist layer may be transferred through the inter-tier dielectric layer **180** and the first-tier structure (**132**, **142**, **170**, **165**), through the sacrificial source-level material layer **104**, and into the lower-level dielectric material layers **760** by a first anisotropic etch process to form the various first-tier openings (**149**, **129**) concurrently, i.e., during the first isotropic etch process. The various first-tier openings (**149**, **129**) may include first-tier memory openings **149** and first-tier support openings **129**. Locations of steps S in the first alternating stack (**132**, **142**) are illustrated as dotted lines in FIG. **20**B.

[0184] The first-tier memory openings **149** are openings that are formed in the memory array region **100** through each layer within the first alternating stack (**132**, **142**) and are subsequently used to form memory stack structures therein. The first-tier memory openings **149** may be formed in clusters of first-tier memory openings **149** that are laterally spaced apart along the second horizontal direction hd**2**. Each cluster of first-tier memory openings **149** may be formed as a two-dimensional array of first-tier memory openings **149**.

[0185] The first-tier support openings **129** are openings that are formed in the staircase region **300**, and are subsequently employed to form support pillar structures. A subset of the first-tier support openings **129** that is formed through the first retro-stepped dielectric material portion **165** may be formed through a respective horizontal surface of the first stepped surfaces.

[0186] In one embodiment, the first anisotropic etch process may include an initial step in which the materials of the first-tier alternating stack (**132**, **142**) are etched concurrently with the material of the first retro-stepped dielectric material portion **165**. The chemistry of the initial etch step may alternate to optimize etching of the first and second materials in the first-tier alternating stack (**132**, **142**) while providing a comparable average etch rate to the material of the first retro-stepped dielectric material portion **165**. The first anisotropic etch process may use, for example, a series of reactive ion etch processes or a single reaction etch process (e.g., $CF_4/O_2/Ar$ etch). The sidewalls of the various first-tier openings (**149**, **129**) may be substantially vertical, or may be tapered. After etching through the alternating stack (**132**, **142**) and the first retro-stepped dielectric material portion **165**, the chemistry of a terminal portion of the first anisotropic etch process may be selected to etch through the sacrificial source-level material layer **104**.

[0187] Optionally, the portions of the first-tier memory openings **149** and the first-tier support openings **129** at the level of the inter-tier dielectric layer **180** may be laterally expanded by an isotropic etch. In this case, the inter-tier dielectric layer **180** may comprise a dielectric material (such as borosilicate glass) having a greater etch rate than the first insulating layers **132** (that may include undoped silicate glass) in dilute hydrofluoric acid. An isotropic etch (such as a wet etch using HF) may be used to expand the lateral dimensions of the first-tier memory openings **149** at the level of the inter-tier dielectric layer **180**. The portions of the first-tier memory openings **149** located at the level of the inter-tier dielectric layer **180** may be optionally widened to provide a larger landing pad for second-tier memory openings to be subsequently formed through a second-tier alternating stack (to be subsequently formed prior to formation of the second-tier memory openings).

[0188] Referring to FIG. **21**, sacrificial first-tier opening fill portions (**148**, **128**) may be formed in the various first-tier openings (**149**, **129**). For example, a sacrificial first-tier fill material is deposited concurrently deposited in each of the first-tier openings (**149**, **129**). The sacrificial first-tier fill material includes a material that may be subsequently removed selective to the materials of the first insulating layers **132** and the first sacrificial material layers **142**.

[0189] In one embodiment, the sacrificial first-tier fill material may include a semiconductor material such as silicon (e.g., a-Si or polysilicon), a silicon-germanium alloy, germanium, a III-V compound semiconductor material, or a combination thereof. Optionally, a thin etch stop liner (such as a silicon oxide layer or a silicon nitride layer having a thickness in a range from 1 nm to 3 nm) may be used prior to depositing the sacrificial first-tier fill material. The sacrificial first-tier fill material may be formed by a non-conformal deposition or a conformal deposition method.

[0190] In another embodiment, the sacrificial first-tier fill material may include a silicon oxide material having a higher etch rate than the materials of the first insulating layers **132**, the first insulating cap layer **170**, and the inter-tier dielectric layer **180**. For example, the sacrificial first-tier fill material may include borosilicate glass or porous or non-porous organosilicate glass having an etch rate that is at least 100 times higher than the etch rate of densified TEOS oxide (i.e., a silicon oxide material formed by decomposition of tetraethylorthosilicate glass in a chemical vapor deposition process and subsequently densified in an anneal process) in a 100:1 dilute hydrofluoric acid. In this case, a thin etch stop liner (such as a silicon nitride layer having a thickness in a range from 1 nm to 3 nm) may be used prior to depositing the sacrificial first-tier fill material. The sacrificial first-tier fill material may be formed by a non-conformal deposition or a conformal deposition method.

[0191] In yet another embodiment, the sacrificial first-tier fill material may include amorphous silicon or a carbon-containing material (such as amorphous carbon or diamond-like carbon) that may be subsequently removed by ashing, or a silicon-based polymer that may be subsequently removed selective to the materials of the first alternating stack (**132**, **142**).

[0192] Portions of the deposited sacrificial material may be removed from above the topmost layer of the first-tier alternating stack (**132**, **142**), such as from above the inter-tier dielectric layer **180**. For example, the sacrificial first-tier fill material may be recessed to a top surface of the inter-tier dielectric layer **180** using a planarization process. The planarization process may include a recess etch, chemical mechanical planarization (CMP), or a combination thereof. The top surface of the inter-tier dielectric layer **180** may be used as an etch stop layer or a planarization stop layer.

[0193] Remaining portions of the sacrificial first-tier fill material comprise sacrificial first-tier opening fill portions (**148**, **128**). Specifically, each remaining portion of the sacrificial material in a first-tier memory opening **149** constitutes a sacrificial first-tier memory opening fill portion **148**. Each remaining portion of the sacrificial material in a first-tier support opening **129** constitutes a sacrificial first-

tier support opening fill portion **128**. The various sacrificial first-tier opening fill portions (**148**, **128**) are concurrently formed, i.e., during a same set of processes including the deposition process that deposits the sacrificial first-tier fill material and the planarization process that removes the first-tier deposition process from above the first alternating stack (**132**, **142**) (such as from above the top surface of the inter-tier dielectric layer **180**). The top surfaces of the sacrificial first-tier opening fill portions (**148**, **128**) may be coplanar with the top surface of the inter-tier dielectric layer **180**. Each of the sacrificial first-tier opening fill portions (**148**, **128**) may, or may not, include cavities therein.

[0194] Referring to FIG. **22**, a second-tier structure may be formed over the first-tier structure (**132**, **142**, **170**, **148**). The second-tier structure may include an additional alternating stack of insulating layers and spacer material layers, which may be sacrificial material layers. For example, a second alternating stack (**232**, **242**) of material layers may be subsequently formed on the top surface of the first alternating stack (**132**, **142**). The second alternating stack (**232**, **242**) includes an alternating plurality of third material layers and fourth material layers. Each third material layer may include a third material, and each fourth material layer may include a fourth material that is different from the third material. In one embodiment, the third material may be the same as the first material of the first insulating layer **132**, and the fourth material may be the same as the second material of the first sacrificial material layers **142**.

[0195] In one embodiment, the third material layers may be second insulating layers **232** and the fourth material layers may be second spacer material layers that provide vertical spacing between each vertically neighboring pair of the second insulating layers **232**. In one embodiment, the third material layers and the fourth material layers may be second insulating layers **232** and second sacrificial material layers **242**, respectively. The third material of the second insulating layers **232** may be at least one insulating material. The fourth material of the second sacrificial material layers **242** may be a sacrificial material that may be removed selective to the third material of the second insulating layers **232**. The second sacrificial material layers **242** may comprise an insulating material, a semiconductor material, or a conductive material. The fourth material of the second sacrificial material layers **242** may be subsequently replaced with electrically conductive electrodes which may function, for example, as control gate electrodes of a vertical NAND device.

[0196] In one embodiment, each second insulating layer **232** may include a second insulating material, and each second sacrificial material layer **242** may include a second sacrificial material. In this case, the second alternating stack (**232**, **242**) may include an alternating plurality of second insulating layers **232** and second sacrificial material layers **242**. The third material of the second insulating layers **232** may be deposited, for example, by chemical vapor deposition (CVD). The fourth material of the second sacrificial material layers **242** may be formed, for example, CVD or atomic layer deposition (ALD).

[0197] The third material of the second insulating layers **232** may be at least one insulating material. Insulating materials that may be used for the second insulating layers **232** may be any material that may be used for the first insulating layers **132**. The fourth material of the second sacrificial material layers **242** is a sacrificial material that may be removed selective to the third material of the second insulating layers **232**. Sacrificial materials that may be used for the second sacrificial material layers **242** may be any material that may be used for the first sacrificial material layers **142**. In one embodiment, the second insulating material may be the same as the first insulating material, and the second sacrificial material may be the same as the first sacrificial material.

[0198] The thicknesses of the second insulating layers **232** and the second sacrificial material layers **242** may be in a range from 20 nm to 50 nm, although lesser and greater thicknesses may be used for each second insulating layer **232** and for each second sacrificial material layer **242**. The number of repetitions of the pairs of a second insulating layer **232** and a second sacrificial material layer **242** may be in a range from 2 to 1,024, and typically from 8 to 256, although a greater number of repetitions may also be used. In one embodiment, each second sacrificial material layer **242** in the second alternating stack (**232**, **242**) may have a uniform thickness that is substantially invariant within each respective second sacrificial material layer **242**.

[0199] Second stepped surfaces in the second stepped area may be formed in the staircase region **300** using a same set of processing steps as the processing steps used to form the first stepped surfaces in the first stepped area with suitable adjustment to the pattern of at least one masking layer. A second retro-stepped dielectric material portion **265** may be formed over the second stepped surfaces in the staircase region **300**.

[0200] A second insulating cap layer **270** may be subsequently formed over the second alternating stack (**232**, **242**). The second insulating cap layer **270** includes a dielectric material that is different from the material of the second sacrificial material layers **242**. In one embodiment, the second insulating cap layer **270** may include silicon oxide. In one embodiment, the first and second sacrificial material layers (**142**, **242**) may comprise silicon nitride.

[0201] Optionally, drain-select-level isolation structures **72** may be formed through a subset of layers in an upper portion of the second-tier alternating stack (**232**, **242**). The second sacrificial material layers **242** that are cut by the drain-select-level isolation structures **72** correspond to the levels in which drain-select-level electrically conductive layers are subsequently formed. The drain-select-level isolation structures **72** include a dielectric material such as silicon oxide. The drain-select-level isolation structures **72** may laterally extend along a first horizontal direction hd**1**, and may be laterally spaced apart along a second horizontal direction hd**2** that is perpendicular to the first horizontal direction hd**1**. The combination of the second alternating stack (**232**, **242**), the second retro-stepped dielectric material portion **265**, the second insulating cap layer **270**, and the optional drain-select-level isolation structures **72** collectively constitute a second-tier structure (**232**, **242**, **265**, **270**, **72**).

[0202] Referring to FIGS. **23**A and **23**B, various second-tier openings (**249**, **229**) may be formed through the second-tier structure (**232**, **242**, **265**, **270**, **72**). A photoresist layer (not shown) may be applied over the second insulating cap layer **270**, and may be lithographically patterned to form various openings therethrough. The pattern of the openings may be the same as the pattern of the various first-tier openings (**149**, **129**), which is the same as the sacrificial first-tier opening fill portions (**148**, **128**). Thus, the litho-

graphic mask used to pattern the first-tier openings (**149**, **129**) may be used to pattern the photoresist layer.

[0203] The pattern of openings in the photoresist layer may be transferred through the second-tier structure (**232**, **242**, **265**, **270**, **72**) by a second anisotropic etch process to form various second-tier openings (**249**, **229**) concurrently, i.e., during the second anisotropic etch process. The various second-tier openings (**249**, **229**) may include second-tier memory openings **249** and second-tier support openings **229**.

[0204] The second-tier memory openings **249** are formed directly on a top surface of a respective one of the sacrificial first-tier memory opening fill portions **148**. The second-tier support openings **229** are formed directly on a top surface of a respective one of the sacrificial first-tier support opening fill portions **128**. Further, each second-tier support openings **229** may be formed through a horizontal surface within the second stepped surfaces, which include the interfacial surfaces between the second alternating stack (**232**, **242**) and the second retro-stepped dielectric material portion **265**. Locations of steps S in the first-tier alternating stack (**132**, **142**) and the second-tier alternating stack (**232**, **242**) are illustrated as dotted lines in FIG. **7**B.

[0205] The second anisotropic etch process may include an etch step in which the materials of the second-tier alternating stack (**232**, **242**) are etched concurrently with the material of the second retro-stepped dielectric material portion **265**. The chemistry of the etch step may alternate to optimize etching of the materials in the second-tier alternating stack (**232**, **242**) while providing a comparable average etch rate to the material of the second retro-stepped dielectric material portion **265**. The second anisotropic etch process may use, for example, a series of reactive ion etch processes or a single reaction etch process (e.g., $CF_4/O_2/Ar$ etch). The sidewalls of the various second-tier openings (**249**, **229**) may be substantially vertical, or may be tapered. A bottom periphery of each second-tier opening (**249**, **229**) may be laterally offset, and/or may be located entirely within, a periphery of a top surface of an underlying sacrificial first-tier opening fill portion (**148**, **128**). The photoresist layer may be subsequently removed, for example, by ashing.

[0206] Referring to FIG. **24**, the sacrificial first-tier fill material of the sacrificial first-tier opening fill portions (**148**, **128**) may be removed using an etch process that etches the sacrificial first-tier fill material selective to the materials of the first and second insulating layers (**132**, **232**), the first and second sacrificial material layers (**142**, **242**), the first and second insulating cap layers (**170**, **270**), and the inter-tier dielectric layer **180**. A memory opening **49**, which is also referred to as an inter-tier memory opening **49**, is formed in each combination of a second-tier memory openings **249** and a volume from which a sacrificial first-tier memory opening fill portion **148** is removed. A support opening **19**, which is also referred to as an inter-tier support opening **19**, is formed in each combination of a second-tier support openings **229** and a volume from which a sacrificial first-tier support opening fill portion **128** is removed.

[0207] FIGS. **25**A-**25**D provide sequential cross-sectional views of a memory opening **49** during formation of a memory opening fill structure. The same structural change occurs in each of the memory openings **49** and the support openings **19**.

[0208] Referring to FIG. **25**A, a memory opening **49** in the second exemplary device structure of FIG. **24** is illustrated. The memory opening **49** extends through the first-tier structure and the second-tier structure.

[0209] Referring to FIG. **25**B, a stack of layers including a blocking dielectric layer **52**, a charge storage layer **54**, a tunneling dielectric layer **56**, and a semiconductor channel material layer **60**L may be sequentially deposited in the memory openings **49**. The blocking dielectric layer **52** may have the same material composition and the same thickness range as in the first exemplary structure. The charge storage layer **54** may have the same material composition and the same thickness range as in the first exemplary structure. The tunneling dielectric layer may have the same material composition as in the first exemplary structure.

[0210] The semiconductor channel material layer **60**L can have the same material composition as the first semiconductor channel layer **601** and/or the second semiconductor channel layer **602** of the first embodiment. The semiconductor channel material layer **60**L includes a semiconductor material, such as at least one III-V compound semiconductor material. The at least one III-V compound semiconductor material has a doping of a first conductivity type. In one embodiment, the semiconductor channel material layer **60**L includes p-doped GaAs or InGaAs. The semiconductor channel material layer **60**L can be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD). The thickness of the semiconductor channel material layer **60**L can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed. A memory cavity **49'** is formed in the volume of each memory opening **49** that is not filled with the deposited material layers (**52**, **54**, **56**, **60**L). In one embodiment, the semiconductor channel material layer **60**L has a same band gap throughout, i.e., a fixed band gap. The semiconductor channel material layer **60**L may be formed by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD).

[0211] Referring to FIG. **25**C, in case the cavity **49'** in each memory opening is not completely filled by the semiconductor channel material layer **60**L, a dielectric core layer may be deposited in the cavity **49'** to fill any remaining portion of the cavity **49'** within each memory opening. The dielectric core layer includes a dielectric material such as silicon oxide or organosilicate glass. The dielectric core layer may be deposited by a conformal deposition method such as low pressure chemical vapor deposition (LPCVD), or by a self-planarizing deposition process such as spin coating. The horizontal portion of the dielectric core layer overlying the second insulating cap layer **270** may be removed, for example, by a recess etch. The recess etch continues until top surfaces of the remaining portions of the dielectric core layer are recessed to a height between the top surface of the second insulating cap layer **270** and the bottom surface of the second insulating cap layer **270**. Each remaining portion of the dielectric core layer constitutes a dielectric core **62**.

[0212] Referring to FIG. **25**D, the material of the dielectric core layer **62**L can be vertically recessed selective to the semiconductor channel material layer **60**L into each memory opening **49** down to a depth between a first horizontal plane including the top surface of the second insulating cap layer **270** and a second horizontal plane including the bottom

surface of the second insulating cap layer **270**. Each remaining portion of the dielectric core layer **62**L constitutes a dielectric core **62**.

[0213] Portions of the semiconductor channel material layer **60**L that are located above the horizontal plane including the top surface of the dielectric core **62** can be removed, for example, by performing a selective isotropic etch process that etches the semiconductor materials of the semiconductor channel material layer **60**L selective to the dielectric materials of the second insulating cap layer **270** and the memory film **50**. Each remaining portion of the semiconductor channel material layer **60**L comprises a vertical semiconductor channel **60**. The III-V compound material of the vertical semiconductor channel **60** is herein referred to as a III-V compound semiconductor channel material. The III-V compound semiconductor channel material of the vertical semiconductor channel **60** can have a fixed band gap, which is the band gap of the III-V compound semiconductor material of the vertical semiconductor channel **60**.

[0214] Referring to FIG. **25**E, the dielectric core **62** can be vertically recess below the horizontal top surfaces of the vertical semiconductor channel **60**. The top surface of the dielectric core **62** may be recessed down to, or below, the horizontal plane including the top surface of the topmost sacrificial material layer **42**. Top portions of the inner sidewall of the vertical semiconductor channel **60** can be physically exposed to the recess region that is formed over the dielectric core **62**. The recess region can have an upper portion that is laterally bounded by the memory film **50** and a lower portion that is laterally bounded by the inner sidewall of the vertical semiconductor channel **60**.

[0215] Referring to FIG. **25**F, a graded III-V compound semiconductor material layer **63**L can be deposited over the dielectric core **62**, the vertical semiconductor channel **60**, and the second insulating cap layer **270**. The graded III-V compound semiconductor material layer **63**L may be the same as in the first embodiment, and may include a layer stack including at least two III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) having different material compositions and having a doping of a second conductivity type that is the opposite of the first conductivity type. The band gaps of the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) are selected that the band gap of the first III-V compound semiconductor material layer **63**A that is deposited directly on the vertical semiconductor channel **60** may substantially match or be slightly greater than the band gap of the vertical semiconductor channel **60**. Subsequently deposited III-V compound semiconductor material layers (**63**B, **63**C, **63**D) have a respective band gap that is less than the band gap of any previously deposited III-V compound semiconductor material layer. The layer stack including at least two III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) is described above with respect to the first embodiment illustrated in FIG. **7**J, and will not be described again for brevity.

[0216] While an embodiment in which the III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D) are formed as discrete material layers is described above, embodiments are expressly contemplated herein in which a continuously graded III-V compound semiconductor material layer **63**L replaces the discrete III-V compound semiconductor material layers (**63**A, **63**B, **63**C, **63**D), as described with respect to the first embodiment. In this case, the continuously graded III-V compound semiconductor material layer has a composition gradient that provides a continuously decreasing band gap as a function of a distance from the interface with the vertical semiconductor channel **60**. For example, the continuously graded III-V compound semiconductor material layer may include an InGaAs layer in which the atomic concentration of indium continuously increases as a function of a distance from the interface with the vertical semiconductor channel **60**.

[0217] Referring to FIG. **25**G, portion of the graded III-V compound semiconductor material layer **63**L located above the horizontal plane including the top surface of the second insulating cap layer **270** can be removed by performing a planarization process. For example, a chemical mechanical planarization process can be performed to remove portions of the graded III-V compound semiconductor material layer **63**L located above the horizontal plane including the top surface of the second insulating cap layer **270**. Each remaining portion of the graded III-V compound semiconductor material layer **63**L that fills a recess region and contacts a respective one of the vertical semiconductor channels **60** comprises a drain region **63**. Each drain region **63** can include one or more layers of the graded III-V compound semiconductor material layers **63**L.

[0218] Each drain region **63** is formed at an upper end of a respective vertical semiconductor channel **60**. The vertical semiconductor channels **60** have a doping of the first conductivity type, and each drain region **63** has a doping of the second conductivity type that is the opposite of the first conductivity type. Each drain region has a compositional gradient therein. The graded III-V compound semiconductor material layer **63**L within each drain region **63** have different band gaps that decrease step wise or continuously with a distance from an interface between the drain region **63** and the vertical semiconductor channel **60**.

[0219] According to an aspect of the present disclosure, the vertical semiconductor channel **60** within each memory opening **49** comprises a III-V compound semiconductor channel material. In one embodiment, the III-V compound semiconductor channel material has a fixed band gap that is uniform throughout the vertical semiconductor channel **60**. The drain region **63** within each memory opening **49** has a variable band gap that varies within the drain region **63**. In one embodiment, the variable band gap of the drain region **63** can monotonically decrease in a step wise or continuous manner within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. The distance may be measured vertically from a horizontal interface, or may be measured horizontally from a vertical interface.

[0220] In one embodiment, the III-V compound semiconductor channel material comprises a doped gallium arsenide channel material, and the drain region **63** comprises at least one doped indium gallium arsenide layer with a decreasing band gap from the interface with the vertical semiconductor channel **60**. In one embodiment, the drain region **63** comprises a plurality of doped indium gallium arsenide layers including indium atoms at different atomic indium percentages. In one embodiment, the difference between the variable band gap of the drain region **63** and the fixed band gap of the vertical semiconductor channel **60** monotonically increases within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. In one embodiment, the vertical semiconductor channel **60** com-

prises a cylindrical inner sidewall, a cylindrical outer sidewall, and an annular top surface extending between the cylindrical inner sidewall and the cylindrical outer sidewall. The drain region **63** contacts the annular top surface and an upper portion of the cylindrical inner sidewall of the vertical semiconductor channel **60**. The dopant concentration of dopants of the second conductivity type in the drain region **63** can be in a range from $5.0\times10^{18}/cm^3$ to $2.0\times10^{21}/cm^3$, although lesser and greater dopant concentrations can also be employed.

[0221] Referring to FIG. **26**, the second exemplary structure is illustrated after formation of the memory opening fill structures **58**. Support pillar structures **20** are formed in the support openings **19** concurrently with formation of the memory opening fill structures **58**. Each support pillar structure **20** may have a same set of components as a memory opening fill structure **58**.

[0222] Each adjoining pair of a first semiconductor channel layer **601** and a second semiconductor channel layer **602** can collectively form a vertical semiconductor channel **60** through which electrical current can flow when a vertical NAND device including the vertical semiconductor channel **60** is turned on. A tunneling dielectric layer **56** is surrounded by a charge storage layer **54**, and laterally surrounds a portion of the vertical semiconductor channel **60**. Each adjoining set of a tunneling dielectric layer **56**, a charge storage layer **54**, and a blocking dielectric layer **52** collectively constitute a memory film **50**, which includes a vertical stack of memory elements that can store a respective data bit with a macroscopic retention time. As used herein, a macroscopic retention time refers to a retention time suitable for operation of a memory device as a permanent memory device such as a retention time in excess of 24 hours. In alternative embodiments, a blocking dielectric layer **52** may not be formed in each memory opening **49**, and may be subsequently formed in backside recesses that are formed by removal of the sacrificial material layers **42** at a subsequent processing step.

[0223] Each combination of a memory film **50** and a vertical semiconductor channel **60** within a memory opening **49** constitutes a memory stack structure **55**. The memory stack structure **55** is a combination of a semiconductor channel **60**, a tunneling dielectric layer **56**, a plurality of memory elements as embodied as portions of the charge storage layer **54**, and a blocking dielectric layer **52**. Each combination of a memory stack structure **55**, a dielectric core **62**, and a drain region **63** within a memory opening **49** is herein referred to as a memory opening fill structure **58**. Each combination of a memory film **50**, a vertical semiconductor channel **60**, a dielectric core **62**, and a drain region **63** within each support opening **19** fills the respective support openings **19**, and constitutes a support pillar structure.

[0224] Referring to FIGS. **27**A and **27**B, a first contact-level dielectric layer **280** may be formed over the second-tier structure (**232**, **242**, **270**, **265**, **72**). The first contact-level dielectric layer **280** includes a dielectric material such as silicon oxide, and may be formed by a conformal or non-conformal deposition process. For example, the first contact-level dielectric layer **280** may include undoped silicate glass and may have a thickness in a range from 100 nm to 600 nm, although lesser and greater thicknesses may also be used.

[0225] A photoresist layer (not shown) may be applied over the first contact-level dielectric layer **280**, and may be lithographically patterned to form discrete openings within the area of the memory array region **100** in which memory opening fill structures **58** are not present. An anisotropic etch may be performed to form vertical interconnection region cavities **585** having substantially vertical sidewalls that extend through the first contact-level dielectric layer **280**, the second-tier structure (**232**, **242**, **270**, **265**, **72**), and the first-tier structure (**132**, **142**, **170**, **165**) may be formed underneath the openings in the photoresist layer. A top surface of a lower-level metal interconnect structure **780** may be physically exposed at the bottom of each vertical interconnection region cavity **585**. The photoresist layer may be removed, for example, by ashing.

[0226] Referring to FIG. **28**, a dielectric material such as silicon oxide may be deposited in the vertical interconnection region cavities **585** by a conformal deposition process (such as low pressure chemical vapor deposition) or a self-planarizing deposition process (such as spin coating). Excess portions of the deposited dielectric material may be removed from above the top surface of the first contact-level dielectric layer **280** by a planarization process. Remaining portions of the dielectric material in the vertical interconnection region cavities **585** constitute interconnection region dielectric fill material portions **584**.

[0227] Referring to FIGS. **29**A and **29**B, a photoresist layer may be applied over the first contact-level dielectric layer **280** and may be lithographically patterned to form elongated openings that extend along the first horizontal direction hd**1** between clusters of memory opening fill structures **58**. Backside trenches **79** may be formed by transferring the pattern in the photoresist layer (not shown) through the first contact-level dielectric layer **280**, the second-tier structure (**232**, **242**, **270**, **265**, **72**), and the first-tier structure (**132**, **142**, **170**, **165**), and into the sacrificial source-level material layer **104**. Portions of the first contact-level dielectric layer **280**, the second-tier structure (**232**, **242**, **270**, **265**, **72**), the first-tier structure (**132**, **142**, **170**, **165**), and the sacrificial source-level material layer **104** that underlie the openings in the photoresist layer may be removed to form the backside trenches **79**. In one embodiment, the backside trenches **79** may be formed between clusters of memory stack structures **55**. The clusters of the memory stack structures **55** may be laterally spaced apart along the second horizontal direction hd**2** by the backside trenches **79**.

[0228] Referring to FIGS. **30** and **31**A, a backside trench spacer **77** may be formed on sidewalls of each backside trench **79**. For example, a conformal spacer material layer may be deposited in the backside trenches **79** and over the first contact-level dielectric layer **280**, and may be anisotropically etched to form the backside trench spacers **77**. The backside trench spacers **77** include a material that is different from the material of the sacrificial source-level material layer **104**. For example, the backside trench spacers **77** may include silicon nitride.

[0229] Referring to FIG. **31**B, an etchant that etches the material of the sacrificial source-level material layer **104** selective to the materials of the first alternating stack (**132**, **142**), the second alternating stack (**232**, **242**), the first and second insulating cap layers (**170**, **270**), the first contact-level dielectric layer **280**, the at least one second dielectric material layer **768**, and the memory films **50** may be introduced into the backside trenches in an isotropic etch process. For example, if the sacrificial source-level material layer **104** includes undoped amorphous silicon or polysilicon, the backside trench spacers **77** include silicon nitride, a

wet etch process using hot trimethyl-2 hydroxyethyl ammonium hydroxide ("hot TMY") or tetramethyl ammonium hydroxide (TMAH) may be used to remove the sacrificial source-level material layer **104** selective to the memory films **50**. A source cavity **109** is formed in the volume from which the sacrificial source-level material layer **104** is removed. The source cavity **109** is vertically bounded by insulating surfaces.

[0230] Referring to FIG. **31**C, a sequence of isotropic etchants, such as wet etchants, may be applied to the physically exposed portions of the memory films **50** to sequentially etch the various component layers of the memory films **50** from outside to inside, and to physically expose cylindrical surfaces of the vertical semiconductor channels **60** at the level of the source cavity **109**. The source cavity **109** may be expanded in volume by removal of the portions of the memory films **50** at the level of the source cavity **109**. The source cavity **109** is formed by isotropically etching the sacrificial source-level material layer **104** and a sidewall portion of each of the memory films **50** selective to the bottommost insulating layer **32**, the at least one dielectric material layer **768**, and the vertical semiconductor channels **60**.

[0231] Referring to FIG. **31**D, a III-V compound semiconductor source region **14** can be formed in the source cavity **109** by performing a series of selective III-V compound deposition process(es) while suppressing growth of any III-V compound material from insulating surfaces (e.g., from the insulating layers **132**). The III-V compound semiconductor source region **14** has a shape of an annular III-V compound semiconductor material portion that is selectively deposited on the exposed portion of the III-V compound semiconductor material of the vertical semiconductor channel **60** exposed in the source cavity **109**.

[0232] Each III-V compound semiconductor source region **14** includes a graded III-V compound semiconductor material layer, which may comprise a single continuously graded III-V compound semiconductor material layer or a layer stack including at least two discrete III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) having different material compositions and having a doping of the second conductivity type that is the opposite of the first conductivity type. Specifically, the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D may include at least two III-V compound semiconductor material layers, such as three or more III-V compound semiconductor material layers having a respective band gap. The band gaps of the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) are selected that the band gap of a first III-V compound semiconductor material layer **14**A that is deposited directly on the vertical semiconductor channel **60** substantially matches or is slightly smaller than the band gap of the vertical semiconductor channel **60**. Subsequently deposited III-V compound semiconductor material layers (**14**B, **14**C, **14**D) have a respective band gap that is less than the band gap of any previously deposited III-V compound semiconductor material layer. The III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) may be deposited by selective III-V compound semiconductor deposition processes (such as chemical vapor deposition processes employing concurrent or alternating flow of an etchant gas).

[0233] In an illustrative example, the III-V compound semiconductor channel material of the vertical semiconductor channel **60** can include p-doped GaAs or InGaAs, and the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) can include a first III-V compound semiconductor material layer **14**A including n-doped GaAs or InGaAs and having the same band gap or substantially the same band gap as the vertical semiconductor channel **60**. For example, if the vertical semiconductor channel **60** comprises p-doped GaAs, then the first III-V compound semiconductor material layer **14**A comprises n-doped GaAs or n-doped InGaAs having a formula $In_xGa_{1-x}As$, where $0<x<0.1$. If the vertical semiconductor channel **60** comprises p-doped InGaAs having a formula $In_yGa_{1-y}As$, then the first III-V compound semiconductor material layer **14**A comprises n-doped InGaAs having a formula $In_xGa_{1-x}As$, where $x>y$. The second III-V compound semiconductor material layer **14**B is deposited on the first III-V compound semiconductor material layer **14**A. The second III-V compound semiconductor material layer **14**B comprises a n-doped InGaAs which contains more indium than the vertical semiconductor channel **60** and the first III-V compound semiconductor material layer **14**A. For example, if the vertical semiconductor channel **60** comprises p-doped GaAs, then the second III-V compound semiconductor material layer **14**B comprises n-doped InGaAs having a formula $In_zGa_{1-z}As$, where $z>0.1$, such as $0.1<z<0.3$. If the vertical semiconductor channel **60** comprises p-doped InGaAs having a formula $In_yGa_{1-y}As$, then the second III-V compound semiconductor material layer **14**B comprises n-doped InGaAs having a formula $In_zGa_{1-z}As$, where $z>x>y$. The third III-V compound semiconductor material layer **14**C may be deposited on the second III-V compound semiconductor material layer **14**B. The third III-V compound semiconductor material layer **14**C comprises a n-doped InGaAs which contains more indium than the second III-V compound semiconductor material layer **14**B. The third III-V compound semiconductor material layer **14**C may have a formula $In_pGa_{1-p}As$, where $p>z$, for example $0.3<p<0.5$. The fourth III-V compound semiconductor material layer **14**D may be deposited on the third III-V compound semiconductor material layer **14**C. The fourth III-V compound semiconductor material layer **14**D comprises a n-doped InGaAs which contains more indium than the third III-V compound semiconductor material layer **14**C. The fourth III-V compound semiconductor material layer **14**D may have a formula $In_qGa_{1-q}As$, where $q>p$, for example $0.5<q<0.7$. Generally, the III-V compound semiconductor material of each successive III-V compound semiconductor material layer can be selected such that the band gap of each subsequently deposited III-V compound semiconductor material layer decreases relative to the band gap of an immediately preceding III-V compound semiconductor material layer.

[0234] While the present disclosure is described employing an embodiment in which the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) include four III-V compound semiconductor material layers, two, three, four, or more layers can be included in the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D). Further, while an example in which each source region **14** includes n-doped GaAs or InGaAs, embodiments are expressly contemplated herein in which each source region **14** includes any III-V compound semiconductor material having a doping of the second conductivity type and having a variable band gap that increases stepwise or continuously with a vertical distance from an interface with the vertical

semiconductor channel **60**. Generally, the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) include any number of III-V compound semiconductor material layers. The first III-V compound semiconductor material layer **14**A that contacts the vertical semiconductor channel **60** has the same band gap as, or has substantially the same band gap as, the vertical semiconductor channel **60**. Each subsequently deposited layer within the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) has a lesser band gaps relative to the band gap of a respective preceding III-V compound semiconductor material layer. The layers in the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) can have a doping of the second conductivity type. The thickness of each source region **14** can be in a range from 20 nm to 60 nm, and top surface of each source region **14** can be at, or below, the top surface of the bottommost insulating layer **132**.

[0235] While an embodiment in which the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D) are formed as discrete material layers is described above, embodiments are expressly contemplated herein in which a single continuously graded III-V compound semiconductor material layer replaces the III-V compound semiconductor material layers (**14**A, **14**B, **14**C, **14**D). In this case, the continuously graded III-V compound semiconductor material layer has a composition gradient that provides a continuously decreasing band gap as a function of a distance from the interface with the vertical semiconductor channel **60**. For example, the continuously graded III-V compound semiconductor material layer may include an InGaAs layer in which the atomic concentration of indium continuously increases as a function of a distance from the interface with the vertical semiconductor channel **60**. The atomic concentration of indium in the continuously graded III-V compound semiconductor material layer may increase, for example, from 0% to 10% at the interface to a range from 50% to 100% at a distal portion of the continuously graded III-V compound semiconductor material layer.

[0236] Generally, each source region **14** can be formed as a III-V compound semiconductor source region comprising a doped III-V compound material, and can be formed on the lower side surface of the vertical semiconductor channel **60**. The III-V compound semiconductor source region **14** comprises a graded III-V compound semiconductor material having a horizontal compositional gradient that provides a variable band gap (e.g., varying continuously or step wise) that decreases with a horizontal distance from an interface with the vertical semiconductor channel **60**. The horizontal composition gradient may be stepwise (i.e., including stepwise changes in composition) or may be gradual (i.e., including a continuous change in composition).

[0237] Referring to FIG. **31**E, a tubular silicon-germanium alloy portion **15** can be selectively grown on the outer sidewall of each III-V compound semiconductor source region **14** while suppressing growth of a silicon-germanium alloy material from the insulating surfaces around the source cavity **109**. The tubular silicon-germanium alloy portions **15** can be grown by a selective silicon-germanium alloy deposition process in which source gases for silicon and germanium are flowed into a process chamber concurrently with, or alternatively with, an etchant gas. For example, the source gases may include germane and disilane or silane, and the etchant gas can include hydrogen chloride gas. Alternative source gases and/or alternative etchant gas may also be employed. The lateral thickness of each tubular silicon-germanium alloy portion **15** (i.e., the distance between an inner sidewall and an outer sidewall of each tubular silicon-germanium alloy portion **15**) may be in a range from 10 nm to 60 nm, although lesser and greater thicknesses may also be employed. The atomic percentage of germanium in the silicon-germanium alloy material of the tubular silicon-germanium alloy portions **15** may be in a range from 15% to 85%, such as from 30% to 70%, although lesser and greater percentages may also be employed.

[0238] Referring to FIG. **31**F, a sacrificial source-level metallic layer **16** can be conformally deposited by a conformal deposition process, such as a chemical vapor deposition process. The sacrificial source-level metallic layer **16** includes a material that forms a metallic compound with a silicon-germanium alloy. Specifically, the sacrificial source-level metallic layer **16** includes a metal that forms a germanosilicide (e.g., a silicon containing germanide, a germanium containing silicide or a germanide-silicide) upon reaction with a silicon-germanium alloy material. For example, the sacrificial source-level metallic layer **16** can include nickel, titanium, cobalt, platinum, or tungsten. The sacrificial source-level metallic layer **16** can be formed on an outer sidewall of each annular metal germanosilicide portion **18**. The thickness of the sacrificial source-level metallic layer **16** can be in a range from 10 nm to 100 nm, such as from 20 nm to 50 nm, although lesser and greater thicknesses can also be employed.

[0239] Referring to FIG. **31**G, a thermal anneal process is performed at an elevated temperature to induce metallization of the tubular silicon-germanium alloy portions **15**. The semiconductor material of the tubular silicon-germanium alloy portions **15** reacts with the metal of the sacrificial source-level metallic layer **16** to form annular metal germanosilicide portions **18**. The annular metal germanosilicide portions **16** include a metal germanosilicide material, such as nickel germanosilicide (NiGeSi) derived from metallization of the tubular silicon-germanium alloy portions **15**. The tubular silicon-germanium alloy portions **15** are converted into the annular metal germanosilicide portions **18**.

[0240] Referring to FIG. **31**H, remaining portions of the sacrificial source-level metallic layer **16** can be subsequently removed selective to the annular metal germanosilicide portions **18** and to the insulating materials of the at least one second dielectric material layer **768**, the bottommost insulating layer **132**, and the backside trench spacers **77**. For example, a wet etch process that etches metal selective to metal germanosilicide material can be performed to remove the remaining portions of the sacrificial source-level metallic layer **16**.

[0241] Referring to FIG. **32**A, the sacrificial material layers (**142**, **242**) are may be removed selective to the insulating layers (**132**, **232**), the first and second insulating cap layers (**170**, **270**), the first contact-level dielectric layer **280**, the annular metal germanosilicide portions **18**, the dielectric semiconductor oxide plates **122**, and the annular dielectric semiconductor oxide spacers **124**. For example, an etchant that selectively etches the materials of the sacrificial material layers (**142**, **242**) with respect to the materials of the insulating layers (**132**, **232**), the first and second insulating cap layers (**170**, **270**), the retro-stepped dielectric material portions (**165**, **265**), and the material of the outermost layer of the memory films **50** may be introduced into the backside trenches **79**, for example, using an isotropic etch process.

For example, the sacrificial material layers (**142**, **242**) may include silicon nitride, the materials of the insulating layers (**132**, **232**), the first and second insulating cap layers (**170**, **270**), the retro-stepped dielectric material portions (**165**, **265**), and the outermost layer of the memory films **50** may include silicon oxide materials.

[0242] The isotropic etch process may be a wet etch process using a wet etch solution, or may be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside trench **79**. For example, if the sacrificial material layers (**142**, **242**) include silicon nitride, the etch process may be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials used in the art.

[0243] Backside recesses (**143**, **243**) are formed in volumes from which the sacrificial material layers (**142**, **242**) are removed. The backside recesses (**143**, **243**) include first backside recesses **143** that are formed in volumes from which the first sacrificial material layers **142** are removed and second backside recesses **243** that are formed in volumes from which the second sacrificial material layers **242** are removed. Each of the backside recesses (**143**, **243**) may be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each of the backside recesses (**143**, **243**) may be greater than the height of the respective backside recess (**143**, **243**). A plurality of backside recesses (**143**, **243**) may be formed in the volumes from which the material of the sacrificial material layers (**142**, **242**) is removed. Each of the backside recesses (**143**, **243**) may extend substantially parallel to the top surface of the substrate semiconductor layer **5**. A backside recess (**143**, **243**) may be vertically bounded by a top surface of an underlying insulating layer (**132**, **232**) and a bottom surface of an overlying insulating layer (**132**, **232**). In one embodiment, each of the backside recesses (**143**, **243**) may have a uniform height throughout.

[0244] Referring to FIG. **32**B, a backside blocking dielectric layer (not shown) may be optionally deposited in the backside recesses (**143**, **243**) and the backside trenches **79** and over the first contact-level dielectric layer **280**. The backside blocking dielectric layer includes a dielectric material such as a dielectric metal oxide, silicon oxide, or a combination thereof. For example, the backside blocking dielectric layer may include aluminum oxide. The backside blocking dielectric layer may be formed by a conformal deposition process such as atomic layer deposition or chemical vapor deposition. The thickness of the backside blocking dielectric layer may be in a range from 1 nm to 20 nm, such as from 2 nm to 10 nm, although lesser and greater thicknesses may also be used.

[0245] At least one conductive material may be deposited in the plurality of backside recesses (**143**, **243**), in the source cavity **1-9**, on the sidewalls of the backside trenches **79**, and over the first contact-level dielectric layer **280**. The at least one conductive material may be deposited by a conformal deposition method, which may be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, or a combination thereof. The at least one conductive material may include an elemental metal, an intermetallic alloy of at least two elemental metals, a conductive nitride of at least one elemental metal, a conductive metal oxide, a conductive doped semiconductor material, a conductive metal-semiconductor alloy such as a metal silicide, alloys thereof, and combinations or stacks thereof.

[0246] In one embodiment, the at least one conductive material may include at least one metallic material, i.e., an electrically conductive material that includes at least one metallic element. Non-limiting exemplary metallic materials that may be deposited in the backside recesses (**143**, **243**) include tungsten, tungsten nitride, titanium, titanium nitride, tantalum, tantalum nitride, cobalt, and ruthenium. For example, the at least one conductive material may include a conductive metallic nitride liner that includes a conductive metallic nitride material such as TiN, TaN, WN, or a combination thereof, and a conductive fill material such as W, Co, Ru, Mo, Cu, or combinations thereof. In one embodiment, the at least one conductive material for filling the backside recesses (**143**, **243**) may be a combination of titanium nitride layer and a tungsten fill material.

[0247] Electrically conductive layers (**146**, **246**) may be formed in the backside recesses (**143**, **243**) by deposition of the at least one conductive material. A plurality of first electrically conductive layers **146** may be formed in the plurality of first backside recesses **143**, a plurality of second electrically conductive layers **246** may be formed in the plurality of second backside recesses **243**, and a continuous metallic material layer (not shown) may be formed on the sidewalls of each backside trench **79** and over the first contact-level dielectric layer **280**. A source-level metallic layer **112** can be formed in the source cavity **109**. Each of the first electrically conductive layers **146** and the second electrically conductive layers **246** may include a respective conductive metallic nitride liner and a respective conductive fill material. Thus, the first and second sacrificial material layers (**142**, **242**) may be replaced with the first and second electrically conductive layers (**146**, **246**), respectively. Specifically, each first sacrificial material layer **142** may be replaced with an optional portion of the backside blocking dielectric layer and a first electrically conductive layer **146**, and each second sacrificial material layer **242** may be replaced with an optional portion of the backside blocking dielectric layer and a second electrically conductive layer **246**. A backside cavity is present in the portion of each backside trench **79** that is not filled with the continuous metallic material layer.

[0248] Residual conductive material may be removed from inside the backside trenches **79**. Specifically, the deposited metallic material of the continuous metallic material layer may be etched back from the sidewalls of each backside trench **79** and from above the first contact-level dielectric layer **280**, for example, by an anisotropic or isotropic etch. Each remaining portion of the deposited metallic material in the first backside recesses constitutes a first electrically conductive layer **146**. Each remaining portion of the deposited metallic material in the second backside recesses constitutes a second electrically conductive layer **246**. Sidewalls of the first electrically conductive material layers **146** and the second electrically conductive layers may be physically exposed to a respective backside trench **79**. The backside trenches may have a pair of curved sidewalls having a non-periodic width variation along the first horizontal direction hd**1** and a non-linear width variation along the vertical direction.

[0249] Each electrically conductive layer (**146**, **246**) may be a conductive sheet including openings therein. A first subset of the openings through each electrically conductive layer (**146**, **246**) may be filled with memory opening fill structures **58**. A second subset of the openings through each electrically conductive layer (**146**, **246**) may be filled with the support pillar structures **20**. Each electrically conductive layer (**146**, **246**) may have a lesser area than any underlying electrically conductive layer (**146**, **246**) because of the first and second stepped surfaces. Each electrically conductive layer (**146**, **246**) may have a greater area than any overlying electrically conductive layer (**146**, **246**) because of the first and second stepped surfaces.

[0250] In some embodiments, drain-select-level isolation structures **72** may be provided at topmost levels of the second electrically conductive layers **246**. A subset of the second electrically conductive layers **246** located at the levels of the drain-select-level isolation structures **72** constitutes drain select gate electrodes. A subset of the electrically conductive layer (**146**, **246**) located underneath the drain select gate electrodes may function as combinations of a control gate and a word line located at the same level. The control gate electrodes within each electrically conductive layer (**146**, **246**) are the control gate electrodes for a vertical memory device including the memory stack structure **55**.

[0251] Each of the memory stack structures **55** comprises a vertical stack of memory elements located at each level of the electrically conductive layers (**146**, **246**). A subset of the electrically conductive layers (**146**, **246**) may comprise word lines for the memory elements. The semiconductor devices in the underlying peripheral device region **700** may comprise word line switch devices configured to control a bias voltage to respective word lines. The memory-level assembly is located over the substrate semiconductor layer **5**. The memory-level assembly includes at least one alternating stack (**132**, **146**, **232**, **246**) and memory stack structures **55** vertically extending through the at least one alternating stack (**132**, **146**, **232**, **246**).

[0252] A source-level contact layer **114** is formed at the source level. The source-level contact layer **114** includes the source-level metallic layer **112** that includes the same material as the electrically conductive layers (**146**, **246**), annular metal germanosilicide portions **18** laterally surrounding a respective one of the vertical semiconductor channels **60**, and III-V compound semiconductor source regions **14** including a graded III-V compound semiconductor material. The sacrificial source-level material layer **104** is replaced with the source-level contact layer **114**. The source-level contact layer **114** comprises III-V compound semiconductor source regions **14** that contact an outer cylindrical sidewall of a respective one of the vertical semiconductor channels **60**.

[0253] Referring to FIGS. **33**A-**33**C, a dielectric fill material layer may be conformally deposited in the backside trenches **79** and over the first contact-level dielectric layer **280** by a conformal deposition process. The dielectric fill material layer may include, for example, silicon oxide. Each portion of the dielectric fill material layer that fills a backside trench **79** comprises a dielectric wall structure **176**.

[0254] A second contact-level dielectric layer **282** may be formed over the first contact-level dielectric layer **280**. The second contact-level dielectric layer **282** includes a dielectric material such as silicon oxide, and may have a thickness in a range from 100 nm to 600 nm, although lesser and greater thicknesses may also be used. The second contact-level dielectric layer **282** may comprise a horizontal portion of the dielectric fill material layer that is deposited over the first contact-level dielectric layer **280**.

[0255] Referring to FIGS. **34**A and **34**B, a photoresist layer (not shown) may be applied over the second contact-level dielectric layer **282**, and may be lithographically patterned to form various contact via openings. For example, openings for forming drain contact via structures may be formed in the memory array region **100**, and openings for forming staircase region contact via structures may be formed in the staircase region **300**. An anisotropic etch process is performed to transfer the pattern in the photoresist layer through the second and first contact-level dielectric layers (**282**, **280**) and underlying dielectric material portions. The drain regions **63** and the electrically conductive layers (**146**, **246**) may be used as etch stop structures. Drain contact via cavities may be formed over each drain region **63**, and staircase-region contact via cavities may be formed over each electrically conductive layer (**146**. **246**) at the stepped surfaces underlying the first and second retro-stepped dielectric material portions (**165**, **265**). The photoresist layer may be subsequently removed, for example, by ashing.

[0256] Drain contact via structures **88** are formed in the drain contact via cavities and on a top surface of a respective one of the drain regions **63**. Staircase-region contact via structures **86** are formed in the staircase-region contact via cavities and on a top surface of a respective one of the electrically conductive layers (**146**, **246**). The staircase-region contact via structures **86** may include drain select level contact via structures that contact a subset of the second electrically conductive layers **246** that function as drain select level gate electrodes. Further, the staircase-region contact via structures **86** may include word line contact via structures that contact electrically conductive layers (**146**, **246**) that underlie the drain select level gate electrodes and function as word lines for the memory stack structures **55**.

[0257] Referring to FIG. **35**, peripheral-region via cavities may be formed through the second and first contact-level dielectric layers (**282**, **280**), the second and first retro-stepped dielectric material portions (**265**, **165**), and the at least one second dielectric material layer **768** to top surfaces of a first subset of the lower-level metal interconnect structure **780** in the peripheral device region **400**. Through-memory-region via cavities may be formed through the interconnection region dielectric fill material portions **584** and the at least one second dielectric material layer **768** to top surfaces of a second subset of the lower-level metal interconnect structure **780**. At least one conductive material may be deposited in the peripheral-region via cavities and in the through-memory-region via cavities. Excess portions of the at least one conductive material may be removed from above the horizontal plane including the top surface of the second contact-level dielectric layer **282**. Each remaining portion of the at least one conductive material in a peripheral-region via cavity constitutes a peripheral-region contact via structure **488**. Each remaining portion of the at least one conductive material in a through-memory-region via cavity constitutes a through-memory-region via structure **588**.

[0258] At least one additional dielectric layer may be formed over the contact-level dielectric layers (**280**, **282**), and additional metal interconnect structures (herein referred to as upper-level metal interconnect structures) may be

formed in the at least one additional dielectric layer. For example, the at least one additional dielectric layer may include a line-level dielectric layer **290** that is formed over the contact-level dielectric layers (**280**, **282**). The upper-level metal interconnect structures may include bit lines **98** contacting a respective one of the drain contact via structures **88**, and interconnection line structures **96** contacting, and/or electrically connected to, at least one of the staircase-region contact via structures **86** and/or the peripheral-region contact via structures **488** and/or the through-memory-region via structures **588**. The word line contact via structures (which are provided as a subset of the staircase-region contact via structures **86**) may be electrically connected to the word line driver circuit through a subset of the lower-level metal interconnect structures **780** and through a subset of the peripheral-region contact via structures **488**.

[0259] Referring to FIGS. **17**A-**35** and according to various embodiments of the present disclosure, a three-dimensional memory device is provided, which comprises: a source-level contact layer **114** overlying a substrate and comprising a III-V compound semiconductor source region **14**; at least one alternating stack of insulating layers (**132**, **232**) and electrically conductive layers (**146**, **246**) located over the source-level contact layer **114**; a memory opening **49** vertically extending through the at least one alternating stack {(132, 246), (232, 246)}; and a memory opening fill structure **58** located in the memory opening **49** and comprising a vertical semiconductor channel **60** comprising a III-V compound semiconductor channel material in contact with an inner sidewall of the III-V compound semiconductor source region **14**, and a memory film **50** located adjacent to the vertical semiconductor channel **60**.

[0260] In one embodiment, the source-level contact layer **114** further comprises an annular metal germanosilicide portion **18** contacting and laterally surrounding the III-V compound semiconductor source region **14**. In one embodiment, the source-level contact layer **114** further comprises a source-level metallic layer **112** contacting an outer sidewall of the annular metal germanosilicide portion **18**. In one embodiment, a bottom surface of a bottommost one of the insulating layers (**132**, **232**) contacts an annular top surface of the III-V compound semiconductor source region **14**, the metal germanosilicide portion **18**, and the source-level metallic layer **112**. In one embodiment, the electrically conductive layers (**146**, **246**) have a same material composition as the source-level metallic layer **112**. In one embodiment, the annular metal germanosilicide portion **18** comprises nickel germanosilicide.

[0261] In one embodiment, the III-V compound semiconductor channel material comprises GaAs or InGaAs having a fixed band gap that is uniform throughout the vertical semiconductor channel **60**; and the III-V compound semiconductor source region **14** comprises InGaAs that has a variable band gap that is smaller than the fixed band gap of the III-V compound semiconductor channel material.

[0262] In one embodiment, the variable band gap of the III-V compound semiconductor source region **14** monotonically decreases within the III-V compound semiconductor source region **14** with a lateral distance from a cylindrical interface with the vertical semiconductor channel **60**.

[0263] In one embodiment, the III-V compound semiconductor source region **14** comprises a doped indium gallium arsenide layer having a graded indium concentration which increases within the III-V compound semiconductor source region **14** with a distance from an interface with the vertical semiconductor channel **60**.

[0264] In another embodiment, the III-V compound semiconductor source region **14** comprises a stack of cylindrical III-V compound material layers having different material compositions; and the cylindrical III-V compound material layers have different band gaps that decrease with a lateral distance from a cylindrical interface with the vertical semiconductor channel **60**. In one embodiment, the vertical semiconductor channel **60** comprises a gallium arsenide material; and the stack of cylindrical III-V compound material layers comprises at least one indium gallium arsenide layer.

[0265] In one embodiment, the vertical semiconductor channel **60** has a doping of a first conductivity type; and the III-V compound semiconductor source region **14** has a doping of a second conductivity type that is an opposite of the first conductivity type. In one embodiment, a drain region **63** can be provided, which includes a graded III-V compound semiconductor material having a doping of a second conductivity type that is an opposite of the first conductivity type. In one embodiment, the drain region **63** has a compositional gradient therein such that a variable band gap within the drain region **63** decreases with a distance from an interface with the vertical semiconductor channel **60**.

[0266] In one embodiment, the memory film **50** comprises a tunneling dielectric layer **56** contacting the vertical semiconductor channel **56**; a charge storage layer **54** in contact with the tunneling dielectric layer **54**; and a blocking dielectric layer **52** located between the charge storage layer **54** and the electrically conductive layers (**146**, **246**).

[0267] Referring to FIGS. **1**-**35** and according to various embodiments of the present disclosure, a three-dimensional memory device is provided, which comprises: at least one alternating stack of insulating layers {(**32** or (**132**, **232**))} and electrically conductive layers {(**46** or (**146**, **246**))} located over a substrate; a memory opening **49** vertically extending through the at least one alternating stack; and a memory opening fill structure **58** located in the memory opening **49** and comprising a vertical semiconductor channel **60** comprising a III-V compound semiconductor channel material having a doping of a first conductivity type, a memory film located adjacent to the vertical semiconductor channel, and a drain region **63** including a graded III-V compound semiconductor material having a doping of a second conductivity type that is an opposite of the first conductivity type and having a compositional gradient therein.

[0268] In one embodiment, the III-V compound semiconductor channel material has a fixed band gap that is uniform throughout the vertical semiconductor channel **60**; and the drain region **63** has a variable band gap that varies within the drain region **63**. In one embodiment, the variable band gap of the drain region **63** monotonically decreases within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**.

[0269] In one embodiment, the III-V compound semiconductor channel material comprises a doped gallium arsenide channel material; and the drain region **63** comprises at least one doped graded indium gallium arsenide layer. In one embodiment, the drain region **63** comprises a plurality of discrete doped indium gallium arsenide layers (**63**A-**63**D)

having an indium concentration which increases within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. In another embodiment, the drain region **63** comprises a doped indium gallium arsenide layer having a graded indium concentration which increases within the drain region **63** with a distance from an interface with the vertical semiconductor channel **60**. In yet another embodiment, the III-V compound semiconductor channel material comprises a doped indium gallium arsenide channel material, and the drain region **63** comprises at least one doped graded indium gallium arsenide layer having a higher indium concentration than the III-V compound semiconductor channel material.

[0270] In one embodiment, the vertical semiconductor channel **60** comprises a cylindrical inner sidewall, a cylindrical outer sidewall, and an annular top surface extending between the cylindrical inner sidewall and the cylindrical outer sidewall; and the drain region **63** contacts the annular top surface and an upper portion of the cylindrical inner sidewall of the vertical semiconductor channel **60**. In one embodiment, the memory opening fill structure **58** comprises a dielectric core **62** located within the vertical semiconductor channel **60** and contacting the inner cylindrical sidewall of the vertical semiconductor channel **60**; and the drain region **63** contacts a top surface of the dielectric core **62**.

[0271] In one embodiment, the substrate comprises a III-V compound substrate semiconductor layer **930**; and the memory opening fill structure **58** comprises a III-V compound semiconductor pedestal **11** located between the vertical semiconductor channel **60** and the III-V compound substrate semiconductor layer **930**. The substrate comprises: a single crystalline silicon layer **9**; and a germanium-containing buffer layer **920** located on top of the single crystalline silicon layer **9**, wherein the III-V compound substrate semiconductor layer **930** is located over the germanium-containing buffer layer **920**.

[0272] In the first embodiment, the three-dimensional memory device comprises: a III-V compound semiconductor source region **14** comprising a doped III-V compound semiconductor material and contacting a top surface of III-V compound substrate semiconductor layer **930**; an insulating spacer **74** contacting sidewalls of the at least one alternating stack; and a backside contact via structure **76** laterally surrounded by the insulating spacer **74** and contacting a top surface of the III-V compound semiconductor source region **14**.

[0273] In the second embodiment, the three-dimensional memory device comprises a source-level contact layer **114** overlying the substrate and contacting an outer sidewall of the vertical semiconductor channel **60**. In one embodiment, the source-level contact layer **114** comprises: a III-V compound semiconductor source region **14** having a doping of an opposite conductivity type as the vertical semiconductor channel **60** and contacting the outer sidewall of the vertical semiconductor channel **60**; and an annular metal germanosilicide portion **18** contacting and laterally surrounding the III-V compound semiconductor source region **14**.

[0274] In one embodiment, the memory film **50** comprises a tunneling dielectric layer **56** contacting the vertical semiconductor channel **60**; a charge storage layer **54** in contact with the tunneling dielectric layer **56**; and a blocking dielectric layer **52** located between the charge storage layer **54** and the electrically conductive layers {(**46** or (**146**, **246**))}.

[0275] The various embodiments of the present disclosure can be employed to provide a III-V compound semiconductor contact region (e.g., drain **63** and/or source **14**) having a gradually decreasing band gap width at end portions of semiconductor channels {(**930**, **11**, **60**) or **60**} that include a III-V compound semiconductor material. The gradually decreasing band gap may be a function of gradually decreasing gallium content (and increasing indium content) in the semiconductor contact region. This provides a higher quality semiconductor material due to closer lattice match between the channel and gradually varying composition of the contact material compared to a case with an abruptly decreasing gallium content between the channel and the contact region.

[0276] Furthermore, when the semiconductor channels comprise GaAs and the semiconductor contact regions comprises InAs or InGaAs, a metal contact to the InAs or InGaAs contact region exhibits a lower contact resistance than if the metal contact was made to a GaAs semiconductor contact region. This is because the Fermi level for n-type InAs or indium rich InGaAs pins very close to the conduction band, resulting in a smaller barrier for electrons to move across the metal-semiconductor junction. In contrast, the Fermi level for n-type GaAs pins within the band gap, leading to a net positive barrier height (i.e., a larger barrier) for electrons to move across the metal-semiconductor junction.

[0277] Finally, the III-V compound semiconductor material of the vertical semiconductor channels {(**930**, **11**, **60**) or **60**} can provide enhanced charge carrier mobility to provide enhanced on-current for the vertical semiconductor channels of three-dimensional memory devices.

[0278] Although the foregoing refers to particular embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Compatibility is presumed among all embodiments that are not alternatives of one another. The word "comprise" or "include" contemplates all embodiments in which the word "consist essentially of" or the word "consists of" replaces the word "comprise" or "include," unless explicitly stated otherwise. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

What is claimed is:

1. A three-dimensional memory device comprising:

a source-level contact layer overlying a substrate and comprising a III-V compound semiconductor source region;

at least one alternating stack of insulating layers and electrically conductive layers located over the source-level contact layer;

a memory opening vertically extending through the at least one alternating stack; and

a memory opening fill structure located in the memory opening and comprising a vertical semiconductor channel comprising a III-V compound semiconductor chan-

nel material in contact with an inner sidewall of the III-V compound semiconductor source region, and a memory film located adjacent to the vertical semiconductor channel.

2. The three-dimensional memory device of claim **1**, wherein the source-level contact layer further comprises an annular metal germanosilicide portion contacting and laterally surrounding the III-V compound semiconductor source region.

3. The three-dimensional memory device of claim **2**, wherein the source-level contact layer further comprises a source-level metallic layer contacting an outer sidewall of the annular metal germanosilicide portion.

4. The three-dimensional memory device of claim **3**, wherein a bottom surface of a bottommost one of the insulating layers contacts an annular top surface of the III-V compound semiconductor source region, the annular metal germanosilicide portion, and the source-level metallic layer.

5. The three-dimensional memory device of claim **3**, wherein the electrically conductive layers have a same material composition as the source-level metallic layer.

6. The three-dimensional memory device of claim **3**, wherein the annular metal germanosilicide portion comprises nickel germanosilicide.

7. The three-dimensional memory device of claim **1**, wherein:

the III-V compound semiconductor channel material comprises gallium arsenide or indium gallium arsenide having a fixed band gap that is uniform throughout the vertical semiconductor channel; and

the III-V compound semiconductor source region comprises indium gallium arsenide that has a variable band gap that is smaller than the fixed band gap of the III-V compound semiconductor channel material, and that decreases within the III-V compound semiconductor source region with a lateral distance from a cylindrical interface with the vertical semiconductor channel.

8. The three-dimensional memory device of claim **7**, wherein the III-V compound semiconductor source region comprises a doped indium gallium arsenide layer having a graded indium concentration which increases within the III-V compound semiconductor source region with a distance from an interface with the vertical semiconductor channel.

9. The three-dimensional memory device of claim **1**, wherein:

the III-V compound semiconductor source region comprises a stack of cylindrical III-V compound material layers having different material compositions; and

the cylindrical III-V compound material layers have different band gaps that decrease with a lateral distance from a cylindrical interface with the vertical semiconductor channel.

10. The three-dimensional memory device of claim **9**, wherein:

the vertical semiconductor channel comprises a gallium arsenide material; and

the stack of cylindrical III-V compound material layers comprises at least one indium gallium arsenide layer.

11. The three-dimensional memory device of claim **9**, wherein:

the vertical semiconductor channel has a doping of a first conductivity type; and

the III-V compound semiconductor source region has a doping of a second conductivity type that is an opposite of the first conductivity type.

12. The three-dimensional memory device of claim **11**, further comprising a drain region including a graded III-V compound semiconductor material having a doping of a second conductivity type that is an opposite of the first conductivity type.

13. The three-dimensional memory device of claim **12**, wherein the drain region has a compositional gradient therein such that a variable band gap within the drain region decreases with a distance from an interface with the vertical semiconductor channel.

14. The three-dimensional memory device of claim **1**, wherein the memory film comprises:

a tunneling dielectric layer contacting the vertical semiconductor channel;

a charge storage layer in contact with the tunneling dielectric layer; and

a blocking dielectric layer located between the charge storage layer and the electrically conductive layers.

15. A method of forming a three-dimensional memory device, comprising:

forming a sacrificial source-level material layer overlying a substrate;

forming at least one alternating stack of insulating layers and spacer material layers located over the sacrificial source-level material layer, wherein the spacer material layers are formed as, or are subsequently replaced with, electrically conductive layers;

forming a memory opening through the at least one alternating stack;

forming a memory opening fill structure in the memory opening, wherein the memory opening fill structure comprises a vertical semiconductor channel including a III-V compound semiconductor channel material, and a memory film located adjacent to the vertical semiconductor channel; and

replacing the sacrificial source-level material layer with a source-level contact layer, wherein the source-level contact layer comprises a III-V compound semiconductor source region that contacts an outer cylindrical sidewall of the vertical semiconductor channel.

16. The method of claim **15**, wherein the source-level contact layer further comprises an annular metal germanosilicide portion that is formed on an outer sidewall of the III-V compound semiconductor source region.

17. The method of claim **16**, further comprising:

removing the sacrificial source-level material layer to form a source cavity vertically bounded by insulating surfaces;

selectively growing a tubular silicon-germanium alloy portion on the outer sidewall of the III-V compound semiconductor source region while suppressing growth of a silicon-germanium alloy material from the insulating surfaces around the source cavity; and

forming the annular metal germanosilicide portion by reacting the tubular silicon-germanium alloy portion with a metal.

18. The method of claim **17**, further comprising depositing a source-level metallic layer on an outer sidewall of the annular metal germanosilicide portion.

19. The method of claim **18**, further comprising:

forming backside recesses by removing the spacer material layers selective to the insulating layers;

depositing a metal in the backside recesses and in unfilled portions of the source cavity after formation of the annular metal germanosilicide portion, wherein portions of the metal deposited in the backside recesses comprise the electrically conductive layers, and portions of the metal deposited in the unfilled portions of the source cavity comprise the source-level metallic layer.

20. The method of claim **15**, wherein the III-V compound semiconductor source region is formed by selectively depositing at least one cylindrical III-V compound material layer having a graded band gap that decreases with a lateral distance from a cylindrical interface with the vertical semiconductor channel, while suppressing growth of any III-V compound material from insulating surfaces.

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