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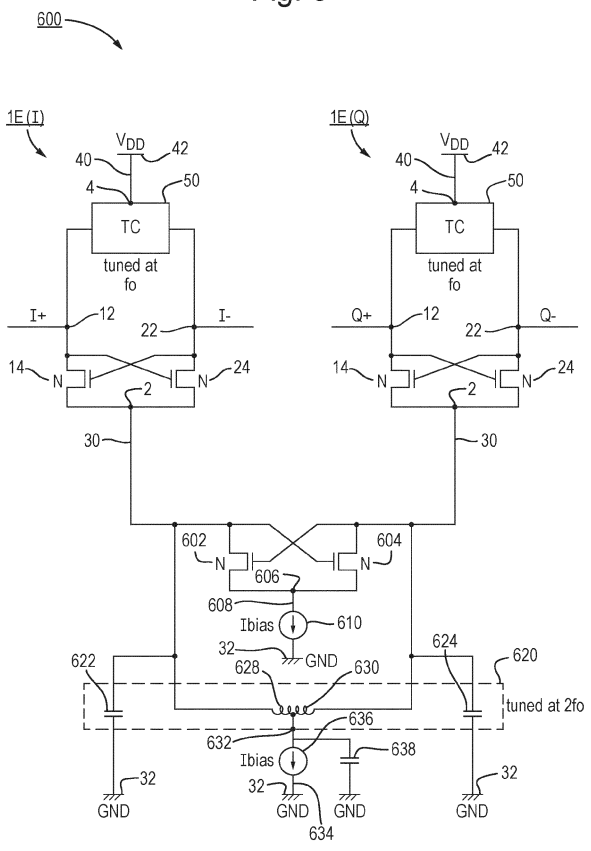
(54) QUADRATURE OSCILLATOR CIRCUITRY AND CIRCUITRY COMPRISING THE SAME

(57) Quadrature oscillator circuitry, comprising: a first differential oscillator circuit having differential output nodes and configured to generate a first pair of differential oscillator signals at those output nodes, respectively; a second differential oscillator circuit having differential output nodes and configured to generate a second pair of differential oscillator signals at those output nodes, respectively; and a cross-coupling circuit connected to cross-couple the first and second differential oscillator circuits. The cross-coupling circuit may comprise a pair of cross-coupled transistors.

Fig. 6



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Description

[0001] The present invention relates to oscillator circuitry, in particular to quadrature oscillator circuitry comprising first and second differential oscillator circuits each configured to generate a pair of differential oscillator signals.

[0002] In such circuitry, the two pairs of differential oscillator signals are controlled such that they form a set of quadrature oscillator signals, i.e. signals mutually 90° out of phase with one another. Such signals may have relative phases of 0°, 90°, 180° and 270°, respectively, which may be referred to as I+, Q+, I- and Q- phases, respectively.

[0003] Such oscillator circuitry may be configured to be voltage controlled, where an input voltage control signal controls a frequency (operation frequency) of the oscillator signals, for example by controlling a resonant frequency of one of more LC tank circuits of the oscillator circuitry. Oscillator circuitry configured in this way may be referred to as a voltage-controlled oscillator (VCO), in particular a quadrature VCO where the two pairs of differential oscillator signals form a set of quadrature oscillator signals.

[0004] The present invention also relates to circuitry comprising such quadrature oscillator circuitry, such as a phase lock loop (PLL).

[0005] By way of background, **Figure 1** is a circuit diagram presenting previously-considered differential oscillator circuits 1, 100, 200, 1E, 100E and 200E, which are each configured to generate a pair of differential oscillator signals. Thus, any of these differential oscillator circuits may generate one of the two pairs of differential oscillator signals mentioned above, so that these differential oscillator circuits (and variations of them) may be used interchangeably. The present disclosure will be understood accordingly.

[0006] Differential oscillator circuit 1 comprises a first tail node 2, a second tail node 4 and a pair of parallel current paths 10, 20 which extend in parallel between the first tail node 2 and the second tail node 4. A pair of output nodes 12, 22 are located (e.g. mid-way) along the current paths 10, 20, respectively, at which a pair of differential oscillator signals OUT+ and OUT- (having relative phases of 0° and 180°, respectively) are generated.

[0007] A pair of cross-coupled transistors 14, 24, in this case NMOS field-effect transistors (FETs), are provided along the current paths 10, 20, respectively, between the respective output nodes 12, 22 and the first tail node 2, so that their channels form respective parts of those current paths. The source terminals of the transistors 14, 24 are connected together to the first tail node 2 and their drain terminals are connected to the output nodes 12, 22 respectively. The gate terminals of the transistors 14, 24 are connected to each other's drain terminals so that they form a cross-coupled pair.

[0008] Capacitors 16, 26 are connected between the output nodes 12, 22, respectively, and a voltage supply node, in this case ground supply (GND). Inductors 18, 28 are connected along the current paths 10, 20, respectively, between the respective output nodes 12, 22 and the second tail node 4, so that they form respective parts of those current paths 10 20. The inductors 18, 28 may be implemented together as a centre-tapped inductor (winding/coil) whose centre tap (i.e. contact) is connected to the second tail node 4 and whose respective ends are connected to the output nodes 12, 22, as shown in Figure 1.

[0009] A first tail current path 30 connects the first tail node 2 to a first voltage-source node 32, in this case ground supply (GND), and a second tail current path 40 connects the second tail node 4 to a second voltage-source node 42, in this case VDD. Thus, in this case, the first voltage-source node 32 may be (or be for connection to) a low-voltage source and the second voltage-source node 42 may be (or be for connection to) a high-voltage source. A current source 34 is located along (i.e. forms part of) the first tail current path 30 so as to regulate or control a bias current Ibias flowing along that current path 30 as indicated. The current source 34 thus also regulates or controls a bias current Ibias flowing along the second tail current path 40, that current being divided between the first and second current paths 10, 20.

[0010] In operation, the cross-coupled pair of transistors 14, 24 act as cross-coupled inverting amplifiers so as to force (or bias or urge) the voltages at the output nodes 12, 22 to be differential. The capacitors 16, 26 and inductors 18, 28 form parts of an LC tank circuit which then causes the voltages at the output nodes 12, 22 to oscillate at a frequency f_0 (resonant frequency) defined by the capacitance and inductance values of those components 16, 26, 18, 28. By implementing the capacitors 16, 26 as variable capacitors and/or the inductors 18, 28 as variable inductors, the frequency f_0 may be tuned (i.e. adapted by adapting the capacitance and/or inductance values). Where the values are adapted under voltage control (for example, by implementing the capacitors 16, 26 as a voltage controlled switched array of capacitors), the differential oscillator circuit 1 may be referred to as a VCO.

[0011] Of course, the skilled reader will recognize that the capacitors 16, 26 need not be provided between the output nodes 12, 22 and ground supply GND as indicated. An equivalent LC tank circuit could be implemented by placing those capacitors 16, 26 in series between the output nodes 12, 22. With this in mind, reference is made to differential oscillator circuit 100.

[0012] Differential oscillator circuit 100 is similar to differential oscillator circuit 1, and as such like elements are denoted by like reference signs and duplicate description is omitted. Differential oscillator circuit 100 differs from differential oscillator circuit 1 in that the capacitors 16, 26 are replaced with varactors (varactor diodes, or variable capacitance diodes) 116, 126, respectively, and in that those varactors are connected in series between the current paths 10, 20, effectively between the output nodes

12, 22. The parallel connection of the capacitors 18, 28 and the varactors 116, 126 form the LC tank circuit of the differential oscillator circuit 100.

[0013] A control voltage Vtune is applied to the node between the varactors 116, 126 as indicated. As is known, by varying the control voltage Vtune the capacitance of the varactors 116, 126 is varied, thereby varying (or tuning) the resonant frequency f_0 and thus the frequency of the differential oscillator signals OUT+ and OUT-. Differential oscillator circuit 100 may thus be referred to as a VCO.

[0014] Differential oscillator circuit 200 is also similar to differential oscillator circuit 1, and again like elements are denoted by like reference signs and duplicate description is omitted. Differential oscillator circuit 200 differs from differential oscillator circuit 1 in that the capacitors 16, 26 are replaced with a capacitor 316 connected between the current paths 10, 20, effectively between the output nodes 12, 22. Further, the inductors 18, 28 have been replaced with an inductor 318 also connected between the current paths 10, 20, effectively between the output nodes 12, 22 and in parallel with the capacitor 316. Also, a further pair of cross-coupled transistors 315, 325, in this case PMOS field-effect transistors (FETs), are provided along the current paths 10, 20, respectively, between the output nodes 12, 22 and the second tail node 4, so that their channels form respective parts of those current paths.

[0015] The source terminals of the transistors 315, 325 are connected together to the second tail node 4 and their drain terminals are connected to the output nodes 12, 22, respectively. The gate terminals of the transistors 315, 325 are connected to each other's drain terminals so that they form a cross-coupled pair. Like transistors 14, 24, the transistors 315, 325 act as cross-coupled inverting amplifiers. Indeed, the combination of the transistors 14, 24, 315, 325 act as a cross-coupled pair of CMOS inverters. The parallel connection of the capacitor 316 and inductor 318 form the LC tank circuit of the differential oscillator circuit 200.

[0016] Thus, it will be apparent that the operation of differential oscillator circuits 100, 200 corresponds to that of the differential oscillator circuit 1, and that differential oscillator signals are produced at the output nodes 12, 22, respectively. The capacitor 316 and/or inductor 318 could be tuneable for example to form a VCO. Thus, any of the differential oscillator circuits disclosed herein (and, by extension, any of the quadrature oscillator circuitry disclosed herein) could be implemented as a VCO. The present disclosure will be understood accordingly.

[0017] Differential oscillator circuit 1E is equivalent to differential oscillator circuit 1, with its LC tank circuit shown in schematic form as LC tank circuit 50, with the capacitors 16, 26 effectively assumed to be within that LC tank circuit 50 (i.e. as if they were connected in series between the output nodes 12, 22 as mentioned earlier). Similarly, differential oscillator circuit 100E is equivalent to differential oscillator circuit 100, with its LC tank circuit shown in schematic form as LC tank circuit (TC) 150, with the inductors 18, 28 and varactors 116, 126 effectively assumed to be within that LC tank circuit 150. Differential oscillator circuit 200E is equivalent to differential oscillator circuit 200, with its LC tank circuit shown schematically as LC tank circuit 250, with the capacitors 316 and inductors 318 effectively assumed to be within that tank circuit 250. The reference signs used for differential oscillator circuits 1, 100, 200 apply equally to circuits 1E, 100E, 200E where like elements are shown, but only a subset of those reference signs have been shown in the equivalent circuits for simplicity.

[0018] It will thus be appreciated that the present invention may be applied to a wide variety of differential oscillator circuit topologies, and that these may be represented in "full" as in circuits 1, 100, 200 or in "simplified form" as in circuits 1E, 100E, 200E. For convenience of explanation, the circuits 1 and 1E will be focussed on hereinafter but it will be understood as demonstrated in Figure 1 that the techniques disclosed herein apply across the topologies. That is, where a differential oscillator circuit is disclosed later herein and is based on differential oscillator circuit 1, it will be appreciated that an equivalent differential oscillator circuit could be based on any of differential oscillator circuits 100, 200, 1E, 100E and 200E. Also, it will be apparent that other similar differential oscillator circuits could be arrived at by combining elements from circuits 100, 200, 1E, 100E and 200E, for example by employing the capacitors 16 and 26 in the circuit 200 in place of the capacitor 316, and are thus equally relevant.

[0019] Incidentally, although field-effect transistors (in this case, MOSFETs) are shown in Figure 1, the circuits disclosed herein could also be implemented using bipolar junction transistors (BJTs). Also, the circuits shown could be implemented "upside down" using PMOS transistors in place of NMOS transistors, for example, and similar considerations apply to circuits employing BJTs. Further, although in general the current sources 34 usefully regulate bias currents as mentioned earlier, in some arrangements those current sources 34 may be considered optional. In some arrangements the current sources 34 could simply be omitted, and in other arrangements they could be replaced with resistors, but these are just examples.

[0020] As mentioned earlier, the present invention relates in particular to oscillator circuitry which generates two pairs of differential oscillator signals where the two pairs form a set of quadrature oscillator signals. **Figure 2** is a schematic diagram of previously-considered quadrature oscillator circuitry 300.

[0021] Oscillator circuitry 300 comprises an I-side differential oscillator circuit 310I and a Q-side differential oscillator circuit 310Q, here shown schematically, coupled together by a cross-coupling circuit 320. Both of these differential oscillator circuits 310I, 310Q may be implemented as any of the differential oscillator circuits of Figure 1, for example. Taking the differential oscillator

circuit 1 as a running example, the I+ and I- outputs of the differential oscillator circuit 310I correspond to the OUT+ and OUT- outputs, respectively, of one instance of the circuit 1, and the Q+ and Q- outputs of the differential oscillator circuit 310Q correspond to the OUT+ and OUT- outputs, respectively, of another instance of the circuit 1. Those outputs are then cross-coupled by virtue of the cross-coupling circuit 320.

[0022] The cross-coupling circuit 320 comprises Gm-cells (transconductance cells) 330 and 340, both of which could be implemented for example as in the implementation 330-1 of the cell 330 shown explicitly in Figure 2. Cell 330 injects current into the current paths 10, 20 of the Q-side differential oscillator circuit 310Q that is proportional to the differential voltage output swing I+, I- of the I-side differential oscillator circuit 3101. Similarly, cell 320 injects current into the current paths 10, 20 of the I-side differential oscillator circuit 310I that is proportional to the differential voltage output swing Q+, Q-of the Q-side differential oscillator circuit 310Q but with inverted polarity (e.g. by reversing the connection of either the inputs Vin+, Vin- or the outputs Vout+, Vout-, for which see circuit 330-1). As a result of this injected current, the I-side and Q-side differential oscillator circuits 310I and 310Q are coupled together and are "forced" to work in quadrature.

[0023] However, the approach in Figure 2 has drawbacks. The added Gm-cells 320, 330 are implemented (see circuit 330-1, for example) with active circuitry. Extra current is needed for these added cells that does not contribute to the actual oscillator gain or swing (i.e. I+, I-, Q+, Q-), which in turn increases the overall power consumption. Moreover, the added Gm-cells significantly increase the phase noise and deteriorate the oscillator performance.

[0024] It is desirable to solve such problems, in particular to provide more efficient and/or accurate quadrature oscillator circuitry.

[0025] According to an embodiment of a first aspect of the present invention, there is provided quadrature oscillator circuitry, comprising: first and second differential oscillator circuits, each differential oscillator circuit comprising first and second tail nodes, a pair of output nodes, and a pair of parallel current paths which extend in parallel between its first and second tail nodes via its output nodes, respectively, and each differential oscillator circuit configured to generate a pair of differential oscillator signals at its respective output nodes; and a cross-coupling circuit connected to cross-couple the differential oscillator circuits, wherein: for each of the differential oscillator circuits, a first tail current path connects the first tail node to a first voltage-source node and a second tail current path connects the second tail node to a second voltage-source node, one of the first and second voltage-source nodes for connection to a high-voltage source and the other of the first and second voltage-source nodes for connection to a low-voltage source; each of the differential oscillator circuits comprises a common-mode voltage node at which a common-mode voltage signal is produced, the common-mode voltage node either being an intermediate node of a potential divider connected between the parallel current paths (e.g. between the output nodes) of that differential oscillator circuit or being a node of the second tail current path of that differential oscillator circuit; and the cross-coupling circuit comprises, for at least one or each of the differential oscillator circuits, a current-control device which forms part of the first tail current path of that differential oscillator circuit and is configured to control the current flowing along that first tail current path based on the common-mode voltage signal of the other one of the differential oscillator circuits to cause the common-mode voltage signals of the respective differential oscillator circuits to be substantially in antiphase.

[0026] Such quadrature oscillator circuitry could be referred to simply as oscillator circuitry or an oscillator. When the frequency of the oscillator signals is controlled by a voltage control signal, the circuitry may be referred to as a VCO. Similar considerations apply to the other quadrature oscillator circuitry disclosed herein.

[0027] By causing the common-mode voltage signals of the respective differential oscillator circuits to be substantially in antiphase, the pairs of differential oscillator signals are controlled to form a set of quadrature oscillator signals.

[0028] The cross-coupling circuit may comprise an inverting amplifier configured, for at least one or each of the differential oscillator circuits, to control the current-control device of that differential oscillator circuit based on the common-mode voltage signal of the other one of the differential oscillator circuits. In this way, the desired antiphase relationship may be achieved.

[0029] The cross-coupling circuit may comprise first and second transistors as current-control devices for the first and second differential oscillator circuits, respectively. The first and second transistors may form respective parts of the first tail current paths of the first and second differential oscillator circuits, respectively, so that current flowing along the respective first tail current paths flows through the first and second transistors, respectively. The gate or base terminals of the first and second transistors may be connected to the common-mode nodes of the second and first differential oscillator circuits, respectively, so that they are controlled by the common-mode voltage signals produced at the common-mode nodes of the second and first differential oscillator circuits, respectively. In this way, the transistors may be cross-coupled and act as a pair of cross-coupled inverting amplifiers.

[0030] Each of the differential oscillator circuits may comprise a current source which forms part of its second tail current path and is configured to regulate a bias current flowing along that current path. The common-mode voltage nodes of the first and second differential oscillator circuits may be their second tail nodes or nodes of their second tail current paths between their second tail nodes and their current sources.

[0031] The gate or base terminals of the first and second transistors may be connected to the common-mode nodes of the second and first differential oscillator circuits, respectively, via impedances. Those impedances may be or comprise capacitors.

[0032] The common-mode voltage nodes of the first and second differential oscillator circuits may be the intermediate nodes of their respective potential dividers. In that case, for each of the differential oscillator circuits, its potential divider may comprise a potential-divider impedance connected between one of its parallel current paths (e.g. at one of the output nodes) and its intermediate node and another potential-divider impedance connected between the other one of its parallel current paths (e.g. at the other one of its output nodes) and its intermediate node. The potential-divider impedances may be or comprise capacitors.

[0033] Each of the differential oscillator circuits may comprise a current source which forms part of its second tail current path to regulate a bias current flowing along that current path.

[0034] The gate or base terminals of the first and second transistors may be connected via respective impedances (such as resistances, for DC biasing) to their drain or collector terminals or to a voltage-source node.

[0035] According to an embodiment of a second aspect of the present invention, there is provided quadrature oscillator circuitry, comprising: first and second differential oscillator circuits, each differential oscillator circuit comprising first and second tail nodes, a pair of output nodes, and a pair of parallel current paths which extend in parallel between its first and second tail nodes via its output nodes, respectively, and each differential oscillator circuit configured to generate a pair of differential oscillator signals at its respective output nodes; and a cross-coupling circuit comprising first and second transistors connected to cross-couple the differential oscillator circuits, wherein: for each of the differential oscillator circuits, a first tail current path connects the first tail node to a first voltage-source node and a second tail current path connects the second tail node to a second voltage-source node, one of the first and second voltage-source nodes for connection to a high-voltage source and the other of the first and second voltage-source nodes for connection to a low-voltage source; the first and second transistors are connected to form respective parts of the first tail current paths of the differential oscillator circuits, respectively, so that current flowing along the respective first tail current paths flows through the respective transistors; the gate or base terminals of the first and second transistors are connected to the first tail nodes of the second and first differential oscillator circuits, respectively, so that they are controlled by voltage signals produced at the first tail nodes of the second and first differential oscillator circuits, respectively; the first tail current paths extend from the first tail nodes via the first and second transistors, respectively, to a shared tail node; a shared tail current path connects the shared tail node to a shared voltage-source node, being the first voltage-source node of both of the differential oscillator circuits; each of said differential oscillator circuits comprises an LC tank circuit configured to have a target resonant frequency; and the quadrature oscillator circuitry comprises an auxiliary LC tank circuit shared by the differential oscillator circuits and configured to have a resonant frequency which is substantially twice the target resonant frequency.

[0036] The cross-coupling circuit comprising first and second transistors may act as cross-coupled inverting amplifiers. In particular, each of the transistors may act as a current-control device which forms part of the first tail current path of its differential oscillator circuit and be configured to control the current flowing along that first tail current path based on the first tail node voltage signal of the other one of the differential oscillator circuits to cause the first tail node voltage signals of the respective differential oscillator circuits to be substantially in antiphase. By causing the first tail node voltage signals of the respective differential oscillator circuits to be substantially in antiphase, the pairs of differential oscillator signals are controlled to form a set of quadrature oscillator signals.

[0037] The LC tank circuits of the differential oscillator circuits define the target resonant frequency and the auxiliary LC tank circuit shared by the differential oscillator circuits is configured to have a resonant frequency which is substantially twice the target resonant frequency so that the gain of the cross-coupling circuit is focussed at twice the target resonant frequency. DC gain and gain at an unwanted parasitic frequency of the cross-coupling circuit may also be avoided/attenuated in this way.

[0038] The first and second transistors may be connected as a cross-coupled pair of transistors. The auxiliary LC tank circuit may be connected between the first tail nodes or the first tail current paths of the differential oscillator circuits. The auxiliary LC tank circuit may be connected in parallel with the cross-coupled pair of transistors.

[0039] A shared current source or impedance may form part of the shared tail current path. Such a shared current source may be configured to regulate a bias current flowing along that current path.

[0040] The quadrature oscillator circuitry may comprise an auxiliary shared tail node. For each of the differential oscillator circuits, an auxiliary tail current path may form part of the auxiliary LC tank circuit and connect the first tail node to the auxiliary shared tail node via an auxiliary impedance (which is part of the auxiliary LC tank circuit). An auxiliary shared tail current path may connect the auxiliary shared tail node to an auxiliary shared voltage-source node. An auxiliary shared current source may form part of the auxiliary shared tail current path and be configured to regulate a bias current flowing along that current path. The auxiliary impedances may be or comprise inductors. The auxiliary impedances may be implemented together as a centre tapped inductor whose centre tap is the auxiliary shared tail node.

[0041] A capacitor may be connected in parallel with the auxiliary shared current source or the auxiliary shared tail current path, for example to filter out noise.

[0042] The auxiliary LC tank circuit may comprise a pair of first-node capacitors connecting the first tail nodes, respectively, to a voltage-source node. The pair of first-node capacitors may be implemented together as a single capacitor. The pair of first-node capacitors may be implemented as parasitic capacitances at the nodes concerned.

[0043] According to an embodiment of a third aspect of the present invention, there is provided quadrature oscillator circuitry, comprising: a first differential oscillator circuit having differential output nodes and configured to generate a first pair of differential oscillator signals at those output nodes, respectively; a second differential oscillator circuit having differential output nodes and configured to generate a second pair of differential oscillator signals at those output nodes, respectively; and a cross-coupling circuit comprising first and second transistors connected to cross-couple the first and second differential oscillator circuits. The first and second transistors may be connected as a cross-coupled pair of transistors.

[0044] According to an embodiment of a fourth aspect of the present invention, there is provided quadrature oscillator circuitry, comprising: first and second differential oscillator circuits, each differential oscillator circuit comprising first and second tail nodes, a pair of output nodes, and a pair of parallel current paths which extend in parallel between its first and second tail nodes via its output nodes, respectively, and each differential oscillator circuit configured to generate a pair of differential oscillator signals at its respective output nodes; and a cross-coupling circuit connected to cross-couple the differential oscillator circuits, wherein: for each of the differential oscillator circuits, a first tail current path connects the first tail node to a first voltage-source node and a second tail current path connects the second tail node to a second voltage-source node, one of the first and second voltage-source nodes for connection to a high-voltage source and the other of the first and second voltage-source nodes for connection to a low-voltage source; each of the differential oscillator circuits comprises a common-mode voltage node at which a common-mode voltage signal is produced, the common-mode voltage node either being an intermediate node of a potential divider connected between the output nodes of that differential oscillator circuit or being a node of the second tail current path of that differential oscillator circuit; and the cross-coupling circuit is connected to the common-mode nodes of the differential oscillator circuits and configured to control operation of one or both of the differential oscillator circuits to cause the common-mode voltage signals of the respective differential oscillator circuits to be substantially in antiphase.

[0045] In any of the aforementioned aspects, the pairs of differential oscillator signals of the first and second differential oscillator circuits may form a set of quadrature oscillator signals.

[0046] In any of the aforementioned aspects, the quadrature oscillator circuitry may be IQ oscillator circuitry. In such a case, the first differential oscillator circuit may be an I-side differential oscillator circuit, the pair of differential oscillator signals of the first differential oscillator circuit may be !+ and I- differential oscillator signals, respectively, the second differential oscillator circuit may be a Q-side differential oscillator circuit, and the pair of differential oscillator signals of the second differential oscillator circuit may be Q+ and Q-differential oscillator signals, respectively.

[0047] According to an embodiment of a fifth aspect of the present invention, there is provided phase lock loop circuitry comprising the quadrature oscillator circuitry of any of the aforementioned aspects.

[0048] According to an embodiment of a sixth aspect of the present invention, there is provided integrated circuitry, such as an IC chip, comprising the quadrature oscillator circuitry of any of the aforementioned first to fourth aspects or the phase lock loop circuitry of the aforementioned fifth aspect.

[0049] According to an embodiment of a seventh aspect of the present invention, there are provided analogue-to-digital converters (ADCs), digital-to-analogue converters (DACs), Serializer/Deserializer circuits (SERDES), Clock Data Recovery circuits (CDRs), Wireless Transceivers, Processors, or clocking circuitry comprising the quadrature oscillator circuitry of any of the aforementioned first to fourth aspects or the phase lock loop circuitry of the aforementioned fifth aspect.

[0050] According to an embodiment of an eighth aspect of the present invention, there is provided quadrature oscillator circuitry, comprising: a first differential oscillator circuit having differential output nodes and configured to generate a first pair of differential oscillator signals at those output nodes, respectively; a second differential oscillator circuit having differential output nodes and configured to generate a second pair of differential oscillator signals at those output nodes, respectively; and a cross-coupling circuit connected to cross-couple the first and second differential oscillator circuits. The cross-coupling circuit may comprise a pair of cross-coupled transistors.

[0051] Reference will now be made, by way of example, to the accompanying drawings, of which:

Figure 1, as mentioned above, is a circuit diagram presenting previously-considered differential oscillator circuits;

Figure 2, as mentioned above, is a schematic diagram of previously-considered quadrature oscillator circuitry;

Figure 3 presents two graphs showing voltage waveforms of differential oscillator circuits by way of example;

Figure 4 is a schematic circuit diagram of previously-considered quadrature oscillator circuitry;

Figure 5 is a schematic circuit diagram of previously-considered quadrature oscillator circuitry;
Figure 6 is a schematic circuit diagram of quadrature oscillator circuitry embodying the present invention;
Figure 7 presents two graphs showing voltage waveforms of differential oscillator circuits similar to those of Figure 3;
Figure 8 is a schematic circuit diagram of quadrature oscillator circuitry embodying the present invention;
Figure 9 is a schematic circuit diagram of quadrature oscillator circuitry embodying the present invention;
Figure 10 is a schematic circuit diagram of quadrature oscillator circuitry embodying the present invention;
Figure 11 is a schematic circuit diagram of PLL circuitry embodying the present invention; and
Figure 12 is a schematic circuit diagram of integrated circuitry embodying the present invention.

[0052] Before considering embodiments of the present invention, a number of previously-considered circuit arrangements and related analysis will be considered.

[0053] **Figure 3** presents two graphs showing voltage waveforms of differential oscillator circuits by way of example.

[0054] The upper graph shows voltage waveforms for the differential oscillator circuit 1 (as an example differential oscillator circuit of those of Figure 1), along with an indication of the nodes of the circuit to which the waveforms apply. The waveforms OUT+, OUT- are thus voltage waveforms taken at the output nodes 12 and 22, respectively. The waveform Vtail is a voltage waveform taken at the first tail node 2. Assuming that the LC tank circuit of the differential oscillator circuit 1 is tuned to have a resonant frequency f_0, so that the waveforms OUT+, OUT- have the frequency f_0, it can be seen that there is a component at double the resonant frequency, i.e. at $2f_0$, at the first tail node 2. The waveform Vtail thus peaks at the "zero-crossings" of the differential output swing OUT+, OUT-.

[0055] The lower graph shows the same voltage waveforms as the upper graph, but for two instances of the differential oscillator circuit 1, which may be referred to as differential oscillator circuit 1(I), being an I-side oscillator circuit, and differential oscillator circuit 1(Q), being a Q-side oscillator circuit. It is also assumed that the differential oscillator circuits 1(I) and 1(Q) are operating in quadrature so that their output differential oscillator signals may be referred to as I+ and I-, corresponding to OUT+ and OUT- for circuit 1(I), and Q+ and Q-, corresponding to OUT+ and OUT- for circuit 1(Q), where I+, I-, Q+ and Q- are a set of quadrature signals.

[0056] The waveforms I+ and I- are thus voltage waveforms taken at the output nodes 12 and 22 of circuit 1(I), respectively, and the waveforms Q+ and Q- are voltage waveforms taken at the output nodes 12 and 22 of circuit 1(Q), respectively. The waveform Vtail I is taken at the first tail node 2 of circuit 1(I) and the waveform Vtail Q is taken at the first tail node 2 of circuit 1(Q). Again, it is assumed that the LC tank circuits (LC tanks) of the circuits 1(I) and 1(Q) are tuned to have a resonant frequency f_0. The components at $2f_0$ for the two circuits 1(I) and 1(Q), i.e. Vtail I and Vtail Q, then form a differential pair as indicated. It therefore follows that if the waveforms at the first tail nodes 2 of the circuits 1(I) and 1(Q) are "forced" (or urged) to be differential, then quadrature operation can be achieved, i.e. where I+, I-, Q+ and Q- form a set of quadrature signals.

[0057] **Figure 4** is a schematic diagram showing differential oscillator circuits 1(I) and 1(Q) as discussed above. As before, like elements are denoted by like reference signs and thus the differential oscillator circuits 1(I) and 1(Q) will be understood based on the description of differential oscillator circuit 1 of Figure 1 above. Together, the differential oscillator circuits 1(I) and 1(Q) constitute quadrature oscillator circuitry 400, in particular by virtue of the inverting amplifier 402 shown schematically as coupling the first tail nodes 2 of the two circuits 1(I) and 1(Q) together, so as to force the waveforms at those tail nodes 2 to be differential. Although the inverting amplifier 402 coupling may appear one-way coupling from Figure 4, the coupling may be considered two-way so that the inverting amplifier 402 coupling is an inverting amplifier cross-coupling.

[0058] **Figure 5** is a schematic diagram of previously-considered quadrature oscillator circuitry 500 being an example implantation of the quadrature oscillator circuitry 400. Here, the circuits 1(I) and 1(Q) represented as equivalent circuits 1E(I) and 1E(Q), respectively, in line with circuit 1E of Figure 1, for simplicity. Again, like elements are denoted with like reference signs and duplicate description is omitted.

[0059] As shown in Figure 5, the inverting amplifier 402 coupling is implemented by providing transformer coils 502 and 504 along the first tail current paths 30 of the circuits 1E(I) and 1E(Q), respectively, along with respective parallel capacitors 506 and 508. The tank circuits (TC) 50 are tuned at the resonant frequency f_0 as before, and thus the parallel connected coils and capacitors 502 and 506, and 504 and 508, are tuned at twice that frequency (i.e. at $2f_0$,) in line with Figure 3. As indicated by the transformer dot notation (following the well-known dot convention), the transformer coils 502 and 504 (serving as primary and secondary transformer coils) are coupled to form a transformer which supplies a gain of -1. This causes the signals at the tail nodes 2 to be differential (see the lower graph of Figure 3), and thus the desired quadrature operation is achieved.

[0060] However, implementing such transformers in integrated circuitry, for example on an IC chip, with identical primary and secondary turns, is complicated and requires a large area.

[0061] **Figure 6** is a schematic diagram of quadrature oscillator circuitry 600 also being an implementation of the quadrature oscillator circuitry 400 using circuits 1E(I) and 1E(Q) as in Figure 5, but with an improved imple-

mentation of the inverting amplifier 402 coupling. Again, like elements are denoted with like reference signs and duplicate description is omitted. Quadrature oscillator circuitry 600 embodies the present invention.

[0062] As shown in Figure 6, the inverting amplifier 402 coupling is implemented by providing cross-coupled transistor 602 and 604, in this case NMOS FETs, along the respective first tail current paths 30, which current paths 30 are configured to meet at a shared tail node 606. A shared tail current path 608 (shared by both current paths 30) connects the shared tail node 606 to a shared voltage-source node being the first voltage-source node 32, in this case ground supply (GND). A shared current source 610 is provided along the shared tail current path 608 to regulate or control a bias current Ibias flowing along that path (and thus a combination of the currents flowing along the two current paths 30). As such, the individual current sources 34 are not needed. The shared current source 610 could be replaced with an impedance such as a resistor.

[0063] The source terminals of the transistors 602, 604 are connected to the shared tail node 606 and their drain terminals are connected to the respective first tail nodes 2, such that their channels form respective parts of the respective first tail current paths 30. The gate terminals of the transistors 602 and 604 are connected to each other's drain terminals. The cross-coupled transistors 602 and 604 act as cross-coupled inverting amplifiers, forcing the waveforms at the respective first tail nodes 2 to be differential.

[0064] Also provided is an auxiliary LC tank circuit 620 which serves to focus the gain of the cross-coupled pair of transistors 602, 604 at the desired frequency $2f_0$ (see Figure 3), prevent large gain at DC (i.e. at 0 Hz), and also avoid or reduce oscillation at an (unwanted) parasitic frequency as with e.g. a relaxation oscillator. The LC tank circuit 620 is connected between the first nodes 2 or between the first tail current paths 30, effectively in parallel with the cross-coupled transistors 602, 604.

[0065] The LC tank circuit 620 comprises auxiliary capacitors 622 which connect the respective first tail nodes 2 to the voltage-source node 32, in this case to ground supply (GND). Further, auxiliary inductors 628 and 630 connect the respective first tail nodes 2 to an auxiliary shared tail node 632 along respective auxiliary tail current paths. An auxiliary shared tail current path 634 connects the auxiliary shared tail node 632 to an auxiliary shared voltage-source node, in this case being the first voltage source-node 32, i.e. ground supply (GND). An auxiliary shared current source 636 is provided along the auxiliary shared tail current path 634 to regulate or control a bias current Ibias flowing along that path. A capacitor 638 is connected in parallel with the current source 636 (e.g. between the node 632 and GND) so as to filter out noise from the current source 636.

[0066] The inductors 628, 630 may be implemented together as a centre-tapped inductor (winding/coil) whose centre tap (i.e. contact) is connected to node 632 and whose respective ends are connected to the first tail nodes 2, as shown in Figure 6. Such a centre-tapped inductor may be referred to as a differential inductor. The decoupling capacitor 638 is used to AC ground the centre tap.

[0067] The auxiliary shared current source 636 could be replaced with an impedance such as a resistor.

[0068] Along with the auxiliary LC tank circuit 620 being tuned at $2f_0$, the LC tank circuits 50 are tuned at f_0 as before. Thus, the desired quadrature operation is achieved (see Figure 3), but without needing the transformer of Figure 5.

[0069] The differential inductor is much easier to implement compared to transformers (see Figure 5) and has more compact area and a higher Q-factor. Moreover, the current used in the added differential pair of transistors 602, 604 flows also via the first tail nodes 2 (i.e. via the cores of the two differential oscillator circuits), thus contributing to the gain and swing of the quadrature output signals I+, I-, Q+, Q-. It will be appreciated that the same applies to the embodiments disclosed later herein.

[0070] The inventors have also considered other ways to implement quadrature oscillator circuitry. In this regard, reference is made to **Figures 7 and 8.**

[0071] Starting first with Figure 8, there is shown a schematic diagram of quadrature oscillator circuitry 700, embodying the present invention, which is the same as quadrature oscillator circuitry 400 of Figure 4, except that the inverting amplifier 402 has been removed. Instead, in each of the circuits 1(I) and 1(Q) of Figure 8, a pair of impedances 702 are connected in series between the two parallel current paths 10, 20 (effectively between the output nodes 12, 22) so as to define a common-mode node 704 therebetween at which a common-mode voltage signal is generated. The impedances 702 could for example be, or comprise, capacitors. An inverting amplifier 706 is connected between the common-mode nodes 704. As before, like elements are denoted with like reference signs between Figures 4 and 8 so that duplicate description is omitted.

[0072] Figure 7 presents two graphs which are the same as those in Figure 3 except that the Vtail waveforms taken at the relevant first tail nodes 2 have been replaced with Vcm waveforms (common-mode waveforms) taken at the relevant common-mode node 704.

[0073] Thus, in the upper graph, which represents a single differential oscillator circuit 1, the common-mode voltage waveform Vcm is equivalent to one taken at node 704 in circuit 1(I) of Figure 8. Assuming again that the LC tank circuit of the circuit 1 (and 1(I)) is tuned to have a resonant frequency f_0, it can be seen that there is component (i.e. Vcm) at double the resonant frequency, i.e. at $2f_0$, at the common-mode nodes 704. The waveform Vcm thus peaks at the "zero-crossings" of the differential output swing OUT+, OUT-.

[0074] In the lower graph, which corresponds to the pair of differential oscillator circuits 1(I) and 1(Q) in Figure 8, the common-mode voltage waveforms Vcm-I and

Vcm-Q are taken at the nodes 704 of the differential oscillator circuits 1(I) and 1(Q), respectively. Again, it is assumed that the LC tank circuits of the circuits 1(I) and 1(Q) are tuned to have a resonant frequency f_0. The components at $2f_0$ for the two circuits 1 (I) and 1 (Q), i.e. Vcm-I and Vcm-Q, then form a differential pair as indicated.

[0075] It therefore follows that if the waveforms at the common-mode nodes 704 of the circuitry 1(I) and 1(Q) are forced (or urged) to be differential, then quadrature operation can be achieved, i.e. where I+, I-, Q+, Q- form a set of quadrature signals. The connection of the inverting amplifier 706 between the common-mode nodes 704 of the circuits 1(I) and 1(Q) in Figure 8 serves to create this operation. Although the inverting amplifier 802 coupling may appear one-way coupling from Figure 8, the coupling may be considered two-way so that the inverting amplifier 802 coupling is an inverting amplifier cross-coupling.

[0076] Of course, it will be appreciated that such common-mode nodes 704 could be provided in a similar way for pairs of the other differential oscillator circuits shown in Figure 1, for example, and the waveforms at those nodes controlled with an inverting amplifier arrangement as with inverting amplifiers 706 in Figure 8, to arrive at other embodiments of the present invention. The present disclosure will be understood accordingly.

[0077] **Figure 9** is a schematic diagram of quadrature oscillator circuitry 800 embodying the present invention, being an implementation of the quadrature oscillator circuitry 700, with the circuits 1(I) and 1(Q) represented as equivalent circuits 1E(I) and 1E(Q), respectively, in line with circuit 1E of Figure 1. Again, like elements are denoted with like reference signs and duplicate description is omitted.

[0078] As shown in Figure 9, the inverting amplifier coupling 706 is implemented by providing cross-coupled transistors 802 and 804, in this case NMOS FETs, along the respective first tail current paths 30 which current paths 30 are configured to meet at a shared tail node 806. A shared tail current path 808 (shared by both current paths 30) connects the shared tail node 806 to a shared voltage-source node being the first voltage-source node 32, in this case ground supply (GND).

[0079] Current sources 810, 812 are provided along the second current paths 40 as indicated, to regulate or control respective bias currents Ibias flowing along those paths. As such, the current sources 34 are not needed. The current sources 810, 812 could each be replaced with an impedance such as a resistor, but of course in this case the bias current would not be regulated.

[0080] The source terminals of the transistors 802, 804 are connected to the shared tail node 806 and their drain terminals are connected to the respective first tail nodes 2, such that their channels form respective parts of the respective first tail current paths 30. The gate terminals of the transistors 802 and 804 are connected to the common-mode nodes 704 of each other's differential oscillator circuit. That is, the gate terminal of the transistor 802 is connected to the common-mode node 704 of the circuit 1E(Q) and the gate terminal of the transistor 804 is connected to the common-mode node 704 of the circuit 1E(I). In this sense, the transistors 802 and 804 are cross-coupled. Recall that the impedances 702 may be capacitors. With this in mind, the gate terminals of the transistors 802, 804 are coupled by respective resistors 814, 816 to their drain terminals to DC bias (self-bias) their gate voltages. Thus, at DC the transistors 802, 804 are diode-connected. Of course, the gate terminals of the transistors 802 and 804 could be resistor coupled to a voltage-source node instead for similar reasons.

[0081] At 2fo the transistors 802, 804 operate as a cross-coupled pair, i.e. as cross-coupled inverting amplifiers, forcing a differential AC current signal into the circuits 1E(I) and 1E(Q), which in turn forces the waveforms at the respective common-mode nodes 704 to be differential. Thus, the desired quadrature operation is achieved (see Figure 7).

[0082] Again, the current used in the added differential pair of transistors 802, 804 flows also via the first tail nodes 2 (i.e. via the cores of the two differential oscillator circuits), thus contributing to the gain and swing of the quadrature output signals I+, I-, Q+, Q-. That is, the differential pair of transistors 802, 804 reuse the current flowing through the two differential oscillator circuits and no extra current is needed. Further, the Figure 9 embodiment is smaller in terms of needed circuit area as compared to the Figure 6 embodiment.

[0083] **Figure 10** is a schematic diagram of quadrature oscillator circuitry 900 embodying the present invention, being another implementation of the quadrature oscillator circuitry 700, with the circuits 1(I) and 1(Q) represented as equivalent circuits 1E(I) and 1E(Q), respectively, in line with circuit 1E of Figure 1.

[0084] The Figure 10 embodiment is similar to the Figure 9 embodiment, and as such like elements are denoted with like reference signs and duplicate description is omitted.

[0085] The difference between quadrature oscillator circuitry 900 and quadrature oscillator circuitry 800 is that the impedances 702 (and thus nodes 704) have been removed. The gate terminals of the transistors 802 and 804 are connected to the second tail nodes 4 of each other's differential oscillator circuit (which serve as common-mode nodes) via respective capacitors 902, 904, rather than to nodes 704. That is, the gate terminal of the transistor 802 is connected to the second tail node 4 of the circuit 1E(Q) via capacitor 904, and the gate terminal of the transistor 804 is connected to the second tail node 4 of the circuit 1E(I) via capacitor 902. In this sense, the transistors 802 and 804 are cross-coupled in Figure 10.

[0086] Given the capacitors 902, 904, the gate terminals of the transistors 802, 804 are coupled by respective resistors 814, 816 to their drain terminals to DC bias (self-bias) their gate voltages and similar considerations apply as in Figure 9. Of course, the gate terminals of the transistors 802 and 804 could be resistor coupled to a volt-

age-source node instead for similar reasons.

[0087] Again, at 2fo the transistors 802, 804 operate as a cross-coupled pair, i.e. as cross-coupled inverting amplifiers, forcing a differential AC current signal into the circuits 1E(I) and 1E(Q), which in turn forces the waveforms at the respective common-mode nodes (in this case, the second tail nodes 4) to be differential. Thus, the desired quadrature operation is achieved (see Figure 7). It will be appreciated that other nodes along the second tail current paths 40 could serve as the common-mode nodes.

[0088] Again, the current used in the added differential pair of transistors 802, 804 flows also via the first tail nodes 2 (i.e. via the cores of the two differential oscillator circuits), thus contributing to the gain and swing of the quadrature output signals I+, I-, Q+, Q-. That is, the differential pair of transistors 802, 804 reuse the current flowing through the two differential oscillator circuits and no extra current is needed. Further, the Figure 10 embodiment is smaller in terms of needed circuit area as compared to the Figure 6 embodiment.

[0089] It will be appreciated that the waveforms at such common-mode nodes 704 and 4 could be utilised in a similar way for pairs of the other differential oscillator circuits shown in Figure 1, for example, and controlled with an inverting amplifier arrangement as in Figures 9 and 10 to arrive at other embodiments of the present invention. The present disclosure will be understood accordingly.

[0090] **Figure 11** is a schematic diagram of phase lock loop (PLL) circuitry 1000 embodying the present invention.

[0091] The PLL circuitry comprises a phase detector 1002, a (low-pass) filter 1004, a VCO 1006 and a divider 1008, connected together as shown in Figure 11. The VCO may be implemented using any of the quadrature oscillator circuitry embodiments disclosed herein, bearing in mind that the differential oscillator circuits of those quadrature oscillator circuitry embodiments may be implemented in many different ways as exemplified by way of the range of circuits depicted in Figure 1.

[0092] The skilled reader will understand the basic operation of PLL circuitry such as that depicted in Figure 11. Nevertheless, as a brief summary, the VCO 1006 generates the output signal O/P and the phase detector 1002 compares the phase of that output signal O/P (as divided by the divider 1008) with the phase of an input (periodic) reference signal REF. The output of the phase detector 1002 depends on the detected phase difference and is filtered by the filter 1004 before being input to the VCO 1006 to control the frequency of the output signal O/P. In the present case, the output signal O/P may be considered to be a quadrature output signal in line with the quadrature oscillator circuitry embodiments considered above, however the phase detector 1002 may be supplied (via the divider 1008) with just one of the four oscillator signals which make up the quadrature output signal.

[0093] Of course, Figure 11 depicts just one possible PLL topology and the present invention extends to any PLL topology where its VCO is implemented using any of the quadrature oscillator circuitry embodiments disclosed herein.

[0094] Any of the circuitry disclosed herein may be implemented as integrated circuitry, for example as (or as part of) and IC chip, such as a flip chip. **Figure 12** is a schematic diagram of integrated circuitry 2000 and 3000 embodying the present invention.

[0095] Integrated circuitry 2000 and 3000 may be representative of some or all of an IC chip. Integrated circuitry 2000 comprises quadrature oscillator circuitry according to the present invention, for example quadrature oscillator circuitry 600, 700, 800 or 900. Integrated circuitry 3000 comprises PLL circuitry according to the present invention, for example PLL circuitry 1000 which comprises VCO 1006. VCO 1006 may be implemented as quadrature oscillator circuitry 600, 700, 800 or 900, albeit with e.g. the L or C elements of their tank circuits adapted to be controlled with voltage control as explained earlier.

[0096] The present invention extends to integrated circuitry and IC chips as mentioned above, circuit boards comprising such IC chips, and communication networks (for example, internet fiber-optic networks and wireless networks) and network equipment of such networks, comprising such circuit boards. It will be appreciated that PLL circuitry (that has quadrature outputs) may be employed in various applications where clocking is required. The present invention extends to such applications, and examples include, but are not limited to, analogue-to-digital converters (ADCs), digital-to-analogue converters (DACs), Serializer/Deserializer circuits (SERDES), Clock Data Recovery circuits (CDRs), Wireless Transceivers, Processors and related clocking circuitry, etc..

[0097] The present invention may be embodied in many different ways in the light of the above disclosure, within the spirit and scope of the appended claims.

[0098] The disclosure extends to the following set of numbered statements:

S1. Quadrature oscillator circuitry, comprising:

first and second differential oscillator circuits, each differential oscillator circuit comprising first and second tail nodes, a pair of output nodes, and a pair of parallel current paths which extend in parallel between its first and second tail nodes via its output nodes, respectively, and each differential oscillator circuit configured to generate a pair of differential oscillator signals at its respective output nodes; and

a cross-coupling circuit connected to cross-couple the differential oscillator circuits,

wherein:

for each of the differential oscillator circuits,

a first tail current path connects the first tail node to a first voltage-source node and a second tail current path connects the second tail node to a second voltage-source node, one of the first and second voltage-source nodes for connection to a high-voltage source and the other of the first and second voltage-source nodes for connection to a low-voltage source;

each of the differential oscillator circuits comprises a common-mode voltage node at which a common-mode voltage signal is produced, the common-mode voltage node either being an intermediate node of a potential divider connected between the parallel current paths of that differential oscillator circuit or being a node of the second tail current path of that differential oscillator circuit; and

the cross-coupling circuit comprises, for at least one or each of the differential oscillator circuits, a current-control device which forms part of the first tail current path of that differential oscillator circuit and is configured to control the current flowing along that first tail current path based on the common-mode voltage signal of the other one of the differential oscillator circuits to cause the common-mode voltage signals of the respective differential oscillator circuits to be substantially in antiphase.

S2. The quadrature oscillator circuitry of statement S1, wherein:

the cross-coupling circuit comprises an inverting amplifier configured, for at least one or each of the differential oscillator circuits, to control the current-control device of that differential oscillator circuit based on the common-mode voltage signal of the other one of the differential oscillator circuits.

S3. The quadrature oscillator circuitry of statement S1 or S2, wherein:

the cross-coupling circuit comprises first and second transistors as current-control devices for the first and second differential oscillator circuits, respectively;

the first and second transistors form respective parts of the first tail current paths of the first and second differential oscillator circuits, respectively, so that current flowing along the respective first tail current paths flows through the first and second transistors, respectively; and

the gate or base terminals of the first and second transistors are connected to the common-mode nodes of the second and first differential oscillator circuits, respectively, so that they are controlled by the common-mode voltage signals produced at the common-mode nodes of the second and first differential oscillator circuits, respectively.

S4. The quadrature oscillator circuitry of statement S3, wherein:

each of the differential oscillator circuits comprises a current source which forms part of its second tail current path and is configured to regulate a bias current flowing along that current path; and

the common-mode voltage nodes of the first and second differential oscillator circuits are their second tail nodes or nodes of their second tail current paths between their second tail nodes and their current sources.

S5. The quadrature oscillator circuitry of statement S4, wherein:

the gate or base terminals of the first and second transistors are connected to the common-mode nodes of the second and first differential oscillator circuits, respectively, via impedances,

optionally wherein said impedances are or comprise capacitors.

S6. The quadrature oscillator circuitry of statement S3, wherein:

the common-mode voltage nodes of the first and second differential oscillator circuits are the intermediate nodes of their respective potential dividers; and

for each of the differential oscillator circuits, its potential divider comprises a potential-divider impedance connected between one of its parallel current paths and its intermediate node and another potential-divider impedance connected between the other one of its parallel current paths and its intermediate node,

optionally wherein said potential-divider impedances are or comprise capacitors.

S7. The quadrature oscillator circuitry of statement S6, wherein each of the differential oscillator circuits comprises a current source which forms part of its second tail current path to regulate a bias current flowing along that current path.

S8. The quadrature oscillator circuitry of any of statements S3 to S7, wherein the gate or base terminals of the first and second transistors are connected via respective impedances to their drain or collector terminals or to a voltage-source node.

S9. Quadrature oscillator circuitry, comprising:

first and second differential oscillator circuits, each differential oscillator circuit comprising first and second tail nodes, a pair of output nodes, and a pair of parallel current paths which extend in parallel between its first and second tail nodes via its output nodes, respectively, and each differential oscillator circuit configured to generate a pair of differential oscillator signals at its respective output nodes; and
a cross-coupling circuit comprising first and second transistors connected to cross-couple the differential oscillator circuits,
wherein:

for each of the differential oscillator circuits, a first tail current path connects the first tail node to a first voltage-source node and a second tail current path connects the second tail node to a second voltage-source node, one of the first and second voltage-source nodes for connection to a high-voltage source and the other of the first and second voltage-source nodes for connection to a low-voltage source;
the first and second transistors are connected to form respective parts of the first tail current paths of the differential oscillator circuits, respectively, so that current flowing along the respective first tail current paths flows through the respective transistors;
the gate or base terminals of the first and second transistors are connected to the first tail nodes of the second and first differential oscillator circuits, respectively, so that they are controlled by voltage signals produced at the first tail nodes of the second and first differential oscillator circuits, respectively;
the first tail current paths extend from the first tail nodes via the first and second transistors, respectively, to a shared tail node;
a shared tail current path connects the shared tail node to a shared voltage-source node, being the first voltage-source node of both of the differential oscillator circuits;
each of said differential oscillator circuits comprises an LC tank circuit configured to have a target resonant frequency; and
the quadrature oscillator circuitry comprises an auxiliary LC tank circuit shared by the differential oscillator circuits and configured to have a resonant frequency which is substantially twice the target resonant frequency.

S10. The quadrature oscillator circuitry of statement S9, wherein:

the first and second transistors are connected as a cross-coupled pair of transistors; and/or
the auxiliary LC tank circuit is connected between the first tail nodes or the first tail current paths of the differential oscillator circuits; and/or
the auxiliary LC tank circuit is connected in parallel with the cross-coupled pair of transistors.

S11. The quadrature oscillator circuitry of statement S9 or S10, wherein:
a shared current source or impedance forms part of the shared tail current path, the shared current source configured to regulate a bias current flowing along that current path.

S12. The quadrature oscillator circuitry of any of statements S9 to S11, comprising an auxiliary shared tail node, wherein:

for each of the differential oscillator circuits, an auxiliary tail current path forms part of the auxiliary LC tank circuit and connects the first tail node to the auxiliary shared tail node via an auxiliary impedance; and
an auxiliary shared tail current path connects the auxiliary shared tail node to an auxiliary shared voltage-source node,
optionally wherein:

an auxiliary shared current source forms part of the auxiliary shared tail current path and is configured to regulate a bias current flowing along that current path; and/or
the auxiliary impedances are or comprise inductors; and/or
the auxiliary impedances are implemented together as a centre tapped inductor whose centre tap is the auxiliary shared tail node.

S13. The quadrature oscillator circuitry of any of statements S9 to S12, wherein the auxiliary LC tank circuit comprises a pair of first-node capacitors connecting the first tail nodes, respectively, to a voltage-source node.

S14. Phase lock loop circuitry comprising the quadrature oscillator circuitry of any of the preceding statements.

S15. Integrated circuitry, such as an IC chip, comprising the quadrature oscillator circuitry of any of statements S1 to S13 or the phase lock loop circuitry of statement S14.

Claims

1. Quadrature oscillator circuitry, comprising:

first and second differential oscillator circuits, each differential oscillator circuit comprising first and second tail nodes, a pair of output nodes, and a pair of parallel current paths which extend in parallel between its first and second tail nodes via its output nodes, respectively, and each differential oscillator circuit configured to generate a pair of differential oscillator signals at its respective output nodes; and

a cross-coupling circuit comprising first and second transistors connected to cross-couple the differential oscillator circuits,

wherein:

for each of the differential oscillator circuits, a first tail current path connects the first tail node to a first voltage-source node and a second tail current path connects the second tail node to a second voltage-source node, one of the first and second voltage-source nodes for connection to a high-voltage source and the other of the first and second voltage-source nodes for connection to a low-voltage source;

the first and second transistors are connected to form respective parts of the first tail current paths of the differential oscillator circuits, respectively, so that current flowing along the respective first tail current paths flows through the respective transistors;

the gate or base terminals of the first and second transistors are connected to the first tail nodes of the second and first differential oscillator circuits, respectively, so that they are controlled by voltage signals produced at the first tail nodes of the second and first differential oscillator circuits, respectively;

the first tail current paths extend from the first tail nodes via the first and second transistors, respectively, to a shared tail node;

a shared tail current path connects the shared tail node to a shared voltage-source node, being the first voltage-source node of both of the differential oscillator circuits;

each of said differential oscillator circuits comprises an LC tank circuit configured to have a target resonant frequency; and

the quadrature oscillator circuitry comprises an auxiliary LC tank circuit shared by the differential oscillator circuits and configured to have a resonant frequency which is substantially twice the target resonant frequency.

2. The quadrature oscillator circuitry as claimed in claim 1, wherein:

the first and second transistors are connected as a cross-coupled pair of transistors; and/or

the auxiliary LC tank circuit is connected between the first tail nodes or the first tail current paths of the differential oscillator circuits; and/or

the auxiliary LC tank circuit is connected in parallel with the cross-coupled pair of transistors.

3. The quadrature oscillator circuitry as claimed in claim 1 or 2, wherein:

a shared current source or impedance forms part of the shared tail current path, the shared current source configured to regulate a bias current flowing along that current path.

4. The quadrature oscillator circuitry as claimed in any of claims 1 to 3, comprising an auxiliary shared tail node, wherein:

for each of the differential oscillator circuits, an auxiliary tail current path forms part of the auxiliary LC tank circuit and connects the first tail node to the auxiliary shared tail node via an auxiliary impedance; and

an auxiliary shared tail current path connects the auxiliary shared tail node to an auxiliary shared voltage-source node,

optionally wherein:

an auxiliary shared current source forms part of the auxiliary shared tail current path and is configured to regulate a bias current flowing along that current path; and/or

the auxiliary impedances are or comprise inductors; and/or

the auxiliary impedances are implemented together as a centre tapped inductor whose centre tap is the auxiliary shared tail node; and/or

a capacitor is connected in parallel with the auxiliary shared current source or the auxiliary shared tail current path.

5. The quadrature oscillator circuitry as claimed in any of claims 1 to 4, wherein the auxiliary LC tank circuit comprises a pair of first-node capacitors connecting the first tail nodes, respectively, to a voltage-source node.

6. Phase lock loop circuitry comprising the quadrature oscillator circuitry as claimed in any of the preceding claims.

7. Integrated circuitry, such as an IC chip, comprising the quadrature oscillator circuitry as claimed in any of claims 1 to 5 or the phase lock loop circuitry as claimed in claim 6.

Fig. 1

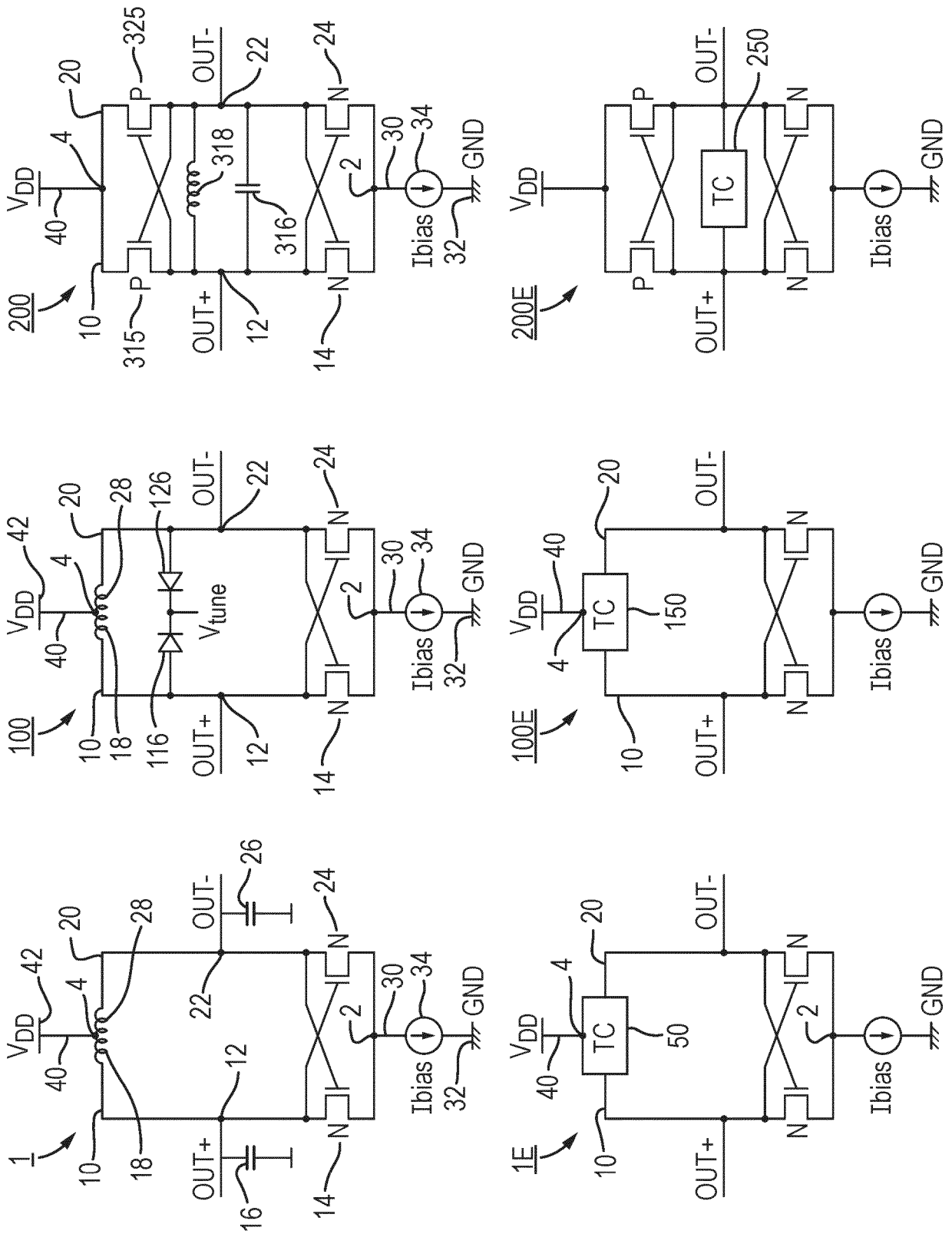
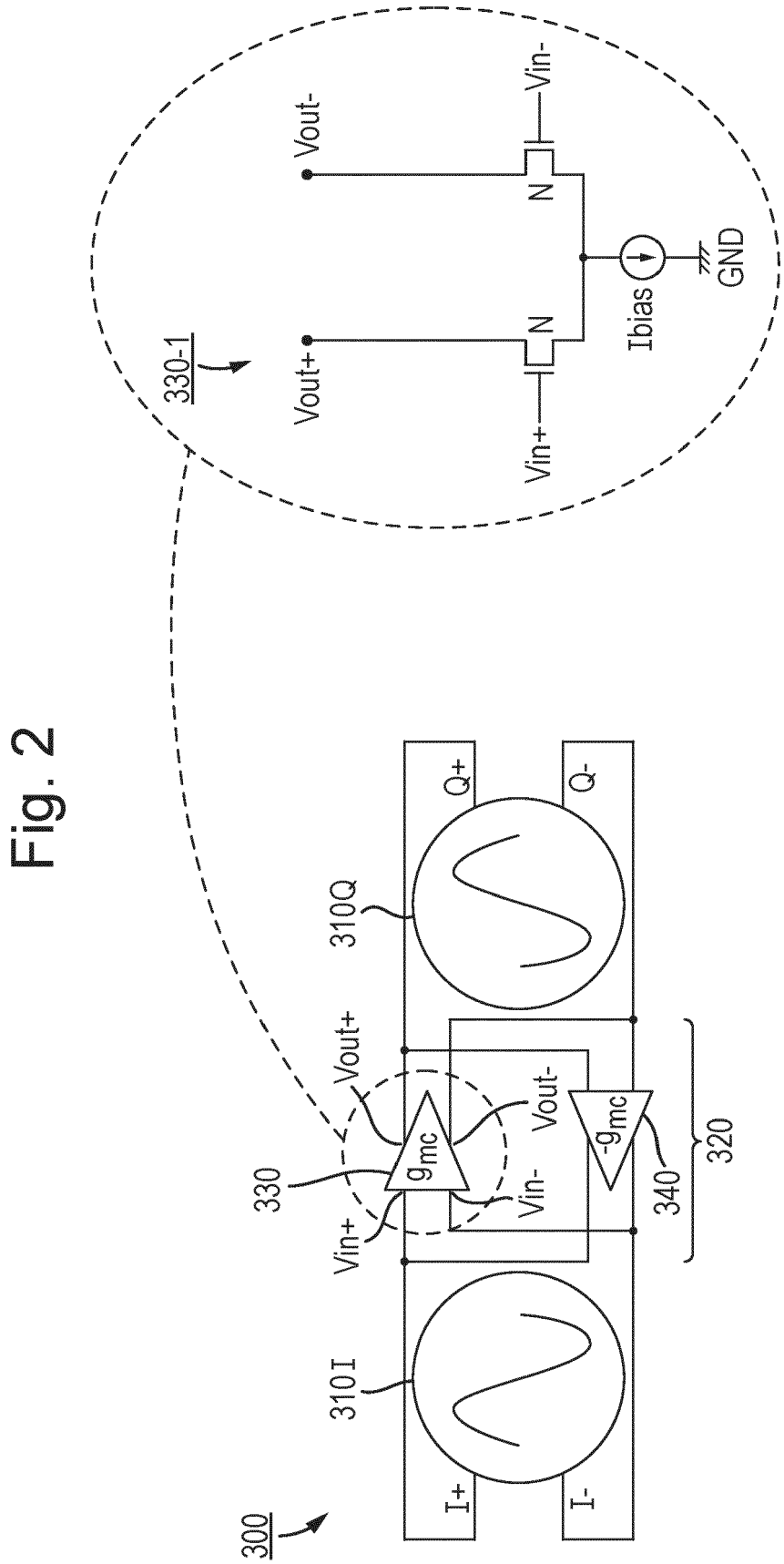


Fig. 2


300
I+
I-
310I
Q+
Q-
310Q
330
Vout+
Vout-
Vin+
Vin-
g_{mc}
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320
340
330-1
N
N
Ibias
GND

Fig. 3

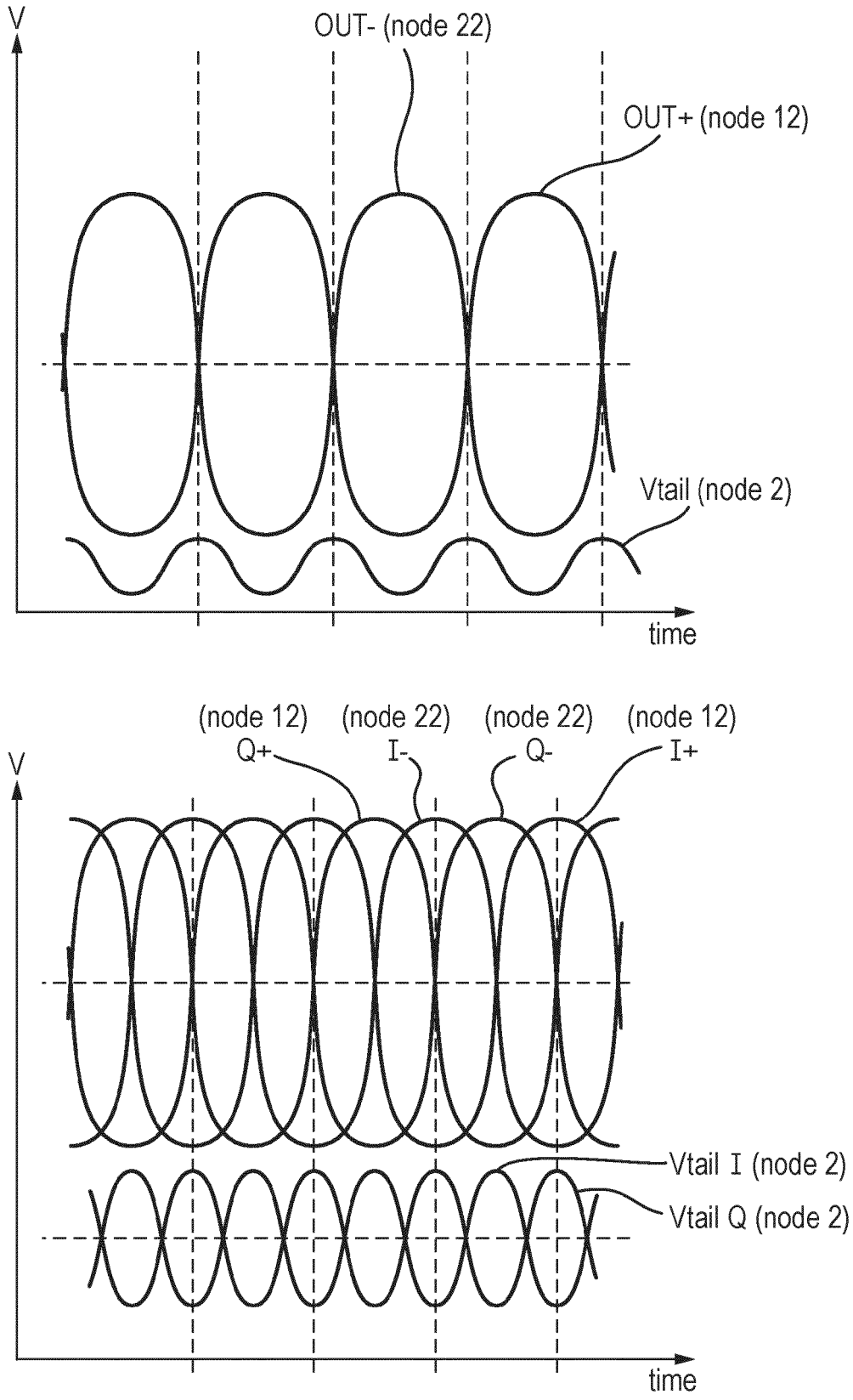

V
OUT- (node 22)
OUT+ (node 12)
Vtail (node 2)
time
(node 12)
Q+
(node 22)
I-
(node 22)
Q-
(node 12)
I+
V
Vtail I (node 2)
Vtail Q (node 2)
time

Fig. 4

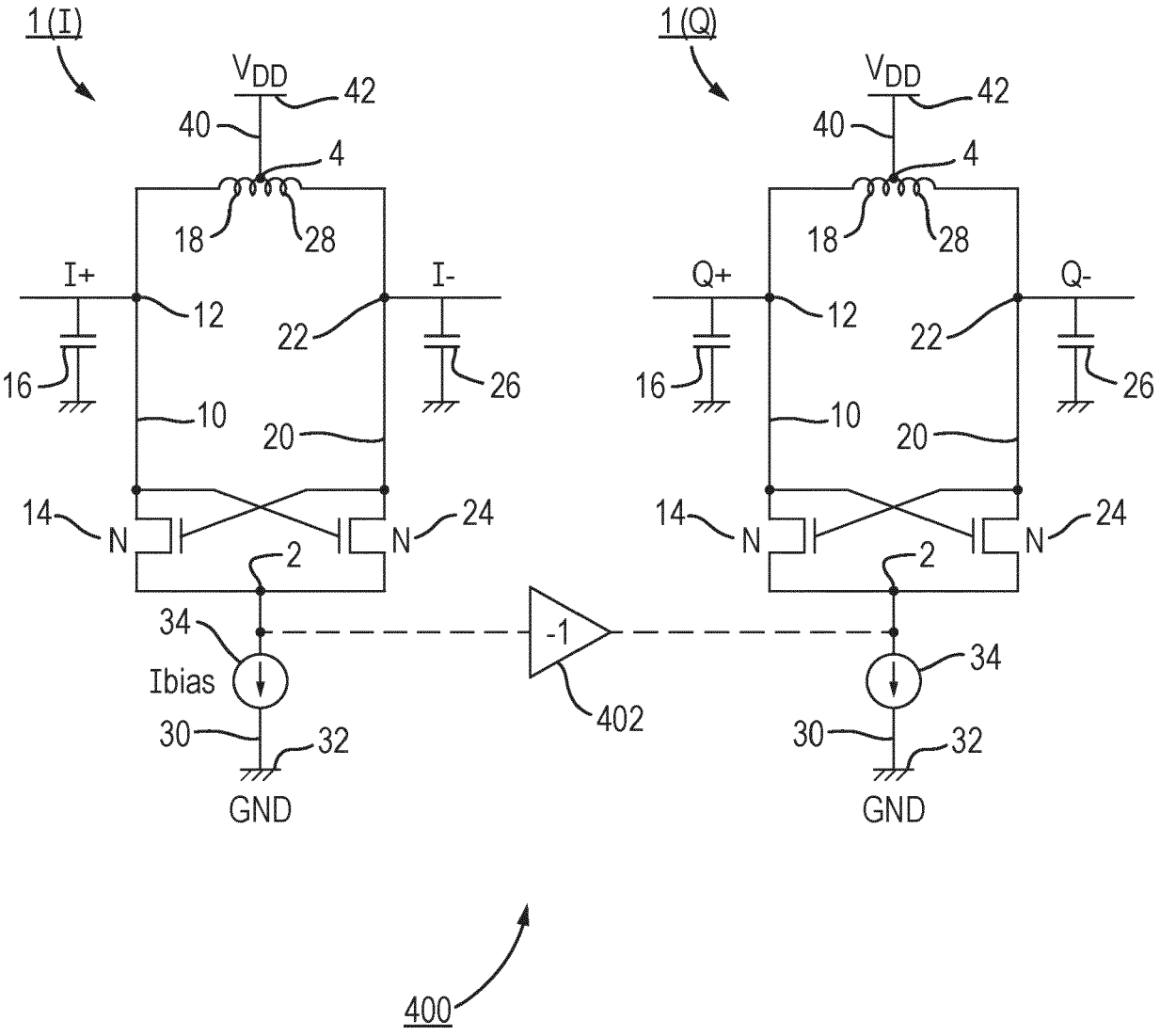

1(I)
1(Q)
VDD
42
40
4
18
28
I+
I-
Q+
Q-
12
22
16
26
10
20
14
N
24
2
34
Ibias
-1
402
30
32
GND
400

Fig. 5

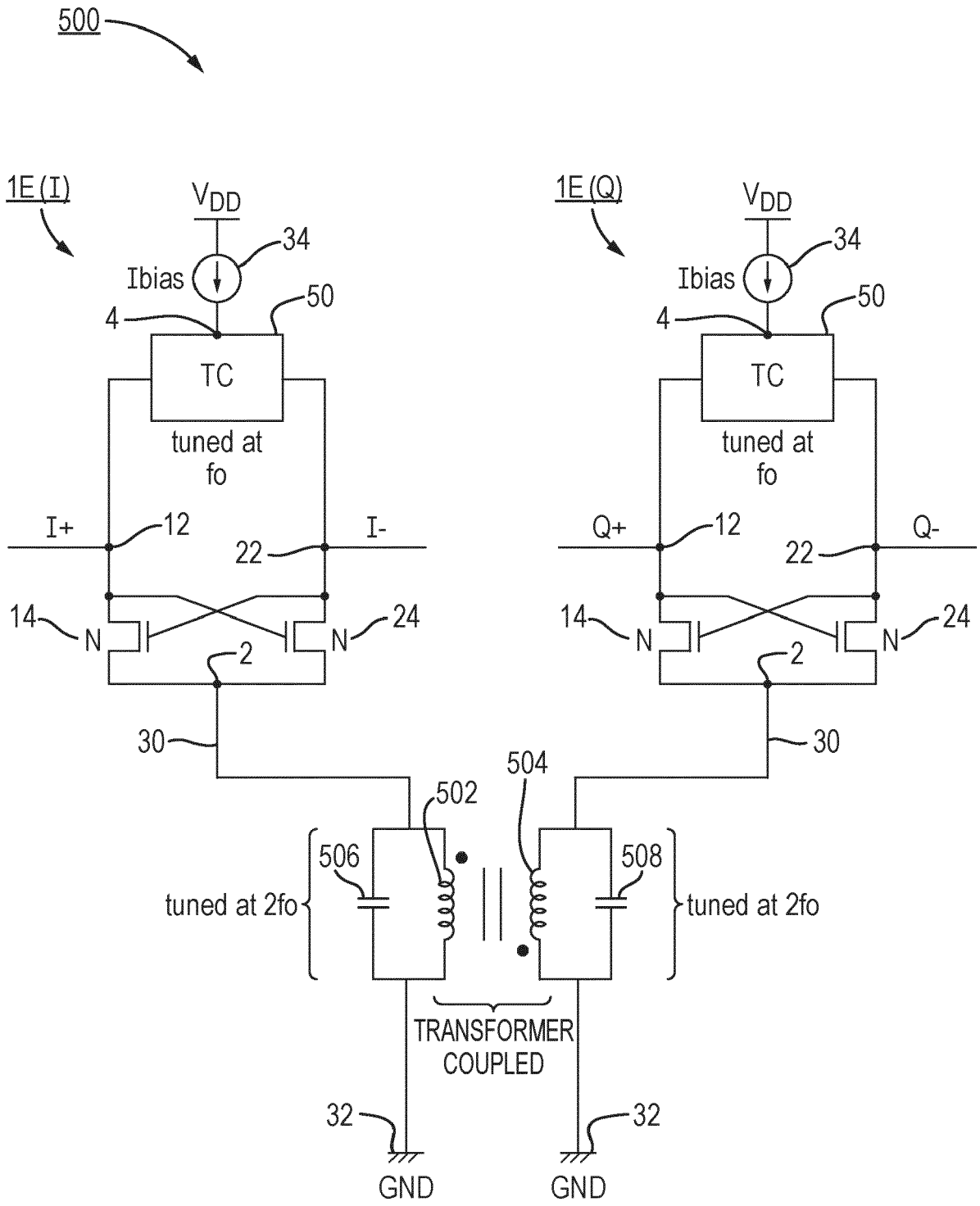

500
1E(I)
VDD
34
Ibias
50
4
TC
tuned at
fo
I+
12
22
I-
14
N
N
24
2
30
1E(Q)
VDD
34
Ibias
50
4
TC
tuned at
fo
Q+
12
22
Q-
14
N
N
24
2
30
504
502
506
508
tuned at 2fo
tuned at 2fo
TRANSFORMER
COUPLED
32
32
GND
GND

Fig. 6

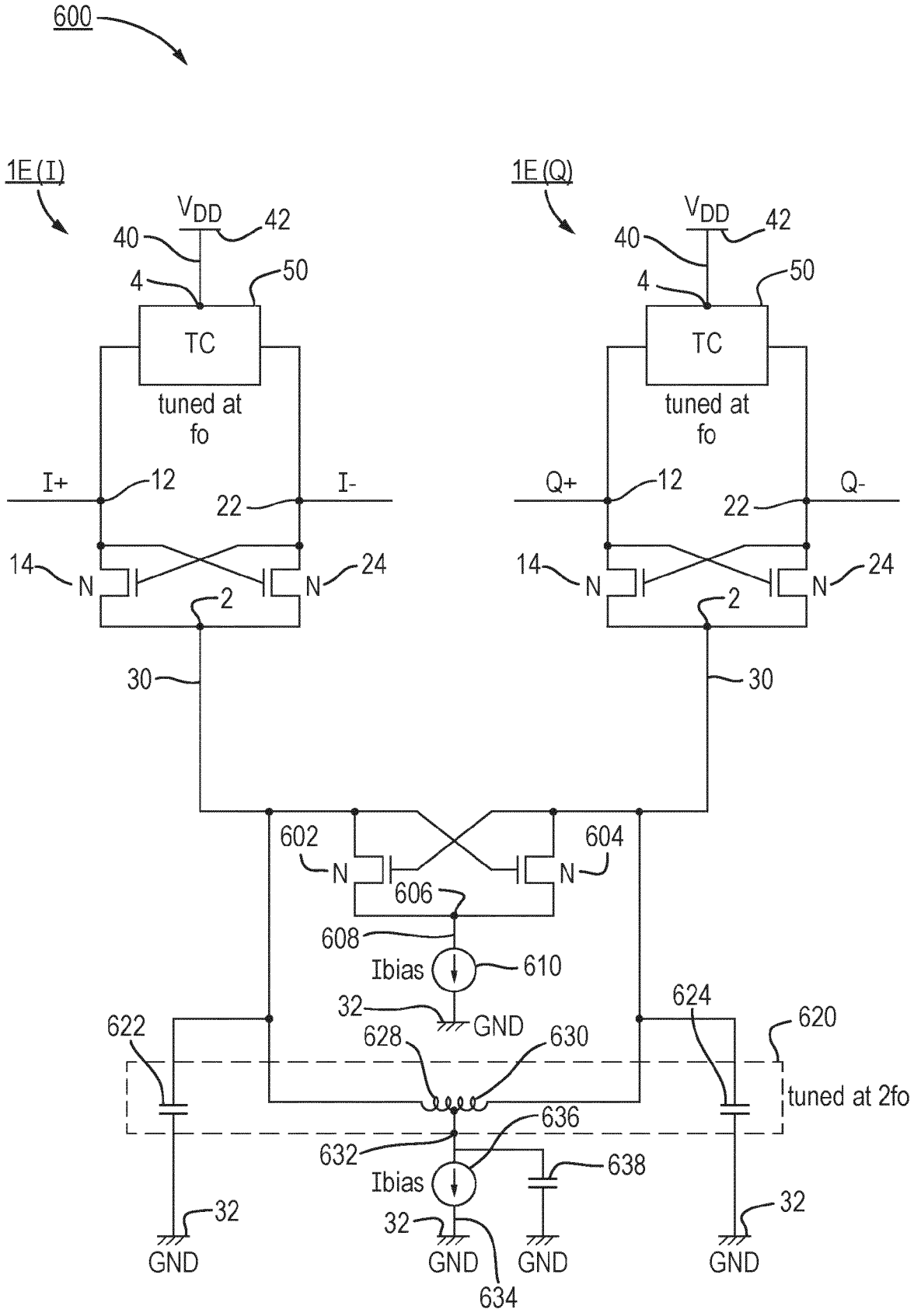

600
1E(I)
1E(Q)
VDD
42
40
4
50
TC
tuned at fo
I+
I-
Q+
Q-
12
22
14
N
24
2
30
602
604
606
608
Ibias
610
32
GND
622
624
620
628
630
636
632
638
634
tuned at 2fo

Fig. 7

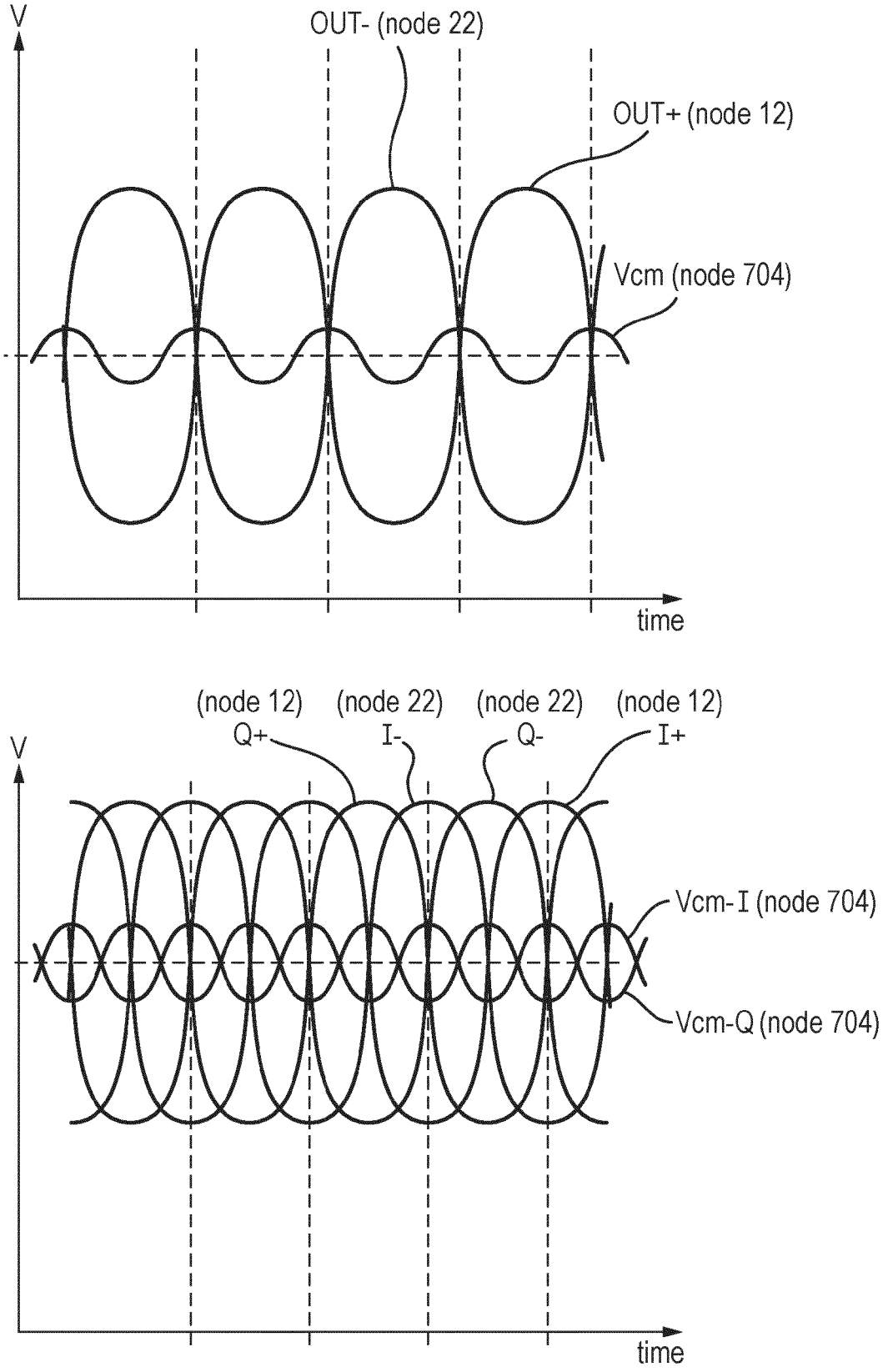

V
OUT- (node 22)
OUT+ (node 12)
Vcm (node 704)
time
(node 12)
Q+
(node 22)
I-
(node 22)
Q-
(node 12)
I+
V
Vcm-I (node 704)
Vcm-Q (node 704)
time

Fig. 8

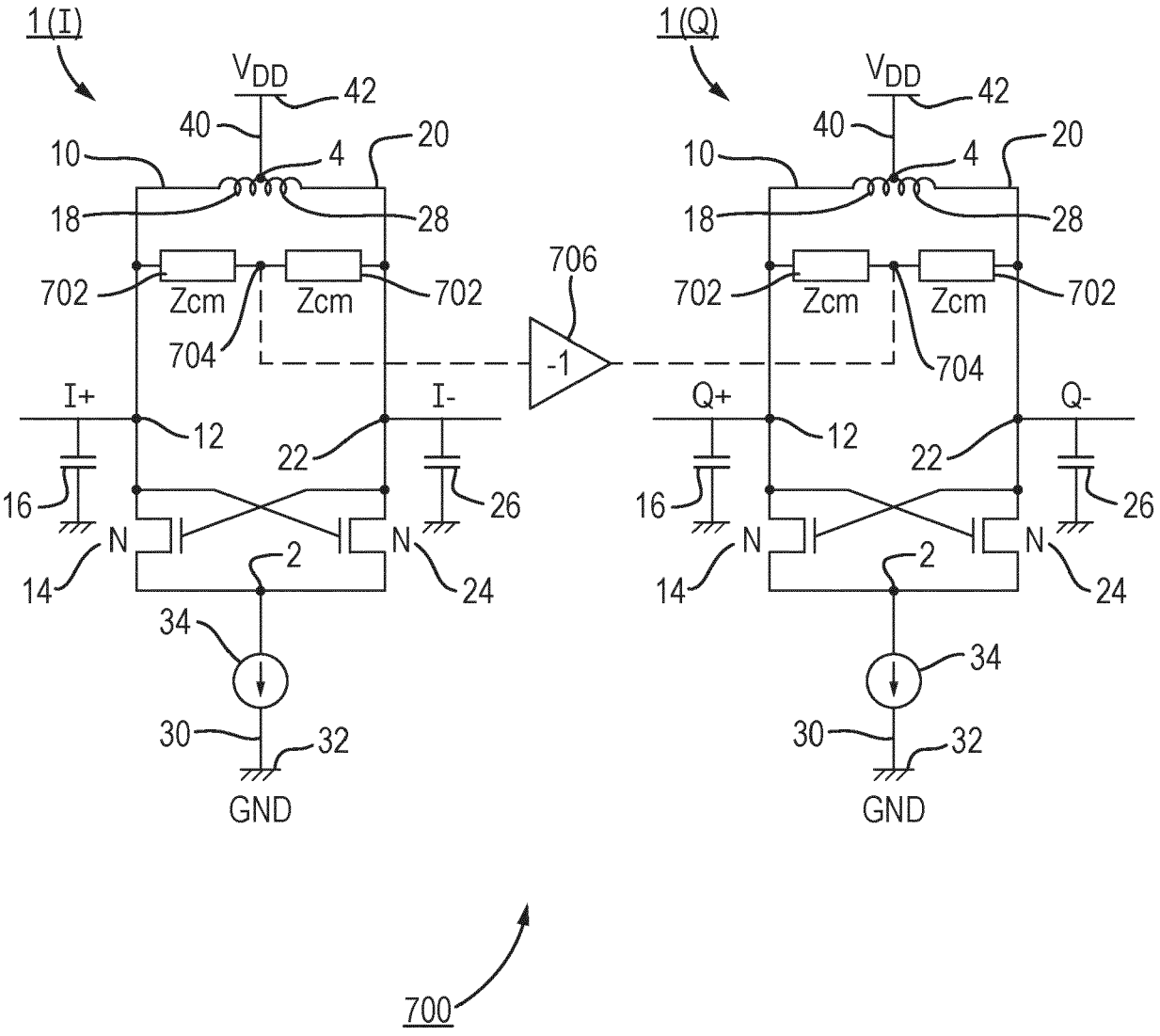

1(I)
1(Q)
VDD
42
40
4
20
10
18
28
706
702
Zcm
Zcm
704
-1
I+
I-
Q+
Q-
12
22
16
26
N
2
14
24
34
30
32
GND
700

Fig. 9

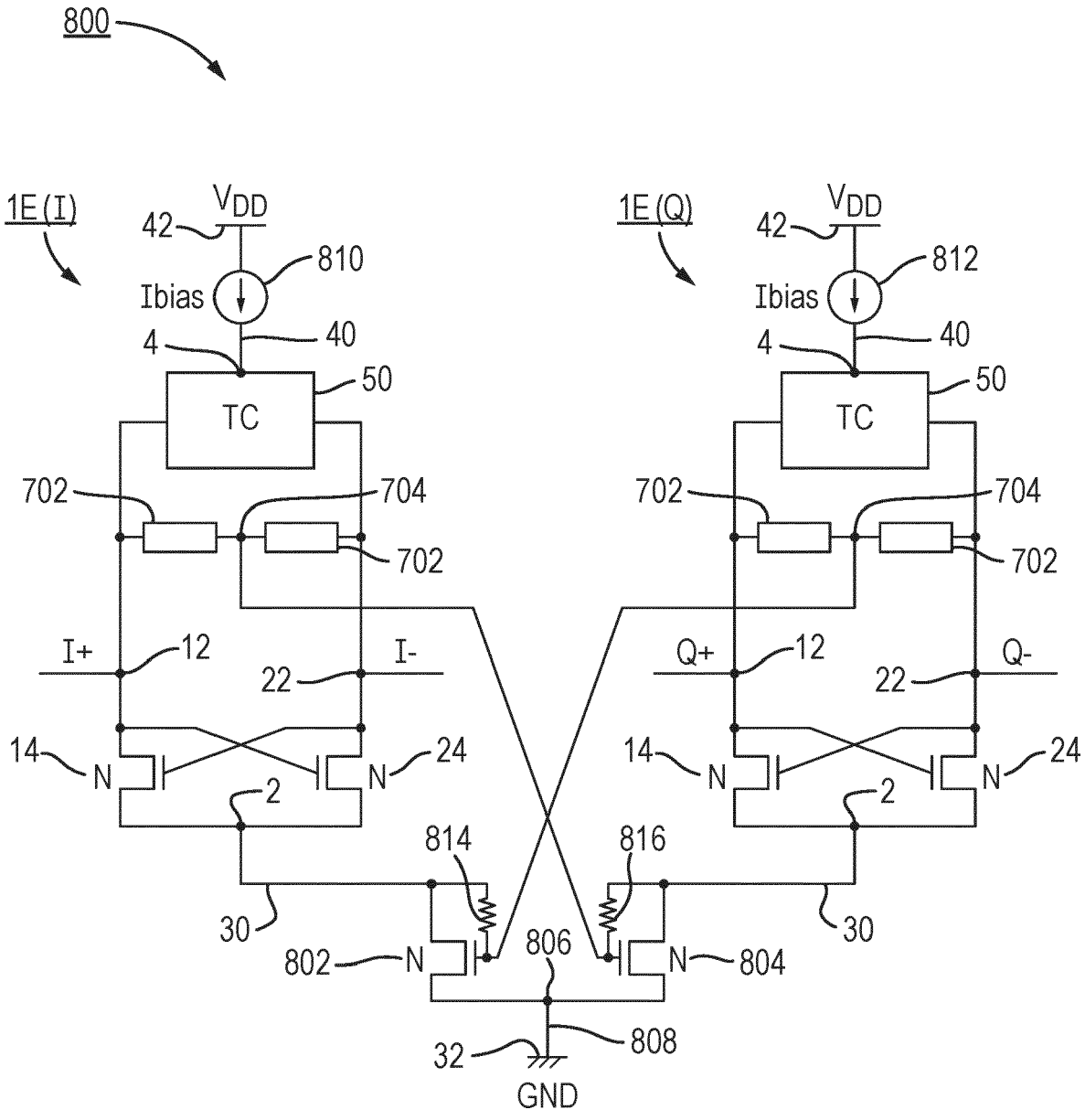

800
1E(I)
1E(Q)
VDD
42
Ibias
810
812
4
40
TC
50
702
704
I+
I-
Q+
Q-
12
22
14
N
24
2
814
816
30
802
806
804
32
808
GND

Fig. 10

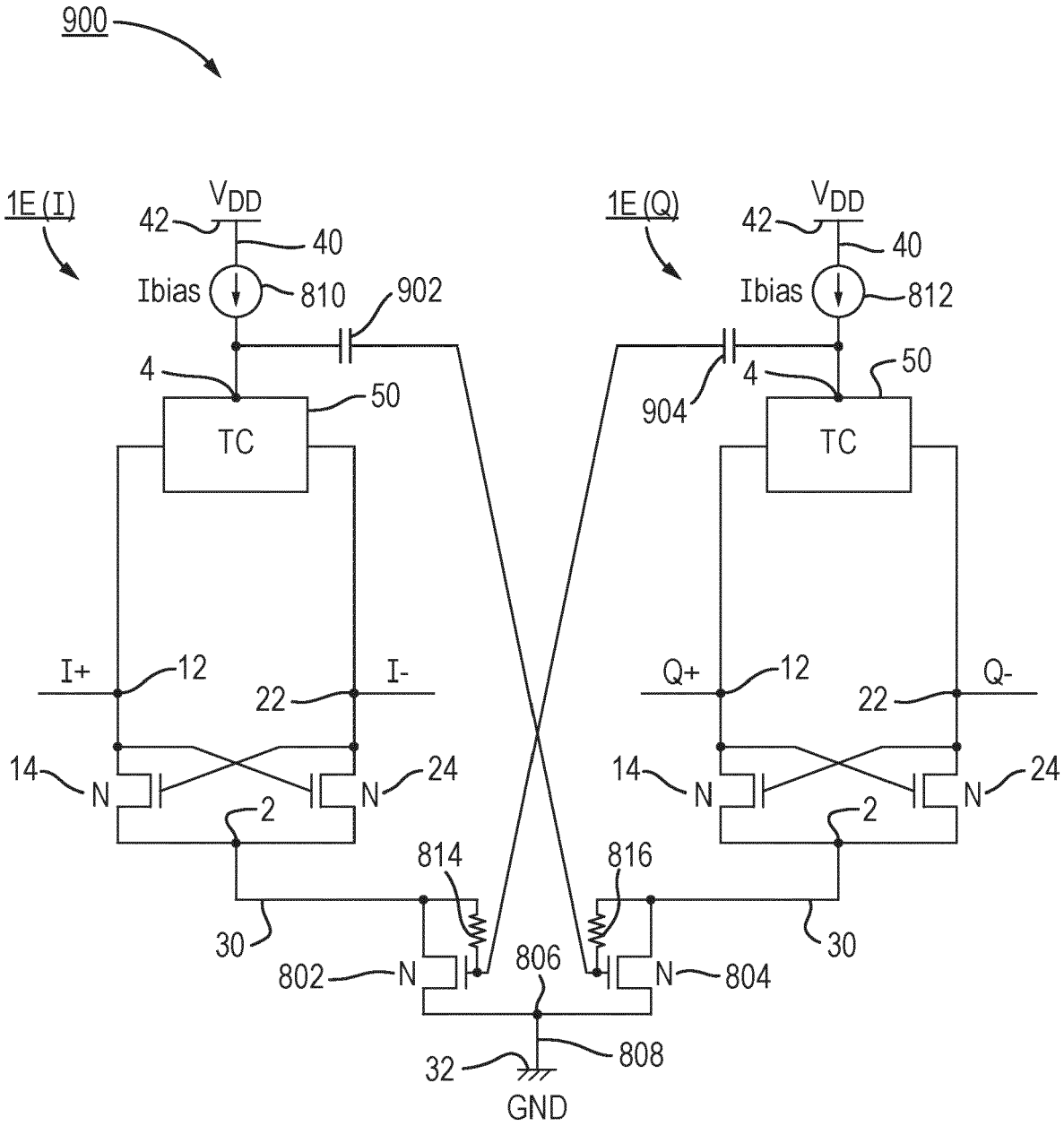

900
1E (I)
1E (Q)
VDD
42
40
Ibias
810
812
902
904
4
50
TC
I+
I-
Q+
Q-
12
22
14
N
24
2
814
816
30
802
804
806
808
32
GND

Fig. 11

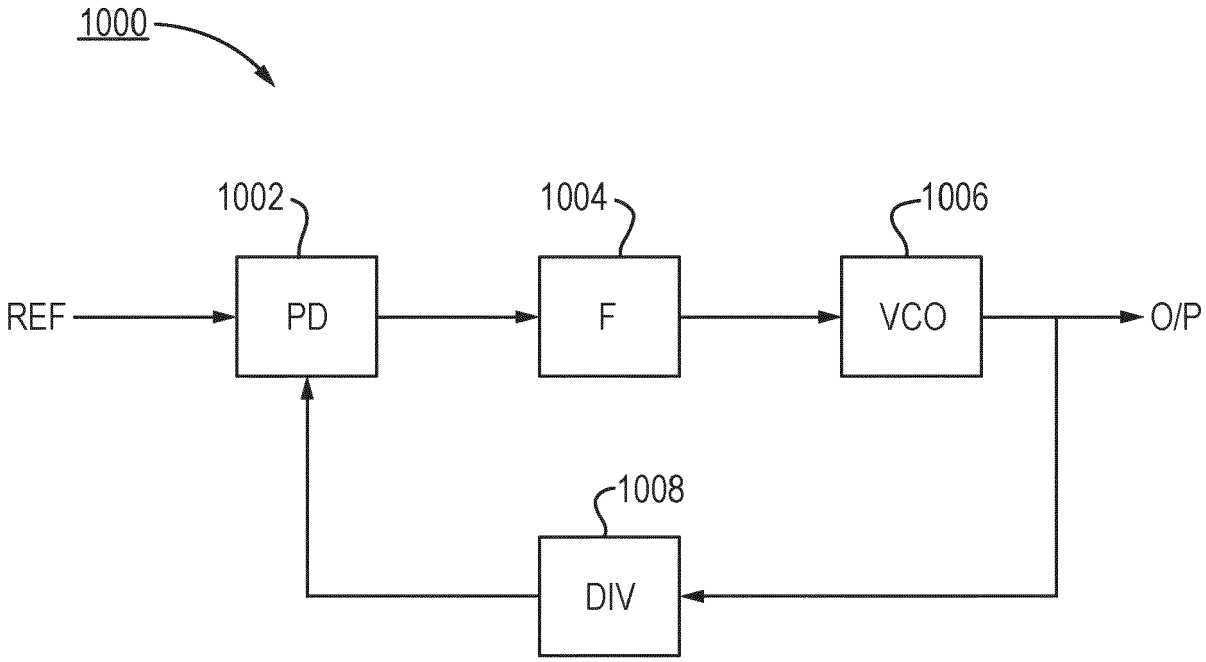
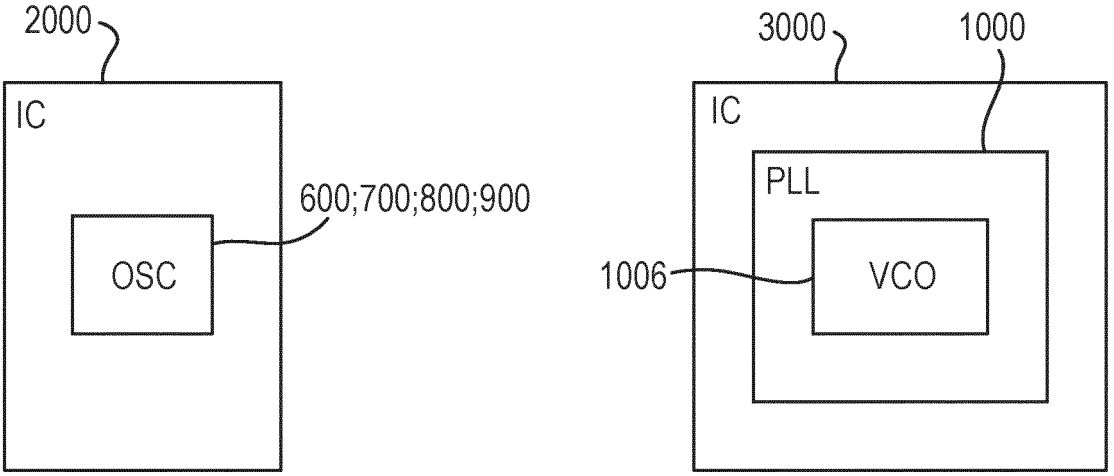

1000
1002
1004
1006
REF
PD
F
VCO
O/P
1008
DIV

Fig. 12


2000
IC
600;700;800;900
OSC
3000
1000
IC
PLL
1006
VCO