(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2003 (03.01.2003)

PCT

(10) International Publication Number
WO 03/001585 A1

(51) International Patent Classification[7]: H01L 21/60, H05K 3/34, H01L 23/485

(21) International Application Number: PCT/EP02/06922

(22) International Filing Date: 4 June 2002 (04.06.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/885,853 20 June 2001 (20.06.2001) US

(71) Applicant *(for all designated States except MC)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NJ 10504 (US).

(71) Applicant *(for MC only)*: **COMPANIE IBM FRANCE** [FR/FR]; Tour Descartes, 2, Avenue Gambetta, F-92066 la Défense Cedex (FR).

(72) Inventors: **BERNIER, William, E.**; 905 Vidka Lane, Endwell, NY 13760 (US). **CAREY, Charles, E.**; 1138 Elton Drive, Endicott, NY 13760 (US). **GRAMATZKI, Eberhard, B.**; 187 Brown River Road, Essex Junction, VT 05452 (US). **HOMA, Thomas, R.**; 432 Crocker Hill Road, Binghamton, NY 13904 (US). **JOHNSON, Eric, A.**; 7 Jeffrey Heights, Greene, NY 13778 (US). **LANGEVIN, Pierre**; 767 de la Venerie, Granby, Quebec, J2G 8C6 (CA). **MEMIS, Irving**; 3136 Briarcliff Avenue, Vestal, NY 13850 (US). **TRAN, Son, K.**; 2651 Clearview Drive, Endwell, NY 13760 (US). **WHITE, Robert, F.**; 16 Wildwood Drive, Essex Junction, VT 05452 (US).

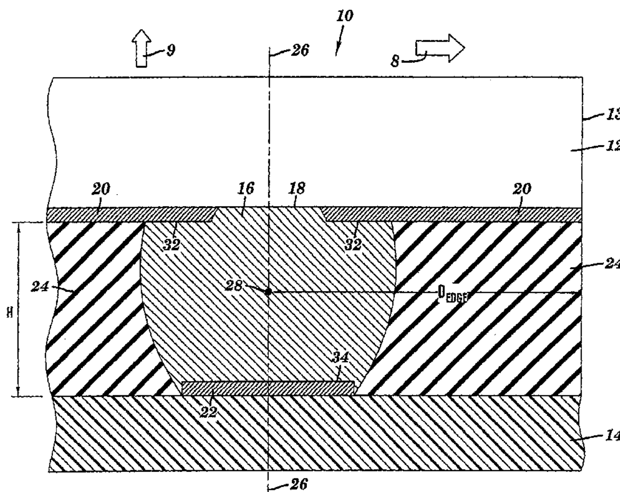
(74) Agent: **DE PENA, Alain**; Compagnie IBM France, Direction de la Propriété Intellectuelle, F-06610 La Gaude (FR).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL IN A CHIP TO SUBSTRATE CONNECTION



(57) Abstract: A method and structure for coupling a semiconductor substrate (e.g., a semiconductor chip) to an organic substrate (e.g., a chip carrier). The coupling interfaces a solder member (e.g., a solder ball) to both a conductive pad on the semiconductor substrate and a conductive pad on the organic substrate. Thermal strains on the solder member during thermal cycling may be reduced by having a surface area of the pad on the semiconductor substrate exceed a surface area of the pad on the organic substrate. Thermal strains on the solder member during thermal cycling may also be reduced by having a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate exceed about 0.25 mm.

WO 03/001585 A1

European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

EXTENSION OF FATIGUE LIFE FOR C4 SOLDER BALL IN A CHIP TO SUBSTRATE CONNECTION

Background of the Invention

1. Technical Field

5 The present invention relates to a method and structure for coupling a semiconductor chip to an organic chip carrier by a solder ball.

2. Related Art

A solder ball that couples a semiconductor chip to an organic chip carrier is subject to thermally induced strain during thermal cycling. The thermally induced strain 10 inevitably causes damage to the solder leading to cracking and electrical failure if sufficient cycles occur. Thus, a method and structure is needed for reducing the aforementioned thermally induced strain and increasing the fatigue life.

Summary of the Invention

The present invention provides an electronic structure, comprising:

15 a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

a solder member electrically coupling the first pad to the second pad.

The present invention provides an electronic structure, comprising:

20 a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon; and

a solder member electrically coupling the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.

25 The present invention provides a method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second pad; and

electrically coupling, by use of a solder member, the first pad to the second pad.

5 The present invention provides a method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad

10 thereon; and

electrically coupling, by use of a solder member, the first pad to the second pad, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm.

The present invention reduces thermally induced strain that occurs in a solder

15 ball during thermal cycling, wherein the solder ball couples a semiconductor chip to an organic chip carrier.

Brief Description of the Drawings

FIG. 1 depicts a front cross-sectional view of a semiconductor chip coupled to an organic chip carrier by a solder ball, in accordance with embodiments of the

20 present invention.

FIG. 2 is a table of thermal cycling fatigue test data for the solder ball of FIG. 1.

FIG. 3 is a plot of shear strain on the solder ball of FIG. 1 as a function of distance between the center of the chip and the solder ball centerline.

FIG. 4 is a plot of axial strain on the solder ball of FIG. 1 as a function of

25 distance between the center of the chip and the solder ball centerline.

Detailed Description of the Invention

FIG. 1 illustrates a front cross-sectional view of an electronic structure **10**, in accordance with embodiments of the present invention. The electronic structure **10** includes a semiconductor substrate **12** coupled to an organic substrate **14** by a solder

30 member **16**. The solder member **16** is mechanically and electrically coupled to an electrically conductive pad **20** on the semiconductor substrate **12**. The solder member

16 is likewise mechanically and electrically coupled to an electrically conductive pad **22** on the organic substrate **14**.

The semiconductor substrate **12** may include, *inter alia*, a semiconductor chip (e.g., a silicon chip or a germanium chip). The semiconductor substrate **12** may have
5 a coefficient of thermal expansion (CTE) of about 3 ppm/°C, wherein ppm stands for parts per million.

The organic substrate **14** includes, *inter alia*, an organic material such as an epoxy, a polyimide, a polytetrafluoroethylene (PTFE), glass cloth, copper-invar-copper or other reinforcing layers, and combinations thereof. The organic substrate **14** may
10 include, *inter alia*, an organic chip carrier. The organic substrate **14** has a CTE between about 10 ppm/°C and about 18 ppm/°C.

The solder member **16** may include, *inter alia*, a solder ball such as a controlled collapse chip connection (C4) solder ball. The solder member **16** may include, *inter alia*, a eutectic lead- tin alloy (i.e., about 63% lead and 37% tin, by weight), a high-melt
15 lead-tin alloy, a eutectic-tipped, high-melt alloy, an unleaded solder, etc. As an example, the high-melt lead-tin alloy may have lead and tin in a ratio of 97:3 by weight with a melting temperature of about 330 °C. The solder member **16** has a CTE between about 21 ppm/°C and about 28 ppm/°C. In particular, a lead-tin alloy having a 97:3 weight concentration ratio has a CTE of about 28 ppm/°C.

20 An underfill material **24** exists between the semiconductor substrate **12** and the organic substrate **14**, wherein the underfill material **24** encapsulates the solder member **16**, and wherein the underfill material **24** has an elastic modulus of at least about 1 gigapascal (GPa). The underfill material **24** serves to reduce thermal stresses on the solder member **16**, wherein such thermal stresses may occur during thermal
25 cycling operations. Any underfill material known to one of ordinary skill in the art may be used for the underfill material **24**. Examples of known underfill materials include, *inter alia*, Dexter CNB840-38 and Namics U8437-2.

The electronic structure **10** may be fabricated as follows. The semiconductor substrate **12** is formed, or otherwise provided, with the pad **20** thereon. The organic
30 substrate **14** is formed, or otherwise provided, with the pad **22** thereon. A high-melt lead-tin solder is deposited and shaped on the pad **20** of the semiconductor substrate **12** to form a solder ball. A eutectic lead-tin solder paste is deposited on the pad **22** of the organic substrate **14**. The high-melt solder on the pad **20** is placed in contact with

the eutectic solder paste on the pad **22**. The solder paste is reflowed at a temperature below the melting temperature of the high-melt lead-tin solder, and then cooled, to form the solder member **16** that mechanically and electrically couples the semiconductor substrate **12** to the organic substrate **14**. The underfill material **24** may be subsequently placed between the semiconductor substrate **12** and the organic substrate **14** such that the underfill material **24** encapsulates the solder member **16**.

Notwithstanding the role of the underfill material **24** in mitigating thermal stresses on the solder member **16**, such reduced thermal stresses may nonetheless cause cracking of the solder member **16** at the interface between the solder member **16** and the pad **20**. The interface between the solder member **16** and the pad **20** is more prone to thermal stress damage than is the interface between the solder member **16** and the pad **22**, because the local mismatch in CTE between the solder member **16** and the semiconductor substrate **12**, that is coupled to the pad **20**, is greater than the mismatch between the solder member **16** and the organic substrate **14** which is coupled to the pad **22**. The thermal stress damage adversely impacts the fatigue life of the interface between the solder member **16** and the pad **20**.

The present invention discloses two inventive techniques for extending the fatigue life of the interface between the solder member **16** and the pad **20**. With the first inventive technique, a ratio S1/S2 exceeds 1, wherein S1 is a surface area of the surface **32** of the pad **20** of the semiconductor substrate **12** that is wetted by the solder, and S2 is a surface area of the surface **34** of the pad **22** of the organic substrate **14**. With the second inventive technique, a distance in a direction **8** from a centerline **26** of the solder member **16** to a closest lateral edge **13** of the semiconductor substrate **12** exceeds about 0.25 mm. The centerline **26** is defined as passing through a centroid **28** of the solder member **16** and being oriented in a direction **9** that is perpendicular to the surface **32**.

By increasing S1 relative to S2, the first inventive technique of having S1/S2 exceed 1 reduces the thermal stress and consequent thermal strain on the solder member **16** at the pad **20** as compared with the thermal stress and consequent thermal strain on the solder member **16** at the pad **22**. The first inventive technique offsets a portion of the higher thermal stress on the solder member **16** at the pad **20**, wherein said higher thermal stress is due to the relatively higher CTE differential

between the solder member **16** and the semiconductor substrate **12**, as compared with the CTE differential between the solder member **16** and the organic substrate **14**.

FIG. 2 is a table of thermal cycling fatigue test data for the solder member **16** of FIG. 1, which demonstrates that increasing S1/S2 increases the fatigue life of an interface between the solder member **16** and the pad **20** of FIG. 1. In the tests underlying FIG. 2, the electronic structure **10** was thermally cycled from 100°C to 0°C, and back to 100 °C, in each cycle. The semiconductor substrate **12** is a silicon semiconductor chip, the organic substrate **14** is an organic chip carrier comprising a glass epoxy core with organic buildup layers, and the solder member **16** is a C4 solder ball comprising a lead-tin alloy having weight concentrations of about 97% lead and about 3% tin. An underfill **24** material of Namics U8437-2 material having an elastic modulus of 7 GPa was used.

The column titles appearing in the first row of the FIG. 2 are as follows. The "Row" column denotes row numbers. The "Sample Size" column denotes the number of same electronic structure **10** samples used in each batch tested. The "Chip Size" denotes the chip dimensions along surface **18** of the chip **12**. The pad **22** has a diameter as denoted in the "Organic Substrate Pad Diameter, D2" column. The pad **20** has a diameter as denoted in the "Chip Pad Diameter, D1" column. The "D1/D2" column denotes the ratio of D1 to D2. The "S1/S2" column denotes S1/S2 such that $S1/S2= (D1/D2)^2$. The "Solder Ball Height" column denotes the height H in the direction **9** shown in FIG. 1. The "Distance (D_{EDGE}) From Solder Ball Centerline To Chip Edge" column denotes the distance D_{EDGE} in the direction **8** shown in FIG. 1. The "No. Of Cycles to 50% Fails" column denotes the number of cycles at which 50% of the samples failed, which was computed by averaging over the Sample Size. The "First Cycle To Fail" column has a tolerance of 500 cycles, since the samples were tested for failure at every 500 cycles, with the exception of row 5 for which the samples were tested for failure at every 100 cycles. A failure of a sample is defined as crack in the solder member **16** or a delamination of the solder member **16** from the pad **20**.

As seen in rows 4 and 3 in FIG. 2, as S1/S2 is increased from 0.40 to 0.77, the No. of Cycles to 50% Fails increases from 3250 to 7963, and the First cycle to Fail increases from 600 to 2500. Note that rows 2 and 3 are consistent with rows 3 and 4, since as S1/S2 increases from 0.77 to 0.81, the No. of Cycles to 50% Fails increases from 7963 to 8430. Note that in rows 2, 3, and 4, D_{EDGE} has the same value of 100 µm.

The preceding results confirm that increasing S1/S2 improves fatigue life, which is the basis for the first inventive technique of the present invention. Finite element modeling has been used to predict the increase in fatigue life over an extended range of the ratio S1/S2. The first inventive technique includes several embodiments with respect to S1/S2. A first embodiment of the first inventive technique is S1/S2 > 1. A second embodiment of the first inventive technique is having S1 exceed S2 by a factor of at least about 1.2. A third embodiment of the first inventive technique is having S1 exceed S2 by a factor between about 1.1 and about 1.3. A fourth embodiment of the first inventive technique is having S1 exceed S2 by a factor between about 1.3 and about 2.0.

Rows 1 and 3 of FIG. 2 demonstrate the second inventive technique of the present invention. D_{EDGE} equals 230 μm (i.e., .23 mm or 9 mils) and 100 μm (i.e., .10 mm or 4 mils) for rows 1 and 3, respectively. For rows 1 and 3, FIG. 2 shows that the Number of Cycles to 50% Fails increases from 7963 cycles to 13260 cycles to as D_{EDGE} is increased from 100 μm to 230 μm (i.e., from .10 mm to .23mm). Thus, at distances D_{EDGE} within hundreds of microns from the nearest chip edge **13** (see FIG. 1), increasing D_{EDGE} results in going to more cycles to reach the 50% failure level. Note that in rows 1 and 3, S1/S2 has the same value of 0.77.

The beneficial effect of increasing D_{EDGE} within hundreds of microns from the nearest chip edge **13** is also illustrated by FIGS. 3 and 4. FIGS. 3 and 4 are plots of average shear strain and average axial strain, respectively, on the solder member **16** at the interface between the solder member **16** and the pad **20** of the semiconductor substrate **12**. The average shear strain in FIG. 3 is in a plane that is defined by directions **8** and **9** in FIG. 1, whereas the average axial strain in FIG. 4 is parallel to the direction **9**. Both the shear strain in FIG. 3 and the axial strain in FIG. 4 are spatially averaged over the portion of the pad surface **32** that interfaces the C4 solder ball **16**.

In FIGS. 3 and 4, the semiconductor substrate **12** is a silicon semiconductor chip, the organic substrate **14** is an organic chip carrier comprising a glass epoxy core with organic buildup layers, and the solder member **16** was a C4 solder ball comprising a lead-tin alloy having weight concentrations of about 97% lead and about 3% tin. An underfill **24** material is present with a modulus of from 2 to 11 GPa. The edge **13** of the chip **12** is about 8 mm from the center (not shown) of the chip **12**. The

surface **18** of the chip **12** has dimensions of 16mm x 16mm. The height H of the C4 solder ball is 0.1 mm.

In the simulations underlying FIGS. 3 and 4, the electronic structure **10** was thermally cycled from 100°C to 0°C, and back to 100 °C, in each cycle. The resulting shear strain in FIG. 3 and axial strain in FIG. 4 are each plotted as a function of D_C, wherein D_C is a distance in the direction **8** from the center of the semiconductor substrate **12** to the centerline **26** of the solder member **16** (see FIG. 1). FIG. 3 shows three shear strain curves **102**, **105**, and **111**, respectively corresponding to elastic modulii of 2 Gpa, 5 Gpa, and 11 Gpa of the underfill **24**. Similarly, FIG. 4 shows three axial strain curves **202**, **205**, and **211**, respectively corresponding to elastic modulii of 2 GPa, 5 GPa, and 11 GPa of the underfill **24**.

In FIG. 3, the average shear strain falls most sharply when the C4 solder ball centerline **26** is between about 0.25 mm and about 0.40 mm from the edge **13** of the chip **12**, depending on which of the three curves **102**, **105**, and **111** is relevant. The 0.25 mm distance is the change in D_C between the point P_1 on the curve **111** (where a sharp change in slope occurs) and D_C = 8 mm corresponding to the edge **13** of the chip **12**. The 0.40 mm distance is the change in D_C between the point P_2 on the curve **105** (where a sharp change in slope occurs) and D_C = 8 mm corresponding to the edge **13** of the chip **12**.

In FIG. 4, the average axial strain falls most sharply when the C4 solder ball centerline **26** is between about 0.30 mm and about 1.0 mm from the edge **13** of the chip **12**, depending on which of the three curves **202**, **205**, and **211** is relevant. The 0.30 mm distance is the change in D_C between the point P_3 on the curve **211** (where a sharp change in slope occurs) and D_C = 8 mm corresponding to the edge **13** of the chip **12**. The 1.0 mm distance is the change in D_C between the point P_4 on the curve **202** (where a sharp change in slope occurs) and D_C = 8 mm corresponding to the edge **13** of the chip **12**. Based on the preceding results, the second inventive technique includes several embodiments with respect to D_{EDGE}. With a first embodiment of the second inventive technique, based on the average shear strain curves of FIG. 3, D_{EDGE} is at least about 0.25 mm. With a second embodiment of the second inventive technique, based on the average shear strain curves of FIG. 3, D_{EDGE} is at least about 0.40 mm. With a third embodiment of the second inventive technique, based on the average axial strain curves of FIG. 4, D_{EDGE} is at least about 0.30 mm. With a third

embodiment of the second inventive technique, based on the average axial strain curves of FIG. 4, D_{EDGE} is at least about 1.00 mm.

The present invention's effectiveness relates to the fact that the interface between the solder member **16** and the pad **20** is more prone to thermal stress
5 damage than is the interface between the solder member **16** and the pad **20**, because there is a greater difference in CTE between the solder member **16** and the pad **20** than between the solder member **16** and the pad **22**. Accordingly, a CTE coupling parameter P characterizes the aforementioned differentials in CTE, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder
10 member **16**, wherein $C_{ORGANIC}$ is a CTE of the organic substrate **14**, and wherein C_{SEMI} is a CTE of the semiconductor substrate **12**. Assuming that $C_{SOLDER} > C_{ORGANIC} > C_{SEMI}$, P must satisfy $0 < P < 1$. P=1 represents a perfectly symmetric distribution of said differential CTE between the pad **20** and the pad **22**, while P=0 represents a perfectly asymmetric distribution of said differential CTE between the pad **20** and the pad **22**.
15 For the ranges of CTE stated *supra* for the solder member **16**, the organic substrate **14**, and the semiconductor substrate **12**, P satisfies $.17 < P < .72$. Thus, a comprehensive range for P is $.15 < P < .75$ for the range of CTEs considered herein.

Claims

1. An electronic structure, comprising:

a semiconductor substrate having a first electrically conductive pad thereon;

an organic substrate having a second electrically conductive pad thereon, wherein
5 a surface area of the first pad exceeds a surface area of the second pad; and

a solder member electrically coupling the first pad to the second pad.

2. The electronic structure of claim 1, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm or 0.40 mm.

10 **3.** The electronic structure of anyone of claim 1 or claim 2 further comprising:

an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

4. The electronic structure of anyone of claim 1 or claim 2, wherein a coefficient of
15 thermal expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

5. The electronic structure of anyone of claim 1 or claim 2, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic
20 substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

6. The electronic structure of anyone of claim 1 or claim 2, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

7. The electronic structure of anyone of claim 1 or claim 2, wherein the solder
25 member includes a controlled collapse chip connection (C4) solder ball.

8. The electronic structure of anyone of claim 1 or claim 2, wherein the solder member includes a lead-tin alloy.

9. The electronic structure of claim 1, where, in the organic substrate, a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2
30 or, between about 1.1 and 1.3 or, between about 1.3 and 2.0 and, a solder member is electrically coupling the first pad to the second pad.

10. A method of forming an electronic structure, comprising:

forming a semiconductor substrate having a first electrically conductive pad thereon;

forming an organic substrate having a second electrically conductive pad thereon, wherein a surface area of the first pad exceeds a surface area of the second
5 pad; and

electrically coupling, by use of a solder member, the first pad to the second pad.

11. The method of claim 10, wherein a distance from a centerline of the solder member to a closest lateral edge of the semiconductor substrate is at least about 0.25 mm or 0.40 mm.

10 **12.** The method of anyone of claim 10 or claim 11 further comprising:

placing an underfill material between the semiconductor substrate and the organic substrate, wherein the underfill material encapsulates the solder member, and wherein the underfill material has an elastic modulus of at least about 1 gigapascal.

13. The method of anyone of claim 10 or claim 11, wherein a coefficient of thermal
15 expansion (CTE) of the organic substrate is between about 10 ppm/°C and about 18 ppm/°C.

14. The method of anyone of claim 10 or claim 11, wherein P is between about .15 and about .75, wherein P is defined as $(C_{SOLDER} - C_{ORGANIC})/(C_{SOLDER} - C_{SEMI})$, wherein C_{SOLDER} is a CTE of the solder member, wherein $C_{ORGANIC}$ is a CTE of the organic
20 substrate, and wherein C_{SEMI} is a CTE of the semiconductor substrate.

15. The method of anyone of claim 10 or claim 11, wherein the organic substrate includes an organic material selected from the group consisting of an epoxy, a polyimide, a polytetrafluoroethylene, and combinations thereof.

16. The method of anyone of claim 10 or claim 11, wherein the solder member
25 includes a controlled collapse chip connection (C4) solder ball.

17. The method of anyone of claim 10 or claim 11 , wherein the solder member includes a lead-tin alloy.

18. The method of claim 10 wherein the forming step, a surface area of the first pad exceeds a surface area of the second pad by a factor of at least about 1.2 or between
30 about 1.1 and 1.3, or between 1.3 and 2.0.

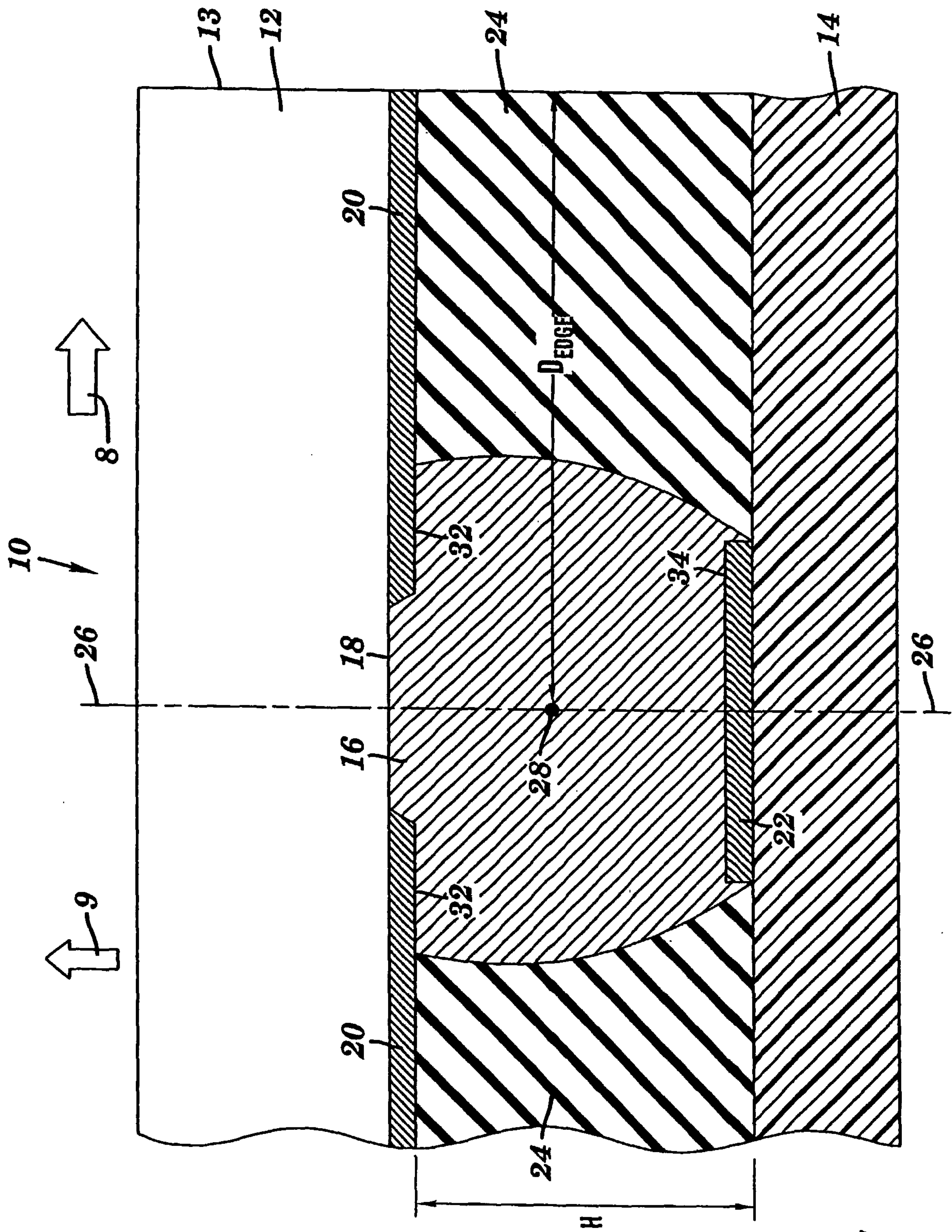


FIG. 1

SOLDER BALL THERMAL CYCLING FATIGUE TEST DATA

ROW	SAMPLE SIZE	CHIP SIZE (mm x mm)	ORGANIC SUBSTRATE PAD DIAMETER, D2 (mm)	CHIP PAD DIAMETER, D1 (mm)	D1/D2	S1/S2	SOLDER BALL HEIGHT (μm)	DISTANCE (D_{EDGE}) FROM SOLDER BALL CENTERLINE TO CHIP EDGE (μm)	NO. OF CYCLES TO 50% FAILS	FIRST CYCLE TO FAIL
1	47	8.7 x 8.7	160	140	0.88	0.77	110	230	13260	2500
2	30	8.7 x 8.7	155	140	0.90	0.81	110	100	8430	2500
3	19	8.7 x 8.7	160	140	0.88	0.77	110	100	7963	2500
4	75	7.68 x 7.68	160	100	0.63	0.40	100	100	3250	600

FIG. 2

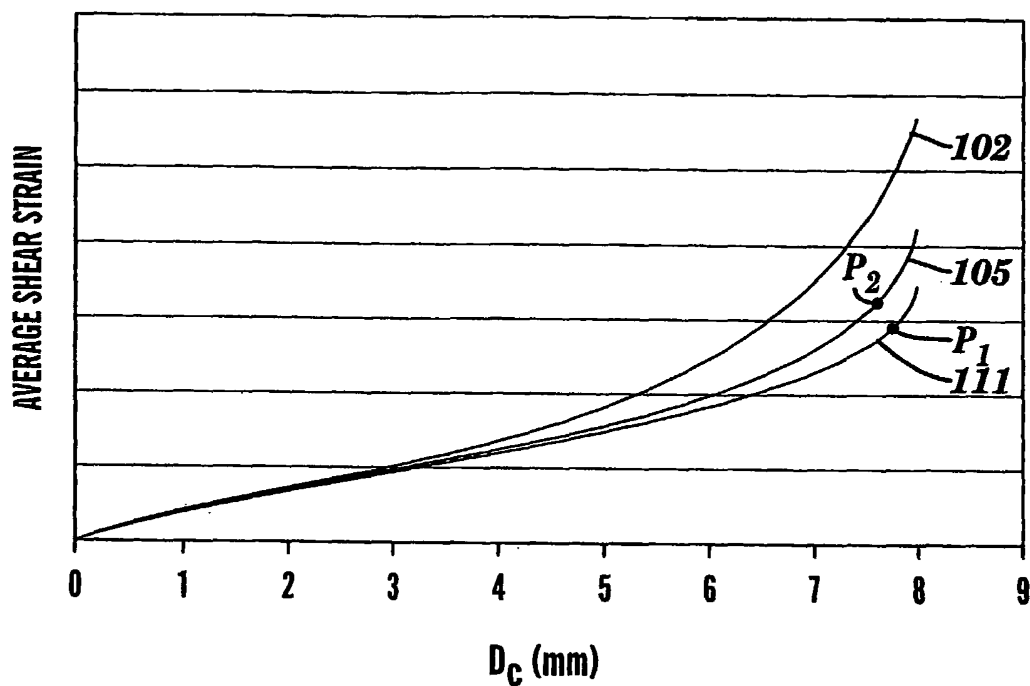


FIG. 3

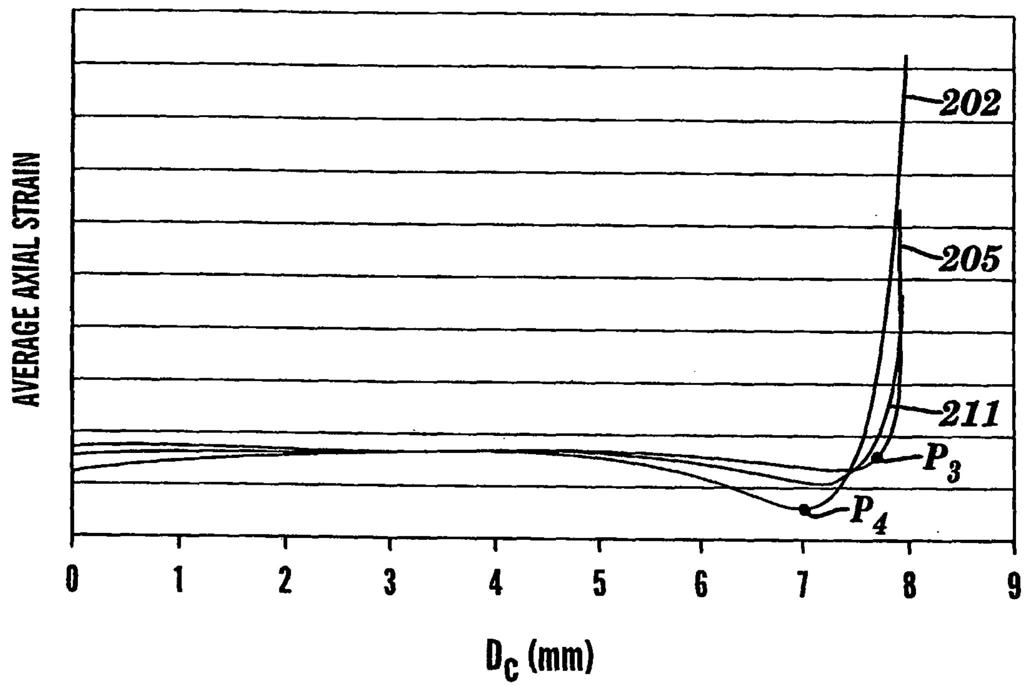


FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 02/06922

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/60 H05K3/34 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 889 326 A (TANAKA KEI) 30 March 1999 (1999-03-30)	1,3-10, 12-18
Y	column 1, line 1-51 column 3, line 8-65; figure 3A	2,11
X	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 14, 5 March 2001 (2001-03-05) -& JP 2000 306951 A (MITSUBISHI ELECTRIC CORP), 2 November 2000 (2000-11-02)	1,3-10, 12-18
Y	abstract	2,11
E	-& US 6 462 425 B1 8 October 2002 (2002-10-08) column 8, line 41 -column 11, line 17; figures 1,2,12	1-18

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 November 2002	18/11/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Edmeades, M

Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
PCT/EP 02/06922

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 56509 A (CHUNG KEVIN KWONG TAI ;AMERASIA INTERNATIONAL TECHNOL (US)) 4 November 1999 (1999-11-04) column 2, line 10 -column 5, line 24 page 14, line 19-29	3-6, 12-15
Y	PATENT ABSTRACTS OF JAPAN vol. 013, no. 168 (E-747), 21 April 1989 (1989-04-21) -& JP 64 002338 A (FUJITSU LTD), 6 January 1989 (1989-01-06) abstract	2,11
A	GB 2 344 463 A (NIPPON ELECTRIC CO) 7 June 2000 (2000-06-07) figure 5	1,10
A	US 5 973 406 A (HARADA MASAHIDE ET AL) 26 October 1999 (1999-10-26) column 5, line 48 -column 6, line 9; figure 3	1,10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 02/06922

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5889326	A	30-03-1999	JP	2803664 B2	24-09-1998
			JP	9293752 A	11-11-1997
JP 2000306951	A	02-11-2000	DE	10018126 A1	02-11-2000
			TW	451370 B	21-08-2001
			US	6462425 B1	08-10-2002
WO 9956509	A	04-11-1999	US	6108210 A	22-08-2000
			US	6297564 B1	02-10-2001
			CN	1298626 T	06-06-2001
			EP	1090535 A1	11-04-2001
			WO	9956509 A1	04-11-1999
JP 64002338 1	A		NONE		
GB 2344463	A	07-06-2000	CN	1258098 A	28-06-2000
			JP	3157817 B2	16-04-2001
			JP	2000228459 A	15-08-2000
			JP	2001177226 A	29-06-2001
US 5973406	A	26-10-1999	JP	10070153 A	10-03-1998