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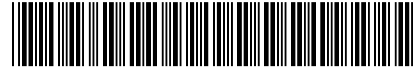

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(71) Applicant: **Kyocera Corporation**
Kyoto-shi, Kyoto 612-8501 (JP)

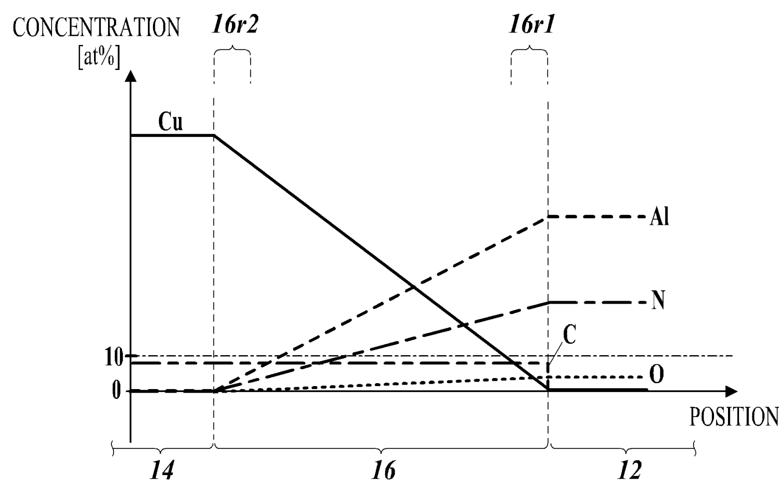
(72) Inventors:
- **YAMASHITA, Kyohei**
Kyoto-shi, Kyoto 612-8501 (JP)
- **HOSOI, Yoshihiro**
Kyoto-shi, Kyoto 612-8501 (JP)

(74) Representative: **Viering, Jentschura & Partner mbB**
Patent- und Rechtsanwälte
Am Brauhaus 8
01099 Dresden (DE)

(54) **CIRCUIT BOARD, ELECTRONIC DEVICE, AND ELECTRONIC MODULE**

(57) Provided is a wiring substrate in which a high bond strength can be obtained between an insulating substrate that contains AlN (aluminum nitride) and a Cu (copper)-based conductor layer. The wiring substrate comprises the insulating substrate that contains AlN, the conductor layer that contains Cu, and an intermediate layer that is located between the insulating substrate and the conductor layer. The intermediate layer has a first region that is close to the insulating substrate and a second region that is close to the conductor layer, wherein the second region has a Cu concentration that is higher than that of the first region and the first region has an Al concentration that is higher than that of the second region.

FIG.2A



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Description

Technical Field

5 **[0001]** The present disclosure relates to a wiring substrate, an electronic device and an electronic module.

Background Art

[0002] In JPH 5-182926 A, there is disclosed a manufacturing method of a wiring substrate in which an Al (aluminum)-based wiring is disposed on a substrate with a barrier metal layer in between. In this manufacturing method, after a small-diameter connecting hole is formed in the surface of the substrate, the barrier metal layer and the wiring layer are successively formed by sputtering. As the barrier metal layer, a Ti-based material is used.

Summary of Invention

Solution to Problem

[0003] A wiring substrate according to the present disclosure includes:

an insulating substrate containing AlN;
a conductor layer containing Cu; and
an interlayer located between the insulating substrate and the conductor layer,
wherein in the interlayer, between a first region near the insulating substrate and a second region near the conductor layer,

Cu concentration is higher in the second region than in the first region, and
Al concentration is higher in the first region than in the second region.

[0004] An electronic device according to the present disclosure includes:

the above wiring substrate; and
an electronic component mounted on the wiring substrate.

[0005] An electronic module according to the present disclosure includes:

the above electronic device; and
a module board where the electronic device is mounted.

Advantageous Effects of Invention

[0006] According to the present disclosure, there can be provided a wiring substrate having high bond strength between an insulating substrate containing AlN and a conductor layer having Cu as a constituent element, and an electronic device and an electronic module each having the wiring substrate.

Brief Description of Drawings

[0007]

FIG. 1A shows a wiring substrate according to an embodiment of the present disclosure.
FIG. 1B is a part-enlarged view of a part of the wiring substrate shown in FIG. 1A.
FIG. 1C shows an electronic module according to the embodiment of the present disclosure.
FIG. 2A shows concentration distributions of constituent elements in and around an interlayer of the wiring substrate of the embodiment.
FIG. 2B shows concentration distributions of the constituent elements in and around an interlayer of a comparative example.
FIG. 3 is a sectional view of structure at and around an interface of an insulating substrate.
FIG. 4 shows concentration distributions of constituent elements in and around the interface in a recess.
FIG. 5 is a diagram to explain an example of a manufacturing method of the wiring substrate of the embodiment.

Description of Embodiments

[0008] Hereinafter, an embodiment(s) of the present disclosure will be described in detail with reference to the drawings.

[0009] FIG. 1A is a sectional view of a wiring substrate according to an embodiment of the present disclosure. FIG. 1B is a part-enlarged view of a part of the wiring substrate shown in FIG. 1A. FIG. 1C is a sectional view of an electronic module according to the embodiment of the present disclosure.

[0010] A wiring substrate 10 of this embodiment has an insulating substrate 12 and a conductor layer 14 formed on the plate surface of the insulating substrate 12. The conductor layer 14 is formed with a pattern on the insulating substrate 12, and functions as a wiring for transmitting signals or electric power or functions as an electrode or a connection pad for connecting an electronic component 20, such as an optical element. In the insulating substrate 12 and on the back surface of the insulating substrate 12 (on a side thereof opposite the conductor layer 14), a wiring(s) and/or a connection pad(s) 31 (FIG. 1C) may also be provided. The wiring substrate 10 may be a package having a recess where the electronic component 20 is housed.

[0011] An electronic device 40 of this embodiment is, as shown in FIG. 1C, configured by mounting the electronic component 20 on the wiring substrate 10 shown in FIG. 1A. The electronic component 20 is mounted such that a terminal of the electronic component 20 is electrically connected to the conductor layer 14. The connection form of the terminal of the electronic component 20 to the conductor layer 14 may be any form, examples of which include connection with a joining material, such as solder, and connection by wire bonding. In FIG. 1C, the electronic component 20 is mounted on the conductor layer 14, but may be mounted, of the wiring substrate 10, a portion where the conductor layer 14 is not present. As the electronic component 20, various electronic components are applicable, which include: optical elements, such as an LD (Laser Diode), a PD (Photo Diode) and an LED (Light Emitting Diode); imagers, such as a CCD (Charge Coupled Device) and a CMOS (Complementary Metal Oxide Semiconductor) device; piezoelectric vibrators, such as a crystal oscillator; surface acoustic wave devices; semiconductor devices, such as a semiconductor integrated circuit (IC) device; electric capacitors; inductors; and resistors.

[0012] An electronic module 100 of this embodiment is, as shown in FIG. 1C, configured by mounting the electronic device 40 on a module board 110. On the module board 110, in addition to the electronic device 40, other electronic component(s) and/or electric component(s) may be mounted. The module board 110 has a circuit wiring and a connection pad 111 that connects components. The electronic device 40 can be mounted on the module board 110, for example, via (with) a joining material 113, such as solder.

<Wiring Substrate>

[0013] The insulating substrate 12 of the wiring substrate 10 contains AlN (aluminum nitride) as a main component of constituent elements. The conductor layer 14 contains Cu (copper) as a constituent element. At the interface between the insulating substrate 12 and the conductor layer 14, an interlayer 16 is present. The interlayer 16 has a thickness of about 20 nm to 80 nm.

[0014] FIG. 2A shows concentration distributions of constituent elements in and around the interlayer of the wiring substrate of the embodiment. FIG. 2B shows concentration distributions of the constituent elements in and around an interlayer of a comparative example. The constituent elements of the interlayer 16 and the concentration distributions of the constituent elements in the interlayer 16 described hereinafter were obtained by measurement with TEM-EELS (Electron Energy-Loss Spectroscopy). The concentration distributions are expressed by concentrations with at% (atomic percent) . The graphs shown in FIG. 2A and FIG. 2B do not show values of the concentration distributions precisely, but show changes of the values in a simplified manner.

[0015] As shown in FIG. 2A, the interlayer 16 contains Al (aluminum), N (nitrogen) and Cu (copper). If, among regions of the interlayer 16, a first region 16r1 near the insulating substrate 12 is compared with a second region 16r2 near the conductor layer 14, Cu concentration is higher in the second region 16r2 than in the first region 16r1. Further, Al concentration is higher in the first region 16r1 than in the second region 16r2. Still further, N concentration may be higher in the first region 16r1 than in the second region 16r2. In the interlayer 16, The Al and N concentrations may gradually decrease in a direction from the insulating substrate 12 to the conductor layer 14. The first region 16r1 and the second region 16r2 are two regions that do not overlap one another and have an arbitrary thickness (e.g. a thickness of 10% of the interlayer 16) in the layer direction. The first region 16r1 may be a region closer to the insulating substrate 12 than the second region 16r2 is, and the second region 16r2 may be a region closer to the conductor layer 14 than the first region 16r1 is. Alternatively, the first region 16r1 may be a region closer to the insulating substrate 12 than to the center of the interlayer 16, and the second region 16r2 may be a region closer to the conductor layer 14 than to the center of the interlayer 16.

[0016] The constituent elements of the interlayer 16 may have the following concentration distributions, to be more specific. That is, Al and N concentration gradients are each a gradient in which the closer the position in the interlayer 16 is to the conductor layer 14, the lower the concentration is, and Cu concentration gradient is a gradient in which the

closer the position in the interlayer 16 is to the conductor layer 14, the higher the concentration is. These concentration gradients may exist from the conductor layer 14 side to the insulating substrate 12 side of the interlayer 16.

[0017] The interlayer 16 may further contain C (carbon). If the interlayer 16 contains C, however, C concentration of the interlayer 16 is 10 at% or less. This C concentration, which is 10 at% or less, may be approximately the same as C concentration of the conductor layer 14.

[0018] FIG. 2B, which shows the comparative example, shows the concentration distributions of the constituent elements of the interface not subjected to sintering under predetermined conditions described below. In the comparative example, changes of the concentrations of the constituent elements (Al, N, Cu) are steep on an insulating substrate 212 side of an interlayer 216 and on a conductor layer 214 side of the interlayer 216.

[0019] Further, the interlayer 216 of the comparative example has high C concentrations and has a portion(s) containing C at a concentration equal to or more than the sum of the Al, N and Cu concentrations, for example. If the conductor layer 214 is generated by plating, carbon component contained in the plating solution gets mixed in the interlayer 216, and the interlayer 216, which is not subjected to the sintering under predetermined conditions described below, has high C concentrations.

<Adhesive Component>

[0020] FIG. 3 is a sectional view of structure at and around an interface of an insulating substrate.

[0021] The insulating substrate 12 has a large number of fine recesses 12D, each of which is as shown in FIG. 3, at the interface between itself and the conductor layer 14. The constituent element(s) of the conductor layer 14 enters each recess 12D, and the interlayer 16 is formed between the insulating substrate 12 and the conductor layer 14 not only at the interface of the region outside the recess 12D but also on the inner surface of the recess 12D. The element components and the concentration distributions of the interlayer 16 are as described with reference to FIG. 2A.

[0022] On the inner surface of the recess 12D, adhesive regions e1 containing TiO_2 (titanium oxide) as a constituent element are scattered. The adhesive regions e1 may also be scattered at the interface between the insulating substrate 12 and the conductor layer 14 of the region outside the recess 12D. The "scattered" means that at the interface between the insulating substrate 12 and the conductor layer 14, the adhesive region(s) e1 and region(s) other than the adhesive region(s) e1 coexist.

[0023] Next, an interlayer 16A at a portion including the adhesive region e1 will be described. The interlayer 16A at the portion including the adhesive region e1 and the interlayer 16 at a portion not including the adhesive region e1 are distinguished from one another by these different reference signs. FIG. 4 shows concentration distributions of constituent elements in and around the interface including the adhesive region(s) e1 in a recess. The graph shown in FIG. 4 does not show values of the concentration distributions precisely, but show changes of the values in a simplified manner.

[0024] The interlayer 16A contains Al, N, Cu, Ti (titanium) and O (oxygen). In the interlayer 16A too, Al, N and Cu concentration gradients in which Al, N and Cu concentrations gradually change exist. Directions of the Al, N and Cu concentration gradients are the same as those of the Al, N and Cu concentration gradients in the interlayer 16 described above. The Al, N and Cu concentration gradients exist from the insulating substrate 12 side to the conductor layer 14 side of the interlayer 16A. In the interlayer 16A too, the C concentration is 10 at% or less.

[0025] Since the interlayer 16A contains Ti and O too, counter diffusion of Cu and Al is promoted in the sintering under predetermined conditions described below. Hence, the Al, N and Cu concentration gradients in the interlayer 16A are gentle as compared with those in the interlayer 16 at the portion not including the adhesive region e1.

[0026] Further, in the interlayer 16A including the adhesive region e1, O (oxygen) concentration gradient occurs on the conductor layer 14 side, so that adhesive strength of the conductor layer 14 is increased. Increase of the adhesive strength between the insulating substrate 12 and the conductor layer 14 in the recess 12D further increases the adhesive strength between the insulating substrate 12 and the conductor layer 14 as a whole.

<Adhesive Strength>

[0027] A test was carried out to obtain the adhesive strength between the conductor layer 14 and the insulating substrate 12 about the wiring substrate 10 of the embodiment and a board not subjected to the sintering under predetermined conditions described below. As the test method, to a first jig fixed to the insulating substrate 12 and a second jig fixed to the conductor layer 14, pull force in a direction to separate these from one another in a direction perpendicular to the interface was applied, and the maximum pull strength was measured as the adhesive strength. As the pull force is increased, the interface between the insulating substrate 12 and the conductor layer 14 fractures, or the insulating substrate 12 fractures. As a fracture mode, a proportion of fracture of the insulating substrate 12 was obtained.

[0028] Three objects were tested, which were a board not subjected to sintering, a board subjected to sintering under conditions different from predetermined conditions described below, and the wiring substrate 10 of the embodiment subjected to the sintering under predetermined conditions described below and having the interface where the adhesive

regions e1 were scattered.

[0029] As a result of the test, as shown in the following comparison table, a great improvement was observed in the adhesive strength of the wiring substrate 10 of the embodiment.

[TABLE I]

[COMPARISON TABLE]		
TREATMENT	FRACTURE MODE	ADHESIVE STRENGTH [kgf/mm^2]
NO SINTERING	FRACTURE OF INSULATING SUBSTRATE: 0%	2.59
DIFFERENT SINTERING	FRACTURE OF INSULATING SUBSTRATE: 20%	3.79
SINTERING UNDER BELOW-DESCRIBED PREDETERMINED CONDUCTIONS	FRACTURE OF INSULATING SUBSTRATE: 100%	5.83

<Manufacturing Method>

[0030] FIG. 5 is a diagram to explain an example of a manufacturing method of the wiring substrate of the embodiment.

[0031] The manufacturing method of the embodiment includes, in chronological order, a pretreatment step J1 of cleaning and drying an AlN substrate 70, a step J2 of applying an organic Ti solution 71 to the AlN substrate 70, and a baking step J3 of baking the AlN substrate 70 to which the organic Ti solution 71 has been applied. In the pretreatment step J1, anisotropic etching using an agent or reactive ions may be performed to form the fine recesses 12D in the surface of the AlN substrate 70. In the baking step J3, baking is performed under conditions of 400°C or higher and 30 minutes or longer. Thus, the organic Ti solution 71 solidifies and becomes a titanium oxide layer 71A. This manufacturing method further includes a step J4 of applying electroless Cu plating 74 to a substrate 72 after the baking and cooling, and a sintering step J5 of performing sintering thereon.

[0032] In this manufacturing method, since the titanium oxide and the conductor layer 14 are formed by the applying, baking and plating, the wiring substrate 10 can be manufactured at low cost.

[0033] In the sintering step J5, in an atmosphere of an inert gas, sintering is performed under conditions of 300°C or higher and 30 minutes or longer. Through the sintering under these conditions, Cu of the electroless Cu plating 74 reaches the AlN substrate 70 through the titanium oxide layer 71A, so that at the interface, the interlayer 16 having Al, N and Cu concentration gradients is formed.

[0034] Further, through the sintering under the conditions, C (carbon) component of the electroless Cu plating 74 diffuses from the interface to the electroless Cu plating 74 side. In addition, through the sintering under the conditions, the C component of the electroless Cu plating 74 reacts with O (oxygen) component contained in the plating solution, and disperses to the outside as CO gas or CO_2 gas. Thus, C concentration of the interlayer 16 decreases to 10 at% or less.

[0035] Further, through the sintering under the conditions, the titanium oxide layer 71A changes to the adhesive regions e1 scattered at the interface, and at the position of each adhesive region e1, the interlayer 16A containing Ti and O is formed.

[0036] As described above, according to the wiring substrate 10 of this embodiment, if, of the interlayer 16, the first region 16r1 near the insulating substrate 12 and the second region 16r2 near the conductor layer 14 are compared with one another, the Cu concentration is higher in the second region 16r2 than in the first region 16r1. Further, the Al concentration is higher in the first region 16r1 than in the second region 16r2. Due to these concentration gradients, from the insulating substrate 12 side to the conductor layer 14 side of the interlayer 16, change in coefficient of thermal expansion is gentle. This can reduce stress concentration due to difference in coefficient of thermal expansion between films, and achieve high adhesive strength between the insulating substrate 12 and the conductor layer 14.

[0037] Further, in the interlayer 16, the N concentration is higher in the first region 16r1 near the insulating substrate 12 than in the second region 16r2 near the conductor layer 14. Hence, change in coefficient of thermal expansion in the interlayer 16 is gentler. This can further reduce stress concentration due to difference in coefficient of thermal expansion between films, and achieve higher adhesive strength between the insulating substrate 12 and the conductor layer 14. Similarly, in the interlayer 16, the AL and N concentrations gradually decrease in the direction from the insulating substrate 12 to the conductor layer 14. Hence, change in coefficient of thermal expansion in the interlayer 16 is gentler. This can

further reduce stress concentration due to difference in coefficient of thermal expansion between films, and achieve higher adhesive strength between the insulating substrate 12 and the conductor layer 14.

[0038] Further, according to the wiring substrate 10 of this embodiment, at the interface of the region outside the fine recesses 12D of the insulating substrate 12 and on the inner surfaces of the recesses 12D, the interlayer(s) 16 having Al, N and Cu concentration gradients is present. This can achieve higher adhesive strength between the insulating substrate 12 and the conductor layer 14.

[0039] Further, according to the wiring substrate 10 of this embodiment, on the inner surfaces of the recesses 12D, the interlayer(s) 16A containing Ti and O is scattered. Ti and O forming no layer but being scattered can achieve gentler Al, N and Cu concentration gradients at portions where the interlayer 16A containing Ti and O is scattered and therearound, and accordingly achieve higher adhesive strength of the interface. Further, achieving higher adhesive strength inside the recesses 12D can further increase the adhesive strength between the insulating substrate 12 and the conductor layer 14 as a whole.

[0040] Further, according to the wiring substrate 10 of this embodiment, in the interlayers 16, 16A, the C concentration is 10 at% or less. If C occupies an interface, strength of the interface decreases. In this embodiment, decrease of the strength due to C of the interface is suppressed. The structural element having the above C concentration and its effect are especially effective if the conductor layer 14 is formed by plating.

[0041] Further, according to the electronic device 40 and the electronic module 100 of this embodiment, the wiring substrate 10 in which the adhesive strength of the conductor layer 14 is high is used. This exhibits an effect of achieving high reliability.

[0042] In the above, an embodiment(s) of the present disclosure has been described. However, the present invention is not limited to the above embodiment. For example, in the above embodiment, at the interface between the insulating substrate 12 and the conductor layer 14, the adhesive regions containing Ti and O are scattered, but this structure may not be provided. Further, the C (carbon) concentration of the interlayer may be different from that described in the above embodiment. Further, in the above embodiment, an example of the manufacturing method of the wiring substrate has been described, but the wiring substrate according to the present invention may be manufactured by a manufacturing method different from that of the above embodiment. Further, the details described in the above embodiment can be appropriately modified within a range not departing from the scope of the invention.

Industrial Applicability

[0043] The present disclosure is applicable to a wiring substrate, an electronic device and an electronic module.

Claims

1. A wiring substrate comprising:

an insulating substrate containing AlN;
a conductor layer containing Cu; and
an interlayer located between the insulating substrate and the conductor layer,
wherein in the interlayer, between a first region near the insulating substrate and a second region near the conductor layer,

Cu concentration is higher in the second region than in the first region, and
Al concentration is higher in the first region than in the second region.

2. The wiring substrate according to claim 1, wherein N concentration is higher in the first region than in the second region.

3. The wiring substrate according to claim 1 or 2, wherein in the interlayer, the Al concentration and N concentration gradually decrease in a direction from the insulating substrate to the conductor layer.

4. The wiring substrate according to any one of claims 1 to 3,

wherein the insulating substrate has a plurality of recesses on a conductor layer side thereof, and
wherein the interlayer is present outside the recesses and in the recesses.

5. The wiring substrate according to claim 4, wherein the interlayer further contains Ti and O.

6. The wiring substrate according to claim 4, wherein Ti of the interlayer is scattered at an interface of the insulating substrate in the recesses.

7. The wiring substrate according to any one of claims 1 to 6, wherein from an insulating substrate side to a conductor layer side of the interlayer, C concentration is 10 at% or less.

8. An electronic device comprising:

the wiring substrate according to any one of claims 1 to 7; and
an electronic component mounted on the wiring substrate.

9. An electronic module comprising:

the electronic device according to claim 8; and
a module board where the electronic device is mounted.

FIG.1A

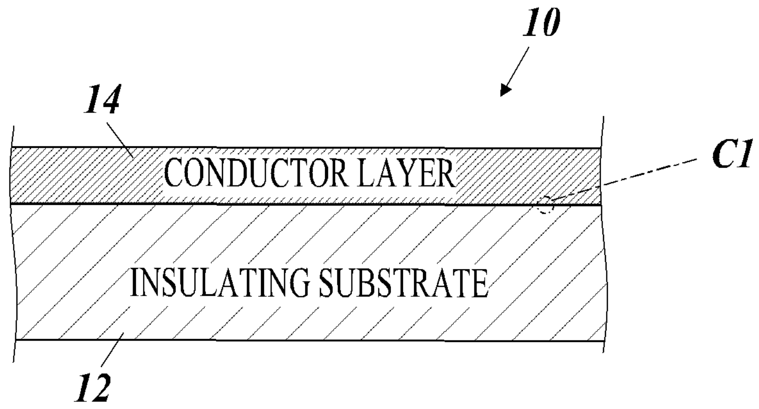


FIG.1B

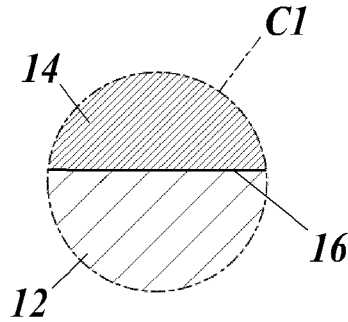


FIG.1C

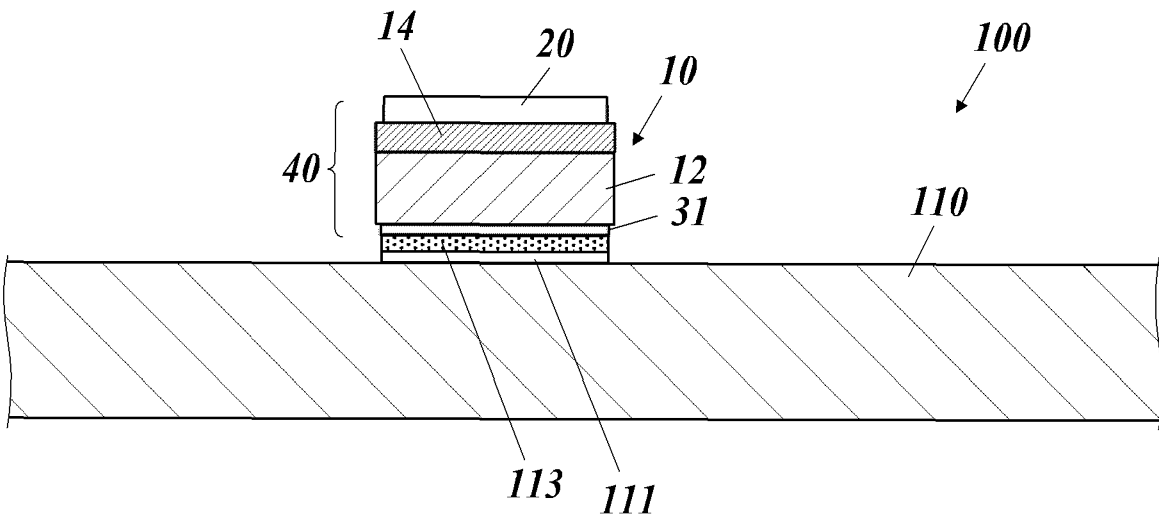


FIG.2A

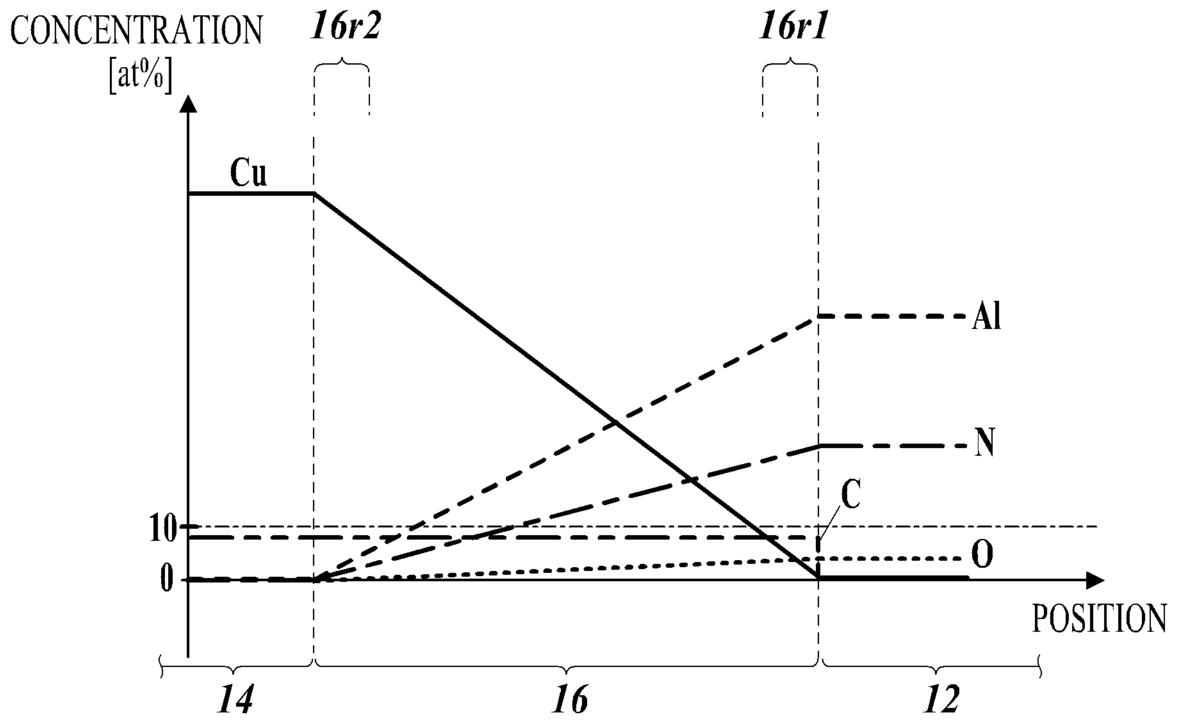


FIG.2B

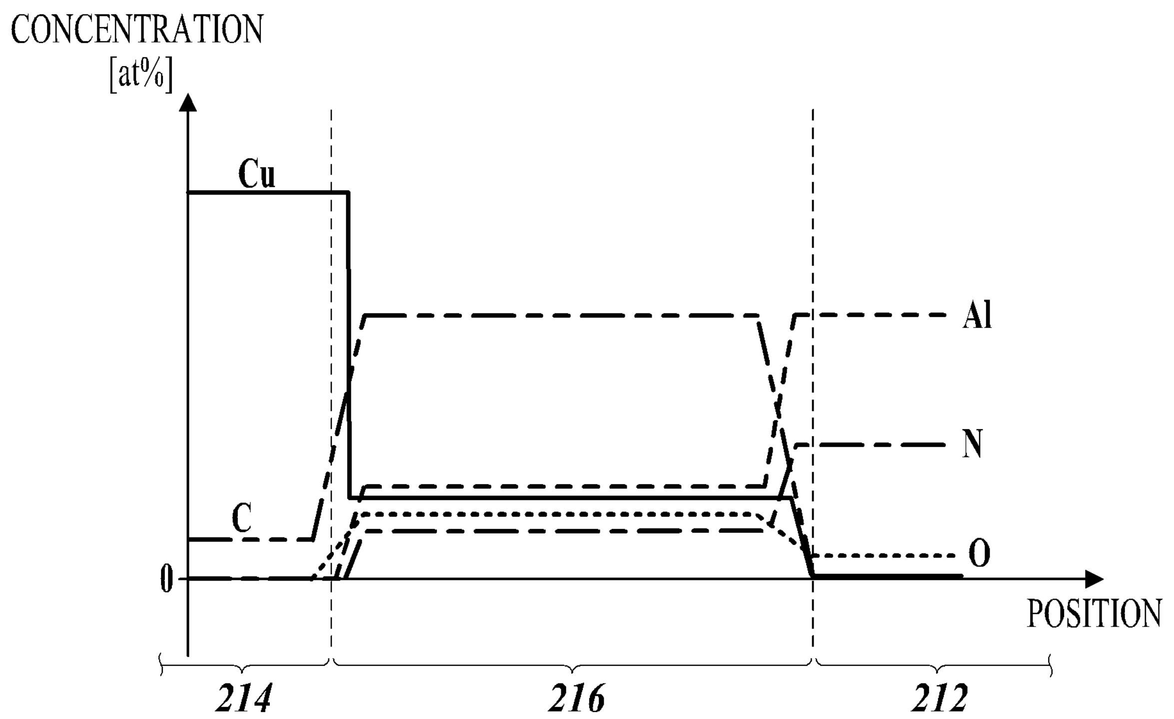


FIG.3

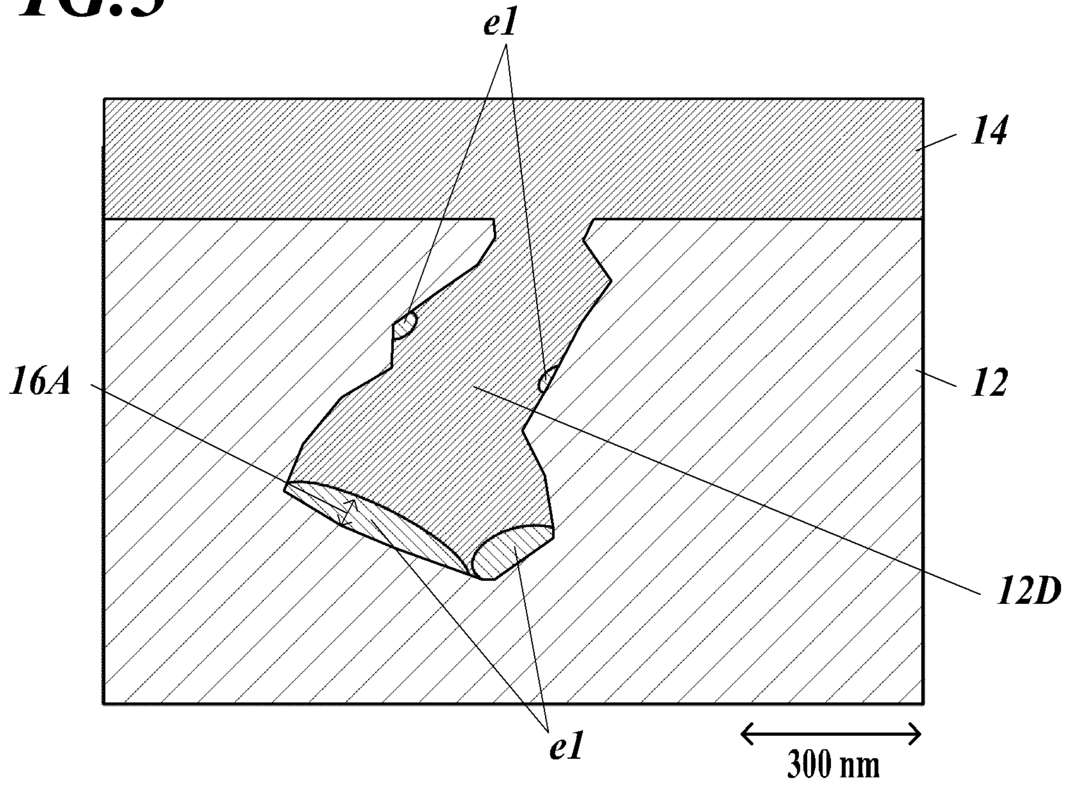


FIG.4

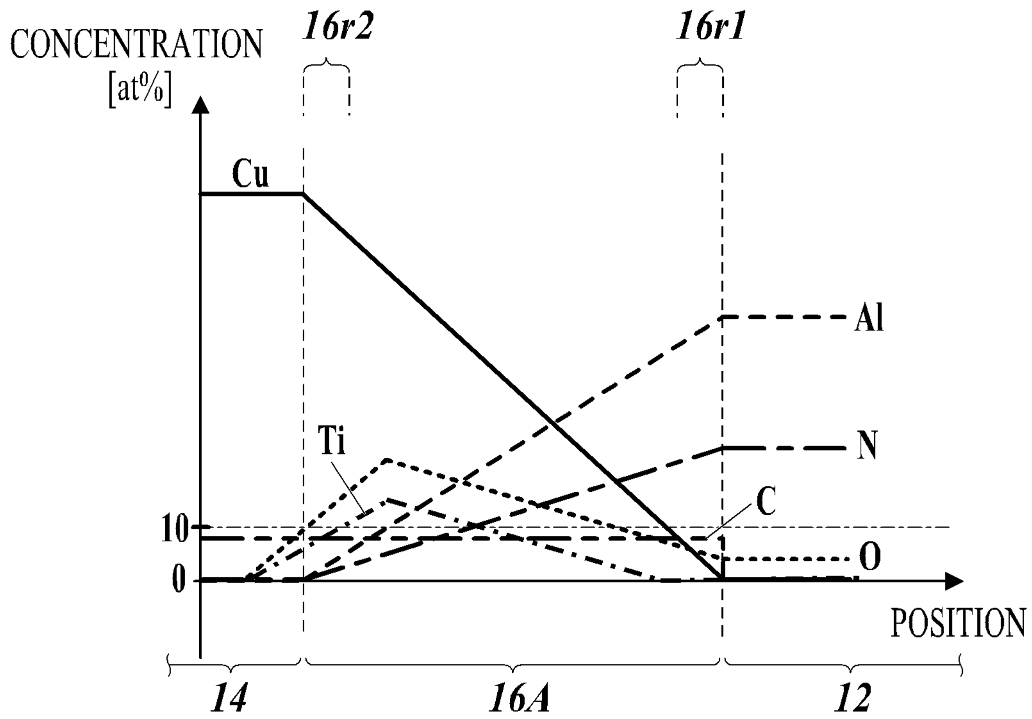
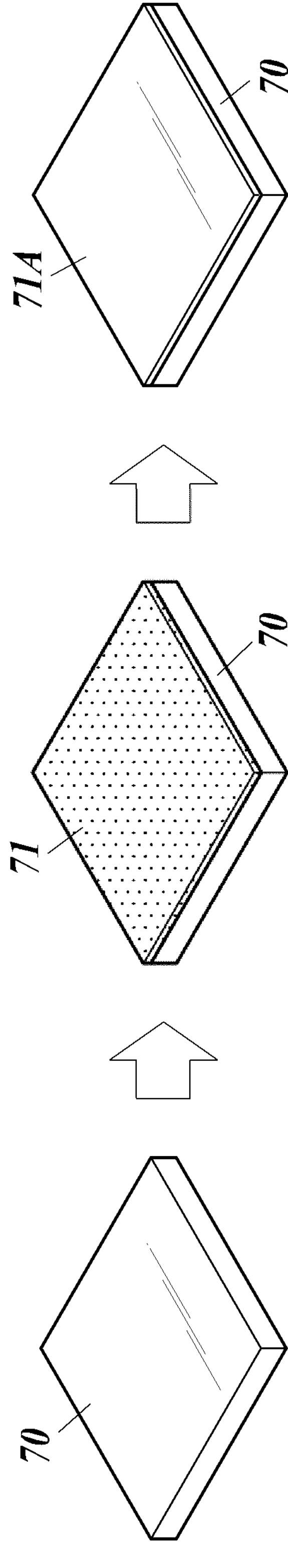


FIG.5

J1 : PRETREATMENT STEP

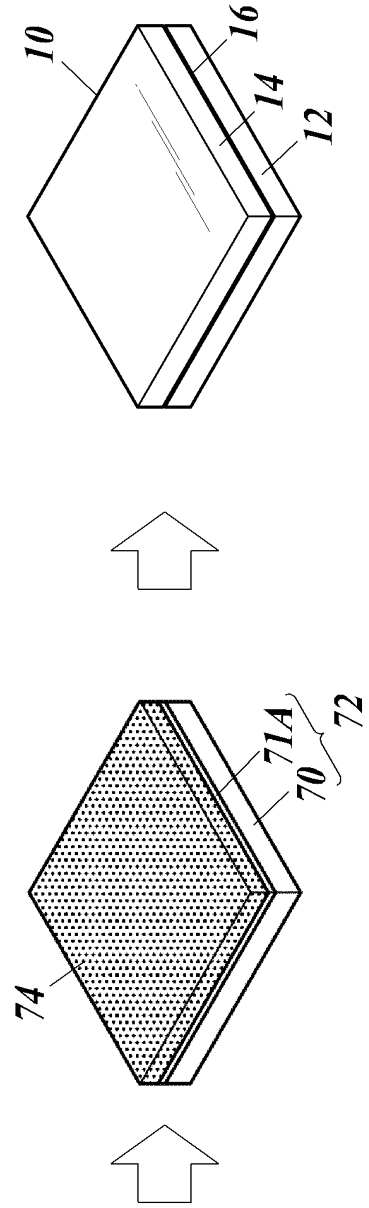
J2 : ORGANIC Ti SOLUTION APPLYING STEP

J3 : BAKING STEP



J4 : ELECTROLESS Cu PLATING STEP

J5 : SINTERING STEP



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2019/046867

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl. H01L23/13(2006.01)i, H05K1/03(2006.01)n, H05K1/09(2006.01)i, H05K3/38(2006.01)i
FI: H05K1/09 A, H05K3/38 B, H01L23/12 C, H05K1/03 610E
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
Int. Cl. H01L23/13, H05K1/03, H05K1/09, H05K3/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2020
Registered utility model specifications of Japan 1996-2020
Published registered utility model applications of Japan 1994-2020

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP 5-218229 A (TOSHIBA CORP.) 27 August 1993, paragraphs [0019]-[0021], [0024]-[0028], fig. 4	1-5, 7-9 6
A	JP 2016-058706 A (JX NIPPON MINING & METALS CORP.) 21 April 2016, paragraphs [0020]-[0043]	1-9
A	JP 60-177634 A (TOSHIBA CORP.) 11 September 1985, page 2, upper right column, line 13 to page 3, upper right column, line 2	1-9

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30.01.2020	10.02.2020

Name and mailing address of the ISA/	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/JP2019/046867

Patent Documents referred to in the Report	Publication Date	Patent Family	Publication Date
JP 5-218229 A	27.08.1993	US 5326623 A column 5, line 40 to column 6, line 49, column 7, line 8 to line 60, fig. 4	
JP 2016-058706 A	21.04.2016	(Family: none)	
JP 60-177634 A	11.09.1985	(Family: none)	

Form PCT/ISA/210 (patent family annex) (January 2015)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP H5182926 A **[0002]**