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(54) **ARRAY SUBSTRATE, PREPARATION METHOD THEREOF, DISPLAY PANEL AND DISPLAY DEVICE**

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(57) **ABSTRACT**

Disclosed are an array substrate, a preparation method thereof, a display panel and a display device. The array substrate includes a base substrate, a first thin film transistor, a photosensitive sensor, and a dielectric layer. The first thin film is on the base substrate and includes a gate, a drain, a source and a conductive channel between the drain and the source. The photosensitive sensor has the drain of the first thin film transistor as an electrode of the photosensitive sensor. The dielectric layer covers the conductive channel of the first thin film transistor, where the dielectric layer is a metal oxide film.

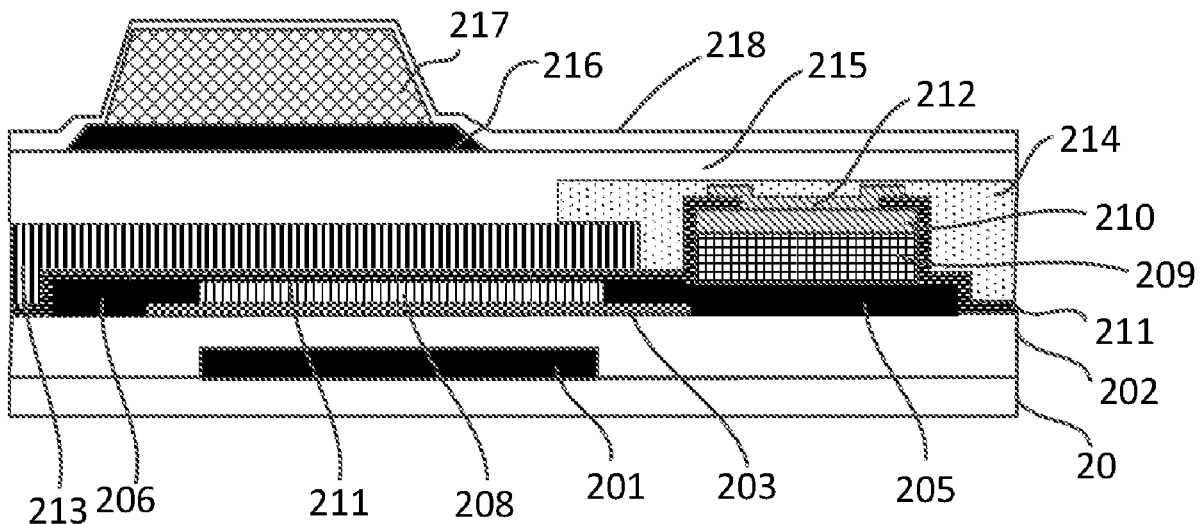
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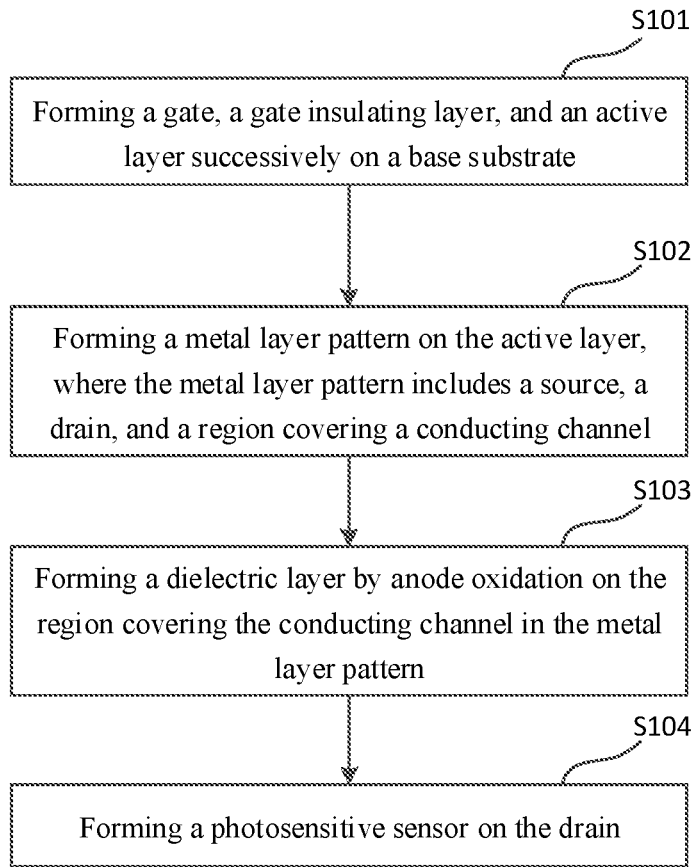


Fig. 1

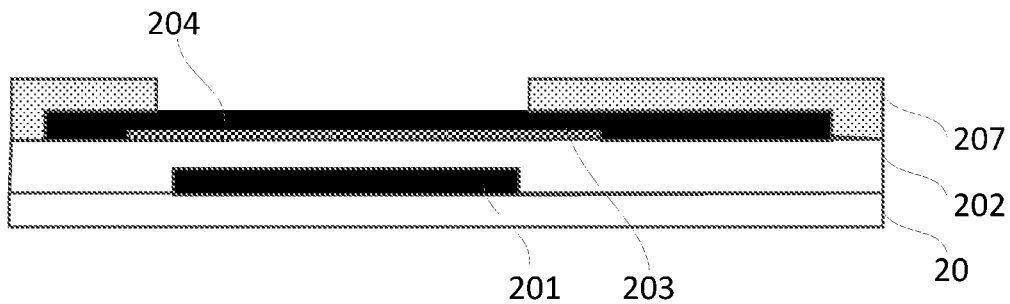


Fig. 2

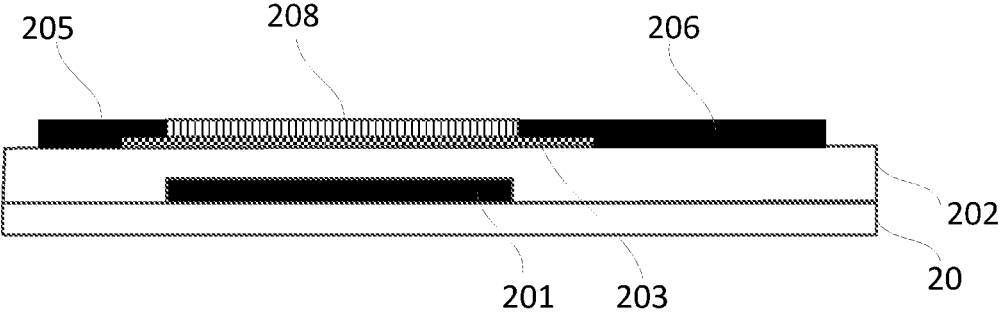


Fig. 3

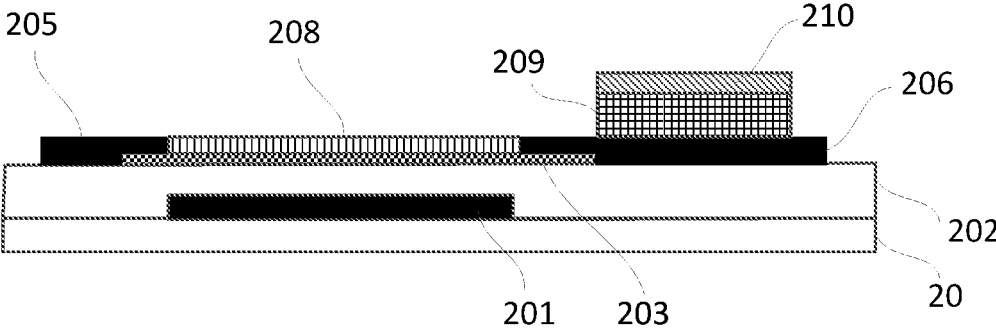


Fig. 4

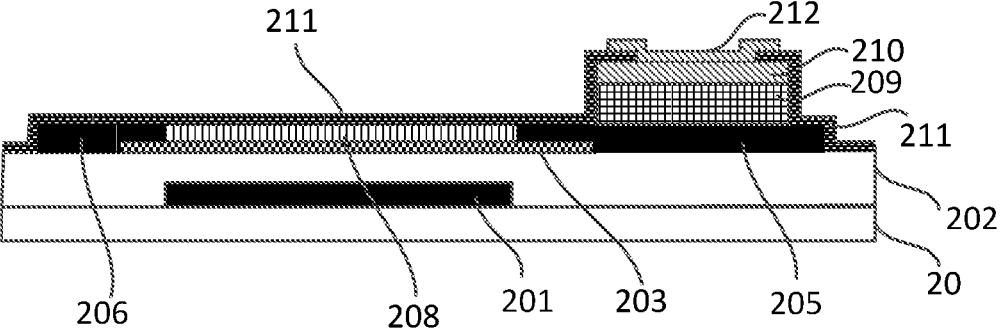


Fig. 5

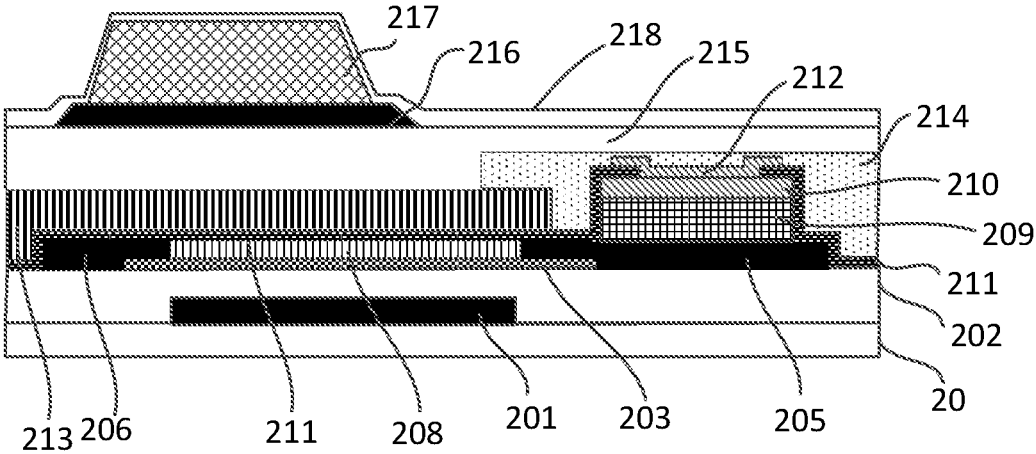


Fig. 6

**ARRAY SUBSTRATE, PREPARATION
METHOD THEREOF, DISPLAY PANEL AND
DISPLAY DEVICE**

CROSS REFERENCE TO RELATED
APPLICATION

[0001] This application claims priority to and is a continuation-in-part application of International Application No. PCT/CN2019/126106, filed on Dec. 17, 2019, designating the United States, and claiming the priority of Chinese Patent Application No. 201910002593.8, filed with the Chinese Patent Office on Jan. 2, 2019 and entitled “Array Substrate, Preparation Method thereof, Display Panel and Display Device”, which are hereby incorporated by reference in their entireties.

FIELD

[0002] The present disclosure relates to the technical field of displays, and in particular, relates to an array substrate, a preparation method thereof, a display panel and a display device.

BACKGROUND

[0003] As the demand of AMOLEDs increases in recent years, market demand on the parameters becomes higher. Brightness is one of important indicators, which matters to a good user experience. As such, customers often put forward higher requirements on brightness uniformity. If the brightness of an entire screen is not uniform, then the brightness of the entire screen is compensated.

SUMMARY

[0004] In a first aspect, an embodiment provides an array substrate. The array substrate includes a base substrate, a first thin film transistor, a photosensitive sensor, and a dielectric layer. The first thin film is on the base substrate and includes a gate, a drain, a source and a conductive channel between the drain and the source. The photosensitive sensor has the drain of the first thin film transistor as an electrode of the photosensitive sensor. The dielectric layer covers the conductive channel of the first thin film transistor, where the dielectric layer is a metal oxide film.

[0005] In some embodiments, the metal used for forming the dielectric layer and the drain of the first thin film transistor are in the same metal layer.

[0006] In a second aspect, a display panel is provided, the display panel including an array substrate in any embodiments provided in the first aspect, where the photosensitive sensor and the first thin film transistor are in a non-display area of the display panel.

[0007] In some embodiments, the display panel is an OLED display panel; the array substrate further includes a light emitting device located in a display area, and a second thin film transistor connected to the light emitting device; and the first thin film transistor and the second thin film transistor are in the same film layer.

[0008] In some embodiments, the display panel is an LCD display panel, and the array substrate further includes a third thin film transistor located in a display area, and the first thin film transistor and the third thin film transistor are in the same film layer.

[0009] In third aspect, an embodiment of the present disclosure provides a display device, the display device including a display panel in any embodiments provided in the second aspect.

[0010] In a fourth aspect, an embodiment of the present disclosure provides a preparation method of an array substrate. The method includes: forming a gate, a gate insulating layer, and an active layer successively on a base substrate; forming a metal layer pattern on the active layer, where the metal layer pattern includes a source, a drain, and a region covering a conductive channel; forming a dielectric layer by anodic oxidation on the region covering the conductive channel in the metal layer pattern; and forming a photosensitive sensor on the drain.

[0011] In some embodiments, forming a dielectric layer by anodic oxidation on the region covering the conductive channel in the metal layer pattern includes: forming a photoresist layer on the metal layer pattern; patterning the photoresist layer to expose the region covering the conductive channel in the metal layer pattern; and performing anodic oxidation on the region covering the conductive channel in the metal layer pattern by using the patterned photoresist layer as a shield, to form the dielectric layer.

[0012] In some embodiments, forming a dielectric layer by anodic oxidation on the region covering the conductive channel in the metal layer pattern includes: forming a metal oxide thin film on a surface of the region covering the conductive channel in the metal layer pattern, via an electrolysis process in a constant current constant voltage mode using a citric acid solution at normal pressure and room temperature.

[0013] In some embodiments, forming a photosensitive sensor on the drain includes: forming a phosphorous or arsenic doped semiconductor layer, an intrinsic semiconductor layer, a boron-doped semiconductor layer, and a transparent conductive oxide layer successively on the drain; and with the same mask, patterning the transparent conductive oxide layer by wet etching, and patterning the phosphorous or arsenic doped semiconductor layer, the intrinsic semiconductor layer, and the boron-doped semiconductor layer by dry etching to form the photosensitive sensor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a schematic flow diagram of a preparation method of an array substrate provided in an embodiment of the present disclosure;

[0015] FIG. 2 is a schematic structural diagram of an array substrate provided in an embodiment of the present disclosure;

[0016] FIG. 3 is another schematic structural diagram of an array substrate provided in an embodiment of the present disclosure;

[0017] FIG. 4 is yet another schematic structural diagram of an array substrate provided in an embodiment of the present disclosure;

[0018] FIG. 5 is still yet another schematic structural diagram of an array substrate provided in an embodiment of the present disclosure; and

[0019] FIG. 6 is a further schematic structural diagram of an array substrate provided in an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0020] At present, methods for screen brightness compensation mainly include internal compensation and external compensation methods. The internal compensation method refers to that before an Organic Light Emitting Diode (OLED) emits light, a threshold voltage and mobility of a Thin Film Transistor (TFT) are compensated by a capacitance inside a display panel. However, the compensation range in this method is relatively small. The external compensation method refers to that a compensation circuit is additionally provided outside a TFT to monitor a threshold voltage for driving the TFT in real time, where the compensation is achieved by rewriting a voltage. Compared with the internal compensation method, the external compensation method may achieve a larger range of compensation.

[0021] However, the above two compensation methods can only compensate for display brightness unevenness caused by changes in the threshold voltage and mobility of the TFT, but cannot compensate for brightness changes caused by aging of display devices.

[0022] As can be seen, there is a technical problem in the related art that the brightness uniformity of an entire screen deteriorates due to aging of display devices.

[0023] To make the objects, technical solutions and advantages of the present disclosure more apparent, the technical solutions in the embodiments of the present disclosure will be described clearly and completely with reference to the drawings in the embodiments of the present disclosure.

[0024] Generally, the more uniform the brightness of a screen of a display device, the better. However, the brightness of a display device such as an OLED display panel is not uniform. Therefore, the brightness of the entire screen needs to be compensated. Methods for screen brightness compensation at present mainly include the internal compensation method and the external compensation method as described above, but the above two compensation methods cannot compensate for brightness changes caused by aging of display devices.

[0025] In view of this, in an embodiment of the present disclosure, a photosensitive sensor connected to a first thin film transistor is provided in an array substrate. The photosensitive sensor detects the actual luminance brightness of pixels of a display panel provided with the array substrate in real time, thereby compensating for the brightness of the display panel in real time to improve the uniformity of the brightness. Moreover, a dielectric layer of a metal oxide film covers a conductive channel of the first thin film transistor. The dielectric layer may prevent hydrogen gas from permeating into a region under the conductive channel to cause an adverse effect on the array substrate, where the hydrogen gas is introduced during preparation of the photosensitive sensor on a drain of the first thin film transistor and electrically connected to the drain.

[0026] Specific implementations of an array substrate, a preparation method thereof, and a display device provided in embodiments of the present disclosure will be described in detail below with reference to the drawings.

[0027] The thickness and shape of each film layer in the drawings do not reflect the true scale, and are merely intended to illustrate the present disclosure.

[0028] Referring to FIG. 1, in conjunction with FIGS. 2 to 5, an embodiment of the present disclosure provides a

preparation method of an array substrate. As shown in FIG. 1, the specific process of the preparation method is as follows.

[0029] Step S101: forming a gate 201, a gate insulating layer 202, and an active layer 204 successively on a base substrate 20.

[0030] In preparation of the array substrate in the embodiment of the present disclosure, a first thin film transistor is prepared first. Specifically, referring to FIG. 2, a gate 201, a gate insulating layer 202, and an active layer 204 may be formed successively on a base substrate 20. In some embodiments, a metal layer may be deposited on the glass, then a photoresist layer is coated on the metal layer, and the photoresist layer is patterned to form a pattern of the gate 201. The material of the metal layer may be a common metal such as Mo, Al, Ti, Au, Cu, Hf, or Ta, and may also be a Cu alloy, such as a MoNd/Cu/MoNd metal layer formed by a Cu process.

[0031] The gate insulating layer 202 (GI layer) and an Act layer are successively deposited on the gate 201, and then the Act layer is patterned by wet etching to form the active layer 204. The material of the GI layer may be silicon oxide, silicon nitride, silicon oxynitride or other insulating material, and the material of the Act layer may be a metal oxide material, such as an IGZO material.

[0032] Step S102: forming a metal layer pattern on the active layer 204, where the metal layer pattern includes a source 205, a drain 206, and a region covering a conductive channel.

[0033] After the active layer 204 is prepared in the embodiment of the present disclosure, a metal layer may be deposited on the active layer 204. The material of the metal layer may be a metal such as Mo, Al, Ti, Au, Hf, or Ta, or an alloy of some of the metals. A metal layer pattern is formed by patterning the metal layer. The formed metal layer pattern includes a source 205, a drain 206, and a region covering a conductive channel.

[0034] Step S103: forming a dielectric layer 207 by anodic oxidation on the region covering the conductive channel in the metal layer pattern.

[0035] Here, anodic oxidation is an accelerated electrochemical oxidation process. It involves the application of an electrical bias at relatively low currents while the substrate is immersed in an acid bath. The films can be very dense and stable, with a variety of microstructural characteristics.

[0036] As shown in FIG. 2, in the embodiment of the present disclosure, a photoresist layer 207 may be formed on the metal layer pattern. The photoresist layer 207 is patterned to expose the region covering the conductive channel in the metal layer pattern, and then anodic oxidation is performed on the region covering the conductive channel in the metal layer pattern by using the patterned photoresist layer 207 as a shield, to form a dielectric layer 208, thus obtaining a first thin film transistor as shown in FIG. 3.

[0037] In some embodiments, the anodic oxidation may be performed via an electrolysis process in a constant current constant voltage mode using a citric acid solution at normal pressure and room temperature to form a metal oxide thin film on the surface of the region covering the conductive channel in the metal layer pattern, such as a metal oxide thin film of a high-K medium such as aluminum oxide, hafnium oxide, tantalum oxide, or zirconium oxide, thus obtaining a dielectric layer 208. As the dielectric layer 208 is a metallic oxide film, it has high compactness and may block a gas or

the like from penetrating into the lower part of the first thin film transistor through the conductive channel to cause an adverse effect on the array substrate.

[0038] Step S104: forming a photosensitive sensor on the drain **206**.

[0039] After the first thin film transistor is prepared in the embodiment of the present disclosure, a photosensitive sensor **209** may be formed on the drain **206** of the first thin film transistor. Specifically, a phosphorous or arsenic doped semiconductor layer, an intrinsic semiconductor layer, a boron-doped semiconductor layer, and a transparent conductive oxide layer **210**, such as an ITO layer, may be formed successively on the drain **206**. With the same mask, the transparent conductive oxide layer **210** is patterned by wet etching, the phosphorous or arsenic doped semiconductor layer, the intrinsic semiconductor layer, and the boron-doped semiconductor layer are patterned by dry etching to form a photosensitive sensor **209** as shown in FIG. 4, thus obtaining an array substrate provided in an embodiment of the present disclosure.

[0040] In preparation of the array substrate in the embodiment of the present disclosure, the first thin film transistor is prepared before the photosensitive sensor **209**. As the conductive channel of the first thin film transistor is provided with the dielectric layer **208** formed by anodic oxidation of a metal, and the dielectric layer **208** has high compactness, the hydrogen gas introduced in the subsequent process of preparing the photosensitive sensor **209** may be blocked from entering the lower part of the first thin film transistor through the conductive channel to affect the array substrate. Furthermore, the photosensitive sensor **209** is prepared after the first thin film transistor as a whole is prepared in the embodiment of the present disclosure, which may avoid an influence on a sidewall of the photosensitive sensor during the wet-etching patterning process in the preparation of the first thin film transistor, so as to reduce a device leakage current.

[0041] After the photosensitive sensor **209** is prepared in the embodiment of the present disclosure, a PVX protective layer **211** may be deposited. The PVX protective layer **211** is patterned to form via holes, where the material of the PVX protective layer **211** may be an insulating material such as silicon oxide, silicon nitride, or silicon oxynitride. A projection of each via hole on the base substrate **20** is located on a projection of a pixel definition layer of the base substrate **20** on the base substrate **20**. A layer of ITO electrode **212** is deposited and patterned on a side of the photosensitive sensor **209** facing away from the base substrate **20** to form a structure shown in FIG. 5.

[0042] The array substrate provided in the embodiment of the present disclosure may be applied to top-emitting cover glass or bottom-emitting cover glass. Subsequent process steps for preparing an array substrate are introduced below by using an array substrate provided in the embodiment of the present disclosure applied to top-emitting cover glass as an example.

[0043] In some embodiments, after the array substrate shown in FIG. 5 is obtained in the embodiment of the present disclosure, a black matrix BM**213** may be further deposited and patterned on the PVX protective layer **211** so that the BM**213** covers the active matrix TFT. A color film CF layer **214** is deposited on the ITO layer **212** on the photosensitive sensor. Specifically, in preparation of the CF layer **214**, R, G, and B color films are successively deposited so that the color

films cover the BM**213** to some extent. Then, an OC layer **215** and an auxiliary electrode **216** may be deposited and patterned on the upper surface of the array substrate obtained after preparation of the BM**213** and the CF layer **214**. The material of the auxiliary electrode **216** may be a common metal such as Mo, Al, Ti, Au, Cu, Hf, or Ta, or may also be an alloy such as AlNd, or MoNb, or may also be multiple layers of metals, such as metal layers of MoNb/Cu/MoNb, or AlNd/Mo/AlNd. Then, a support PS (Photo Spacer) layer may be deposited and a support **217** is formed, and then a layer of transparent conductive oxide TCO film **218** is deposited as a transparent cathode. Where the material of the transparent conductive oxide film **218** may be a common material such as AZO, IZO, or AZTO, or a combination of these materials, thus completing preparation of the cover part, and obtain a structure shown in FIG. 6.

[0044] Further referring to FIG. 4, based on the same inventive concept, an embodiment of the present disclosure further provides an array substrate prepared by the above preparation method. The array substrate includes a base substrate **20**, a first thin film transistor on the base substrate **20**, and a photosensitive sensor **209** connected to the first thin film transistor. Where the photosensitive sensor **209** is on a drain **206** of the first thin film transistor and electrically connected to the drain **206**, and a dielectric layer **208** is formed by anodic oxidation of a metal on a conductive channel of the first thin film transistor.

[0045] In specific implementation of the above-mentioned array substrate provided in the embodiment of the present disclosure, the metal used for forming the dielectric layer **208** and the drain **206** of the first thin film transistor may be in the same metal layer.

[0046] Specifically, further referring to FIG. 4, the array substrate further includes a gate **201**, a gate insulating layer **202** and an active layer **204** on the base substrate **20**, and a metal layer on a side of the active layer **204** facing away from the base substrate **20**. The metal layer may include a source **205**, a drain **206**, and a region covering a conductive channel. Anodic oxidation is performed on the region covering the conductive channel in the metal layer pattern to form the dielectric layer **208**. That is, the metal used for forming the dielectric layer **208** and the drain **206** of the first thin film transistor are in the same metal layer. The photosensitive sensor **209** is obtained by successively forming a phosphorous or arsenic doped semiconductor layer, an intrinsic semiconductor layer, and a boron-doped semiconductor layer on the drain **206**.

[0047] Based on the same inventive idea, an embodiment of the present disclosure further provides a display panel, which includes an array substrate formed by the above preparation method, where the photosensitive sensor **209** and the first thin film transistor are in a non-display area of the display panel.

[0048] The array substrate provided in an embodiment of the present disclosure may be applied to the display field. For example, it may be made into an OLED. The display panel may also be made into an LCD display panel. In some embodiments, the display panel is an OLED display panel, and the array substrate may further include a light emitting device located in a display area, and a second thin film transistor connected to the light emitting device. The first thin film transistor and the second thin film transistor are in the same film layer. In some embodiments, the display panel is an LCD display panel, and the array substrate may further

include a third thin film transistor located in a display area, and the first thin film transistor and the third thin film transistor are in the same film layer.

[0049] Of course, if the array substrate provided in the embodiment of the present disclosure is applied to the field of touch panels, the array substrate further includes components necessary for a touch panel, which will not be described in detail here.

[0050] Based on the same inventive idea, an embodiment of the present disclosure further provides a display device, which includes any above-mentioned display panel provided in an embodiment of the present disclosure. If a color effect is required for the display device, a color filter or other color device such as a quantum dot film may be provided in any layer or multiple layers of any panel of the display panel. The display device may be a mobile phone, a tablet computer, a television, a display, a notebook computer, a digital photo frame, a navigator, or any other product or component with display and touch functions. For the implementation of the display device, reference may be made to the embodiment of the above-mentioned array substrate, and repeated description is omitted here.

[0051] Evidently those skilled in the art may make various modifications and variations to the present disclosure without departing from the spirit and scope of the present disclosure. Thus, the present disclosure is also intended to encompass these modifications and variations thereto so long as the modifications and variations come into the scope of the claims appended to the present disclosure and their equivalents.

We claim:

1. An array substrate, comprising:
 - a base substrate;
 - a first thin film transistor on the base substrate, wherein the first thin film transistor comprises a gate, a drain, a source and a conductive channel between the drain and the source;
 - a photosensitive sensor with the drain of the first thin film transistor as an electrode of the photosensitive sensor; and
 - a dielectric layer covering the conductive channel of the first thin film transistor, wherein the dielectric layer is a metal oxide film.
2. The array substrate according to claim 1, wherein the metal used for the dielectric layer and the drain of the first thin film transistor are in a same metal layer.
3. A display panel, comprising an array substrate, wherein the array substrate comprises:
 - a base substrate;
 - a first thin film transistor on the base substrate, wherein the first thin film transistor comprises a gate, a drain, a source and a conductive channel between the drain and the source;
 - a photosensitive sensor with the drain of the first thin film transistor as an electrode of the photosensitive sensor; and
 - a dielectric layer covering the conductive channel of the first thin film transistor, wherein the dielectric layer is a metal oxide film;
 wherein the photosensitive sensor and the first thin film transistor are in a non-display area of the display panel.

4. The display panel according to claim 3, wherein the display panel is an OLED display panel; and the array substrate further comprises:

- a light emitting device located in a display area; and
 - a second thin film transistor connected to the light emitting device;
- wherein the first thin film transistor and the second thin film transistor are in a same film layer.

5. The display panel according to claim 3, wherein the display panel is an LCD display panel, and the array substrate further comprises:

- a third thin film transistor located in a display area, wherein the first thin film transistor and the third thin film transistor are in a same film layer.

6. A display device, comprising the display panel according to claim 3.

7. A preparation method of an array substrate, comprising: forming a gate, a gate insulating layer, and an active layer successively on a base substrate;

forming a metal layer pattern on the active layer, wherein the metal layer pattern comprises a source, a drain, and a region covering a conductive channel;

forming a dielectric layer by anodic oxidation on the region covering the conductive channel in the metal layer pattern; and

forming a photosensitive sensor on the drain.

8. The method according to claim 7, wherein said that forming the dielectric layer by anodic oxidation on the region covering the conductive channel in the metal layer pattern comprises:

forming a photoresist layer on the metal layer pattern; patterning the photoresist layer to expose the region covering the conductive channel in the metal layer pattern; and

performing anodic oxidation on the region covering the conductive channel in the metal layer pattern by using the patterned photoresist layer as a shield, to form the dielectric layer.

9. The method according to claim 7, wherein said that forming the dielectric layer by anodic oxidation on the region covering the conductive channel in the metal layer pattern comprises:

forming a metal oxide thin film on a surface of the region covering the conductive channel in the metal layer pattern, via an electrolysis process in a constant current constant voltage mode using a citric acid solution at normal pressure and room temperature.

10. The method according to claim 7, wherein said that forming a photosensitive sensor on the drain comprises:

forming a phosphorous or arsenic doped semiconductor layer, an intrinsic semiconductor layer, a boron-doped semiconductor layer, and a transparent conductive oxide layer successively on the drain; and

with a same mask, patterning the transparent conductive oxide layer by wet etching, and patterning the phosphorous or arsenic doped semiconductor layer, the intrinsic semiconductor layer, and the boron-doped semiconductor layer by dry etching to form the photosensitive sensor.

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