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(54) **INTELLIGENT FUNCTION UNIT AND PROGRAMMABLE LOGIC CONTROLLER SYSTEM**

(52) **U.S. Cl.**
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(57) **ABSTRACT**

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An intelligent function unit includes an input selector selecting, as an input signal, an actual input signal or a simulated input signal generated in advance; an output selector selecting whether to output an output signal to the second controlled device; and a calculator causing an input/output controller in which combination and order of use of general circuit blocks are set to process the input signal one step at a time and transmit the output signal to an engineering tool or causing the input/output controller in which combination and order of use of the general circuit blocks are set to process the input signal consecutively for a set period of two or more steps, store the output signal for each step in a logger, and transmit an output signal corresponding to the set period and stored in the logger to the engineering tool.

Publication Classification

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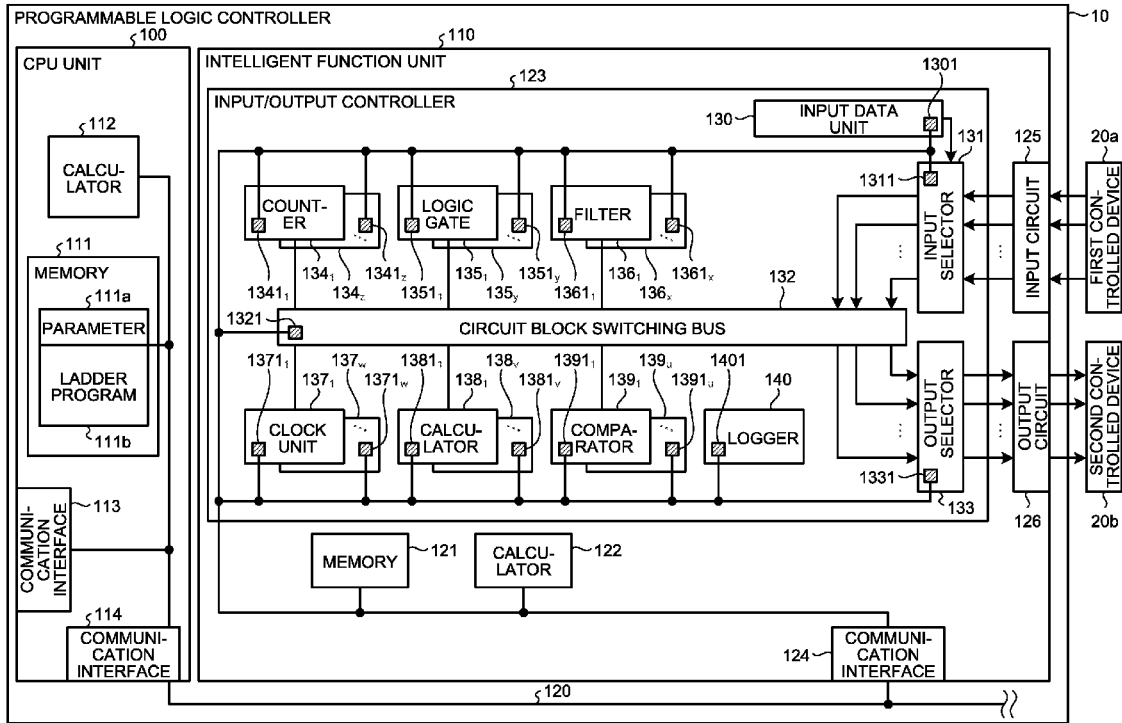


FIG.1

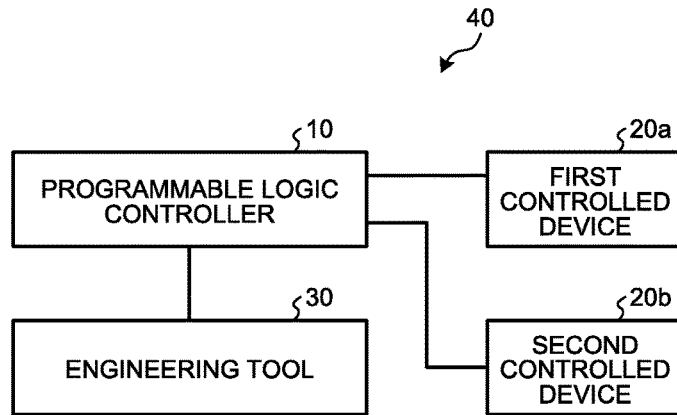


FIG.2

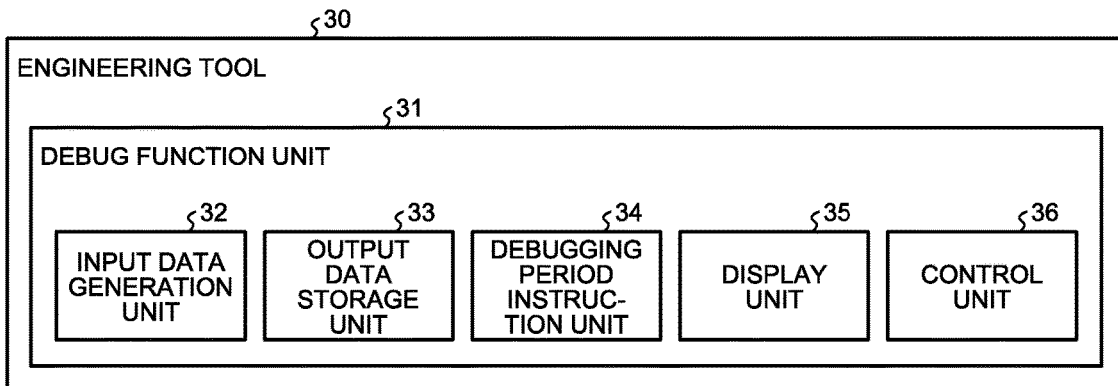


FIG.3

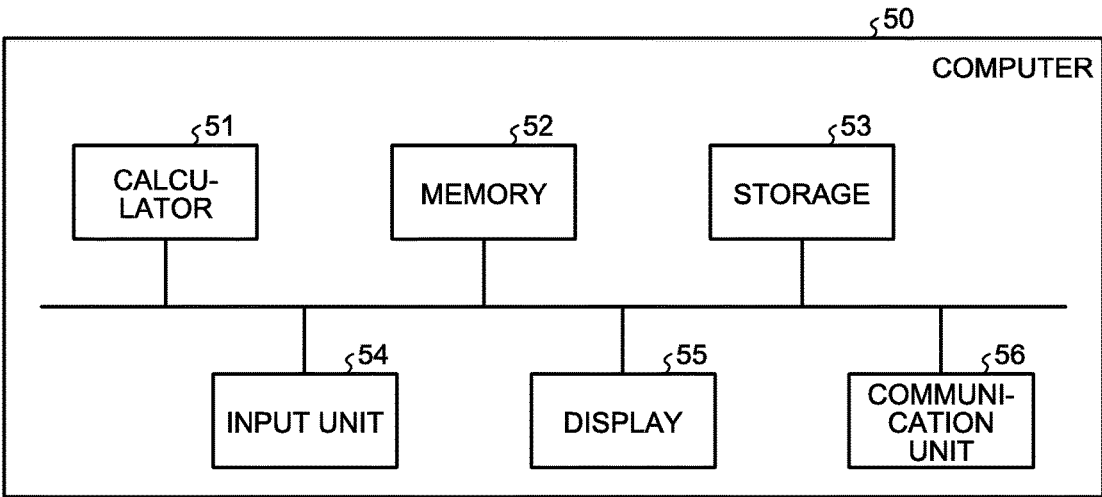


FIG.4

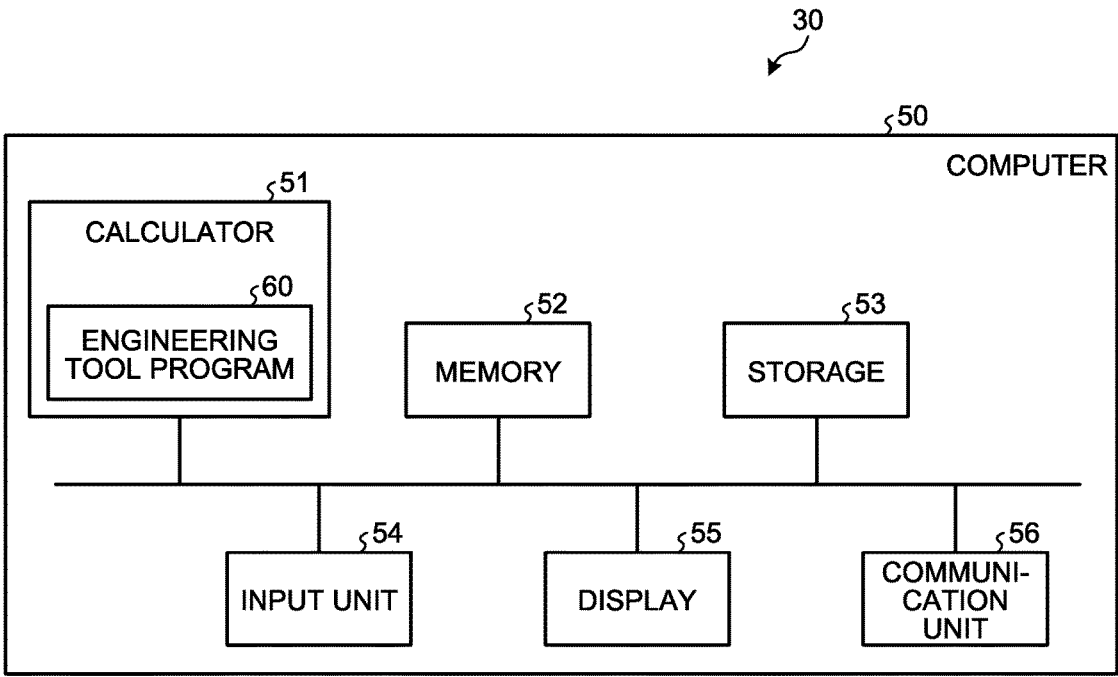


FIG.5

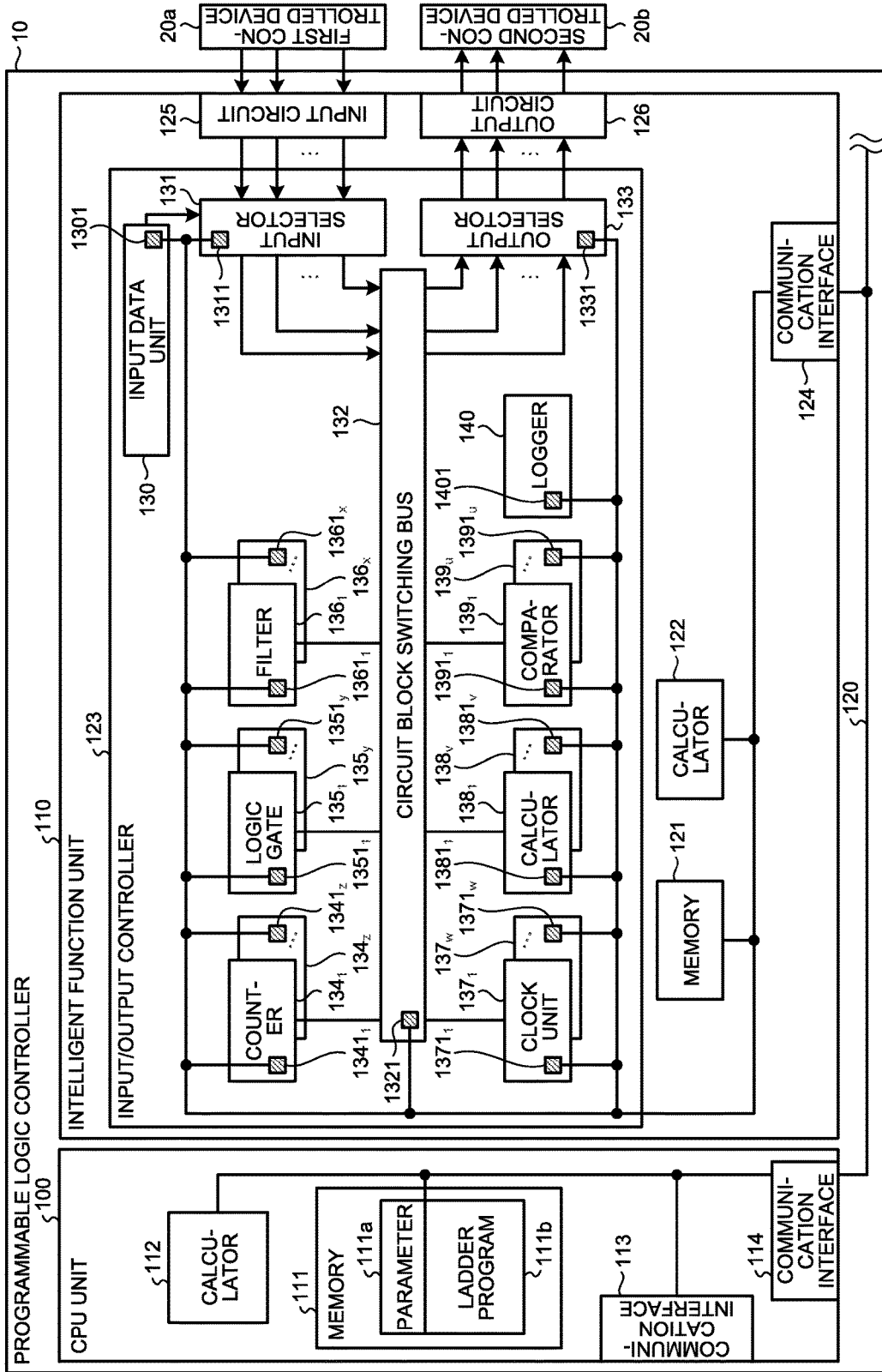


FIG.6

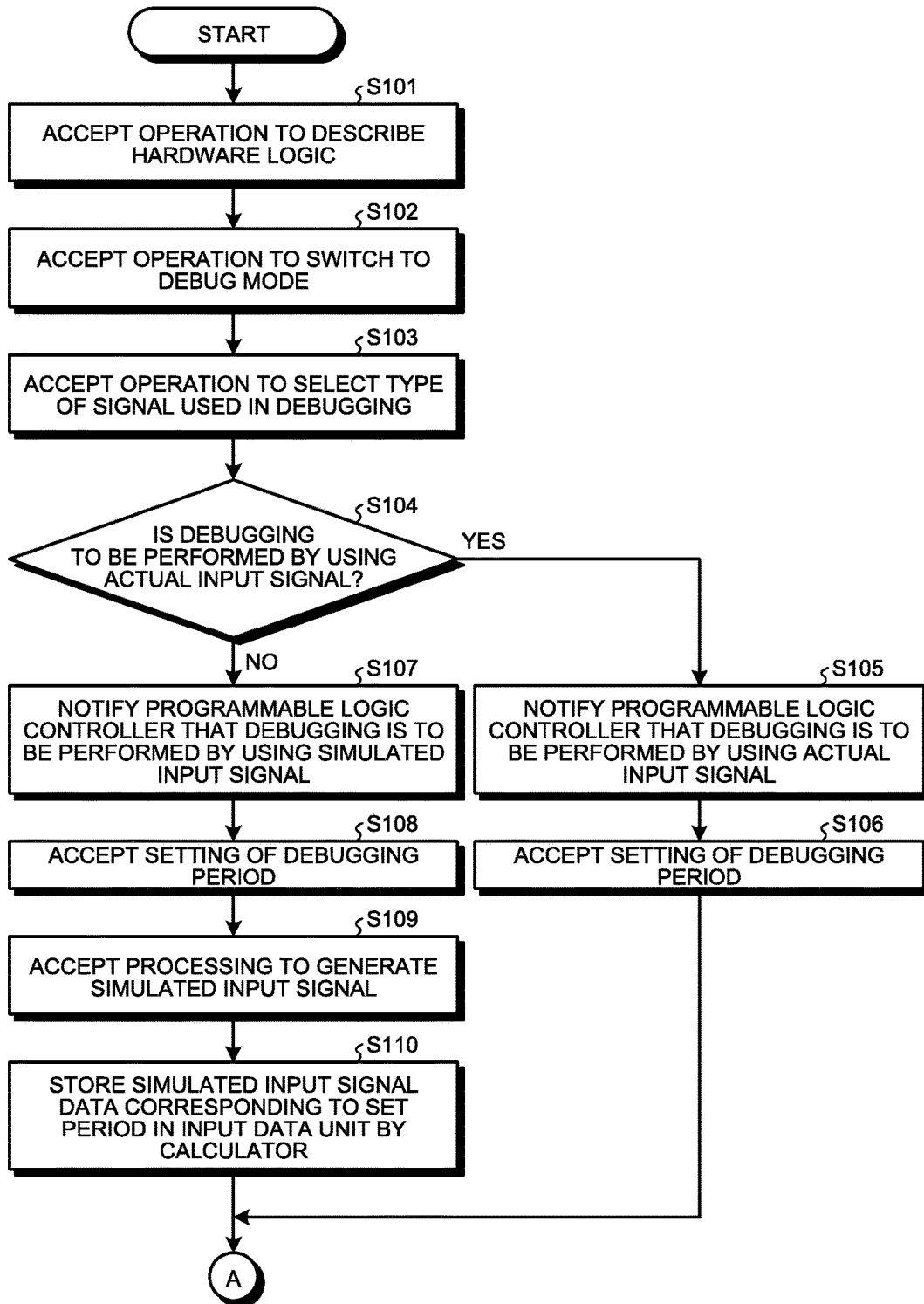


FIG.7

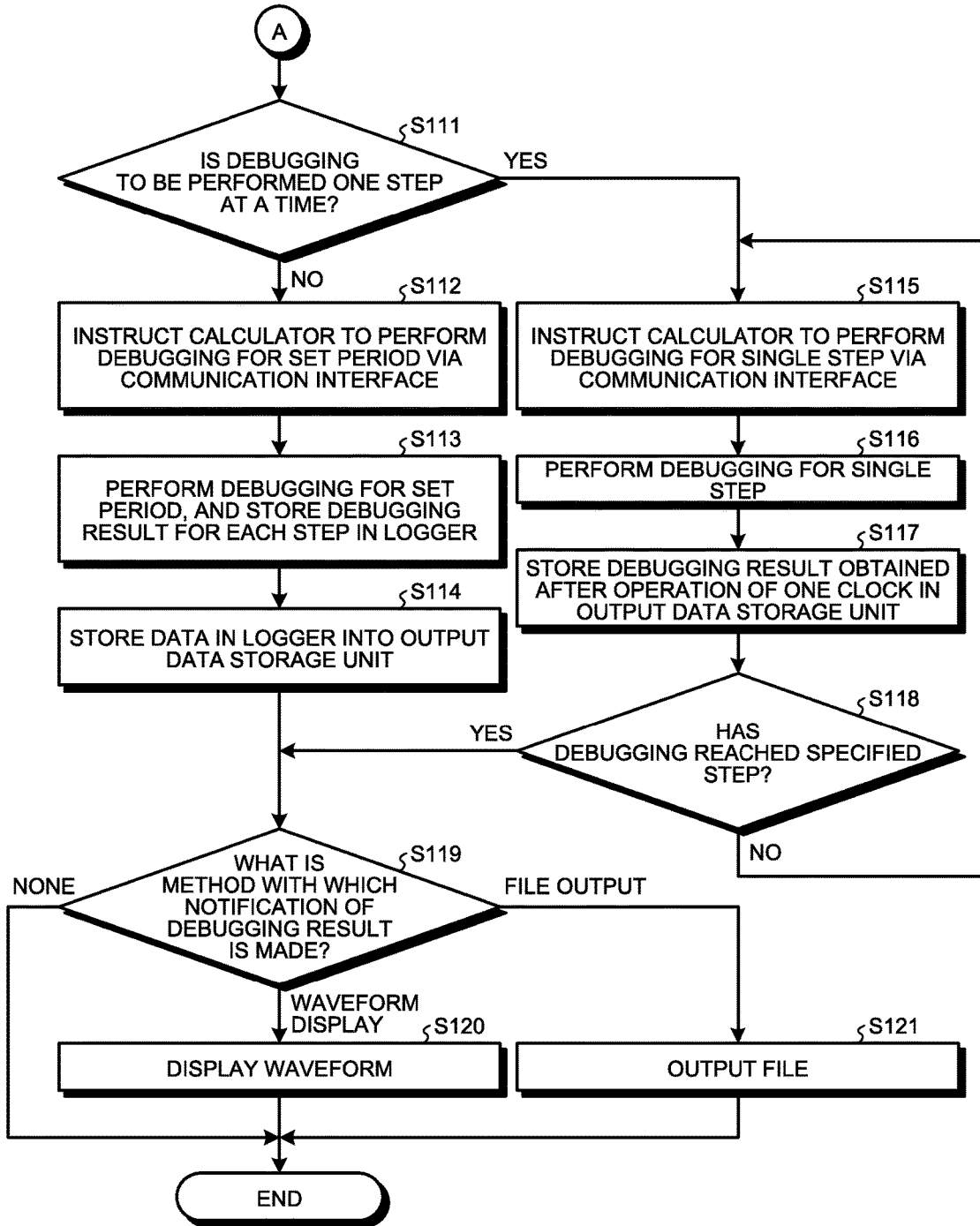


FIG.9

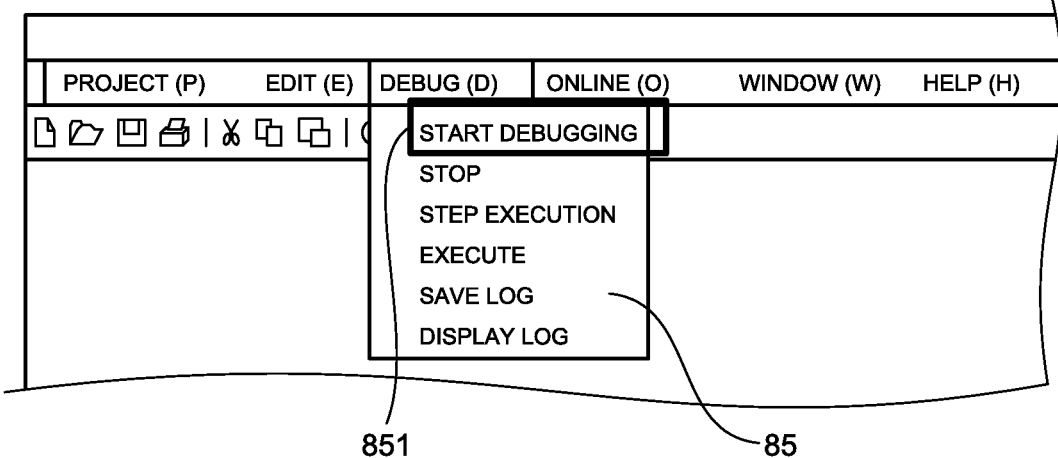


FIG.10

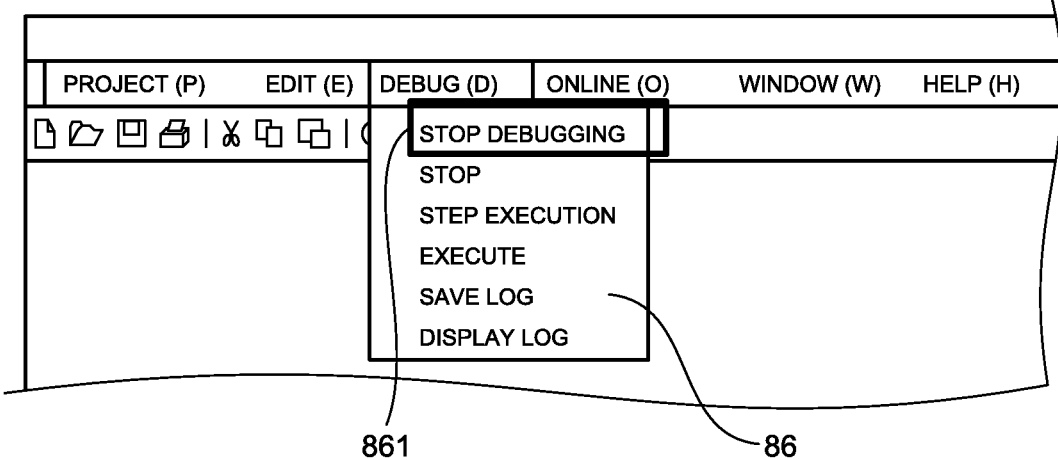


FIG.11

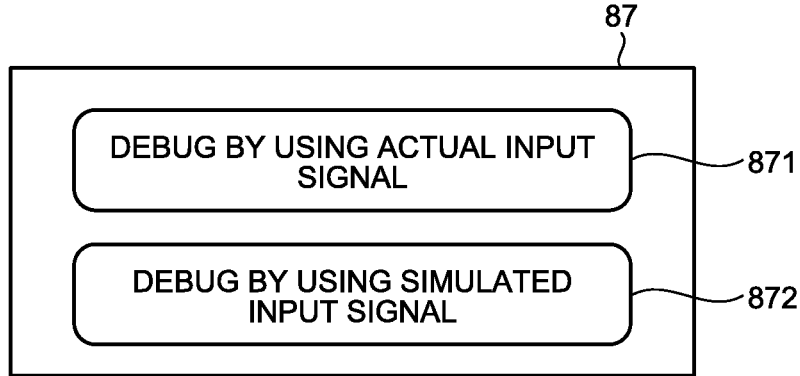


FIG.12

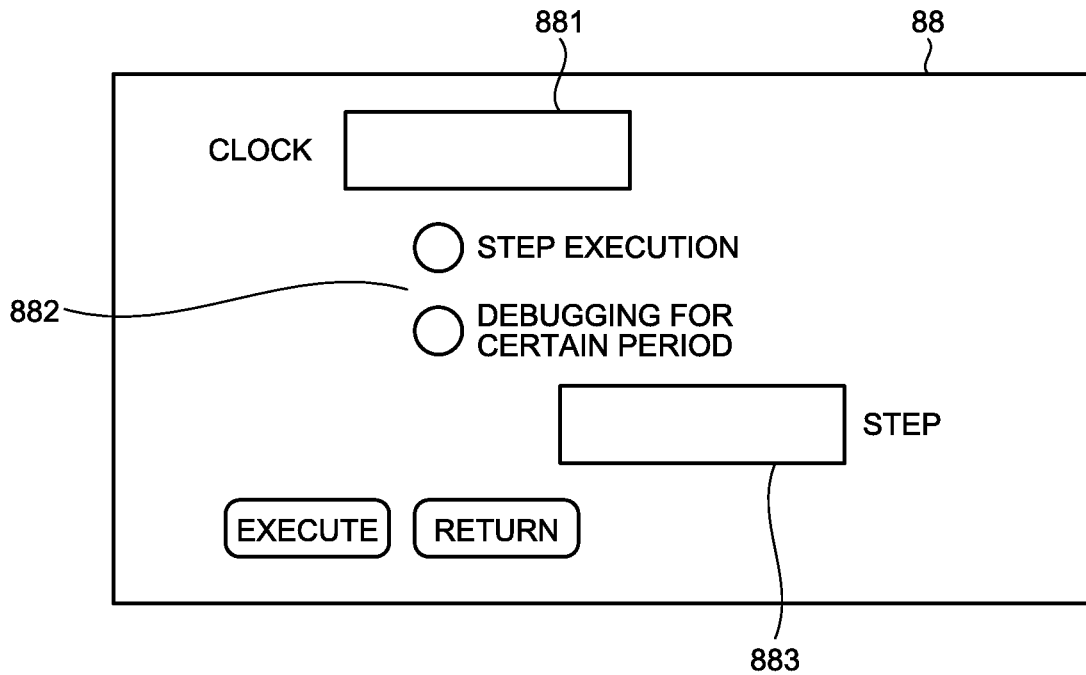


FIG.13

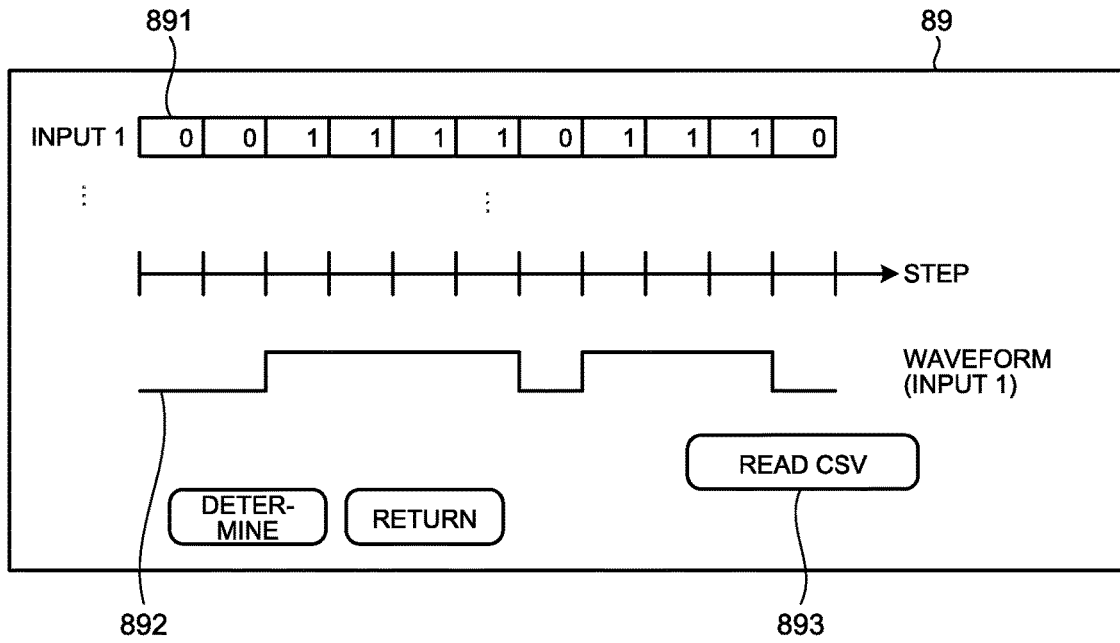


FIG.14

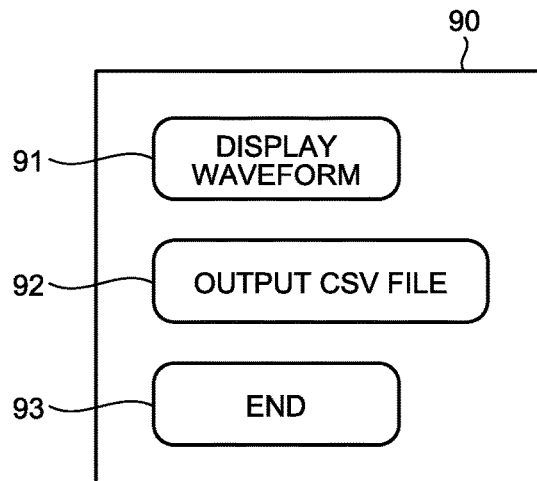


FIG.15

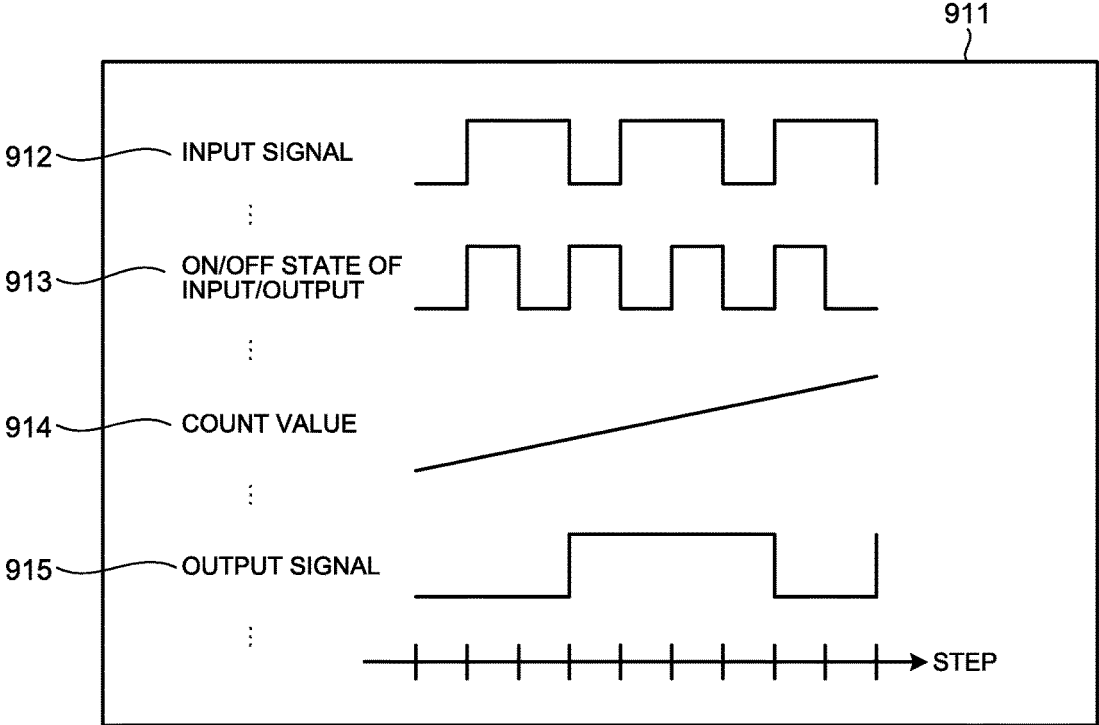


FIG.16

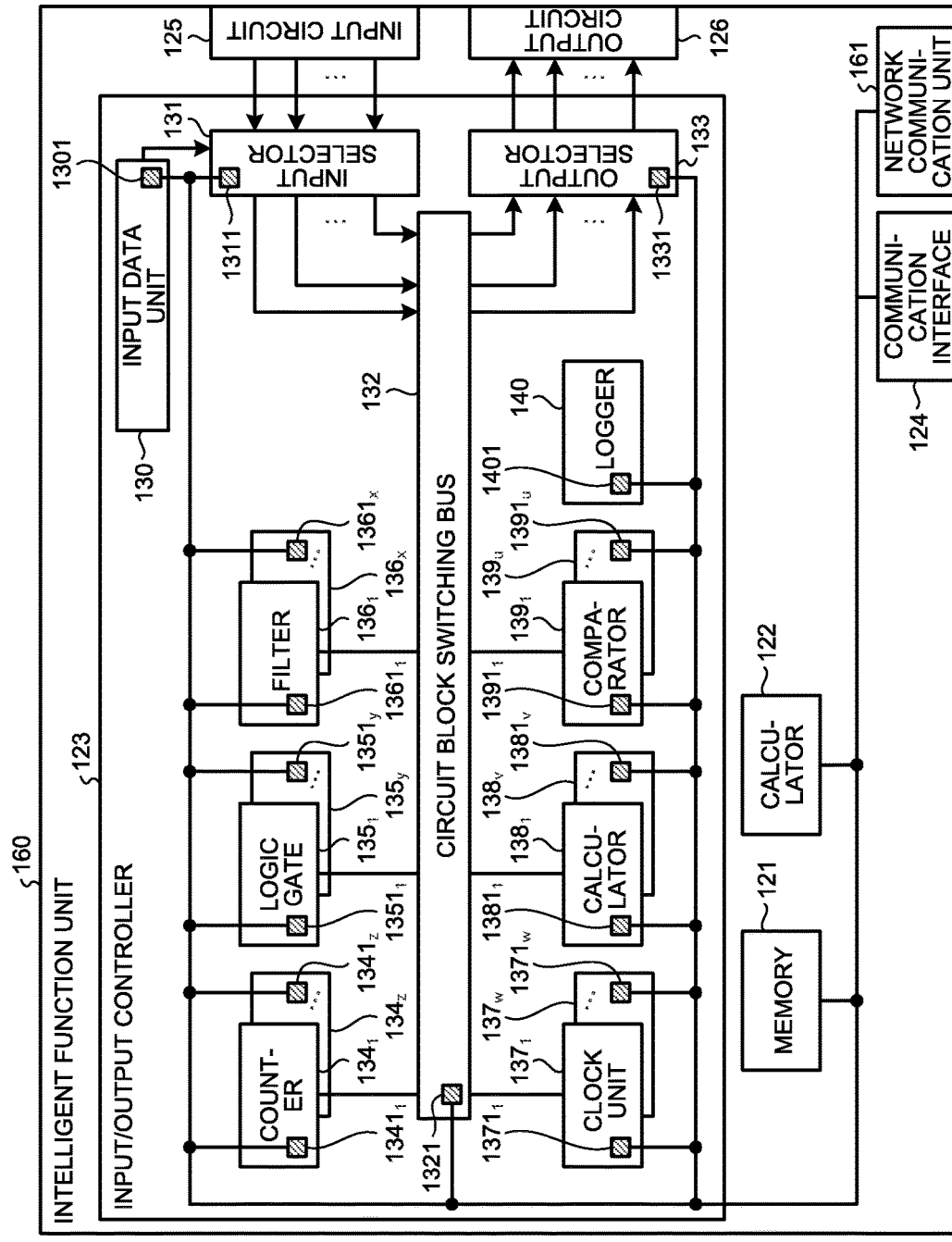


FIG.17

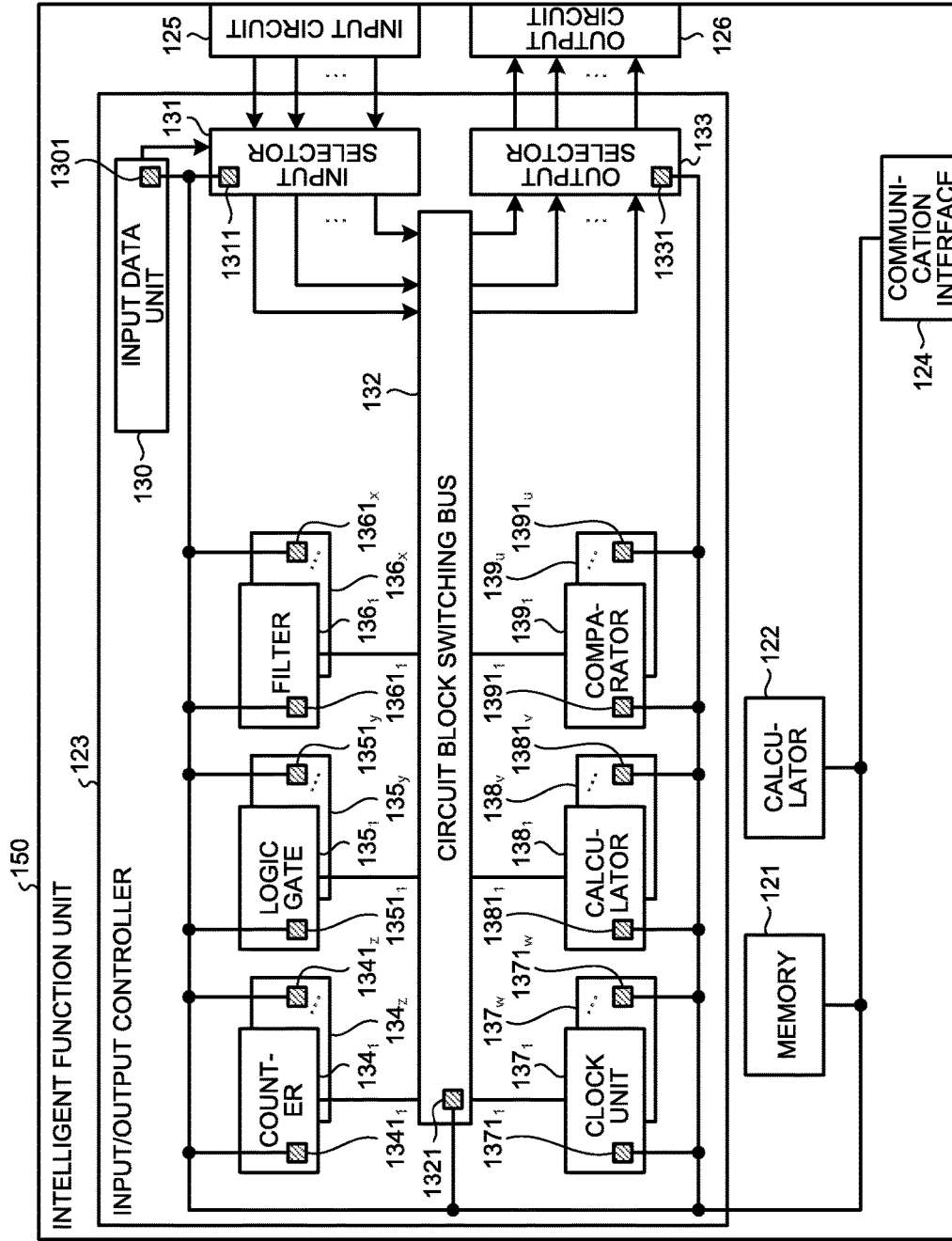


FIG.18

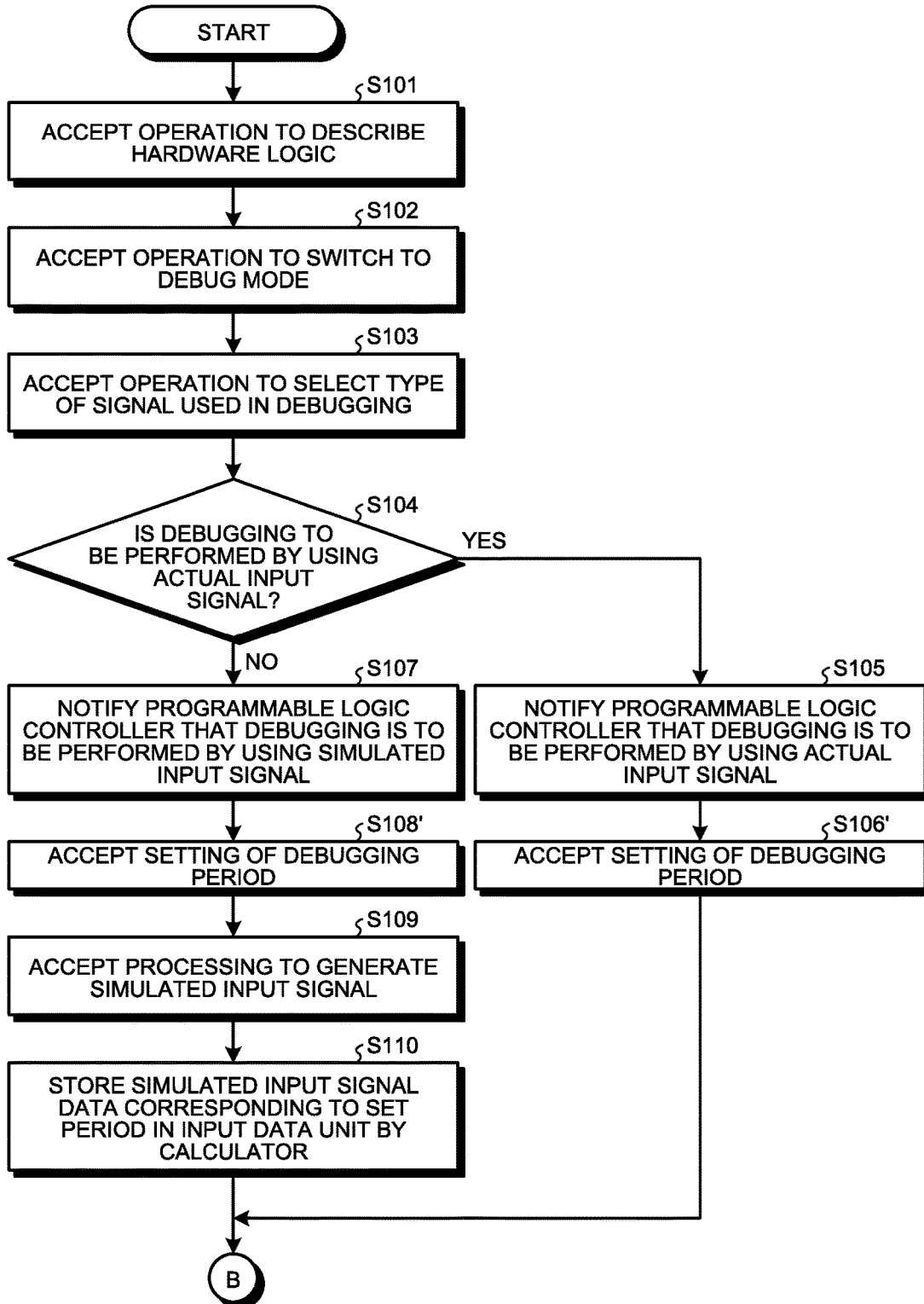
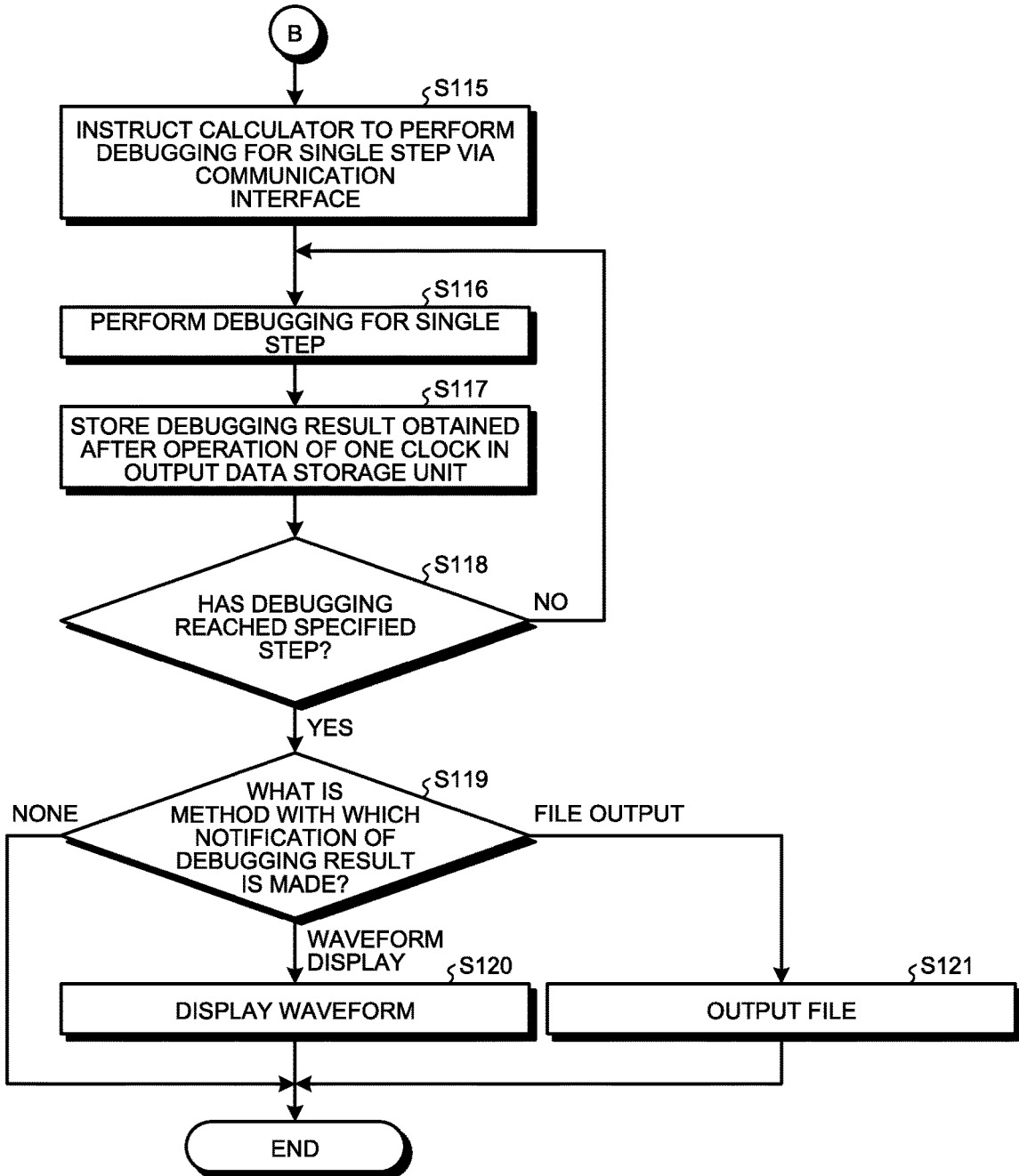


FIG.19



INTELLIGENT FUNCTION UNIT AND PROGRAMMABLE LOGIC CONTROLLER SYSTEM

FIELD

[0001] The present invention relates to an intelligent function unit that implements functions by combining general circuit blocks and to a programmable logic controller system that includes the intelligent function unit.

BACKGROUND

[0002] An intelligent function unit that is a type of unit included in a programmable logic controller combines general circuit blocks such as a clock, a counter, a comparator, a selector, and a logic gate to implement various functions required for input/output control such as a pulse count, a frequency measurement, a timer, and pulse width modulation output.

[0003] The intelligent function unit requires a debug function to verify whether the functions implemented by the combination of the general circuit blocks have an error.

[0004] Patent Literature 1 discloses a technique of comparing, in a reconfigurable circuit, a signal pattern regarded as a simulated user signal with sequentially output snapshots of logic elements to monitor the internal state of the logic elements.

[0005] Patent Literature 2 discloses a technique of changing the system clock and the address of a shift register in the reconfigurable logic cell array to acquire output of a given logic cell at a given point in time.

CITATION LIST

Patent Literature

[0006] Patent Literature 1: Japanese Patent Application Laid-Open No. 2002-544576

[0007] Patent Literature 2: Japanese Patent Application Laid-Open No. H8-95818

SUMMARY

Technical Problem

[0008] The invention disclosed in Patent Literature 1 is configured such that every logic element equivalent to the general circuit block is accompanied with a register, a memory, a network circuit, and a trigger circuit, and this thus increases the circuit scale. Moreover, the literature does not disclose displaying the debugging result of a product equipped with the reconfigurable circuit.

[0009] The invention disclosed in Patent Literature 2 requires a test circuit and a control input terminal in the logic cell equivalent to the general circuit block, and this thus increases the circuit scale. Moreover, the literature does not disclose displaying the debugging result of a product equipped with the reconfigurable circuit.

[0010] The present invention has been made in view of the above and an object of the invention is to obtain an intelligent function unit that can display the debugging result of a reconfigurable circuit while preventing an increase in the circuit scale.

Solution to Problem

[0011] In order to solve the above problems and achieve the object, an aspect of the present invention is an intelligent function unit that includes an input/output controller reconfigurable by changing a combination and an order of use of a plurality of general circuit blocks and that causes the input/output controller to process an actual input signal input from a first controlled device and outputs an output signal to a second controlled device. The intelligent function unit includes: an input selector to select, as an input signal, either the actual input signal or a simulated input signal generated in advance; an output selector to select whether to output the output signal to the second controlled device; and a calculator to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal one step at a time and transmit the output signal to an external device or to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal consecutively for a set period of two or more steps, store the output signal for each step in a logger, and transmit an output signal corresponding to the set period and stored in the logger to the external device.

Advantageous Effects of Invention

[0012] According to the intelligent function unit according to the present invention, an effect is obtained in that the debugging result of the reconfigurable circuit can be displayed while the circuit scale is prevented from increasing.

BRIEF DESCRIPTION OF DRAWINGS

[0013] FIG. 1 is a diagram illustrating the configuration of a programmable logic controller system according to a first embodiment of the present invention.

[0014] FIG. 2 is a diagram illustrating the configuration of an engineering tool in the programmable logic controller system according to the first embodiment.

[0015] FIG. 3 is a diagram illustrating a hardware configuration of a computer that runs an engineering tool program in the programmable logic controller system according to the first embodiment.

[0016] FIG. 4 is a diagram illustrating the computer with the engineering tool program running therein in the programmable logic controller system according to the first embodiment.

[0017] FIG. 5 is a diagram illustrating the configuration of a programmable logic controller in the programmable logic controller system according to the first embodiment.

[0018] FIG. 6 is a flowchart illustrating the flow of a debug operation of the programmable logic controller system according to the first embodiment.

[0019] FIG. 7 is a flowchart illustrating the flow of the debug operation of the programmable logic controller system according to the first embodiment.

[0020] FIG. 8 is a diagram illustrating an example of an engineering tool screen that is displayed on a display by a display unit of the engineering tool in the programmable logic controller system, according to the first embodiment.

[0021] FIG. 9 is a diagram illustrating an example of the engineering tool screen displaying a pull-down menu that includes a menu item to switch from a normal mode to a debug mode, according to the programmable logic controller system of the first embodiment.

[0022] FIG. 10 is a diagram illustrating an example of the engineering tool screen displaying a pull-down menu that includes a menu item to switch from a debug mode to a normal mode, according to the programmable logic controller system of the first embodiment.

[0023] FIG. 11 is a diagram illustrating an example of a selection dialog used to select whether to perform debugging by using an actual input signal or by using a simulated input signal, according to the programmable logic controller system of the first embodiment.

[0024] FIG. 12 is a diagram illustrating an example of a period setting dialog in the programmable logic controller system according to the first embodiment.

[0025] FIG. 13 is a diagram illustrating an example of a simulated input signal setting dialog according to the programmable logic controller system of the first embodiment.

[0026] FIG. 14 is a diagram illustrating an example of an inquiry screen asking about a method with which notification of a debugging result is made, according to the programmable logic controller system of the first embodiment.

[0027] FIG. 15 is a diagram illustrating an example of a debugging result display screen according to the programmable logic controller system of the first embodiment.

[0028] FIG. 16 is a diagram illustrating a modification of the intelligent unit in the programmable logic controller system according to the first embodiment.

[0029] FIG. 17 is a diagram illustrating the configuration of an intelligent function unit according to a second embodiment of the present invention.

[0030] FIG. 18 is a flowchart illustrating the flow of a debug operation of a programmable logic controller system that includes a programmable logic controller equipped with the intelligent function unit, according to the second embodiment.

[0031] FIG. 19 is a flowchart illustrating the flow of the debug operation of the programmable logic controller system that includes the programmable logic controller equipped with the intelligent function unit, according to the second embodiment.

DESCRIPTION OF EMBODIMENTS

[0032] An intelligent function unit and a programmable logic controller system according to embodiments of the present invention will now be described in detail with reference to the drawings. Note that the present invention is not to be limited to the embodiments.

First Embodiment

[0033] FIG. 1 is a diagram illustrating the configuration of a programmable logic controller system according to a first embodiment of the present invention. A programmable logic controller system 40 includes a programmable logic controller 10, which controls a first controlled device 20a and a second controlled device 20b; the first and second controlled devices 20a and 20b, which are controlled by the programmable logic controller 10; and an engineering tool 30, which performs setting of the programmable logic controller 10.

[0034] FIG. 2 is a diagram illustrating the configuration of the engineering tool in the programmable logic controller system according to the first embodiment. The engineering tool 30 includes a debug function unit 31, which debugs the programmable logic controller 10. The debug function unit 31 includes an input data generation unit 32, which gener-

ates a simulated input signal as a substitute for an actual signal; an output data storage unit 33, which stores data received from the programmable logic controller 10; a debugging period instruction unit 34, which instructs the programmable logic controller 10 about a debugging period; a display unit 35, which displays a debug screen on a display (to be described later); and a control unit 36, which has overall control of a debug operation.

[0035] The engineering tool 30 is implemented when a computer runs an engineering tool program. FIG. 3 is a diagram illustrating a hardware configuration of the computer that runs the engineering tool program in the programmable logic controller system according to the first embodiment. A computer 50 includes a calculator 51, which performs calculation processing; a memory 52, which is used as a work area by the calculator 51; a storage 53, which stores an engineering tool program 60 and information; an input unit 54, which is an input interface; a display 55, which displays information; and a communication unit 56, which is used to communicate with the programmable logic controller 10.

[0036] FIG. 4 is a diagram illustrating the computer with the engineering tool program running therein in the programmable logic controller system according to the first embodiment. The engineering tool 30 is implemented by the calculator 51 of the computer 50 executing the engineering tool program 60 while using the memory 52 as the work area. In other words, the input data generation unit 32, the output data storage unit 33, the debugging period instruction unit 34, the display unit 35, and the control unit 36 illustrated in FIG. 2 are implemented when the calculator 51 executes the engineering tool program 60. The above functions may also be implemented by a plurality of calculators and a plurality of memories cooperating with each other.

[0037] FIG. 5 is a diagram illustrating the configuration of the programmable logic controller in the programmable logic controller system according to the first embodiment. The programmable logic controller 10 includes a central processing unit (CPU) 100, which is an operation processing unit (operation processor) that executes a ladder program in accordance with the preset parameter; an intelligent function unit 110, which changes the operation in accordance with the parameter and the ladder program to control the first controlled device 20a and the second controlled device 20b; and a communication bus 120, which connects the CPU unit and the intelligent function unit.

[0038] The CPU unit 100 includes a memory 111, which stores a parameter 111a and a ladder program 111b; a calculator 112, which executes the ladder program 111b stored in the memory 111; a communication interface 113, which is used to communicate with the engineering tool 30; and a communication interface 114, which is used in communication via the communication bus 120.

[0039] The intelligent function unit 110 includes a memory 121, which stores information indicating in which order a plurality of general circuit blocks (to be described) are operated; a calculator 122, which causes an input/output controller (input/output control unit) 123 to perform a debug operation; the input/output controller 123, which is a reconfigurable circuit that includes the general circuit blocks; a communication interface 124, which is used in communication via the communication bus 120; an input circuit 125, which receives an actual input signal from the first controlled device 20a; and an output circuit 126, which outputs

an output signal to the second controlled device **20b**. In the first embodiment, the first controlled device **20a** is a sensor and the second controlled device **20b** is a switch. Note that the first controlled device **20a** and the second controlled device **20b** may be the same device.

[0040] The input/output controller **123** includes an input data unit **130**, which stores a simulated input signal used in debugging; an input selector **131**, which enables or disables the input circuit **125** during the debug operation to select either the actual input signal or the simulated input signal as the input signal; a circuit block switching bus **132**, which can modify the combination and the order of use of the general circuit blocks; and an output selector **133**, which selects whether to transmit an output signal that is a debugging result to the second controlled device **20b**. The output selector **133** disables the output circuit **126** during the debug operation so that the debugging result is not output to the second controlled device **20b**.

[0041] The general circuit blocks included in the input/output controller **123** are a plurality of counters **134₁** to **134_z**, which count numerical values; a plurality of logic gates **135₁** to **135_y**, which perform basic logic operations; a plurality of filters **136₁** to **136_x**, which remove noise from the input signal; a plurality of clock units **137₁** to **137_w**, which supply a clock to the general circuit blocks in the input/output controller **123** to operate the general circuit blocks; a plurality of calculators **138₁** to **138_v**, which perform preset calculation processing; and a plurality of comparators **139₁** to **139_u**, which perform comparison processing. The input/output controller **123** includes a logger **140**, which stores the output signal that is the debugging result for each step. Note that the basic logic operations include logical NOT, AND, OR, XOR, NOR, and NAND operations.

[0042] The input data unit **130** includes a register **1301**, which stores setting. The input selector **131** includes a register **1311**, which stores setting. The circuit block switching bus **132** includes a register **1321**, which stores setting. The output selector **133** includes a register **1331**, which stores setting. The counters **134₁** to **134_z** respectively include registers **1341₁** to **1341_z**, which store setting. The logic gates **135₁** to **135_y** respectively include registers **1351₁** to **1351_y**, which store setting. The filters **136₁** to **136_x** respectively include registers **1361₁** to **1361_x**, which store setting. The clock units **137₁** to **137_w** respectively include registers **1371₁** to **1371_w**, which store setting. The calculators **138₁** to **138_v** respectively include registers **1381₁** to **1381_v**, which store setting. The comparators **139₁** to **139_u** respectively include registers **1391₁** to **1391_u**, which store setting. The logger **140** includes a register **1401**, which stores setting.

[0043] The calculator **122** causes the input/output controller **123** to process an input signal for each step and transmits an output device to the engineering tool **30**. Alternatively, the calculator **122** causes the input/output controller **123** to process the input signal consecutively for a set period corresponding to two or more steps, stores a main signal for each step in the logger **140**, and transmits the output signal corresponding to the set period and stored in the logger **140** to the engineering tool **30**. In the debug operation, the calculator **122** transmits an instruction to the clock units **137₁** to **137_w**, which output a divided clock to the general circuit blocks.

[0044] The intelligent function unit **110** includes the input/output controller **123**, which is reconfigurable by modifying the combination and the order of use of the general circuit

blocks, and the intelligent function unit **110** causes the general circuit blocks to process an input signal and outputs an output signal that is the debugging result.

[0045] In the normal mode not involving debugging, the calculator **112** executes the ladder program **111b** on the basis of the parameter **111a** stored in the memory **111**, and sends an instruction to the calculator **122** via the communication bus **120**. According to the instruction from the calculator **112**, the calculator **122** determines the combination and the order of use of the general circuit blocks to store the setting in the registers **1301**, **1311**, **1321**, **1331**, **1341₁** to **1341_z**, **1351₁** to **1351_y**, **1361₁** to **1361_x**, **1371₁** to **1371_w**, **1381₁** to **1381_v**, and **1391₁** to **1391_u**. The register **1311** of the input selector **131** stores the setting that enables the input circuit **125**. The register **1331** of the output selector **133** stores the setting that enables the output circuit **126**. An actual input signal input from the first controlled device **20a** is then processed by the input/output controller **123**, and an output signal is output from the output circuit **126** to the second controlled device **20b**.

[0046] An operation performed during the debug operation by the engineering tool of the programmable logic controller system according to the first embodiment will be described. FIGS. **6** and **7** are flowcharts illustrating the flow of the debug operation of the programmable logic controller system according to the first embodiment. FIG. **8** is a diagram illustrating an example of an engineering tool screen that is displayed on the display by the display unit of the engineering tool in the programmable logic controller system according to the first embodiment. An engineering tool screen **80** includes a menu bar **81**, which displays a menu; a work window **82**, which displays a hardware logic **84** to be debugged, and a component selection window **83**, which displays components that make up the hardware logic **84**. Specific examples of the components that make up the hardware logic **84** include a parallel encoder block, a multifunction counter block, a logic operation block, and a function block.

[0047] In step **S101**, the control unit **36** of the engineering tool **30** accepts an operation to describe the hardware logic **84** in the work window **82** of the engineering tool screen **80**. The description of the hardware logic **84** is performed by the user selecting a component in the component selection window **83** and placing the component in the work window **82** with the input unit **54**.

[0048] In step **S102**, the control unit **36** accepts an operation to switch to the debug mode. When the user operates the input unit **54** to select "debug" from the menu bar **81** in the engineering tool screen **80**, the display unit **35** displays, in the engineering tool screen **80**, a pull-down menu used to perform switching between the normal mode and the debug mode. In the normal mode, the display unit **35** displays, in the engineering tool screen **80**, a pull-down menu that includes a menu item to shift to the debug mode. FIG. **9** is a diagram illustrating an example of the engineering tool screen displaying the pull-down menu that includes the menu item to switch from the normal mode to the debug mode, according to the programmable logic controller system of the first embodiment. The control unit **36** accepts an operation to select a mode switching menu item **851** in a pull-down menu **85**.

[0049] Note that in the debug mode, the display unit **35** displays, in the engineering tool screen **80**, a pull-down menu that includes a menu item to shift to the normal mode.

FIG. 10 is a diagram illustrating an example of the engineering tool screen displaying the pull-down menu that includes the menu item to switch from the debug mode to the normal mode, according to the programmable logic controller system of the first embodiment. A pull-down menu 86 displayed in the engineering tool screen 80 includes a menu item 861 to shift from the debug mode to the normal mode.

[0050] When the user operates the input unit 54 and selects the menu item to shift to the debug mode, the control unit 36 in step S103 accepts an operation to select the type of a signal used in debugging. Specifically, the display unit 35 displays, in the engineering tool screen 80, a selection dialog used to select whether to perform debugging by using the actual input signal or by using the simulated input signal.

FIG. 11 is a diagram illustrating an example of the selection dialog used to select whether to perform debugging by using the actual input signal or by using the simulated input signal, according to the programmable logic controller system of the first embodiment. A selection dialog 87 includes an actual input signal selection button 871 and a simulated input signal selection button 872. When the user presses the actual input signal selection button 871, the control unit 36 determines that the user makes a selection to perform debugging by using the actual input signal. When the user presses the simulated input signal selection button 872, the control unit 36 determines that the user makes a selection to perform debugging by using the simulated input signal.

[0051] When the user operates the input unit 54 to select debugging using the actual input signal, Yes is determined in step S104. In step S105, the control unit 36 notifies the programmable logic controller 10 that the hardware logic 84 described in the work window 82 is to be debugged by using the actual input signal. The calculator 122 of the intelligent function unit 110 then refers to information stored in the memory 121, determines the combination and the order of use of the general circuit blocks used to process the hardware logic 84, and stores the setting in the registers 1301, 1311, 1321, 1331, 1341₁ to 1341_z, 1351₁ to 1351_y, 1361₁ to 1361_x, 1371₁ to 1371_w, 1381₁ to 1381_v, and 1391₁ to 1391_u. The register 1311 of the input selector 131 stores the setting that enables the input circuit 125. The register 1331 of the output selector 133 stores the setting that disables the output circuit 126.

[0052] In step S106, the debugging period instruction unit 34 accepts setting of the debugging period. Specifically, the debugging period instruction unit 34 displays, on the engineering tool screen 80, a period setting dialog used to specify a clock at which debugging starts, select whether to perform debugging one step at a time or for a certain period, and set the debugging period. FIG. 12 is a diagram illustrating an example of the period setting dialog in the programmable logic controller system according to the first embodiment. A period setting dialog 88 includes a starting step specification field 881, which specifies a step at which debugging starts; an operation type specification section 882, in which the user selects whether to perform debugging one step at a time or consecutively for a set period; and a period specification field 883, which specifies a period for which debugging is performed. The period setting dialog 88 is a graphical user interface of the debugging period instruction unit 34. The user can thus select whether to perform debugging one step at a time or consecutively for the set period in the graphical user interface environment. The operation type specification section 882 includes radio but-

tons that allow the user to select only one of the buttons corresponding to debugging performed one step at a time and debugging performed consecutively for the set period. The debugging period instruction unit 34 accepts an input operation performed on the period setting dialog 88.

[0053] When the user operates the input unit 54 to select debugging using the simulated input signal, No is determined in step S104. In step S107, the control unit 36 notifies the programmable logic controller 10 that the hardware logic 84 described in the work window 82 is to be debugged by using the simulated input signal. The calculator 122 of the intelligent function unit 110 then refers to the information stored in the memory 121, determines the combination and the order of use of the general circuit blocks used to process the hardware logic 84, and stores the setting in the registers 1301, 1311, 1321, 1331, 1341₁ to 1341_z, 1351₁ to 1351_y, 1361₁ to 1361_x, 1371₁ to 1371_w, 1381₁ to 1381_v, and 1391₁ to 1391_u. The register 1311 of the input selector 131 stores the setting that disables a signal from the input circuit 125 and enables a signal from the input data unit 130. The register 1331 of the output selector 133 stores the setting that disables the output circuit 126.

[0054] In step S108, the debugging period instruction unit 34 accepts setting of the debugging period as with step S106. After step S108, the input data generation unit 32 accepts processing to generate the simulated input signal in step S109. Specifically, the input data generation unit 32 displays a simulated input signal setting dialog on the engineering tool screen 80. FIG. 13 is a diagram illustrating an example of the simulated input signal setting dialog according to the programmable logic controller system of the first embodiment. A simulated input signal setting dialog 89 includes a value input field 891, to which a value of 0 or 1 is input for each step, and a waveform display section 892, which displays a waveform obtained by converting the value input to the value input field 891. The simulated input signal is generated by specifying a low or high level with the value of 0 or 1 for each step in the value input field 891. The number of simulated input signals generated corresponds to the number of channels used in debugging. The simulated input signal setting dialog 89 is a graphical user interface of the input data generation unit 32. The user can thus generate the simulated input signals in the graphical user interface environment.

[0055] The simulated input signal setting dialog 89 includes a file read button 893. When the file read button 893 is pressed, a string of 0s and 1s in a file having a comma-separated text format is read from the storage 53, so that the value of 0 or 1 is input to the value input field 891 for each step.

[0056] The input data generation unit 32 converts the simulated input signal, the level of which is set to 0 or 1 for each step, into a waveform and displays the waveform in the waveform display section 892. Displaying the waveform of the simulated input signal in the waveform display section 892 allows the user to visually recognize an error in the specification of the level, i.e., high or low, of the simulated input signal for each step, thereby reducing an error in the setting of the simulated input signal.

[0057] Steps S108 and S109 may be executed in reverse order. That is, the setting of the debugging period may be accepted after the processing to generate the simulated input signal is accepted.

[0058] In step S110, the control unit 36 transmits data of the simulated input signals corresponding to the set period to the programmable logic controller 10. The calculator 122 of the intelligent function unit 110 stores the data of the simulated input signals in the input data unit 130.

[0059] After completion of the processing in step S106 or S110, the control unit 36 in step S111 checks whether the setting is such that debugging is to be performed consecutively for the set period or is such that debugging is to be performed one step at a time. When debugging is to be performed consecutively for the set period, No is determined in step S111. In this case, the control unit 36 proceeds to step S112 and instructs the calculator 122 to perform debugging for the set period via the communication interface. The register 1401 of the logger 140 stores setting that enables the logger 140.

[0060] In step S113, the calculator 122 performs debugging for the set period and stores the debugging result for each step in the logger 140. Specifically, the calculator 122 causes the clock units 137₁ to 137_w to supply clocks for the set period to the other general circuit blocks to operate the other general circuit blocks consecutively for the set period.

[0061] After completion of debugging for the set period, the calculator 122 in step S114 reads the data from the logger 140, transmits it to the engineering tool 30, and stores it in the output data storage unit 33.

[0062] When debugging is to be performed one step at a time, Yes is determined in step S111. In this case, the control unit 36 proceeds to step S115 and instructs the calculator 122 to perform debugging for a single step via the communication interface. The register 1401 of the logger 140 stores setting that disables the logger 140.

[0063] The calculator 122 thus causes the input/output controller 123 in which the combination and the order of use of the general circuit blocks are set to process the input signal one step at a time or consecutively for the set period of two or more steps.

[0064] In step S116, the calculator 122 performs debugging for a single step. Specifically, the calculator 122 supplies one clock from the clock units 137₁ to 137_w to the other general circuit blocks to operate the other general circuit blocks. In step S117, the calculator 122 transmits the debugging result to the engineering tool 30 via the communication interface and stores the result in the output data storage unit 33.

[0065] After step S117, the control unit 36 determines whether debugging has been performed up to the step set in step S106 or S108. That is, the calculator 122 determines whether debugging has reached the specified step. If debugging has been performed up to the step set in step S106 or S108, Yes is determined in step S118 and the processing proceeds to step S119. If debugging has not been performed up to the step set in step S106 or S108, No is determined in step S118 and the processing proceeds to step S115.

[0066] After step S114 or if Yes is determined in step S118, the control unit 36 inquires of the user about the method with which notification of the debugging result is made in step S119. Specifically, the display unit 35 displays, on the display 55, an inquiry screen asking whether the debugging result is displayed as a waveform or is output as a file in a comma-separated text format. FIG. 14 is a diagram illustrating an example of the inquiry screen asking about the method with which notification of the debugging result is made, according to the programmable logic controller

system of the first embodiment. An inquiry screen 90 asking about the method with which notification of the debugging result is made includes a waveform display selection button 91, a file output selection button 92, and an end button 93.

[0067] When the user operates the input unit 54 to press the waveform display selection button 91, “waveform display” is selected in step S119. In step S120, the display unit 35 displays the debugging result on the engineering tool screen 80. FIG. 15 is a diagram illustrating an example of a debugging result display screen according to the programmable logic controller system of the first embodiment. A debugging result display screen 911 displays a waveform 912 of the input signal corresponding to the specified number of steps, an on/off state 913 of the input/output of the input/output controller 123, a count value 914 of the input/output controller 123, and a waveform 915 of the output signal.

[0068] When the file output selection button 92 is pressed, “file output” is selected in step S119. In step S121, the control unit 36 stores the debugging result in the storage 53.

[0069] When the end button 93 is pressed, “none” is selected in step S119, thereby ending the debugging processing.

[0070] Note that the simulated input signal generated by operating the engineering tool 30 in the aforementioned description may instead be generated by operating the intelligent function unit 110 and stored in the input data unit 130.

[0071] Although the intelligent function unit 110 in the aforementioned description is connected to the engineering tool 30 via the CPU unit 100 and transmits the debugging result to the engineering tool 30 via the CPU unit 100, the intelligent function unit 110 may instead be connected to the engineering tool 30 via a network and transmit the debugging result to the engineering tool 30 via the network.

[0072] FIG. 16 is a diagram illustrating a modification of the intelligent unit in the programmable logic controller system according to the first embodiment. An intelligent function unit 160 is different from the intelligent function unit 110 in that the intelligent function unit 160 includes a network communication unit 161. The network communication unit 161 is a communication interface used to communicate with the engineering tool 30 via the network. The intelligent function unit 160 can use the network communication unit 161 to transmit the debugging result to the engineering tool 30 via the network.

[0073] Compared to the intelligent function unit 160 of the modification, the intelligent function unit 110 does not require the network communication unit 161; therefore, the intelligent function unit 110 prevents an increase in the circuit scale more effectively.

[0074] The intelligent function unit 110 of the programmable logic controller system 40 according to the first embodiment includes the input data unit 130; the input selector 131; the output selector 133; and the logger 140 as the components that are included in the input/output controller 123 and that are used for implementing the debug function, whereby a component need not be added to each general circuit block. This can prevent an increase in the circuit scale. Moreover, the calculator 122 transmits the debugging result to the engineering tool 30 when performing debugging one step at a time. When performing debugging consecutively for the set period, the calculator 122 stores the debugging result for each step in the logger 140. Then after

completing debugging for the set period, the calculator 122 transmits the debugging results corresponding to the set period and stored in the logger 140 to the engineering tool 30. The device result of the intelligent function unit 110 can thus be displayed in the debugging result display screen 911 of the engineering tool 30.

[0075] When debugging is performed consecutively for the set period, the control unit 36 of the programmable logic controller system 40 according to the first embodiment need not instruct the calculator 122 to perform debugging every time it is to be performed, whereby the load of the calculator 51 can be reduced.

[0076] In the debug operation, the calculator 122 gives an instruction to supply the divided clocks from the clock units 137₁ to 137_w to operate the other general circuit blocks, so that the general circuit blocks in the input/output controller 123 operating at a higher speed than the calculator 122 in the normal mode can be operated at the operating cycle of the calculator 122 to allow for debugging and checking of the debugging result.

[0077] The programmable logic controller system 40 according to the first embodiment implements the general circuit blocks as hardware in the input/output controller 123 and changes the operating mode of each of the general circuit blocks according to the register setting of the intelligent function unit 110. The general circuit blocks can be selectively combined as well. This allows the intelligent function unit 110 of the programmable logic controller 10 performing various input/output controls to implement the debug function to verify the operation of each general circuit block and the operation of the combination of the general circuit blocks.

Second Embodiment

[0078] FIG. 17 is a diagram illustrating the configuration of an intelligent function unit according to a second embodiment of the present invention. An intelligent function unit 150 according to the second embodiment does not include the logger 140 included in the intelligent function unit 110 of the first embodiment. Except for the absence of the logger 140, the intelligent function unit 150 is similar to the intelligent function unit 110 of the first embodiment.

[0079] FIGS. 18 and 19 are flowcharts illustrating the flow of a debug operation of a programmable logic controller system that includes a programmable logic controller equipped with the intelligent function unit, according to the second embodiment. The debug operation of the second embodiment differs from that of the programmable logic controller system 40 of the first embodiment in that steps S106 and S108 are changed to steps S106' and S108' and that steps S111 to S114 are not included. The rest is the same as the debug operation of the programmable logic controller system 40 according to the first embodiment.

[0080] In steps S106' and S108', a debugging period instruction unit 34 accepts setting of a debugging period. Specifically, the debugging period instruction unit 34 displays, on an engineering tool screen, a period setting dialog used to specify a clock at which debugging starts and set the debugging period. That is, the debug operation of the second embodiment differs from the debug operation of the programmable logic controller system 40 according to the first embodiment in that steps S106' and S108' do not involve selection of whether to perform debugging one step at a time or consecutively for a set period.

[0081] After that, the debug operation of the second embodiment does not perform processing corresponding to steps S111 to S114 in the debug operation of the programmable logic controller system 40 according to the first embodiment. The debug operation is thus performed one step at a time even though the selection of whether to perform debugging one step at a time or consecutively for the set period is not made in step S106' or S108'.

[0082] The intelligent function unit 150 according to the second embodiment is limited to debugging performed one step at a time but does not require the logger; therefore, the configuration can be simplified and the cost can be reduced.

[0083] Note that the second embodiment may also be provided with a network communication unit that is a communication interface used to communicate with the engineering tool 30 via a network, as with the modification of the first embodiment.

[0084] The configurations illustrated in the aforementioned embodiments merely illustrate examples of the content of the preset invention, and can thus be combined with another known technique or partially omitted and/or modified without departing from the gist of the present invention.

REFERENCE SIGNS LIST

[0085] 10 programmable logic controller, 20a first controlled device, 20b second controlled device, 30 engineering tool, 31 debug function unit, 32 input data generation unit, 33 output data storage unit, 34 debugging period instruction unit, 35 display unit, 36 control unit, 50 computer, 51 calculator, 52, 111, 121 memory, 53 storage, 54 input unit, 55 display, 56 communication unit, 60 engineering tool program, 80 engineering tool screen, 81 menu bar, 82 work window, 83 component selection window, 84 hardware logic, 85, 86 pull-down menu, 87 selection dialog, 88 period setting dialog, 89 simulated input signal setting dialog, 90 inquiry screen, 91 waveform display selection button, 92 file output selection button, 93 end button, 100 CPU unit, 110, 150, 160 intelligent function unit, 111a parameter, 111b ladder program, 112, 122 calculator, 113, 114, 124 communication interface, 120 communication bus, 123 input/output controller, 125 input circuit, 126 output circuit, 130 input data unit, 131 input selector, 132 circuit block switching bus, 133 output selector, 134₁, 134_w counter, 135₁, 135_y logic gate, 136₁, 136_x filter, 137₁, 137_w clock unit, 138₁, 138_v calculator, 139₁, 139_u comparator, 140 logger, 161 network communication unit, 851, 861 menu item, 871 actual input signal selection button, 872 simulated input signal selection button, 881 starting step specification field, 882 operation type specification section, 883 period specification field, 891 value input field, 892 waveform display section, 893 file read button, 911 debugging result display screen, 912 waveform of input signal, 913 on/off state, 914 count value, 915 waveform of output signal, 1301, 1311, 1321, 1331, 1341₁, 1341_v, 1351₁, 1351_v, 1361₁, 1361_x, 1371₁, 1371_w, 1381₁, 1381_v, 1391₁, 1391_u, 1401 register.

1. An intelligent function unit that includes an input/output controller reconfigurable by changing a combination and an order of use of a plurality of general circuit blocks and that causes the input/output controller to process an actual input signal input from a first controlled device and outputs an output signal to a second controlled device, the intelligent function unit comprising:

- an input selector to select, as an input signal, either the actual input signal or a simulated input signal generated in advance;
- an output selector to select whether to output the output signal to the second controlled device; and
- a calculator to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal one step at a time and transmit the output signal to an external device or to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal consecutively for a set period of two or more steps, store the output signal for each step in a logger, and transmit an output signal corresponding to the set period and stored in the logger to the external device.
2. An intelligent function unit that includes an input/output controller reconfigurable by changing a combination and an order of use of a plurality of general circuit blocks and that causes the input/output controller to process an actual input signal input from a first controlled device and outputs an output signal to a second controlled device, the intelligent function unit comprising:
- an input selector to select, as an input signal, either the actual input signal or a simulated input signal generated in advance;
- an output selector to select whether to output the output signal to the second controlled device; and
- a calculator to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal one step at a time and transmit the output signal to an external device.
3. The intelligent function unit according to claim 1, wherein the intelligent function unit is connected to the external device via an operation processor and transmits the output signal to the external device via the operation processor.
4. The intelligent function unit according to claim 1, wherein the intelligent function unit is connected to the external device via a network and transmits the output signal to the external device via the network.
5. A programmable logic controller system that includes:
- a programmable logic controller that includes an intelligent function unit that includes an input/output controller reconfigurable by changing a combination and an order of use of a plurality of general circuit blocks and that causes the input/output controller to process an actual input signal input from a first controlled device and outputs an output signal to a second controlled device; and
- an engineering tool equipped with a debug function of the programmable logic controller, wherein

the intelligent function unit includes:

- an input selector to select, as an input signal, either the actual input signal or a simulated input signal generated in advance;
- an output selector to select whether to output the output signal to the second controlled device; and
- a calculator to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal one step at a time and transmit the output signal to the engineering tool or to cause the input/output controller in which the combination and the order of use of the general circuit blocks are set to process the input signal consecutively for a set period of two or more steps, store the output signal for each step in a logger, and transmit an output signal corresponding to the set period and stored in the logger to the engineering tool, and
- the engineering tool includes:
- a processor to execute a program; and
- a memory to store the program which, when executed by the processor, performs
- an input data generation process of generating the simulated input signal and transmitting the simulated input signal to the intelligent function unit;
- a debugging period instruction process of instructing the calculator to cause the input/output controller to process the input signal one step at a time or consecutively for the set period;
- an output data storing process of storing the output signal received from the intelligent function unit; and
- a displaying process of displaying a waveform of the output signal stored in the output data storing process.
6. The programmable logic controller system according to claim 5, wherein
- the input data generation process includes generating the simulated input signal by using a graphical user interface, and
- the debugging period instruction process includes instructing the calculator to cause the general circuit blocks to process the input signal one step at a time or consecutively for the set period by using a graphical user interface.
7. The intelligent function unit according to claim 2, wherein the intelligent function unit is connected to the external device via an operation processor and transmits the output signal to the external device via the operation processor.
8. The intelligent function unit according to claim 2, wherein the intelligent function unit is connected to the external device via a network and transmits the output signal to the external device via the network.

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