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(54) SUBSTRATE PROCESSING APPARATUS, SIGNAL SOURCE DEVICE, METHOD OF PROCESSING MATERIAL LAYER, AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE

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(52) **U.S. Cl.**

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(57) **ABSTRACT**

A substrate processing apparatus includes a processing chamber; a susceptor provided in the processing chamber, wherein the susceptor is configured to support a substrate; a first plasma generator disposed on one side of the processing chamber; and a second plasma generator disposed on another side of the processing chamber, wherein the second plasma generator is configured to generate plasma by simultaneously supplying a sinusoidal wave signal and a non-sinusoidal wave signal to the susceptor. By using a substrate processing apparatus, a signal source device, and a method of processing a material layer according to the inventive concept, a smooth etched surface may be obtained for a crystalline material layer without a risk of device damage by RDC.

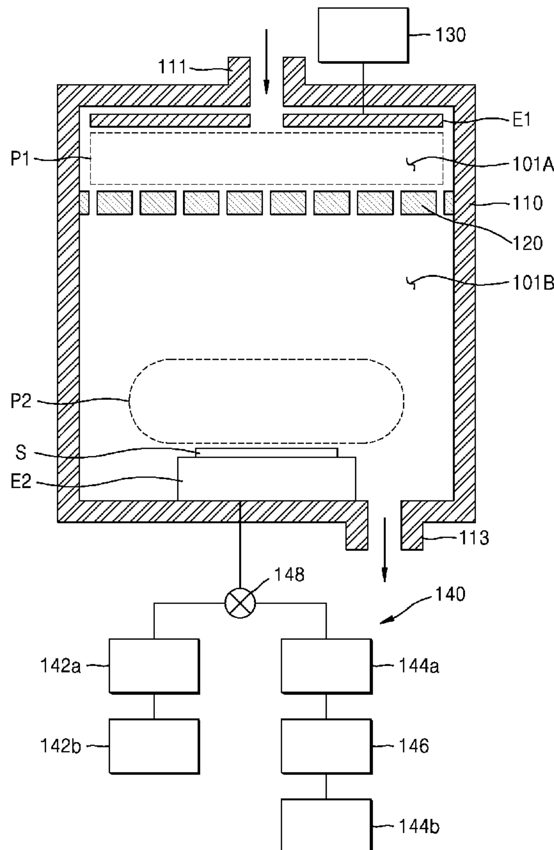


FIG. 1A

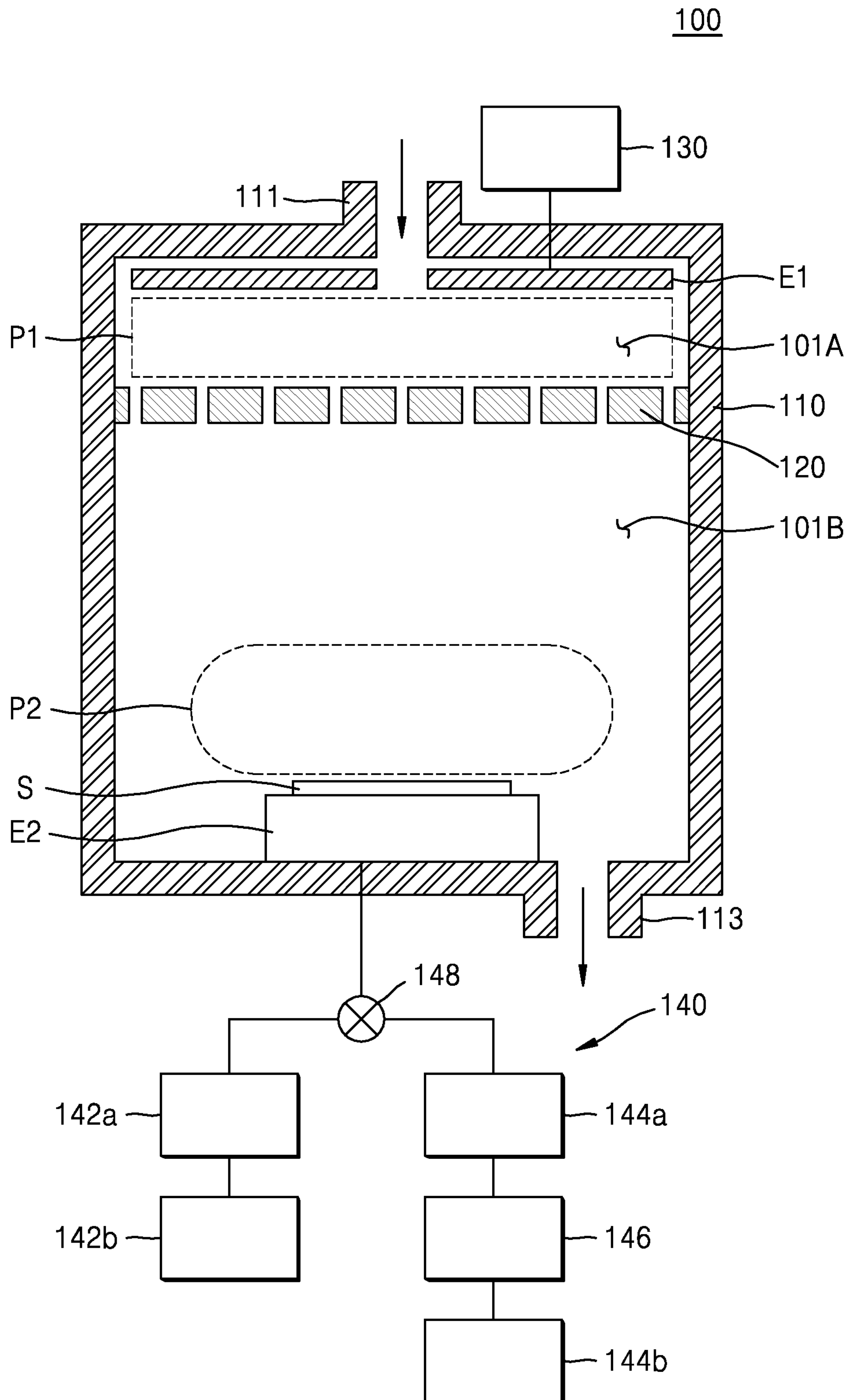


FIG. 1B

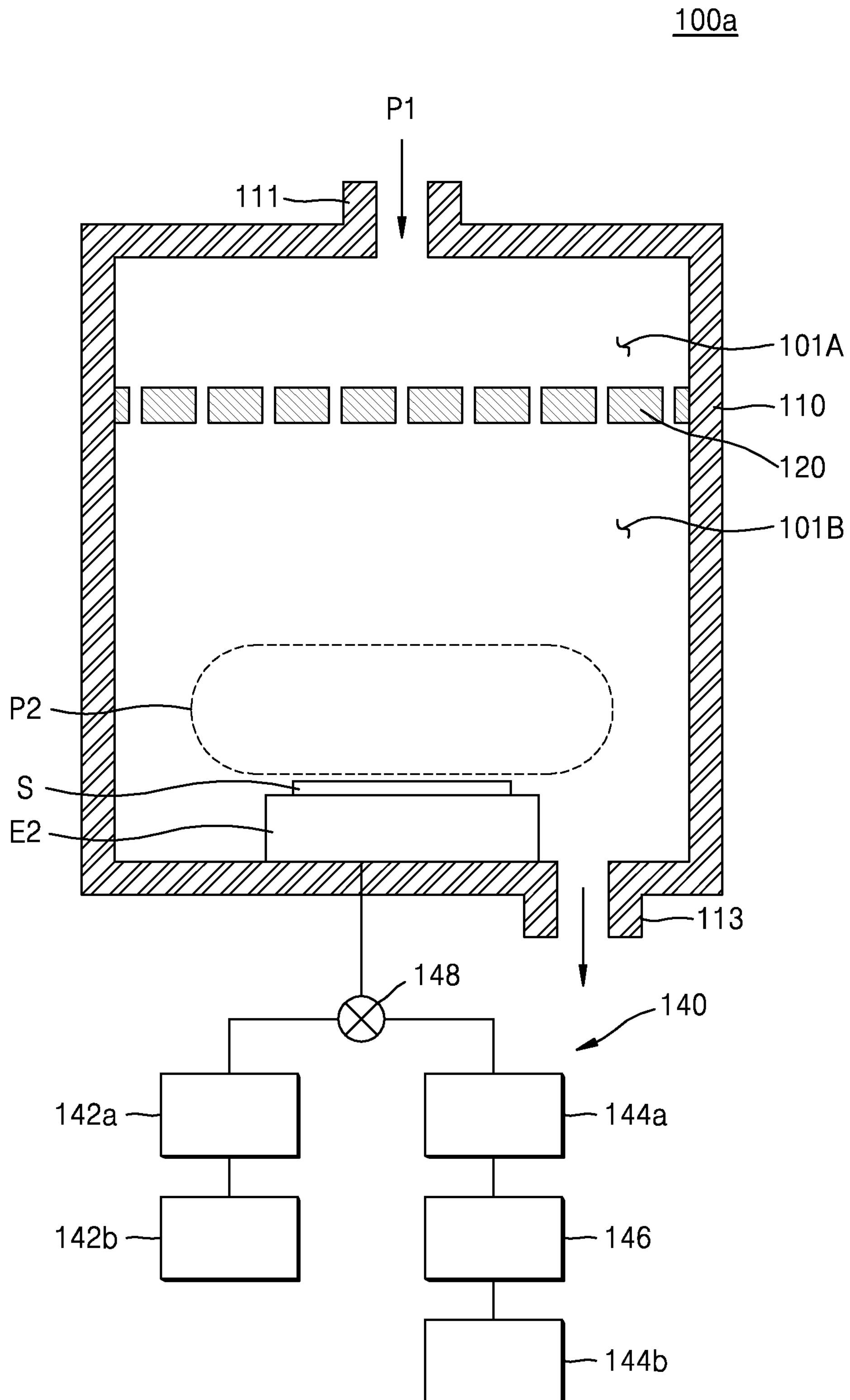


FIG. 2A

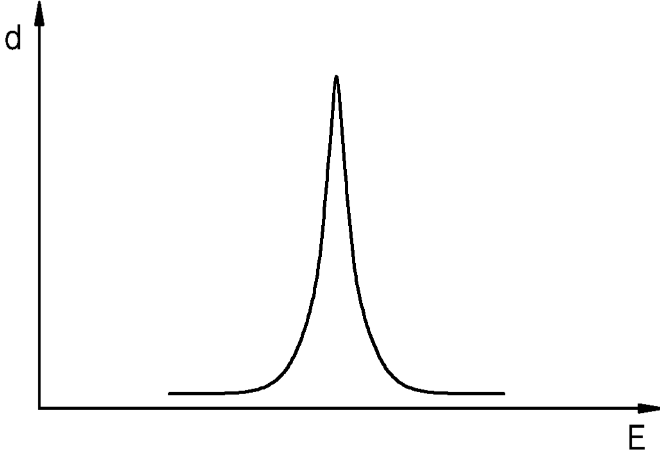


FIG. 2B

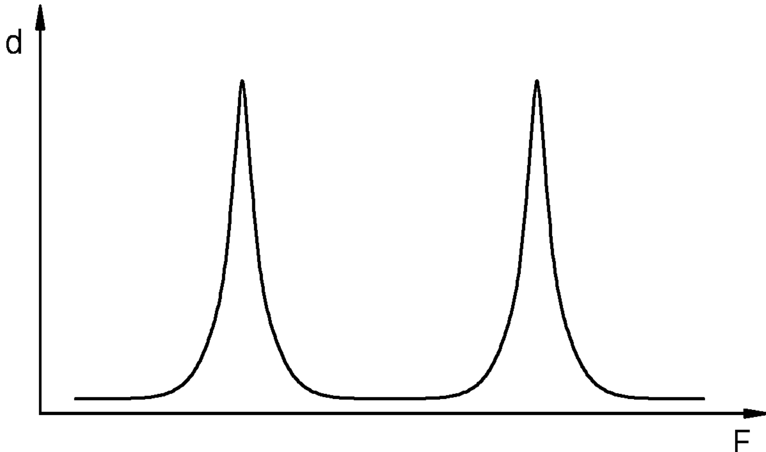


FIG. 3

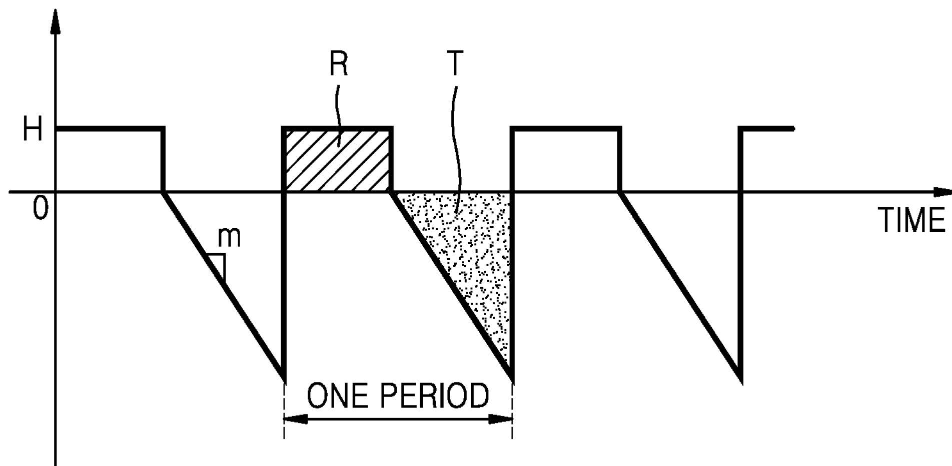


FIG. 4

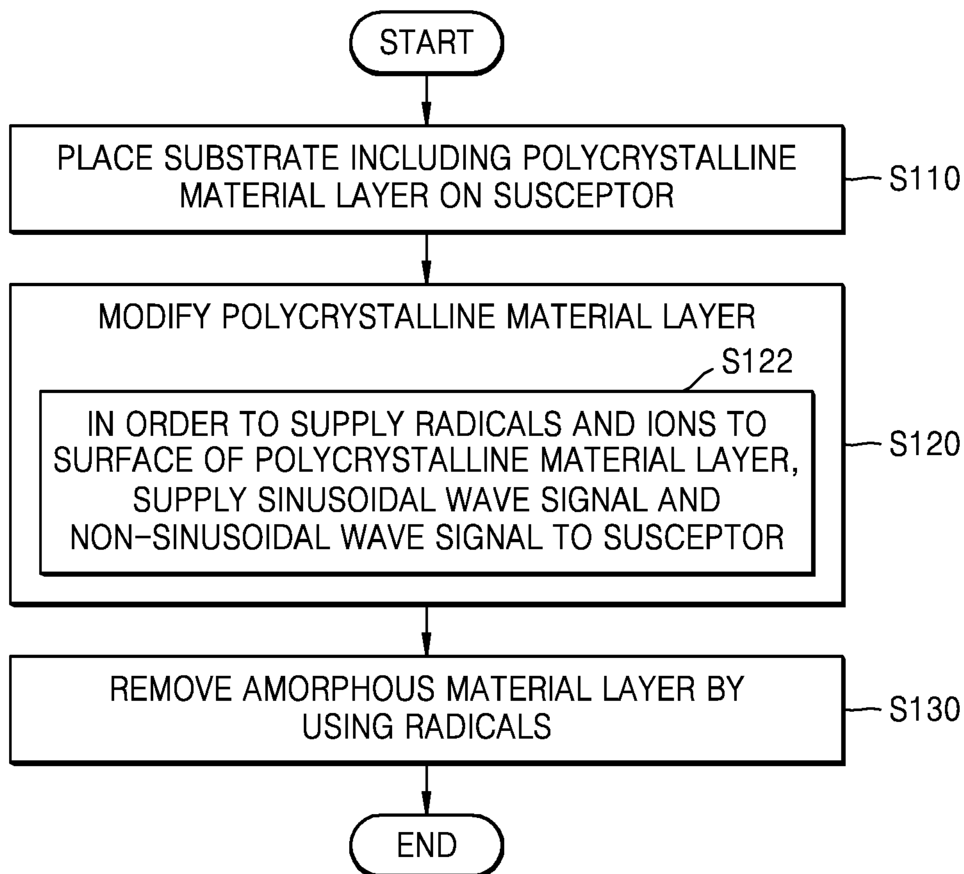


FIG. 5A

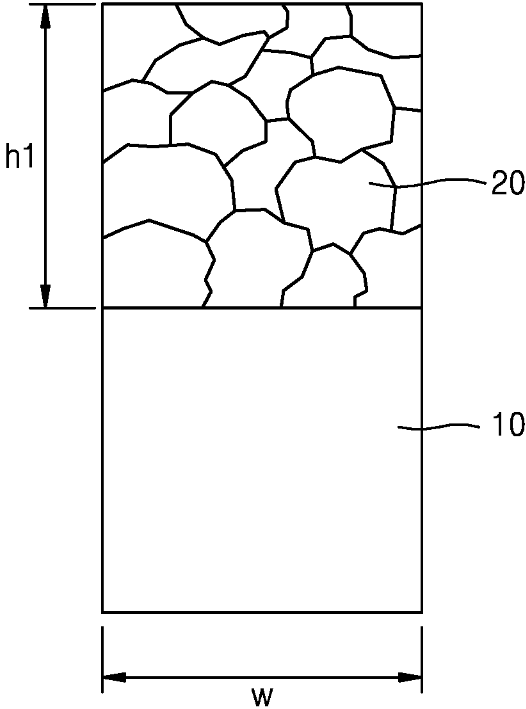


FIG. 5B

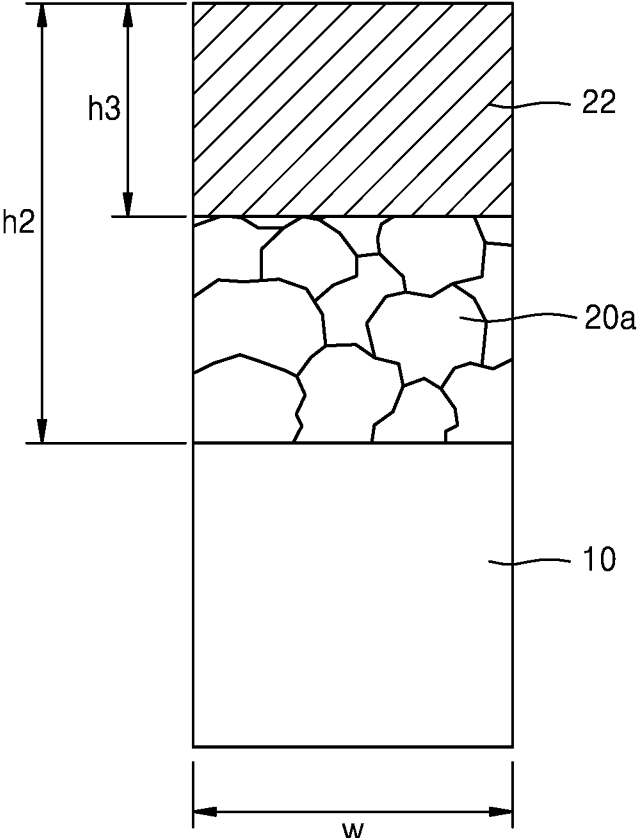


FIG. 5C

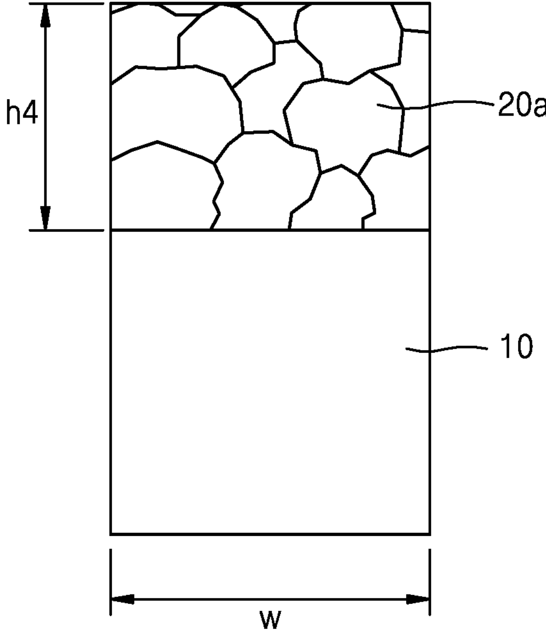


FIG. 6

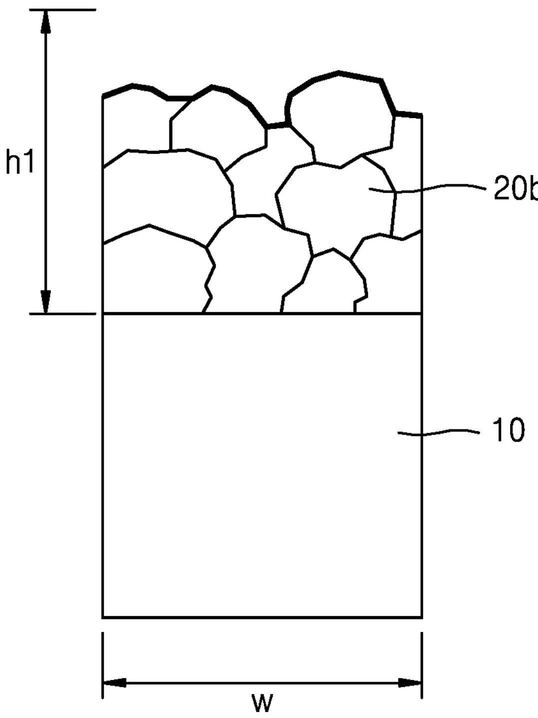


FIG. 7

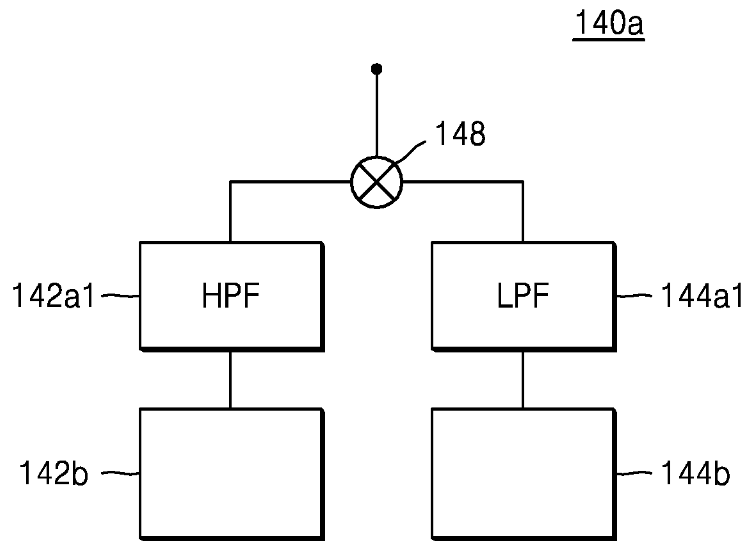


FIG. 8

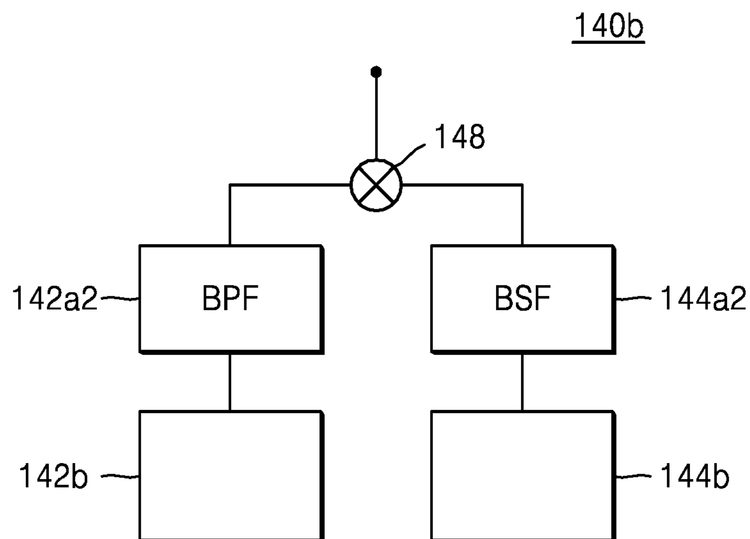


FIG. 9A

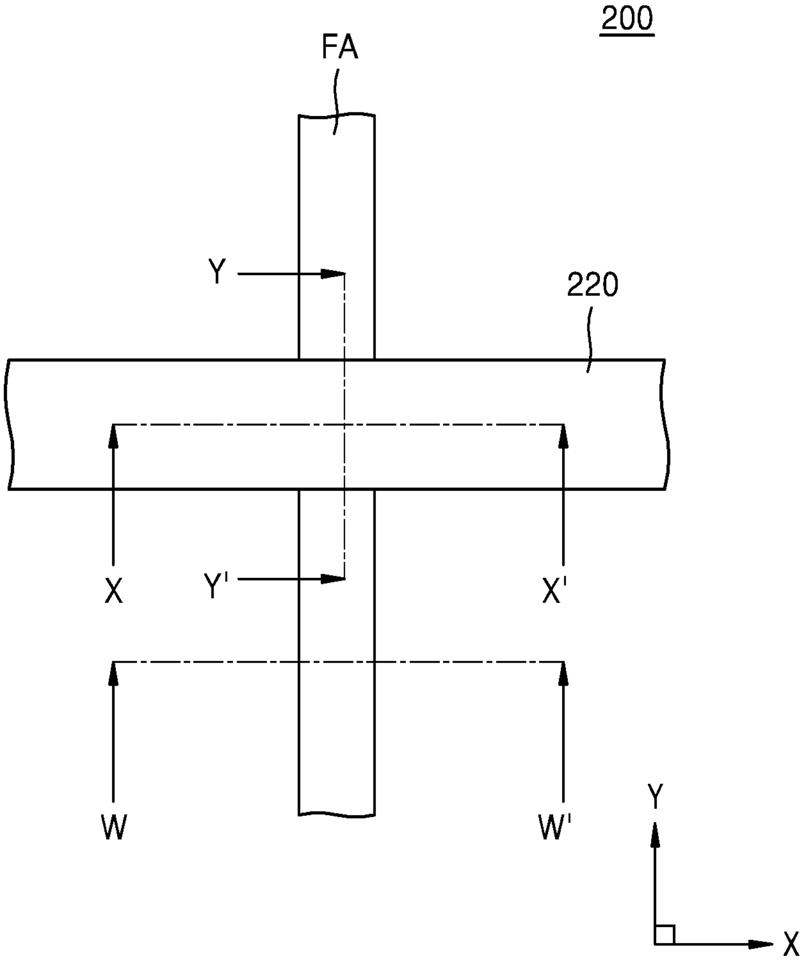


FIG. 9B

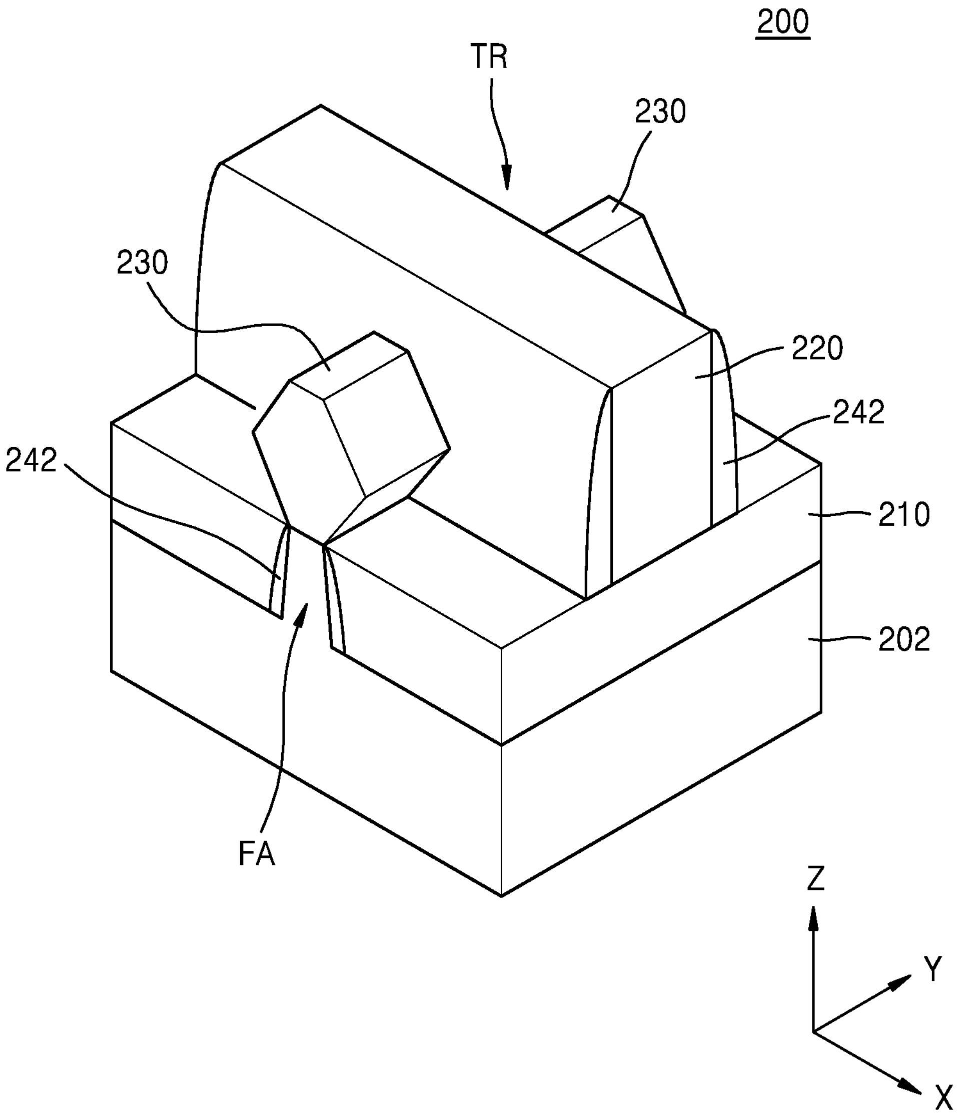


FIG. 9C

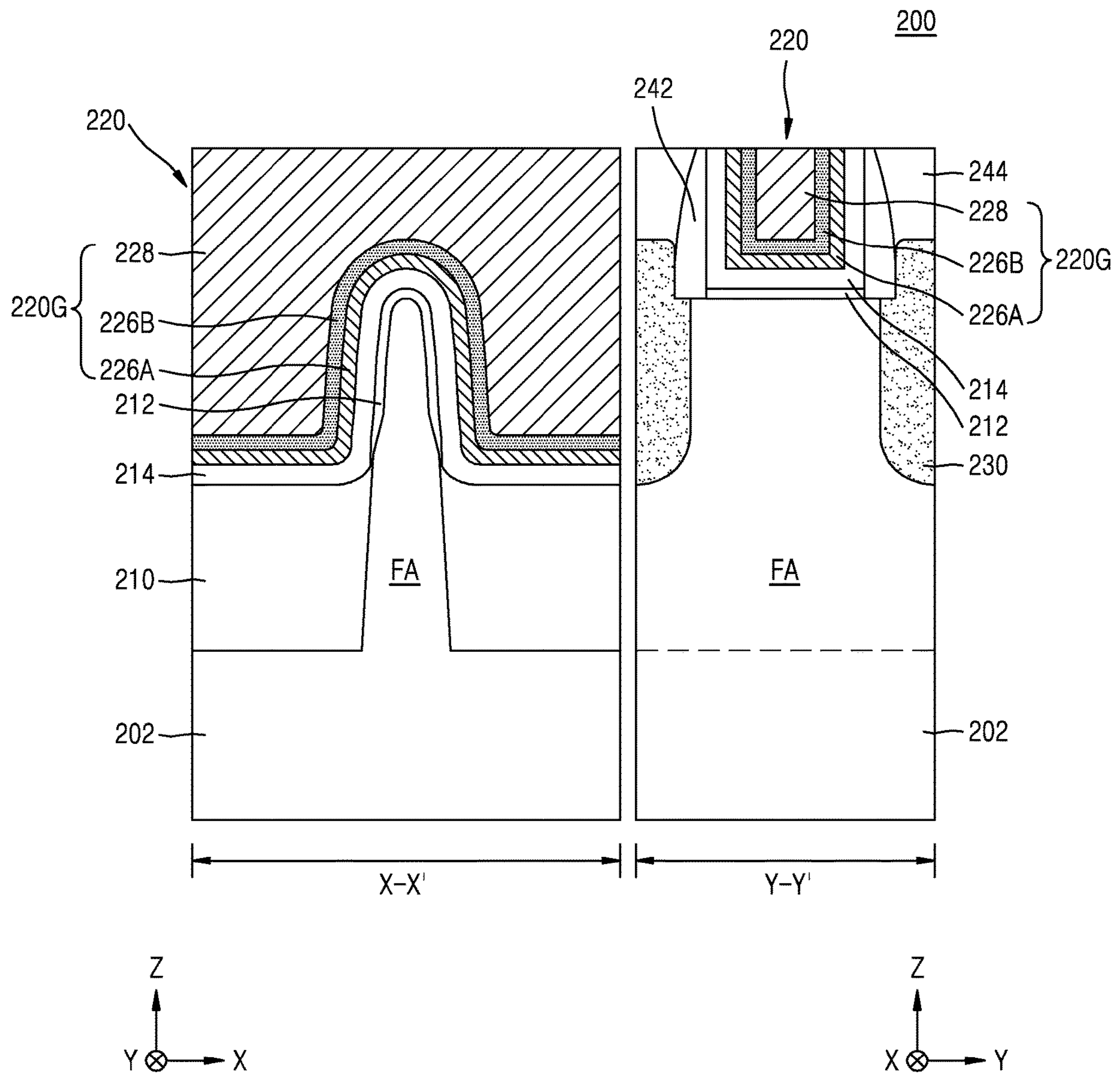


FIG. 10A

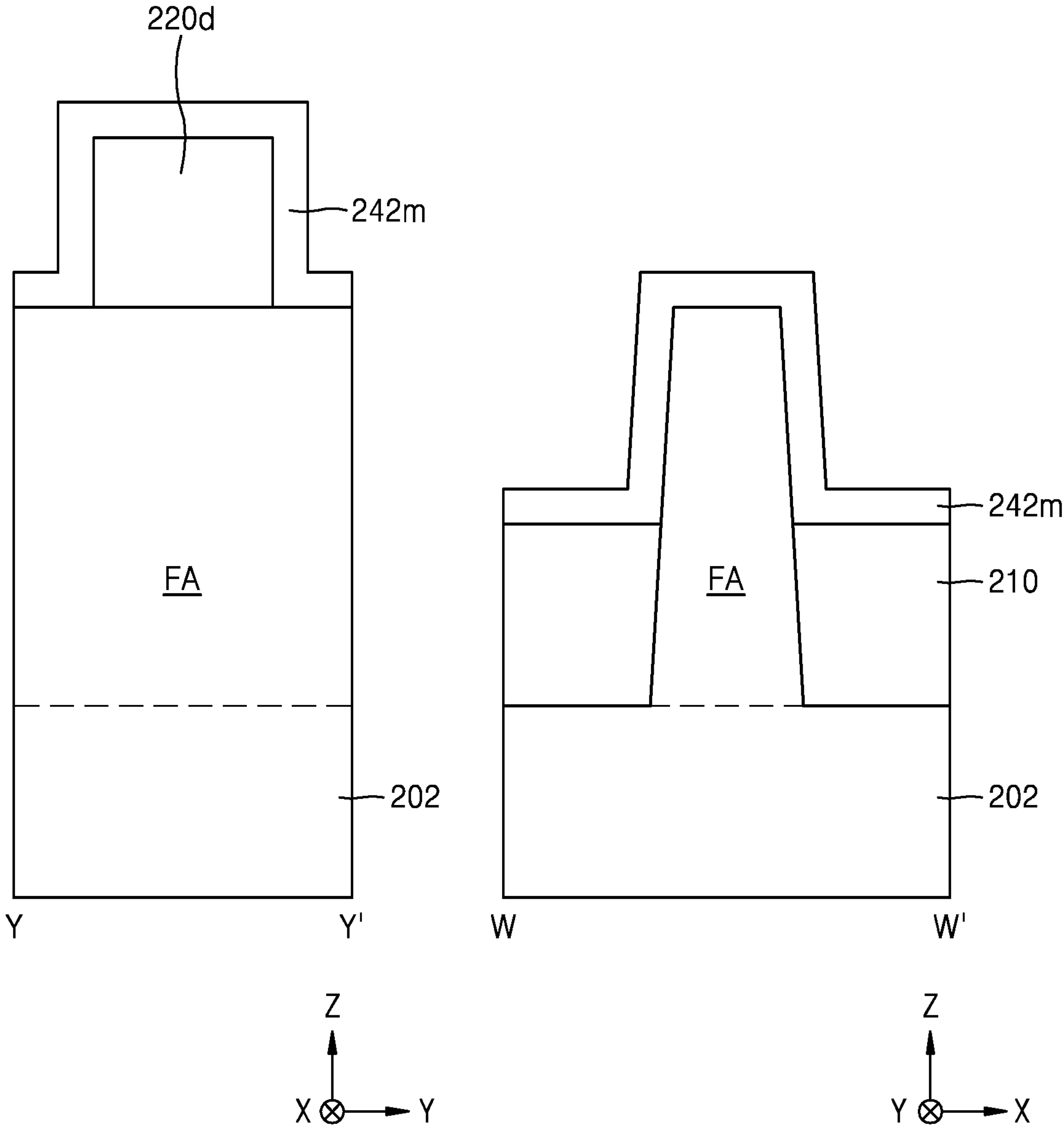


FIG. 10B

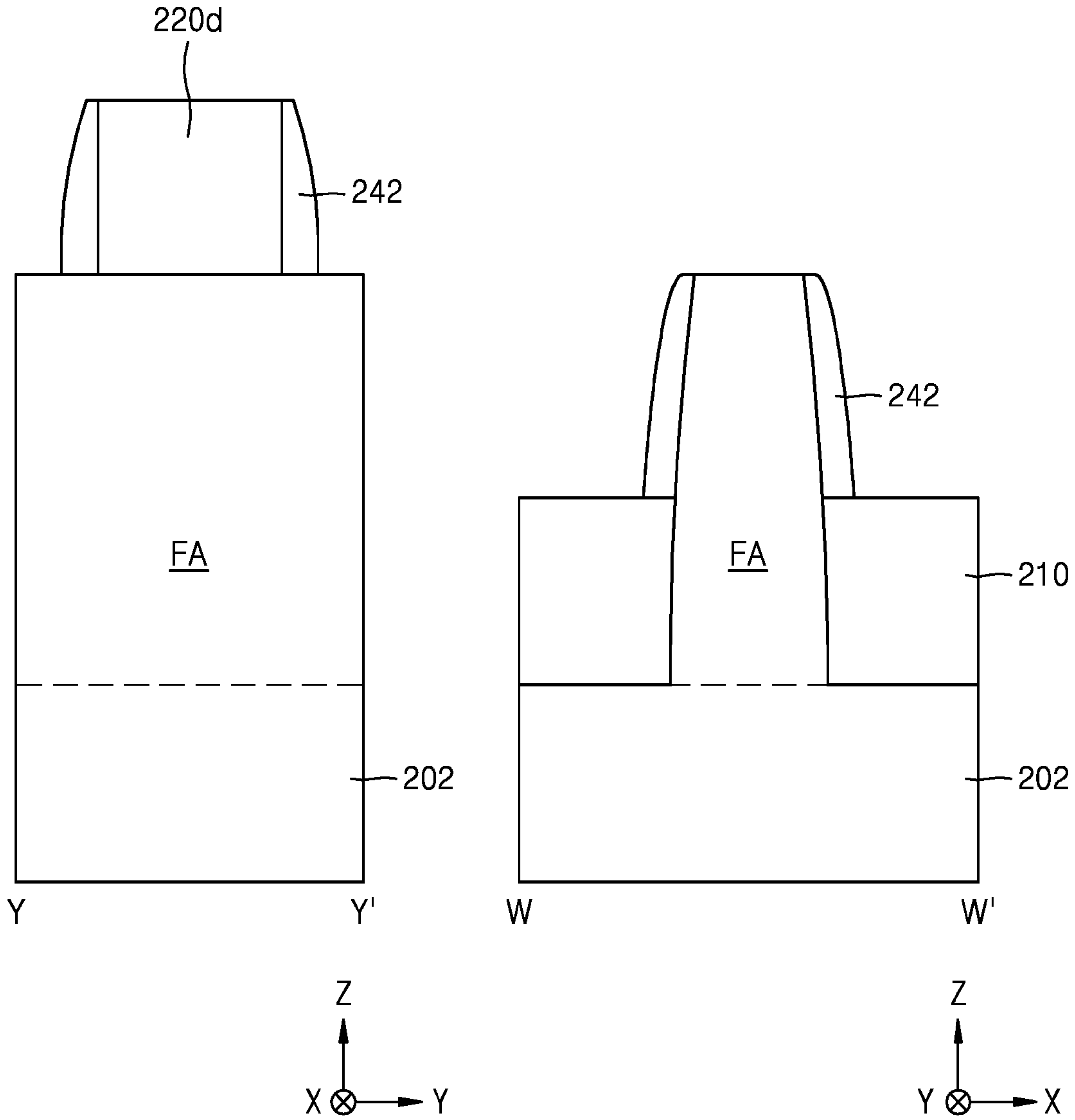


FIG. 10C

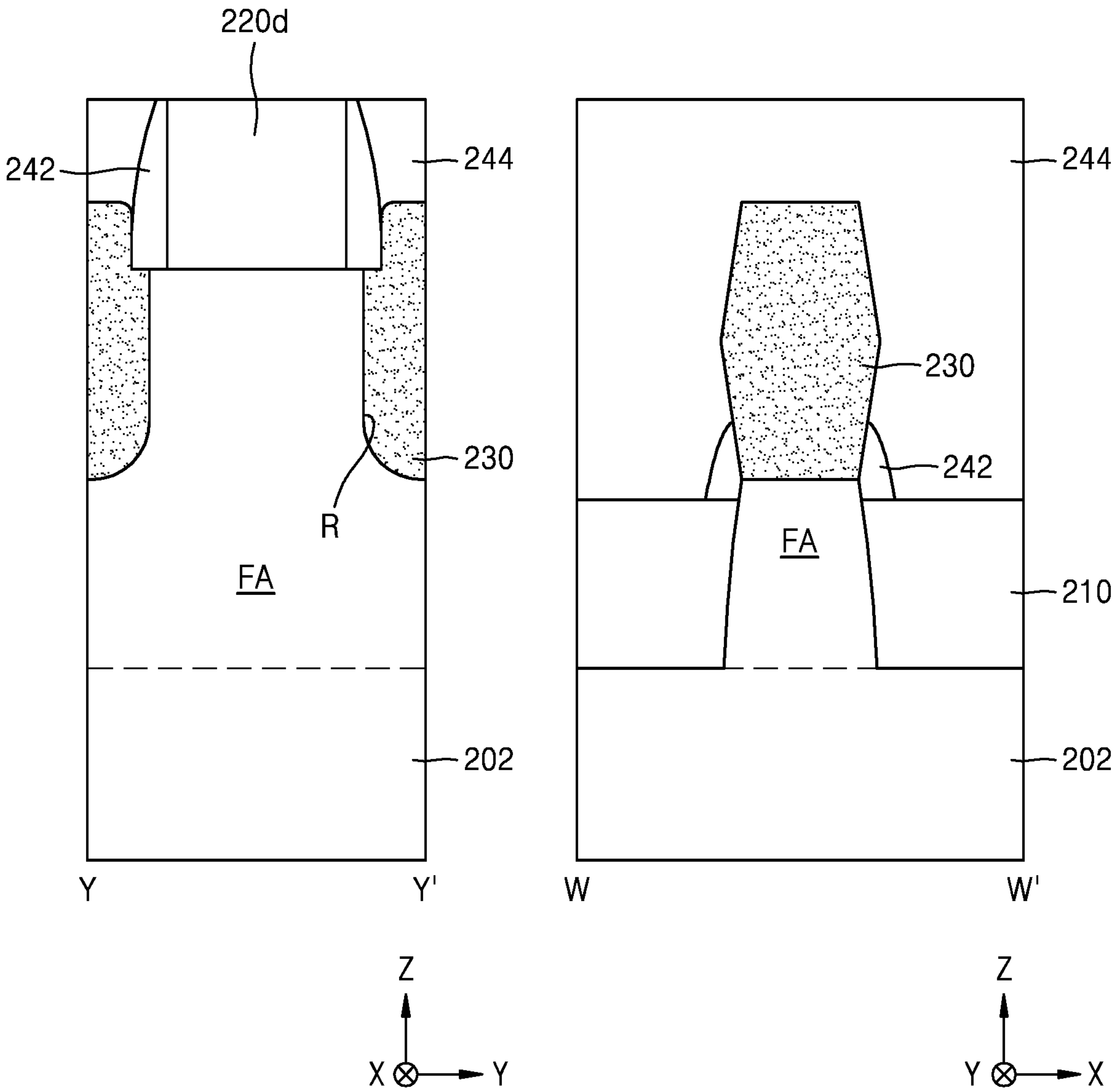


FIG. 10D

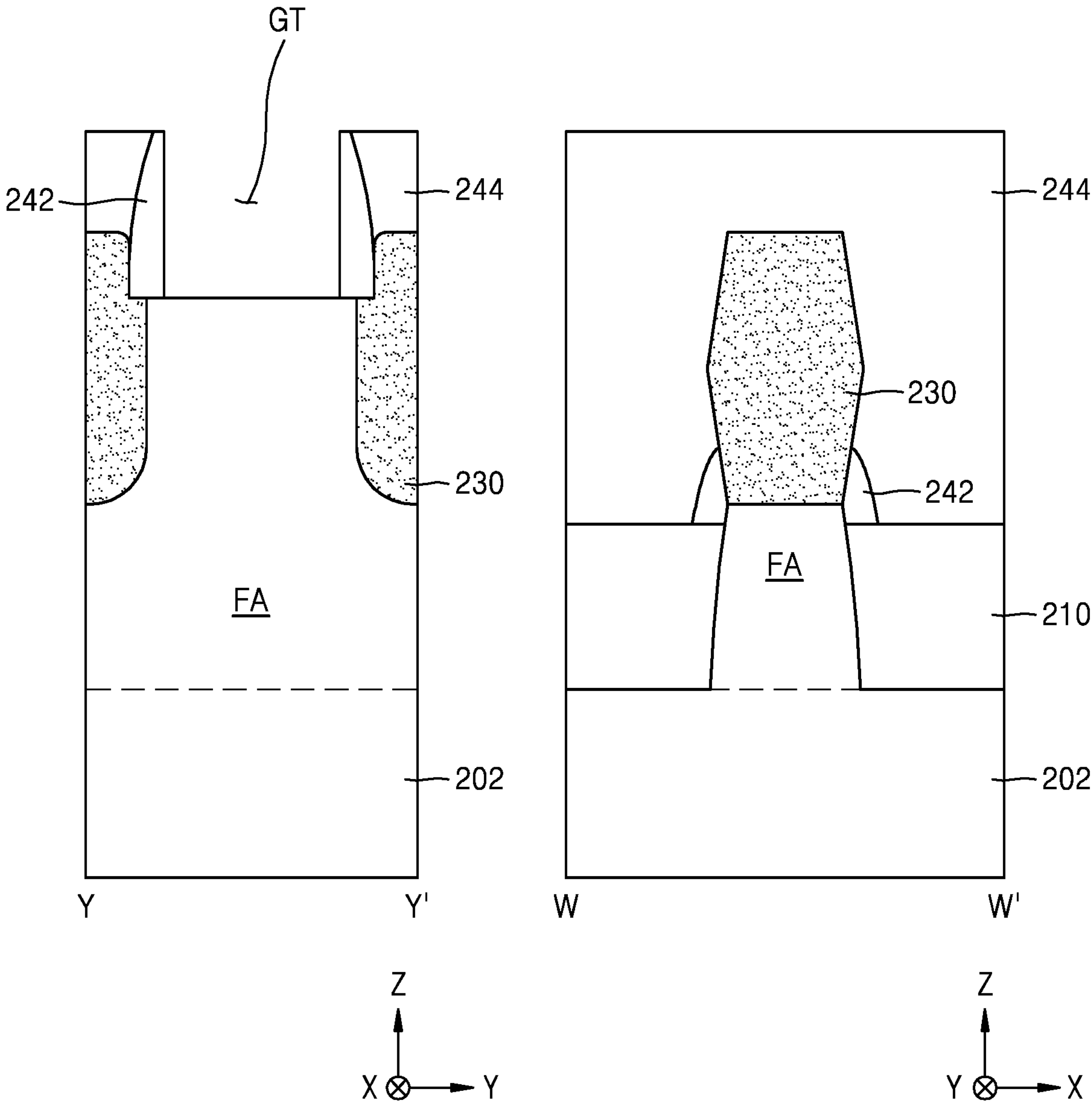


FIG. 10E

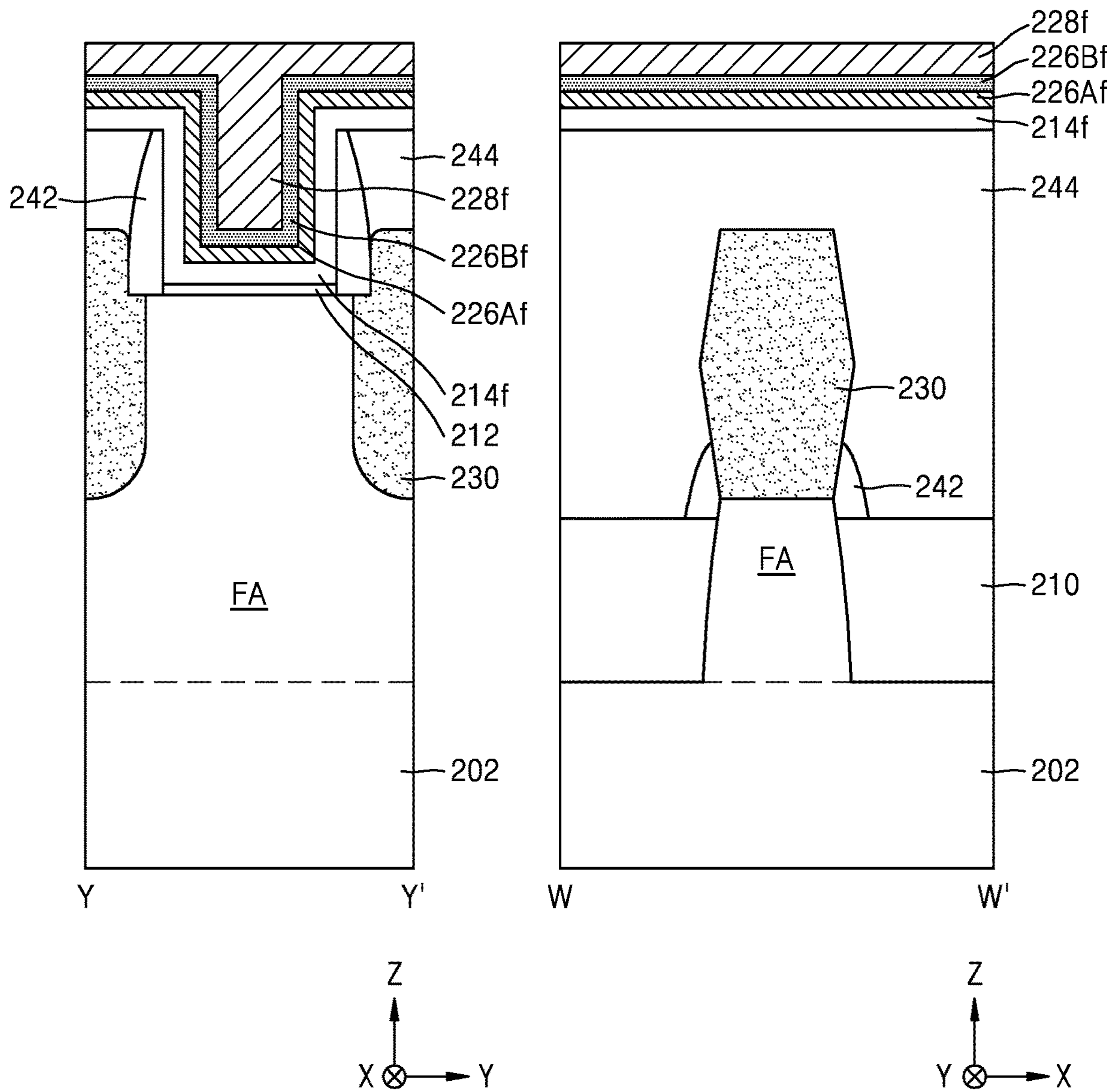


FIG. 10F

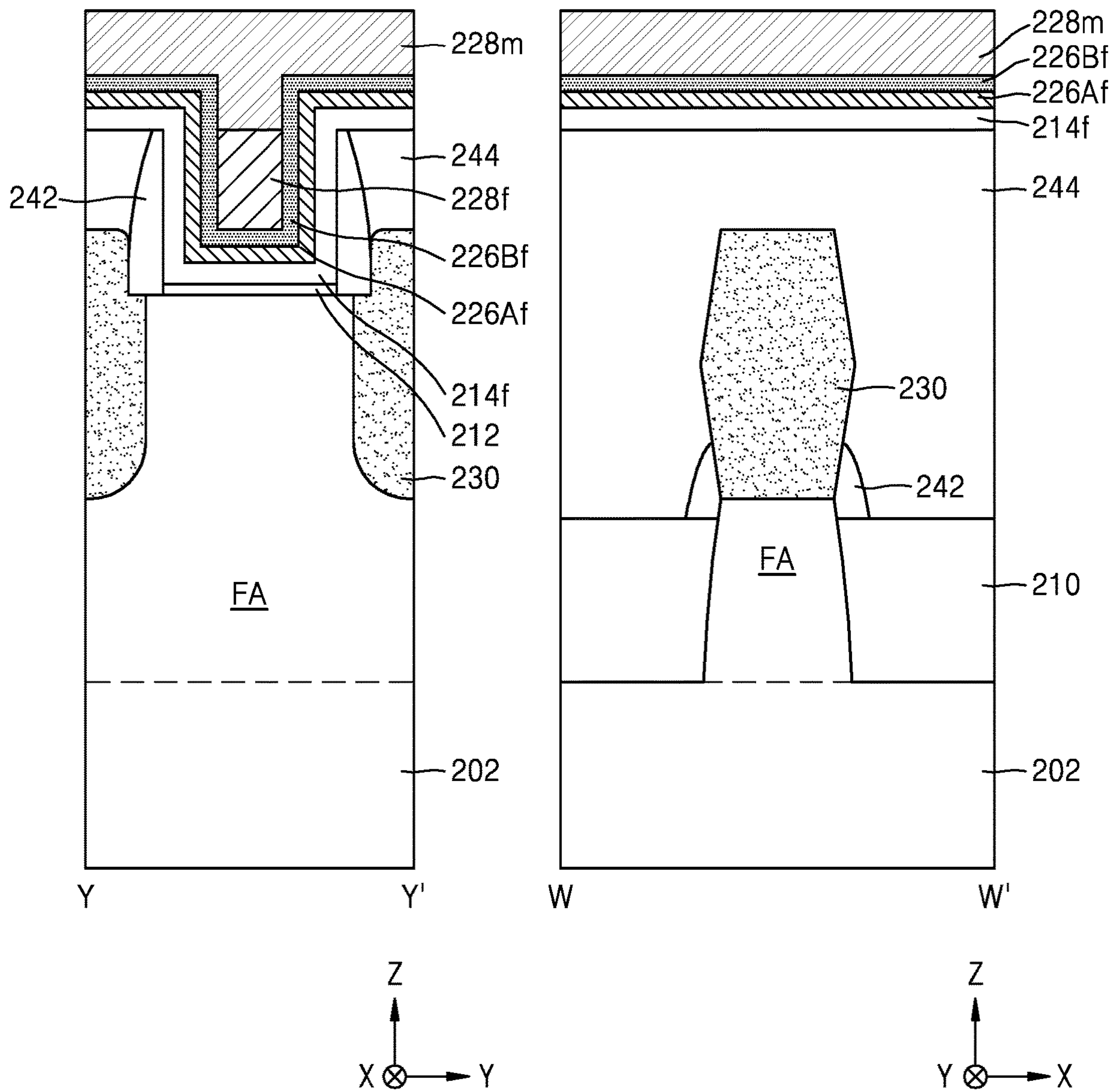
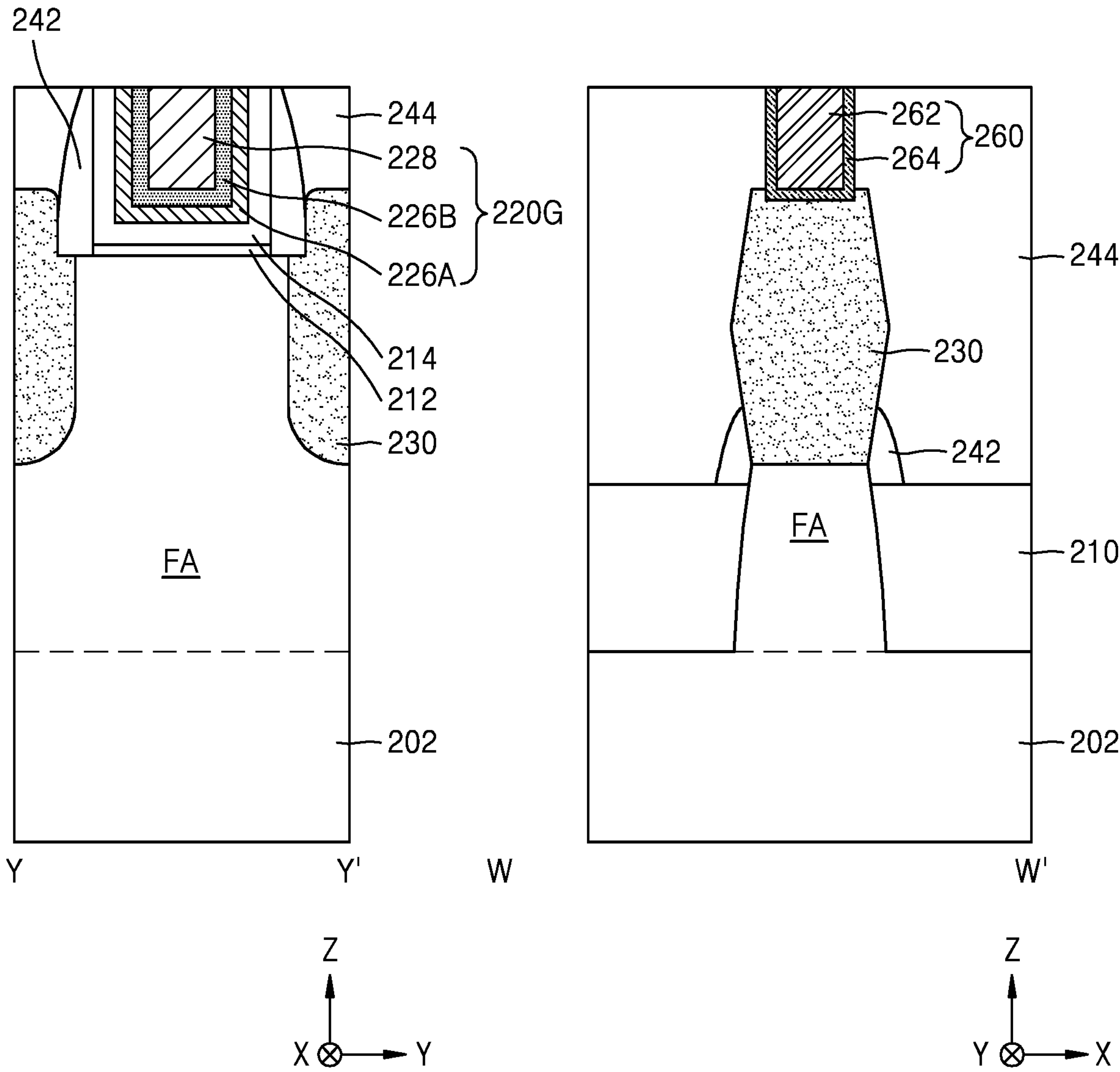


FIG. 10G



SUBSTRATE PROCESSING APPARATUS, SIGNAL SOURCE DEVICE, METHOD OF PROCESSING MATERIAL LAYER, AND METHOD OF FABRICATING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Korean Patent Application No. 10-2018-0071602, filed on Jun. 21, 2018, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

[0002] The inventive concept relates to a substrate processing apparatus, a signal source device, a method of processing a material layer, and a method of fabricating a semiconductor device, and more particularly, to a substrate processing apparatus capable of performing radical dry cleaning (RDC) on a crystalline material layer, a signal source device, a method of processing a material layer, and a method of fabricating a semiconductor device.

[0003] RDC is a process widely used from among processes for processing a semiconductor substrate on which devices are formed. RDC is a dry process and is capable of removing a material isotropically, thus being utilized in various ways. Furthermore, a certain degree of anisotropy may be obtained by applying a slight bias, and thus applicability of RDC is very high. On the other hand, when a crystalline material layer is etched by RDC, a highly rough etching surface may be obtained.

SUMMARY

[0004] The inventive concept provides a substrate processing apparatus capable of obtaining a smooth etched surface without a risk of damaging devices through RDC even for a crystalline material layer.

[0005] The inventive concept also provides a signal source device for a composite RDC that may be used in the substrate processing apparatus.

[0006] The inventive concept also provides a method of processing a material layer, the method by which a smooth etched surface may be obtained without a risk of damaging devices through RDC even for a crystalline material layer.

[0007] The inventive concept also provides a method of fabricating a semiconductor device by using the method of processing a material layer, wherein the semiconductor device has stable electrical characteristics.

[0008] According to an aspect of the inventive concept, provided is a substrate processing apparatus including: a processing chamber; a susceptor disposed in the processing chamber, wherein the susceptor is configured to support a substrate; a first plasma generator, disposed on one side of the processing chamber; and a second plasma generator disposed on another side of the processing chamber, wherein the second plasma generator is configured to generate plasma by simultaneously supplying a sinusoidal wave signal and a non-sinusoidal wave signal to the susceptor.

[0009] According to another aspect of the inventive concept, provided is a substrate processing apparatus including: processing chamber; a susceptor disposed in the processing chamber, wherein the susceptor is configured to support a substrate; an inlet configured to introduce remotely generated plasma into the processing chamber; and a plasma generator configured to generate a plasma by simultaneously supplying a sinusoidal wave signal and a non-sinusoidal wave signal to the susceptor, wherein the plasma generator includes: a sinusoidal wave generator configured to generate a sinusoidal wave signal to supply a sinusoidal wave signal to the susceptor; a non-sinusoidal wave generator configured to generate a non-sinusoidal wave signal to supply a non-sinusoidal wave signal to the susceptor; a first filter configured to prevent the non-sinusoidal wave signal from interfering with the sinusoidal wave generator; a second filter configured to prevent the sinusoidal wave signal from interfering with the non-sinusoidal wave generator; and a mixer configured to mix a sinusoidal wave signal and a non-sinusoidal wave signal respectively supplied from the sinusoidal wave generator and the non-sinusoidal wave generator.

[0010] According to another aspect of the inventive concept, provided is a signal source apparatus for composite radical dry cleaning (RDC), the apparatus including: a sinusoidal wave generator configured to supply a sinusoidal wave signal; a non-sinusoidal wave generator configured to supply a non-sinusoidal wave signal; a mixer configured to receive the sinusoidal wave signal and the non-sinusoidal wave signal from the sinusoidal wave generator and the non-sinusoidal wave generator, respectively; a first filter configured to prevent the sinusoidal wave signal from interfering with the non-sinusoidal wave generator; and a second filter configured to prevent the non-sinusoidal wave signal from interfering with the sinusoidal wave generator.

[0011] According to another aspect of the inventive concept, provided is a method of processing a material layer, the method including: positioning a substrate including a polycrystalline material layer on a susceptor in a processing chamber; converting an upper portion of the polycrystalline material layer into an amorphous material layer; and removing the amorphous material layer by using a radical, wherein the converting of the upper portion of the polycrystalline material layer into the amorphous material layer includes: supplying a sinusoidal wave signal and a non-sinusoidal wave signal to the susceptor to provide radicals and ions to the upper portion of the polycrystalline material layer.

[0012] According to another aspect of the inventive concept, provided is a method of fabricating a semiconductor device, the method including: forming a plurality of active regions on a substrate extending in a first direction and a device isolation film defining the active regions; forming a dummy gate line extending in a second direction intersecting the active regions on the device isolation film; forming source-drain regions in portions of the active regions exposed on both sides of the dummy gate line; forming an insulating film covering the device isolation film and the source-drain regions around the dummy gate line; removing the dummy gate line to form a gate trench extending between the source-drain regions; forming a gate insulating film and a polycrystalline gate material layer in the gate trench; converting an upper portion of the gate material layer into an amorphous material layer; and removing the amorphous material layer by using radicals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Embodiments of the inventive concept will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0014] FIGS. 1A and 1B are schematic block diagrams showing substrate processing apparatuses according to example embodiments;

[0015] FIG. 2A is a graph schematically showing an ion energy distribution in second plasma according to an example embodiment;

[0016] FIG. 2B is a graph schematically showing an ion energy distribution of ions in plasma generated when only a sinusoidal wave is supplied to a substrate;

[0017] FIG. 3 is a timing diagram showing a non-sinusoidal wave signal according to an example embodiment;

[0018] FIG. 4 is a flowchart of a method of processing a crystalline material layer, according to an example embodiment;

[0019] FIGS. 5A to 5C are schematic diagrams showing changes in a crystalline material layer when the crystalline material layer is treated with a single peak, according to an example embodiment;

[0020] FIG. 6 is a schematic lateral diagram showing a surface of a material layer when the surface is removed by using radicals and/or ions without converting a portion of the material layer into an amorphous material layer as shown in FIGS. 5A to 5C;

[0021] FIGS. 7 and 8 are schematic block diagrams showing second plasma generators according to example embodiments;

[0022] FIGS. 9A to 9C are diagrams showing a semiconductor device provided on a semiconductor substrate, wherein FIG. 9A is a plan view of the semiconductor device, FIG. 9B is a perspective view of the semiconductor device, and FIG. 9C is a cross-sectional view of the semiconductor device; and

[0023] FIGS. 10A to 10G are cross-sectional view diagrams sequentially showing a method of fabricating a semiconductor device, according to an example embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0024] FIG. 1 is a block diagram schematically showing a substrate processing apparatus 100 according to an example embodiment.

[0025] Referring to FIG. 1, the substrate processing apparatus 100 includes a processing chamber 110, a first electrode E1 and a second electrode E2 in the processing chamber 110, a first plasma generator 130 configured to supply a high frequency signal to the first electrode E1, and a second plasma generator 140 configured to supply a signal to the second electrode E2.

[0026] In some embodiments, the substrate processing apparatus 100 may be a substrate processing apparatus for radical dry cleaning (RDC).

[0027] The processing chamber 110 may have, for example, a cylindrical shape, and may have a first space 101A and a second space 101B therein. The interior space of the processing chamber 110 may be defined into the first space 101A and the second space 101B by a shower head 120. The inner wall of the processing chamber 110 may include a material like quartz, yttria ($Y2O_3$), etc.

[0028] An inlet 111 through which a process gas is introduced may be provided at the upper portion of the processing chamber 110. The process gas may flow through the inlet 111 into the first space 101A of the processing chamber 110.

[0029] Plasma generated by the first plasma generator 130 may flow toward the shower head 120 in the first space 101A. Although FIG. 1 shows a direct generation mechanism in which plasma is directly generated by the first plasma generator 130 in the first space 101A, plasma generated by a remote source may flow into the first space 101A.

[0030] The first plasma generator 130 may include a high frequency power source and a matcher. The matcher may reduce reflection of high-frequency power from the first electrode E1, thereby maximizing the efficiency of supplying the high-frequency power to the first electrode E1.

[0031] The first plasma generator 130 may generate first plasma P1 in the first space 101A by supplying a high frequency signal from about 2 MHz to about 40 MHz (e.g., 13.56 MHz) to the first electrode E1. The first plasma P1 may include both radicals and ions.

[0032] The first plasma P1 may be relatively uniformly distributed and flow into the second space 101B through the shower head 120. The shower head 120 may be grounded. In this case, the shower head 120 may allow radicals of the first plasma P1 to pass, but may block ions of the first plasma P1.

[0033] As a result, the second space 101B may include primarily or only radicals. In some embodiments, an increased ratio of radicals may be present in the second space 101B as compared to the first space 101A.

[0034] The second plasma generator 140 may include a sinusoidal wave generator 142*b* capable of generating a sinusoidal wave signal and a non-sinusoidal wave generator 144*b* capable of generating a non-sinusoidal wave signal. Here, the sinusoidal wave signal may refer to any periodic signal that may be expressed as a sine and/or cosine function. In addition, the non-sinusoidal wave signal may refer to any signal periodically repeated with a certain waveform other than that of a sinusoidal wave.

[0035] The sinusoidal wave signal and the non-sinusoidal wave signal may be mixed by a mixer 148 and supplied to the second electrode E2. In some embodiments, a first filter 142*a* may be provided to prevent the non-sinusoidal wave signal from interfering with the sinusoidal wave generator 142*b*. In some embodiments, a second filter 144*a* may be provided to prevent the sinusoidal wave signal from interfering with the non-sinusoidal wave generator 144*b*. Although FIG. 1 shows that the first filter 142*a* and the second filter 144*a* are separate from each other, the first filter 142*a* and the second filter 144*a* may be integrated as a single body.

[0036] The second electrode E2 may be a susceptor on which a substrate S is disposed. In some embodiments, the second electrode E2 may be provided separately from a susceptor in which the substrate S is disposed. The substrate S may be, but is not limited to, a semiconductor substrate like a silicon wafer and a glass substrate.

[0037] Inside the susceptor, for example, a cooling unit and a heating unit having annular shapes extending in the circumferential direction may be provided.

[0038] Second plasma P2 may be generated above the second electrode E2 by a non-sinusoidal wave signal and a sinusoidal wave signal supplied through the mixer 148.

[0039] The second plasma P2 may have an ion energy distribution for modifying a certain material layer exposed on a surface of the substrate S.

[0040] FIG. 2A is a graph schematically showing an ion energy distribution in the second plasma P2 according to an example embodiment.

[0041] Referring to FIG. **2**A, the ion energy distribution of ions in the second plasma P**2** may have a distribution having a single peak shape. The peak may have a relatively narrow and sharp distribution. The ion energy distribution having a single peak shape is obtained by supplying a combination of a sinusoidal wave signal and a non-sinusoidal wave signal to the second electrode E**2**.

[0042] FIG. **2**B is a graph schematically showing an ion energy distribution of ions in plasma generated when only a sinusoidal wave is supplied to the substrate S.

[0043] Referring to FIG. **2**B, the ion energy distribution of ions in the plasma has a bipeak-type distribution in which two peaks exist. When a material layer is processed using ions corresponding to one of these two peaks, a material layer, a device, and a structure on the substrate may be damaged by ions corresponding to the other peak.

[0044] On the other hand, as shown in FIG. **2**A, when the ion energy distribution has a single peak shape, an optimal energy distribution for a desired processing of a material layer may be obtained, and thus the possibility of damaging a material layer, a device, and a structure as in the case of a bipeak-type distribution may be significantly reduced.

[0045] As described above, the ion energy distribution having a single peak shape as shown in FIG. **2**A may be obtained based on a combination of a sinusoidal wave signal and a non-sinusoidal wave signal. In detail, the ion energy distribution having a single peak shape may be obtained by combining a sinusoidal wave signal with a particular non-sinusoidal wave signal.

[0046] FIG. **3** is a timing diagram showing the non-sinusoidal wave signal according to an example embodiment.

[0047] Referring to FIG. **3**, a non-sinusoidal wave of one period may have a shape in which a rectangular waveform R and a sawtooth waveform T are combined. However, the inventive concept is not limited thereto, and the non-sinusoidal wave may have a different shape. The shape of the non-sinusoidal wave may be determined to obtain a desired ion energy distribution by being combined with a sinusoidal wave having a certain frequency. In some embodiments, the shape of the non-sinusoidal wave may be determined through trials and errors to obtain a desired ion energy distribution by being combined with a sinusoidal wave having a certain frequency.

[0048] In some embodiments, the magnitude and the location of a peak (i.e., a single peak) in the ion energy distribution may be related, for example, to particular parameters of the non-sinusoidal wave, and, by changing the parameters, the magnitude and the location of the single peak may be adjusted. For example, the parameters of the non-sinusoidal wave for adjusting the magnitude and the location of the single peak may include a height H of the rectangular waveform R and a slope m of the hypotenuse of the sawtooth waveform T. However, the parameters of the non-sinusoidal wave for adjusting the magnitude and the location of the single peak are not limited thereto, and other parameters therefor may exist. One of ordinary skilled in the art will understand that the other parameters also fall within the scope of the inventive concept.

[0049] Referring to FIGS. **1** and **3** together, the second plasma generator **140** may further include a non-sinusoidal wave controller **146** capable of controlling the height H of the rectangular waveform R of the non-sinusoidal wave and the slope m of the hypotenuse of the sawtooth waveform T of the non-sinusoidal wave.

[0050] FIG. **4** is a flowchart of a method of processing a crystalline material layer, according to an example embodiment. FIGS. **5**A to **5**C are schematic diagrams showing changes in a crystalline material layer when the crystalline material layer is treated with a single peak, according to an example embodiment.

[0051] Referring to FIGS. **4** and **5**A, the substrate S including a polycrystalline material layer may be placed on a susceptor (corresponding to the second electrode E**2** in FIG. **1**A) (operation S**110**).

[0052] The substrate S may include a material layer **20** on an underlying material layer **10**. The material layer **20** may be a polycrystalline material layer. The material layer **20** may include, for example, polysilicon, a metal, a conductive metal nitride, a metal silicide, a conductive metal oxide, or a combination thereof. In some embodiments, the material layer **20** may include at least one of TiN, MoN, NbN, CoN, TaN, TiAlN, TaAlN, W, Ti, Ta, Co, Ru, RuO_2, $SrRuO_3$, Ir, IrO_2, Pt, PtO, SRO ($SrRuO_3$), BSRO ($(Ba,Sr)RuO_3$), CRO ($CaRuO_3$), and LSCo ($(La,Sr)CoO_3$), or a combination thereof.

[0053] The material layer **20** may be formed to have a height h**1** in a space having a width W. Here, a case where the material layer **20** is processed to have a height h**4** (here, h**1**>h**4**) will be described.

[0054] Referring to FIGS. **4** and **5**B, the material layer **20** having poly-crystallinity may be at least partially modified (operation S**120**). In FIG. **5**B, it may be seen that an upper portion of the material layer **20** of FIG. **5**A having poly-crystallinity is modified to an amorphous material layer **22**. That is, a portion of the material layer **20** may be converted to the amorphous material layer **22** from a free surface, for example, an upper surface, of the material layer **20**, to a certain depth.

[0055] A method of forming the amorphous material layer **22** by converting a portion of the material layer **20** having poly-crystallinity will be described below. That is, it has been found that, when plasma having the single peak ion energy distribution described above with reference to FIGS. **1** and **2**A is applied to the material layer **20** by using the second plasma generator **140**, at least a portion of the upper portion of the material layer **20** is changed to an amorphous state. That is, the second plasma generator **140** may generate the second plasma P**2** having a single peak ion energy distribution capable of converting an upper portion of the material layer **20** into an amorphous state by appropriately combining a sinusoidal wave and a non-sinusoidal wave, and the material layer **20** may be brought into contact with the second plasma P**2**.

[0056] FIG. **5**B is a schematic cross-sectional view of the material layer (**20***a*, **22**) after processing plasma having a single peak ion energy distribution. The amorphous material layer **22** may have a height h**3**, and a sum h**2** of the height of the amorphous material layer **22** and the height of a remaining material layer **20***a* may be greater than the height h**1** of the material layer **20** before being modified. However, the inventive concept is not limited thereto.

[0057] Referring to FIGS. **4** and **5**C, the amorphous material layer **22** may be easily removed by using radicals (operation S**130**). Since the amorphous material layer **22** may be removed by using radicals only, a sinusoidal wave

and a non-sinusoidal wave do not need to be supplied to the second plasma generator **140**. Thus, in this case, supply of both a sinusoidal wave and a non-sinusoidal wave to the second plasma generator **140** may be blocked. However, when certain directionality is needed to remove the amorphous material layer **22**, a bias may be applied to the second electrode E**2** to provide anisotropy.

[0058] FIG. **6** is a schematic lateral diagram showing a surface of remaining material layer **20***b* when a portion of material layer **20** is removed by using radicals and/or ions without converting a portion of the material layer **20** to the amorphous material layer **22** as shown in FIGS. **5**A to **5**C.

[0059] When the surface of the material layer **20** having a polycrystalline structure is directly removed by using radicals and/or ions, the surface of the material layer **20** is removed by units of crystal grains. In other words, for many of the crystal grains exposed to a processing environment using radicals and/or ions, certain crystal grains are preferentially removed as compared to other crystal grains, and thus a remaining material layer **20***b* having a rough surface is obtained. Here, the expression 'preferentially removed' may indicate that particular crystal grains are removed faster than the other crystal grains. Therefore, the expression 'preferentially removed' does not necessarily indicate that one crystal grain is completely removed before removal of another crystal grain begins.

[0060] The remaining material layer **20***b* having such a rough surface may be problematic, particularly in the case of a conductor with a small width W. When a current flows as a potential is applied to the remaining material layer **20***b*, an electric field may concentrate at an end of a rough surface thereof, and thus electrical characteristics may be unstable. Therefore, a semiconductor device having superior and more stable electrical characteristics may be obtained by fabricating the remaining material layer **20***a* to have a smooth and flat upper surface as shown in FIG. **5**C.

[0061] Referring to FIGS. **1**, **2**A, **3**, and **5**B together, the ion energy distribution of a single peak required to modify the material layer **20**, which is polycrystalline, into the amorphous material layer **22** may vary according to the type of the material layer **20**. As described above, since the ion energy distribution of a single peak may be adjusted by controlling the height H of the rectangular waveform R of a non-sinusoidal wave and the slope m of the hypotenuse of the sawtooth waveform T of the non-sinusoidal wave, the height H and the slope m for modifying the material layer **20** into the amorphous material layer **22** may be found through trial and error.

[0062] FIG. **1**B is a schematic block diagram showing a substrate processing apparatus **100***a* according to another example embodiment.

[0063] The substrate processing apparatus **100***a* of FIG. **1**B differs from the substrate processing apparatus **100** of FIG. **1**A in that the first plasma generator **130** is omitted. Therefore, descriptions identical to those given above will be omitted below, and descriptions below will mainly focus on the difference.

[0064] Referring to FIG. **1**B, in the substrate processing apparatus **100***a*, the first plasma P**1**, which is remotely generated, may be introduced directly into the first space **101**A through the inlet **111**. The first plasma P**1** may be generated remotely by using a magnetron, a waveguide, or the like, and may be supplied to the inlet **111** through a gas supply pipe.

[0065] The first plasma P**1** may flow into the first space **101**A through the inlet **111** and may be supplied into the second space **101**B through the shower head **120** as described above with reference to the substrate processing apparatus **100** of FIG. **1**A. At this time, ions in the first plasma P**1** may be blocked by the shower head **120** and only the radicals may pass through.

[0066] FIG. **7** is a block diagram showing a second plasma generator **140***a* according to an example embodiment.

[0067] Referring to FIG. **7**, the second plasma generator **140***a* may include the sinusoidal wave generator **142***b* and the non-sinusoidal wave generator **144***b*.

[0068] The second plasma generator **140***a* may include a high pass filter (HPF) **142***a***1** to pass therethrough only a sinusoidal wave having a relatively high frequency from among sinusoidal waves generated by the sinusoidal wave generator **142***b*. For example, the HPF **142***a***1** may be a HPF having a frequency transfer characteristic for frequencies between 0.4 MHz and 2 MHz less than or equal to −15 dB and a frequency transfer characteristic for the frequency of 13.56 MHz equal to or greater than −1.5 dB.

[0069] The second plasma generator **140***a* may further include a low pass filter (LPF) **144***a***1** to pass therethrough only a non-sinusoidal wave having a relatively low frequency from among non-sinusoidal waves generated by the non-sinusoidal wave generator **144***b*. For example, the LPF **144***a***1** may be a LPF having a frequency transfer characteristic for frequencies between 0.4 MHz and 2 MHz equal to or greater than −1.5 dB and a frequency transfer characteristic for the frequency of 13.56 MHz less than or equal to −15 dB.

[0070] However, the frequency characteristics of the second plasma generator **140***a* according to example embodiments are not limited to the above values.

[0071] In some embodiments, the HPF **142***a***1** may be a HPF having a reactance equal to or higher than 3000 ohms for the frequency of 0.4 MHz, a reactance equal to or higher than 700 ohms for the range of frequencies from about 0.8 MHz to about 2 MHz, and a reactance less than or equal to 10 ohms for the frequency of 13.56 MHz.

[0072] In some embodiments, the LPF **144***a***1** may be a LPF having a reactance of less than or equal to 10 ohms for the frequency of 0.4 MHz and a reactance equal to or higher than 1000 ohms for the frequency of 13.56 MHz.

[0073] However, the impedance characteristics of the second plasma generator **140***a* according to example embodiments are not limited to the above values.

[0074] A mixer **128** may be an active mixer or a manual mixer.

[0075] FIG. **8** is a block diagram showing a second plasma generator **140***b* according to an example embodiment.

[0076] Referring to FIG. **8**, the second plasma generator **140***b* may include the sinusoidal wave generator **142***b* and the non-sinusoidal wave generator **144***b*.

[0077] The second plasma generator **140***b* may include a band pass filter (BPF) **142***a***2** to pass therethrough only a sinusoidal wave having a relatively high frequency from among sinusoidal waves generated by the sinusoidal wave generator **142***b*. For example, the BPF **142***a***2** may be a BPF having a frequency transfer characteristic for frequencies between 0.4 MHz and 2 MHz less than or equal to −15 dB and a frequency transfer characteristic for the frequency of 13.56 MHz equal to or greater than −1.5 dB.

[0078] The second plasma generator **140*b*** may include a band stop filter (BSF) **144*a*2** to block only a non-sinusoidal wave having a relatively high frequency from among non-sinusoidal waves generated by the non-sinusoidal wave generator **144*b***. For example, the BSF **144*a*2** may be a BSF having a frequency transfer characteristic for frequencies between 0.4 MHz and 2 MHz equal to or greater than −15 dB and a frequency transfer characteristic for the frequency of 13.56 MHz less than or equal to −1.5 dB.

[0079] However, the frequency characteristics of the second plasma generator **140*b*** according to example embodiments are not limited to the above values.

[0080] In some embodiments, the BPF **142*a*2** may be a BPF having a reactance equal to or higher than 3000 ohms for the frequency of 0.4 MHz, a reactance equal to or higher than 700 ohms for the range of frequencies from about 0.8 MHz to about 2 MHz, and a reactance less than or equal to 10 ohms for the frequency of 13.56 MHz.

[0081] In some embodiments, the BSF **144*a*2** may be a BSF having a reactance of less than or equal to 10 ohms for the frequency of 0.4 MHz and a reactance equal to or higher than 1000 ohms for the frequency of 13.56 MHz.

[0082] However, the impedance characteristics of the second plasma generator **140*b*** according to example embodiments are not limited to the above values.

[0083] By using a substrate processing apparatus, a signal source device, and a method of processing a material layer according to the inventive concept, a smooth etched surface may be obtained for a crystalline material layer without a risk of device damage through RDC. Also, by using a method of fabricating a semiconductor device according to the inventive concept, a semiconductor device having a flatter upper surface of a material layer may be fabricated, thereby obtaining a semiconductor device having superior and more stable electrical characteristics.

[0084] Hereinafter, a semiconductor device including a stacked structure in which material layers as described above are stacked will be described.

[0085] FIGS. **9**A to **9**C are diagrams showing a semiconductor device **200** provided on a semiconductor substrate. FIG. **9**A is a plan view of the semiconductor device **200**, FIG. **9**B is a perspective view of the semiconductor device **200**, and FIG. **9**C is a cross-sectional view of the semiconductor device **200**.

[0086] Referring to FIGS. **9**A through **9**C, the semiconductor device **200** includes a fin-type active region FA protruding from a substrate **202**.

[0087] The substrate **202** may include at least one of a Group III-V material and a Group IV material. The Group III-V material may be a binary, ternary, or quaternary compound including at least one Group III element and at least one Group V element. The Group III-V material may be a compound including at least one element of In, Ga, and Al as the Group III element and at least one element of As, P, and Sb as the Group V element. For example, the Group III-V material may be selected from among InP, $In_zGa_{1-z}As$ ($0 \le Z \le 1$), and $Al_zGa_{1-z}As$ ($0 \le Z \le 1$). The binary compound may be any one of InP, GaAs, InAs, InSb, and or GaSb, for example. The ternary compound may be any one of InGaP, InGaAs, AlInAs, InGaSb, GaAsSb, and GaAsP. The Group IV material may be Si and/or Ge. However, the Group III-V materials and the Group IV materials that may be used for forming a thin film according to the inventive concept are not limited to the above examples.

[0088] The Group III-V material and the Group IV material like Ge may be used as a channel material capable of forming a low-power and high-speed transistor. A semiconductor substrate including a Group III-V material having a higher electron mobility than a Si substrate, e.g., a semiconductor substrate including GaAs, and a semiconductor material having a higher hole mobility than a Si substrate, e.g., a SiGe semiconductor substrate including Ge, may be used to form a high-performance CMOS. In some embodiments, when it is intended to form an N-type channel in the semiconductor substrate **202**, the semiconductor substrate **202** may include any one of the above-stated Group III-V materials or SiC. In some other embodiments, when it is intended to form a P-type channel in the semiconductor substrate **202**, the semiconductor substrate **202** may include SiGe.

[0089] The fin-type active region FA may extend in one direction (Y direction in FIGS. **9**A and **9**B). A device isolation film **210** covering the lower sidewall of the fin-type active region FA is formed on the substrate **202**. The fin-type active region FA protrudes in a fin-like shape over the device isolation film **210**. In some embodiments, the device isolation film **210** may include a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a combination thereof, but is not limited thereto.

[0090] Above the device isolation film **210**, a gate structure **220** may extend over the fin-type active region FA in a direction (X direction) intersecting the direction in which the fin-type active region FA extends. Source/drain regions **230** may be formed on both sides of the gate structure **220** over the fin-type active region FA.

[0091] The source/drain regions **230** may include a semiconductor layer epitaxially grown from the fin-type active region FA. The source/drain regions **230** may include an embedded SiGe structure including a plurality of epitaxially grown SiGe layers, an epitaxially grown Si layer, or an epitaxially grown SiC layer. FIG. **9**B exemplifies a case where the pair of source/drain regions **230** have particular cross-sectional shapes. However, according to the inventive concept, the cross-sectional shapes of the source/drain regions **230** are not limited to those shown in FIG. **9**B and may vary. For example, the source/drain regions **230** may have various cross-sectional shapes like a circular shape, an elliptical shape, and a polygonal shape.

[0092] A MOS transistor TR may be formed at a portion where the fin-type active region FA and the gate structure **220** intersect each other. The MOS transistor TR includes a MOS transistor having a 3-dimensional structure in which channels are formed on the upper surface and both side surfaces of the fin-type active region FA. The MOS transistor TR may constitute an NMOS transistor or a PMOS transistor.

[0093] As shown in FIG. **9**C, the gate structure **220** may include an interface layer **212**, a high-k film **214**, a first metal-containing layer **226**A, a second metal-containing layer **226**B, and a gap-fill metal layer **228** that are formed from a surface of the fin-type active region FA in the order stated. The first metal-containing layer **226**A, the second metal-containing layer **226**B, and the gap-fill metal layer **228** of the gate structure **220** may constitute a gate electrode **220**G.

[0094] On both sides of the gate structure **220**, insulation spacers **242** may be provided. Also, the insulation spacers

242 may be provided as source/drain spacers on sidewalls of an active region on both sides of the gate structure **220**.

[0095] The insulation spacer **242** may include a low-k material layer as described above. Particularly, the insulation spacer **242** may be a SiOCN material layer. In some embodiments, the insulation spacer **242** may include a single layer. In some embodiments, the insulation spacer **242** may include multiple layers where two or more material layers are stacked.

[0096] An interlayer insulation film **244** covering the insulation spacer **242** on the opposite side of the gate structure **220** around the insulation spacer **242** may be formed.

[0097] The interface layer **212** may be formed on a surface of the fin-type active region FA. The interface layer **212** may include an insulating material layer like an oxide film, a nitride film, or a nitride oxide film. The interface layer **212** may constitute a gate insulating film together with the high-k film **214**.

[0098] The high-k film **214** may include a material having a dielectric constant that is greater than that of a silicon oxide film. For example, the high-k film **214** may have a dielectric constant from about 10 to about 25. The high-k film **214** may include a material selected from among zirconium oxide, zirconium silicon oxide, hafnium oxide, hafnium oxynitride, hafnium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, and combinations thereof. However, the materials constituting the high-k film **214** are not limited to the above-stated examples.

[0099] In some embodiments, the first metal-containing layer **226**A may include a nitride of Ti, a nitride of Ta, an oxynitride of Ti, or an oxynitride of Ta. For example, the first metal-containing layer **226**A may include TiN, TaN, TiAlN, TaAlN, TiSiN, or a combination thereof. The first metal-containing layer **226**A may be formed by using various deposition methods like ALD, CVD, and PVD.

[0100] In some embodiments, the second metal-containing layer **226**B may include an N-type metal-containing layer needed for an NMOS transistor including an Al compound that contains Ti or Ta. For example, the second metal-containing layer **226**B may include TiAlC, TiAlN, TiAlCN, TiAl, TaAlC, TaAlN, TaAlCN, TaAl, or a combination thereof.

[0101] In some other embodiments, the second metal-containing layer **226**B may include a P-type metal-containing layer that is needed for a PMOS transistor. For example, the second metal-containing layer **226**B may include at least one of Mo, Pd, Ru, Pt, TiN, WN, TaN, Ir, TaC, RuN, and MoN.

[0102] The second metal-containing layer **226**B may include a single layer or multiple layers.

[0103] The second metal-containing layer **226**B may control the work function of the gate structure **220** together with the first metal-containing layer **226**A. The threshold voltage of the gate structure **220** may be adjusted by the work function control of the first metal-containing layer **226**A and the second metal-containing layer **226**B. In some embodiments, either the first metal-containing layer **226**A or the second metal-containing layer **226**B may be omitted.

[0104] The gap-fill metal layer **228** may be formed to fill the remaining gate space on the second metal-containing layer **226**B when the gate structure **220** is formed through a replacement metal gate (RMG) process.

[0105] The gap-fill metal layer **228** is selected from a group consisting of metal nitrides like WN, TiN, and TaN, W, Co, Al, metal carbides, metal silicides, metal aluminum carbides, metal aluminum nitrides, metal silicon nitrides, etc.

[0106] The gap-fill metal layer **228** may have a polycrystalline structure. In this case, the roughness of the upper surface of the gap-fill metal layer **228** may be less than ½ of the average diameter of crystal grains of the gap-fill metal layer **228**.

[0107] Although an integrated circuit device including a FinFET including a channel of a 3-dimensional structure has been described above with reference to FIGS. **9**A to **9**C, the inventive concept is not limited to the above description. For example, one of ordinary skill in the art will understand that, through various modifications and alterations within the scope of the inventive concept as described above, methods of fabricating integrated circuit devices including planar MOSFETs having characteristics according to the inventive concept may be provided.

[0108] FIGS. **10**A to **10**G are cross-sectional view diagrams sequentially showing a method of fabricating a semiconductor device according to an example embodiment. In FIGS. **10**A to **10**G, the Y-Y' cross-section and the W-W' cross-section represent the Y-Y' cross-section and the W-W' cross-section of FIG. **9**A, respectively.

[0109] Referring to FIG. **10**A, a dummy gate electrode **220***d* may be formed on the substrate **202** on which the fin-shaped active region FA is defined by the device isolation layer **210**. Next, a spacer material layer **242***m* may be conformally deposited over the substrate **202** and the dummy gate electrode **220***d*.

[0110] Since the substrate **202** has been described above with reference to FIG. **9**A, further description thereof is omitted here.

[0111] The dummy gate electrode **220***d* may include, for example, polysilicon, but is not limited thereto. The dummy gate electrode **220***d* may be provided to secure a position and a space for forming a gate electrode later.

[0112] The spacer material layer **242***m* may include the low-k material layer described above. In some embodiments, the spacer material layer **242***m* may include a SiOCN material layer. In some embodiments, the spacer material layer **242***m* may include a single material layer of SiOCN. In some embodiments, the spacer material layer **242***m* may include a multi-material layer in which two or more material layers including SiOCN are stacked.

[0113] Referring to FIG. **10**B, the spacers **242** are formed by anisotropically etching the spacer material layer **242***m*. The spacers **242** may be formed on the sidewalls of the dummy gate electrode **220***d*. Also, the spacers **242** may be formed on the sidewalls of the fin-type active region FA on both sides of the dummy gate electrode **220***d*.

[0114] Referring to FIG. **10**C, the fin-type active region FA may be partially removed by using the dummy gate electrode **220***d* and the spacers **242** as an etching mask.

[0115] Anisotropic etching and/or isotropic etching may be performed to partially remove the fin-type active region FA. Particularly, partial etching may be performed by combining anisotropic etching and isotropic etching to expose at least a portion of the bottom surface of the spacer **242** formed on the sidewall of the dummy gate electrode **220***d*.

[0116] More particularly, isotropic etching may be performed through wet etching after an exposed portion of the fin-type active region FA is anisotropically etched to a certain depth. As an etchant for the wet etching, for example, an NH_4OH solution, trimethyl ammonium hydroxide (TMAH), an HF solution, an NH_4F solution, or a mixture thereof may be used. However, the inventive concept is not limited thereto.

[0117] A recess is formed by anisotropic etching using the spacer **242** as an etching mask, and the wet etching is performed on the recess. As a result, a recess R that exposes a portion of the bottom surface of the spacer **242** as shown in FIG. **10**C may be obtained. Particularly, the recess R may expose at least a portion of the bottom surface of the spacer **242** on the side of an impurity region.

[0118] In some embodiments, the wet etching performed to expose a portion of the bottom surface of the spacer **242** may be omitted.

[0119] Next, a source/drain material layer may be formed in the recess R on the side of the impurity region to form source/drain regions **230**. The source/drain material layer may include Si, SiC, or SiGe, but the inventive concept is not limited thereto. The source/drain material layer may be formed, for example, by epitaxial growth. An impurity may be implanted in situ during epitaxial growth of the source/drain material layer or may be implanted through ion implantation after the source/drain material layer is formed. Furthermore, an upper surface of the source/drain regions **230** may be higher than the upper surface of the fin-type active region FA.

[0120] Next, the interlayer insulation film **244** may be formed on the source/drain regions **230**. The interlayer insulation film **244** may include, for example, a silicon oxide, but is not limited thereto.

[0121] Referring to FIG. **10**D, a gate trench GT may be formed by removing the dummy gate electrode **220***d*. A portion of an upper surface of the substrate **202** may be exposed by the gate trench GT. The portion of the semiconductor substrate **202** exposed by the gate trench GT may correspond to a channel region of a semiconductor device fabricated later.

[0122] The dummy gate electrode **220***d* may be removed through, for example, dry etching or wet etching.

[0123] Referring to FIG. **10**E, the interface layer **212** may be formed. Next, a high-k material layer **214***f*, a first metal-containing material layer **226**Af, a second metal-containing material layer **226**Bf, and a gap-fill metal material layer **228***f* are sequentially formed over the interface layer **212**, the sidewalls of the gate trench GT, and the upper surface of the interlayer insulation film **244**, respectively. Particularly, the high-k material layer **214***f*, the first metal-containing material layer **226**Af, and the second metal-containing material layer **226**Bf may be conformally formed along the respective surfaces. Furthermore, the gap-fill metal material layer **228***f* may be formed to fill a trench formed by the second metal-containing material layer **226**Bf.

[0124] The high-k material layer **214***f*, the first metal-containing material layer **226**Af, the second metal-containing material layer **226**Bf, and the gap-fill metal material layer **228***f* may each be independently formed through an ALD process, a CVD process, or a PVD process. However, the inventive concept is not limited thereto.

[0125] Referring to FIG. **10**F, an amorphous material layer **228***m* may be formed by converting a portion of an upper surface side of the gap-fill metal material layer **228***f* into an amorphous state by using the substrate processing apparatus shown in FIG. **1**. The method for converting an upper portion of the gap-fill metal material layer **228***f*, for example, a polycrystalline gap-fill metal material layer into an amorphous state from a free surface to a predetermined depth has been described above with reference to FIGS. **1**, **2**A, **3**, and **5**A to **5**C, and thus detailed description thereof will be omitted below.

[0126] Referring to FIG. **10**G, the semiconductor device **200** may be finally obtained by applying a planarizing process until the upper surface of the interlayer insulation film **244** is exposed. The planarization process may be performed through, for example, isotropic etching using radicals. As is known, by using RDC using radicals, dry etching may be performed as isotropic etching due to the radicals. However, the inventive concept is not limited thereto. As stated above, the RDC may be performed, for example, until the upper surface of the interlayer insulation film **244** is exposed. At this time, the amorphous material layer **228***m* may be removed through the RDC.

[0127] A contact **260** may be connected onto the impurity region constituting source/drain regions **230**. The contact **260** may include a conductive barrier film **264** and a wire layer **262**. In some embodiments, the conductive barrier film **264** may include titanium nitride, tantalum nitride, tungsten nitride, titanium carbon nitride, or a combination thereof, but is not limited thereto. In some embodiments, the wire layer **262** may include a doped semiconductor, a metal like Cu, Ti, W, or Al, a metal suicide like nickel suicide, cobalt suicide, tungsten suicide, tantalum suicide, or a combination thereof, but is not limited thereto. The gate electrode **220**G and the contact **260** may be electrically insulated from each other by the interlayer insulation film **244**.

[0128] Although FIGS. **9**A to **9**C and FIGS. **10**A to **10**G show that the source/drain regions **230** have a raised source/drain (RSD) structure, the inventive concept is not limited thereto. For example, the source/drain regions **230** may include impurity-doped regions formed in corresponding regions of the fin-type active region FA.

[0129] While the inventive concept has been particularly shown and described with reference to example embodiments thereof, it will be understood by one of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the inventive concept as defined by the appended claims. Accordingly, future modifications of the embodiments of the inventive concept will not depart from the scope of the inventive concept.

1. A substrate processing apparatus comprising:

a processing chamber;

a susceptor disposed in the processing chamber, wherein the susceptor is configured to support a substrate;

a first plasma generator disposed on one side of the processing chamber; and

a second plasma generator disposed on another side of the processing chamber, wherein the second plasma generator is configured to generate plasma by simultaneously supplying a sinusoidal wave signal and a non-sinusoidal wave signal to the susceptor.

2. The substrate processing apparatus of claim **1**, wherein the second plasma generator comprises:
a sinusoidal wave generator configured to generate a sinusoidal wave signal to supply the sinusoidal wave signal to the susceptor;
a non-sinusoidal wave generator configured to generate a non-sinusoidal wave signal to supply the non-sinusoidal wave signal to the susceptor; and
a mixer configured to mix the sinusoidal wave signal and the non-sinusoidal wave signal respectively supplied from the sinusoidal wave generator and the non-sinusoidal wave generator.

3. The substrate processing apparatus of claim **2**, wherein the second plasma generator further comprises:
a first filter configured to prevent the non-sinusoidal wave signal from interfering with the sinusoidal wave generator; and
a second filter configured to prevent the sinusoidal wave signal from interfering with the non-sinusoidal wave generator.

4. The substrate processing apparatus of claim **3**, wherein either the first filter or the second filter comprises a band pass filter and the other one comprises a band stop filter.

5. The substrate processing apparatus of claim **1**, wherein the sinusoidal wave signal has a frequency of about 13.56 MHz and the non-sinusoidal wave signal has a frequency from about 0.4 MHz to about 2 MHz.

6. The substrate processing apparatus of claim **1**, wherein one period of the non-sinusoidal wave signal has a shape that is a combination of a rectangular waveform and a sawtooth waveform.

7. The substrate processing apparatus of claim **6**, wherein the second plasma generator is configured such that ions generated by the second plasma generator have a single peak ion energy distribution.

8. The substrate processing apparatus of claim **7**, wherein a position and a size of the single peak ion energy distribution are controlled by at least a height of the rectangular waveform of the non-sinusoidal wave signal and a slope of a hypotenuse of the sawtooth waveform of the non-sinusoidal wave signal.

9. The substrate processing apparatus of claim **1**, wherein the processing chamber comprises:
a first space in which plasma generated by the first plasma generator flows;
a second space in which plasma is generatable by the second plasma generator; and
a shower head configured to selectively pass only radicals in the plasma of the first space and defining the first space and the second space.

10. The substrate processing apparatus of claim **9**, wherein the shower head is grounded.

11. The substrate processing apparatus of claim **1**, wherein the first plasma generator is disposed at an upper portion of the processing chamber, and
the second plasma generator is disposed below the processing chamber.

12. A signal source apparatus for composite radical dry cleaning (RDC) comprising:
a sinusoidal wave generator configured to supply a sinusoidal wave signal;
a non-sinusoidal wave generator configured to supply a non-sinusoidal wave signal;
a mixer configured to receive the sinusoidal wave signal and the non-sinusoidal wave signal from the sinusoidal wave generator and the non-sinusoidal wave generator, respectively;
a first filter configured to prevent the non-sinusoidal wave signal from interfering with the sinusoidal wave generator; and
a second filter configured to prevent the sinusoidal wave signal from interfering with the non-sinusoidal wave generator.

13. The signal source apparatus of claim **12**, wherein the first filter is a high-pass filter (HPF) and the second filter is a low-pass filter (LPF).

14. The signal source apparatus of claim **12**, wherein the first filter is a band pass filter and the second filter is a band stop filter.

15. The signal source apparatus of claim **12**, wherein one period of the non-sinusoidal wave signal has a shape that is a combination of a rectangular waveform and a sawtooth waveform,
the signal source apparatus further comprising a non-sinusoidal wave controller capable of controlling a height of the rectangular waveform and a slope of a hypotenuse of the sawtooth waveform.

16-25. (canceled)

26. A substrate processing apparatus comprising:
a processing chamber;
a susceptor disposed in the processing chamber, wherein the susceptor is configured to support a substrate;
an inlet configured to introduce remotely generated plasma into the processing chamber; and
a plasma generator configured to generate plasma by simultaneously supplying a sinusoidal wave signal and a non-sinusoidal wave signal to the susceptor,
wherein the plasma generator comprises:
a sinusoidal wave generator configured to generate a sinusoidal wave signal to supply the sinusoidal wave signal to the susceptor;
a non-sinusoidal wave generator configured to generate a non-sinusoidal wave signal to supply the non-sinusoidal wave signal to the susceptor;
a first filter configured to prevent the non-sinusoidal wave signal from interfering with the sinusoidal wave generator;
a second filter configured to prevent the sinusoidal wave signal from interfering with the non-sinusoidal wave generator; and
a mixer configured to mix the sinusoidal wave signal and the non-sinusoidal wave signal respectively supplied from the sinusoidal wave generator and the non-sinusoidal wave generator.

27. The substrate processing apparatus of claim **26**, wherein the sinusoidal wave signal has a frequency of about 13.56 MHz and the non-sinusoidal wave signal has a frequency from about 0.4 MHz to about 2 MHz.

28. The substrate processing apparatus of claim **26**, wherein the plasma generator is configured such that ions generated by the plasma generator have a single peak ion energy distribution.

29. The substrate processing apparatus of claim **26**, wherein the first filter is a high-pass filter (HPF) and the second filter is a low-pass filter (LPF).

30. The substrate processing apparatus of claim **26**, wherein the first filter is a band pass filter and the second filter is a band stop filter.

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