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(54) Title: USING NO-REFRESH DRAM IN ERROR CORRECTING CODE ENCODER AND DECODER IMPLEMENTATIONS

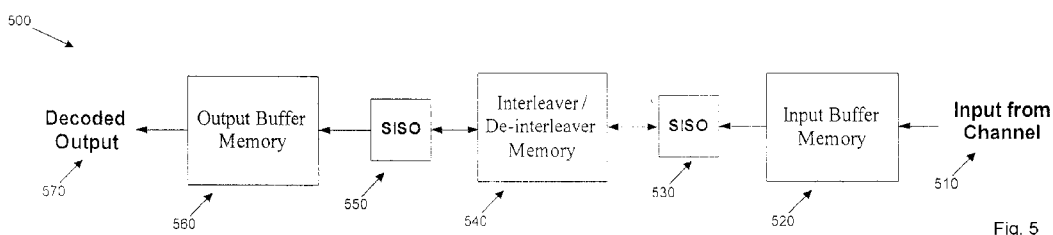


Fig. 5

(57) Abstract: Embodiments of the present invention provide Forward Error Correcting Code encoders and decoder structures that use DRAM in their memory designs. DRAM is a very attractive memory options in many electronic systems due to the high memory density provided by DRAM. However, the DRAM is typically not included in ASIC or FPGA implementations of encoders and decoders due to complex refresh requirements of DRAM that are required to maintain data stored in DRAM and may interfere with user access to the memory space during refresh cycles. Embodiments of the present invention provide FECC encoder and decoder structures that are implemented using DRAM that do not require complex refresh operations to be performed on the DRAM to ensure data integrity. Accordingly, embodiments of the present invention maximize memory density without the added complexity of introduced by the refresh requirements of DRAM.



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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 07/81434

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G11C 29/00 (2008-04)

USPC - 714/767

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 714/767Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 711/100,101,154,157; 712/1,25,27;714/746,763,767Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Electronic Databases Searched: USPTO WEST (PGPUB,USPAT,USOCR,EPAB,JPAB); GOOGLE Patents; DIALOG PRO
Search Terms Used: data block encoding/decoding/forward error correcting (FEC)/error correcting code (ECC) using volatile memory, dynamic random access memory (DRAM) refreshing, memory (de)interleaving, etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0221098 A1 (ITO et al.) 04 November 2004 (04.11.2004)	1-7, 9-17, 19-20
---	Abstract, Para [0002]-[0034],[0072]-[0253]	---
Y		8, 18
Y	US 6,163,871 B1 (YANG) 19 December 2000 (19.12.2000)	8,18
	Abstract, Col 3 Ln 33 - Col 6 Ln 10, Col 6 Ln 58 - Col 13 Ln 44	
A	US 2004/0237023 A1 (TAKAHASHI et al.) 25 November 2004 (25.11.2004)	1-20
	Entire Document	
A	US 7,065,696 B1 (LIU et al.) 20 June 2006 (20.06.2006)	1-20
	Entire Document	

 Further documents are listed in the continuation of Box C.

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

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