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(54) **LED WITH STRESS-BUFFER LAYER UNDER METALLIZATION LAYER**

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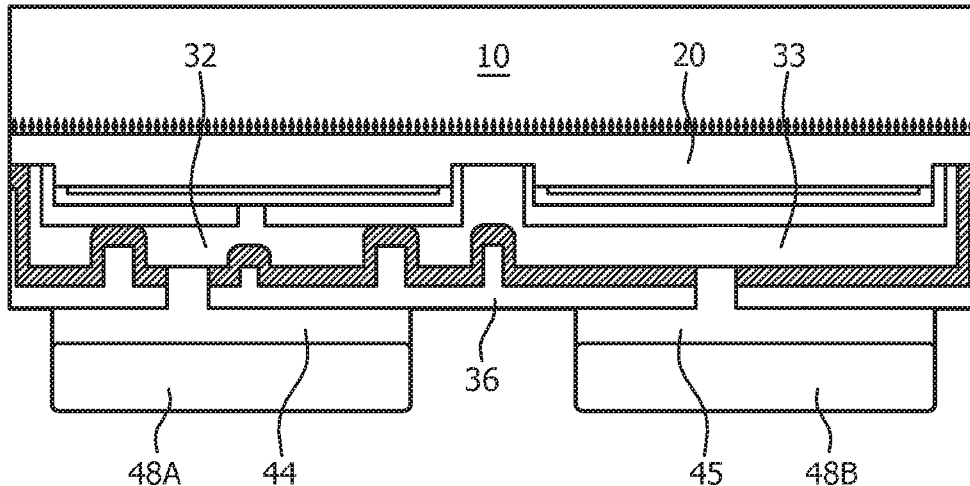
(57) **ABSTRACT**

Semiconductor LED layers are epitaxially grown on a patterned surface of a sapphire substrate. The patterned surface improves light extraction. The LED layers include a p-type layer and an n-type layer. The LED layers are etched to expose the n-type layer. One or more first metal layers are patterned to electrically contact the p-type layer and the n-type layer to form a p-metal contact and an n-metal contact. A dielectric polymer stress-buffer layer is spin-coated over the first metal layers to form a substantially planar surface over the first metal layers. The stress-buffer layer has openings exposing the p-metal contact and the n-metal contact. Metal solder pads are formed over the stress-buffer layer and electrically contact the p-metal contact and the n-metal contact through the openings in the stress-buffer layer. The stress-buffer layer acts as a buffer to accommodate differences in CTEs of the solder pads and underlying layers.



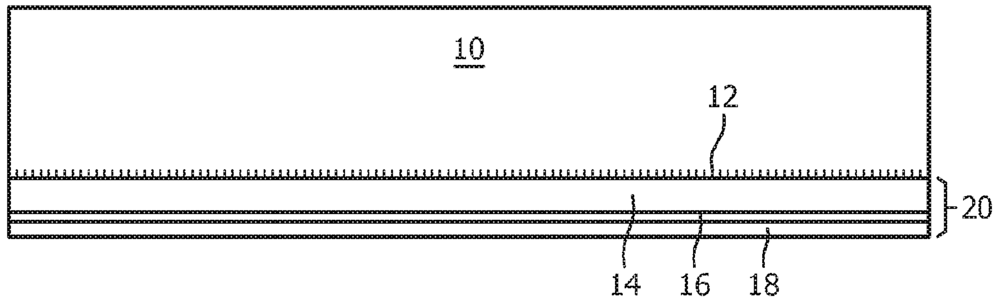


FIG. 1

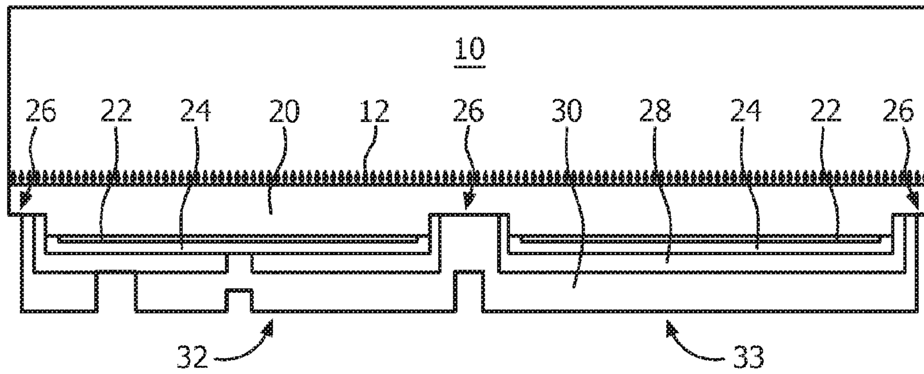


FIG. 2

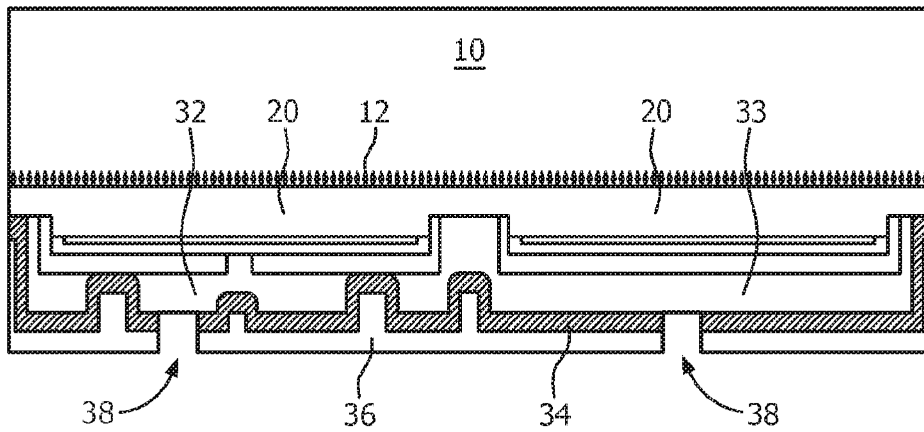


FIG. 3

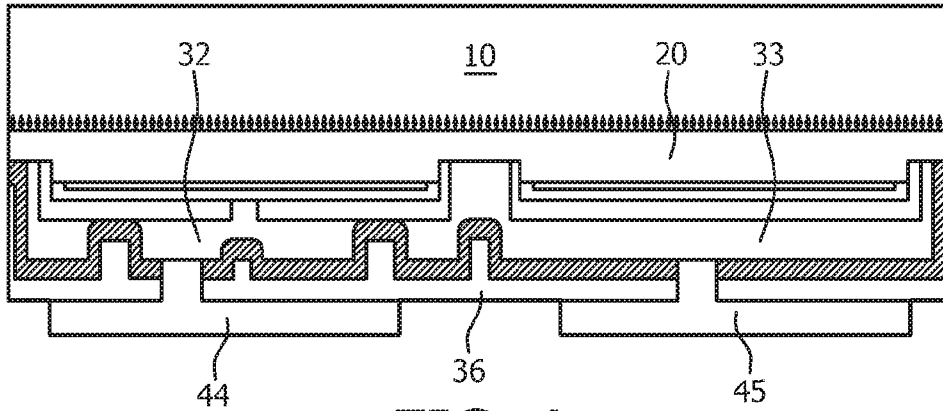


FIG. 4

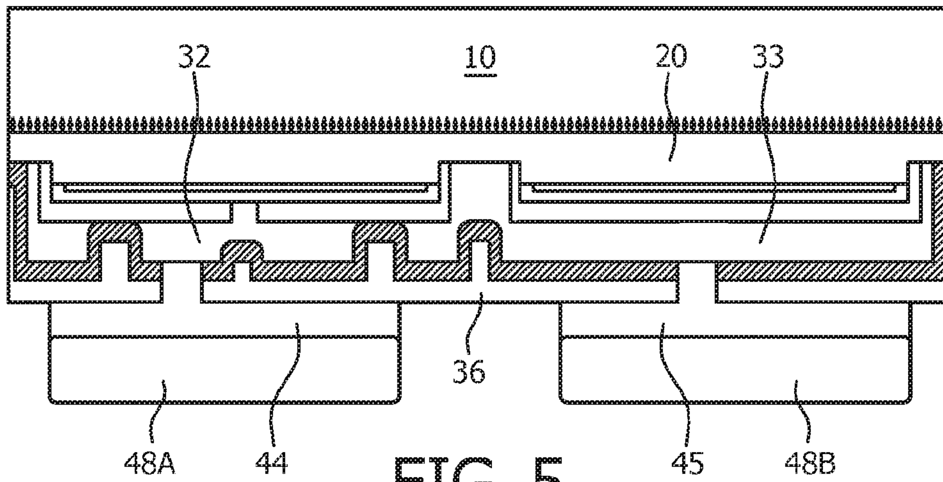


FIG. 5

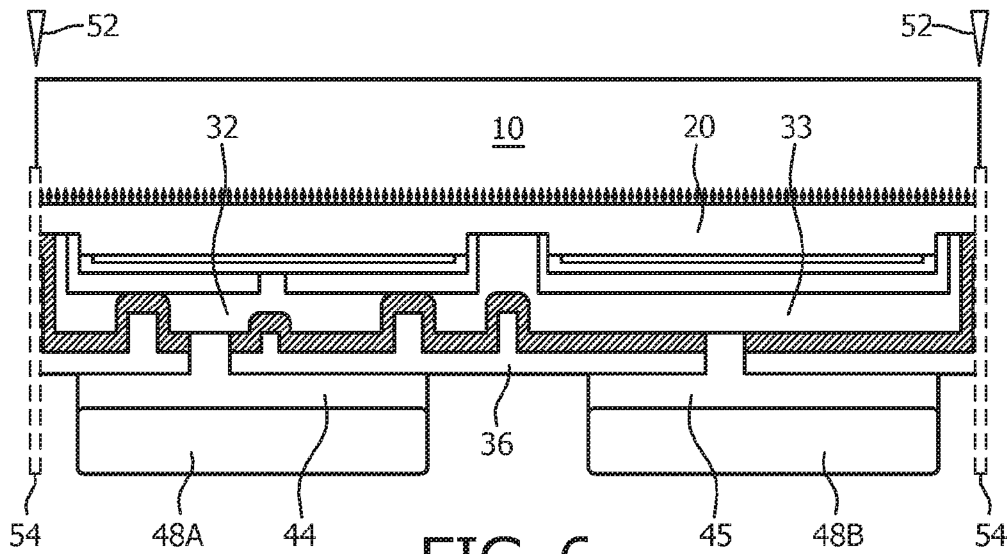


FIG. 6

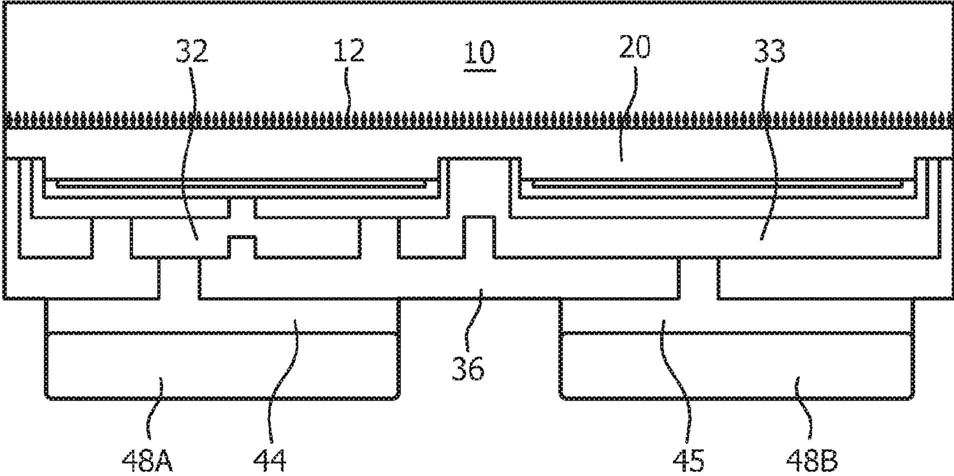


FIG. 7

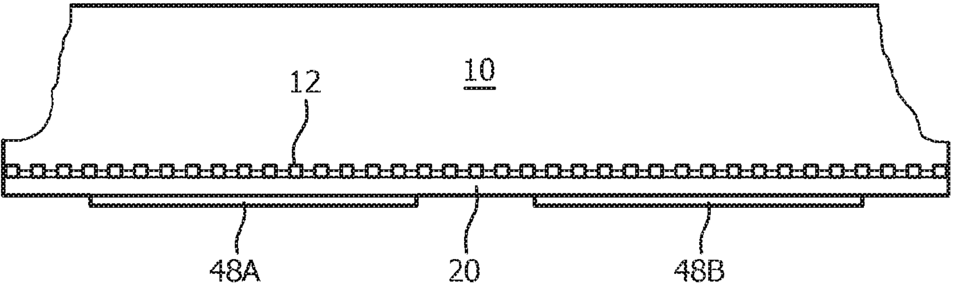


FIG. 8

LED WITH STRESS-BUFFER LAYER UNDER METALLIZATION LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is continuation of U.S. application Ser. No. 14/902,001, filed Dec. 29, 2015, issuing as U.S. Pat. No. 9,640,729 on May 2, 2017, which is a §371 application of International Application No. PCT/IB2014/062535 filed on Jun. 23, 2014 and entitled "LED with Stress-Buffer Layer Under Metallization Layer," which claims the benefit of U.S. Provisional Application Ser. No. 61/842,431, filed Jul. 3, 2013. U.S. application Ser. No. 14/902,001, International Application No. PCT/IB2014/062535, and U.S. Provisional Application No. 61/842,431 are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] This invention relates to packaging light emitting diodes (LEDs) and, in particular, to a stress buffer layer between the LED semiconductor layers and a solder pad metallization layer.

BACKGROUND

[0003] Thin-Film Flip-Chip (TFFC) LEDs have anode and cathode contacts on the bottom surface, opposite the light emitting surface. Therefore, such TFFC LEDs utilize the whole top die area surface for light output, since top-side (light-output side) metallization for a wire-bond is not necessary. However, with TFFC LEDs, die-level processes, including sapphire substrate lift-off (for GaN based LEDs) and epitaxial layer (EPI) roughening (to improve light extraction), are typically used, which significantly increase the packaging cost. It would be beneficial to not require the sapphire substrate to be removed, while still achieving good light output extraction.

[0004] Traditional TFFC LEDs have a rigid dielectric layer formed on the LED semiconductor layers that exposes portions of the p and n-type semiconductor layers. Then, a relatively thin, patterned metal layer (or layers) is deposited over the dielectric layer to directly contact the p and n-type semiconductor layers to create an ohmic contact between the metal and the p and n-type semiconductor layers. Much thicker metal pads (also comprising various metal layers) are then formed over the thin ohmic-contact metal layer(s), such as by plating, for use as the LED's solder pads for mounting the LED to a printed circuit board or other substrate. Solder bumps may then be deposited on the solder pads.

[0005] A problem with such traditional TFFC LEDs and processes is that there are stresses between the semiconductor layers, thin metal layer(s), and thick pad layers, such as due to mismatched coefficients of thermal expansion (CTE). Therefore, heat cycling of the LEDs, such as during operation or processing, creates stress that may cause the metal layers to delaminate from each other and from the semiconductor layers, or cause cracking of brittle layers at stress concentration points, which may cause failure. It would be beneficial to provide a technique to reduce such stress to increase the reliability of the LEDs.

[0006] Another problem with traditional TFFC LEDs and processes is that the surface on which the thick solder pads is formed is not planar. Therefore, it is difficult to obtain flat solder pads of uniform thickness. Flat solder pads with uniform thickness are beneficial for electrical and thermal conduction between the LED and the printed circuit board or other substrate. It would be beneficial to provide a technique to planarize the "bottom" surface of the LED structure prior to depositing (e.g., plating) the solder pads.

SUMMARY

[0007] One embodiment of the present invention solves all the above problems by using a wafer-level-chip-scale-package (WLCSP) process that patterns the sapphire substrate for improved light extraction and forms a stress-buffer layer between the thick metal solder pads and the thin metal that ohmically contacts the semiconductor layers. The stress-buffer layer also planarizes the bottom surface of the LED prior to the thick solder pads being formed. This helps create flatter and more uniform solder pads for improved electrical and thermal conductivity. By keeping the sapphire substrate as part of the packaged LED, there is a beneficial rigid mechanical support for the thin LED layers in the final package. The cost of removing the substrate is also avoided.

[0008] The wafer-level processes described herein reduce the total fabrication cost of device, improve reliability, and maintain the best over-all performance electrically, thermally, and optically.

BRIEF DESCRIPTION OF DRAWINGS

[0009] FIG. **1** is a cross-sectional view of a portion of a patterned sapphire substrate having LED layers epitaxially grown over the patterned surface.

[0010] FIG. **2** illustrates distributed metal contacts making ohmic contact to the p and n-type LED layers.

[0011] FIG. **3** illustrates a planar stress-buffer layer deposited over the distributed metal contacts and patterned to expose portions of the distributed metal contacts. An optional passivation layer is also shown between the stress-buffer layer and the distributed metal contacts for creating a seal and blocking migration of metal atoms from the subsequently formed metal solder pads.

[0012] FIG. **4** illustrates relatively thick metal solder pads plated over the planar stress-buffer layer and exposed portions of the distributed metal contacts.

[0013] FIG. **5** illustrates solder bumps deposited on the metal solder pads.

[0014] FIG. **6** illustrates the substrate being singulated by laser scribing and breaking.

[0015] FIG. **7** illustrates a single LED after being singulated using the singulation method of FIG. **6**. The optional passivation layer is eliminated in FIG. **7**.

[0016] FIG. **8** illustrates a single LED, with the metal layers simplified, after being singulated using a combination of mechanical sawing (for the sapphire substrate) and scribing and breaking (for the LED layers), resulting in the edges of the substrate being roughened and the substrate narrowed.

[0017] Elements that are the same or similar are labeled with the same numeral.

DETAILED DESCRIPTION

[0018] FIGS. **1-8** illustrate a wafer-level process flow in accordance with one embodiment of the invention. Only a single LED area on a much larger wafer is shown for simplicity. Each step shown for an illustrated LED area is applied to all of the LED areas on the large wafer.

[0019] With reference to FIG. **1**, the process flow to create a wafer of LEDs starts with a patterned sapphire substrate (PSS) **10**. The substrate **10** will typically have a disc shape and be substantially transparent to the light emitted by the LED. One surface **12** is roughened (patterned) such as by grinding, "sand" blasting, chemical etching, plasma etching, or other roughening process. The roughening improves light extraction by reducing total internal reflection (TIR). The substrate **10** surface **12** may be patterned in any orderly or random fashion to improve light extraction.

[0020] Roughening the semiconductor layer light emitting surface of a conventional flip-chip LED, after removal of the sapphire substrate, is commonly performed. In contrast, the present process retains the sapphire substrate and roughens its growth surface.

[0021] In one embodiment, conventional GaN-based semiconductor LED layers are then epitaxially grown over the roughened surface **12** of the substrate **10**. In one embodiment, n-type layers **14** are grown over the surface **12**, followed by an active layer **16** and p-type layers **18**. In one embodiment, the active layer **16** produces blue light when the LED is energized.

[0022] For simplicity, the various semiconductor LED layers are shown as a single LED layer **20** in the remaining figures.

[0023] In FIG. **2**, a standard process flow is performed to form the thin metal ohmic contacts. A thin reflective metal layer **22**, such as silver, nickel, or an alloy, or multiple layers, is deposited on the surface of the p-type layer, such as by sputtering, and patterned. The metal layer **22**, after annealing, creates an ohmic contact with the p-type layer.

[0024] A metal layer **24** of titanium, tungsten, or any alloy is then deposited over the metal layer **22** and patterned. The metal layer **24** improves adhesion to a subsequent metal layer. The layer **24** may also serve as a barrier layer to block the migration of atoms across layers. The metal layer **24** may be referred to as an interface layer. The thickness of the combination of metal layers **22** and **24** will typically be less than one micron.

[0025] The LED layer **20** is etched at locations **26** to remove portions of the p-type layers and active layer to expose the n-type layer.

[0026] A dielectric layer **28** is then deposited over the surface and into the openings at locations **26**. Dielectric layer **28** is then patterned to expose portions of the metal layer **24** and to expose the n-type layers at locations **26**.

[0027] A thicker metal layer **30**, such as aluminum, nickel, a titanium-tungsten alloy, copper, gold, or alloys, is then deposited over the dielectric layer **28** and into the openings to ohmically contact the p-type layers and n-type layers. The metal layer **20** may be stacked layers. The metal layer **30** is then patterned to separate the p-metal contacts **32** from the n-metal contacts **33**. The metal layer **30** may be a few microns thick.

[0028] The above metallization process may be conventional so further details are not required for one skilled in the art.

[0029] The metal connections to the p-type layers and n-type layers can be distributed over the entire LED area to more uniformly distribute the current across the LED. This will provide a substantially uniform light emission from the top surface of the LED.

[0030] The resulting metal layer **30** is not planar due to the metal layer **30** filling the openings and being etched. If the metal layer **30** were plated to form the metal solder pads, the solder pads would not be planar and uniformly thick. It is desirable to provide planar and uniformly thick solder pads for good electrical and thermal conductivity.

[0031] In FIG. **3**, an optional thin passivation layer **34**, such as PECVD SiNx, is deposited to block aluminum atom migration into the semiconductor layers from a subsequently formed solder pad. Depending on the metals used for the layers **22**, **24**, and **30** and the solder pads, the passivation layer **34** may not be needed. The passivation layer **34** may also be used for hermetic sealing against any moisture or harsh/corrosive environment. A typical thickness of the passivation layer **34** may be 0.5-1.5 um, and preferably 0.8-1.2 um. SiNx is a known barrier layer for moisture, while SiOx (or SiO2) or a SiOx/SiNx mixture may also be used.

[0032] Since the passivation layer **34** is formed by a PECVD process, it will be fairly uniform over the non-planar surface, so its surface will not be planar.

[0033] Next, in FIG. **3**, a stress-buffer-layer (SBL) **36**, such as BenzoCycloButene (BCB), is coated onto the surface (e.g., by spin-on coating). The SBL **36** is a dielectric polymer deposited as a liquid. Therefore, the deposition process forms a planar layer of the SBL **36**. Deposition by evaporation may also be used. In one embodiment, the thickness of the SBL layer **36** is 1-3 um.

[0034] Before the SBL **36** is cured by heating, the SBL **36** is masked, exposed, and developed to form one or more via openings **38**, which exposes the passivation layer **34**. Photo-BCB is commercially available and has the properties of a photoresist. The SBL **36** is then cured. A passivation layer **34** etch is performed by using the SBL **38** as a masking layer. This exposes the p-metal contact **32** and the n-metal contact **33**.

[0035] The typical thermal conductivity of suitable SBL **36** materials, such as BCB, PBO: polybenzoxazole, or PI: polyimide, is about 0.3 W/m.K. Since the SBL **36** is thin, this is sufficient for very good thermal conductivity for a 1 mm^2 die size. A typical SBL **36** thickness after cure and passivation etch should be a minimum of ~1 um to provide adequate step coverage, which is enough for electrical breakdown strength.

[0036] Note that the etch step to etch into the LED layers **20** also creates a trench surrounding each LED area that is at least partially filled with the SBL **36** and passivation layer **34** for added protection/sealing of the LED.

[0037] In FIG. **4**, a metal redistribution layer (RDL) is deposited that is patterned to form solder pads **44** and **45** electrically connected to the p-type and n-type LED layers **20**. This can be done by a plating-through-photoresist approach as follows. First, a seed metal layer stack (e.g., TiW/Cu 1000/2000 Angstroms thick) is deposited such as by sputtering or evaporation, followed by lithography (photoresist coating, exposure, and development of photoresist) to expose only those areas to be plated. The exposed RDL stack is then electro-plated, such as with Cu/Ni/Au to a thickness of 2-20 um/2 um/0.3 um. The photoresist is stripped, followed by etching the exposed seed metal stack, resulting in the structure of FIG. **4**. The Ni is used as a solder barrier layer and the Au is used as a solder wetting layer. Plating is a well know process for forming thick solder pads.

[0038] Alternatively, the RDL can be deposited and patterned using a patterned etch or lift-off approach, with added material/process cost.

[0039] By providing the SBL **36**, the surface is planarized so that the resulting solder pads **44/45** are fairly flat and uniformly thick to evenly spread heat. Providing flat and uniformly thick solder pads **44/45** improves the electrical and thermal conductivity from the LED layers **20** to the heat sink/substrate that the LED will be ultimately mounted on for operation. At this stage, the wafer can be tested.

[0040] The use of the stress-butter (SBL) **36** relieves stress between the solder pads **44/45** and the underlying layers caused by different CTEs of the materials, reducing the possibility of delamination and reducing the possibility of cracking of brittle layers (e.g. layer **20**) at stress concentration points, which may cause failure. For example, the solder pads **44/45** may expand at a different rate than the underlying material and may either shift with respect to the SBL **36** or deform the SBL **36**. However, even with such different CTEs, the contact points between the solder pads **44/45** and the p-metal contact **32** and n-metal contact **33** are not broken since the stress has been relieved by the SBL **36**. If the SBL **36** was not planar (flat and smooth), the lateral adhesion of the solder pads **44/45** to the SBL **36** would be much greater, reducing the effectiveness of the SBL **36**. For some SBL **36** materials, such as BCB, the SBL **36** may be hard cured or soft cured to retain a target elasticity so as to deform without delaminating from the solder pads **44/45** in the event of different expansions of the materials. The polymer SBL **36** will typically be more elastic than a non-polymer silicon dioxide oxide layer or a silicon nitride layer typically used as a dielectric.

[0041] As previously mentioned, the SBL **36** also improves the quality of the solder pads **44/45** by providing a planarized surface, and the SBL **36** also adds a barrier layer for reducing contamination. The SBL **36** is very thin and is a fairly good conductor of heat, so thermal conduction between the LED and the heat sink is not significantly reduced by the SBL **36**.

[0042] An optimized design or layout provides optimized thermal performance. For instance, a very good thermal resistance Rth from the metal/semiconductor junction to the solder bumps **48**A and **48**B (FIG. **5**) of 2K/W has been achieved for a 1 mm^2 die.

[0043] As shown in FIG. **5**, solder bumps **48**A and **48**B may then be deposited on the solder pads **44** and **45** using conventional techniques. Wafer-level solder bumping can be performed by an electroplating or PVD process with a patterned etch, or performed using a deposition and lift-off technique, or performed using screen printing, or performed using solder balls and a pick and place technique, or performed using any other standard bumping process. Such techniques are well known and do not need to be described in detail. Therefore, the solder bumps **48**A and **48**B may be flat or rounded. In order to reduce die-attach height, improve thermal conductivity, and achieve lower cost if AuSn or other expensive eutectic solder materials are used, the solder bumps **48**A and **48**B should be thin and uniformly coat the solder pads **44/45**. The thickness range of the solder bumps **48**A and **48**B can be 1-100 um, and preferably 5-10 um. The solder bumps **48**A and **48**B may be Au, AuSn, or any other suitable metal or alloy.

[0044] The sapphire substrate **10** may be thinned at this stage and provided with a desired surface texture, such as by grinding and/or blasting, to reduce the LED height and improve light output. The target substrate **10** thickness can vary depending upon die size, such as from 10 to 1000 um, and preferably 200-400 um. The suitability of thicknesses of 100-400 um has been successfully demonstrated using a conventional back-grinding procedure (wafer mounted on a tape film or a frame) without the need for a wafer support system. However, for a target sapphire thickness of less than 100 um, a wafer-support system may be needed to avoid breakage/cracking during grinding.

[0045] Finally, as shown in FIG. **6**, the wafer is singulated into individual LEDs (dice). This has been conducted by laser scribe and break for sapphire thicknesses of 80-300 with die sizes of 0.7-1.4 mm in side-length with excellent scribe and break yield loss of <<0.5%. The laser scribe of the substrate **10** is represented by the blades **52**, and the break lines are represented by the dashed lines **54**. The edges of the singulated LEDs are relatively precise and vertical.

[0046] By retaining the sapphire substrate **10** on the final LED, processing cost is saved by not having to remove the substrate **10**. Yield is also increased.

[0047] In case a much thicker (e.g., >400 um) sapphire substrate **10** is needed, a combination of mechanical sawing and laser scribe and break works well, but at a reduced throughput due to the slow sawing speed (typically ~1 mm/s for minimized chipping).

[0048] FIG. **7** illustrates the singulated LED without the optional passivation layer **34** (compare with FIG. **3**).

[0049] FIG. **8** illustrates a simplified LED after being singulated by a combination of mechanical sawing of the substrate **10** and laser scribe and break of the LED layer **20**. As a result, the sapphire side of the die is narrowed on each side (by half the width of the saw blade) so that the LED layer **20** extends beyond the substrate **10**. This may be advantageous if the substrate **10** (the light emitting surface) is later coated with a phosphor since the sides will be coated. Also, the rough edges of the substrate **10** may improve light extraction.

[0050] In one embodiment, the singulated LEDs are mounted on a submount wafer by bonding the LED solder pads to pads on the top surface of the submount wafer. A pick and place machine positions the LEDs on the submount, followed by a heating step or an ultrasonic bonding step to bond the LED solder pads to the submount pads. The LEDs are then further processed on a wafer scale, such as being individually encapsulated by a molded silicone lens and/or covered with a phosphor (before or after encapsulation by the lens). The lens material itself may also be infused with phosphor powder. The phosphor may, for example, convert the blue LED light to white light. The submount wafer is then singulated. The submount has robust solder pads on its bottom surface that are electrically connected with vias to the LED solder pads. Alternatively, the LEDs may be directly mounted on printed circuit boards.

[0051] A final cumulative yield after die-attach, phosphor deposition, and dome-lens build has been >99%.

[0052] While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.

1-10. (canceled)

11. A light-emitting device comprising:

a light-emitting semiconductor structure including a first layer, a second layer, and a third layer, the second layer

being disposed between the first layer and the third layer, and the third layer being exposed through an etch that is formed in the first layer and the second layer;

a first non-planar metal layer that is electrically coupled to the first layer;

a second non-planar metal layer that is electrically coupled to the third layer;

a stress-buffer layer that is formed of a dielectric polymer, the stress-buffer layer being disposed over the first metal layer and the second metal layer to form a substantially planar surface, the stress-buffer layer being arranged to at least partially fill a trench formed in a periphery of the semiconductor structure that surrounds a central portion of the semiconductor structure; and

a plurality of metal solder pads disposed over the stress-buffer layer, each of the metal solder pads being electrically connected to one of the first metal layer and the second metal layer through a respective opening formed in the stress-buffer layer.

12. The light-emitting of claim **11**, wherein the stress-buffer layer is elastic so as to deform when the metal solder pads expand at a different rate of thermal expansion than their underlying materials.

13. The light-emitting of claim **11**, wherein the stress-buffer layer comprises BenzoCycloButene (BCB).

14. The light-emitting of claim **11**, wherein the first layer includes a p-type layer, the second layer includes an active layer, and the third layer includes an n-type layer.

15. The light-emitting device of claim **11**, further comprising:

a metal contact layer electrically contacting the first layer; and

a dielectric layer formed over the metal contact layer, the dielectric layer including a first opening arranged to expose the metal contact layer, and a second opening arranged to expose the third layer,

wherein the first non-planar metal layer is coupled to the metal contact layer through the first opening, and

wherein the second non-planar metal layer is coupled to the third layer through the second opening.

16. The light-emitting device of claim **15**, further comprising a passivation layer formed between the stress-buffer layer and the metal contact layer.

17. The light-emitting device of claim **15**, wherein the metal contact layer includes a contact sub-layer coupled to the first layer and an interface sub-layer formed between the contact sub-layer and the solder pads.

18. A light-emitting device comprising:

a light-emitting semiconductor structure including a first layer, a second layer, and a third layer, the second layer being disposed between the first layer and the third layer, and the third layer being exposed through an etch that is formed in the first layer and the second layer;

a first non-planar metal layer arranged to electrically contact the first layer;

a second non-planar metal layer arranged to electrically contact the third layer;

a stress-buffer layer that is formed of a dielectric polymer, the stress-buffer layer being disposed over the first metal layer and the second metal layer to form a surface including at least two openings; and

a plurality of metal solder pads disposed over the stress-buffer layer, each of the metal solder pads being electrically connected to one of the first metal layer and the second metal layer through a respective one of the openings in the surface of the stress-buffer layer.

19. The light-emitting device of claim **18**, wherein the stress-buffer layer is elastic so as to deform when the metal solder pads expand at different rates of thermal expansion than their underlying materials.

20. The light-emitting device of claim **18**, wherein the stress-buffer layer comprises BenzoCycloButene (BCB).

21. The light-emitting device of claim **18**, wherein the first layer includes a p-type layer, the second layer includes an active layer, and the third layer includes an n-type layer.

22. The light-emitting device of claim **18**, wherein the stress-buffer is arranged to fill a trench formed in a periphery of the semiconductor structure that surrounds a central portion of the semiconductor structure.

23. The light-emitting device of claim **18**, further comprising a metal contact layer arranged to electrically contact the first layer.

24. The light-emitting device of claim **23**, further comprising a dielectric layer formed over the metal contact layer, the dielectric layer including a first opening arranged to expose the metal contact layer, and a second opening arranged to expose the third layer, wherein the first non-planar metal layer is arranged to contact the metal contact layer through the first opening in the dielectric layer, and the second non-planar metal layer is arranged to contact the third layer through the second opening in the dielectric layer.

25. A light-emitting device comprising:

a light-emitting semiconductor structure including a first layer, a second layer, and a third layer, the second layer being disposed between the first layer and the third layer, and the third layer being exposed through an etch that is formed in the first layer and the second layer;

a metal contact layer electrically contacting the first layer;

a dielectric layer formed over the metal contact layer, the dielectric layer having a first opening that exposes the metal contact layer and a second opening that exposes the third layer;

a first non-planar metal layer that contacts the metal contact layer through the first opening in the dielectric layer;

a second non-planar metal layer that contacts the third layer through the second opening in the dielectric layer;

a stress-buffer layer formed of a dielectric polymer and disposed over the first metal layer and the second metal layer, the stress-buffer layer forming a substantially planar surface having two or more openings exposing respective portions of the first metal layer and the second metal layer, the stress-buffer layer being arranged to at least partially fill a trench formed in a periphery of the semiconductor structure that surrounds a central portion of the semiconductor structure; and

a plurality of metal solder pads disposed over the stress-buffer layer, each of the metal solder pads being electrically connected to one of the first metal layer and the second metal layer through a respective one of the openings in the stress-buffer layer.

26. The light-emitting of claim **25**, wherein the stress-buffer layer is elastic so as to deform when the metal solder pads expand at a different rate of thermal expansion than their underlying materials.

27. The light-emitting of claim **25**, wherein the stress-buffer layer comprises BenzoCycloButene (BCB).

28. The light-emitting of claim **25**, wherein the first layer includes a p-type layer, the second layer includes an active layer, and the third layer includes an n-type layer.

29. The light-emitting device of claim **28**, further comprising a passivation layer formed between the stress-buffer layer and the metal contact layer.

30. The light-emitting device of claim **28**, wherein the metal contact layer includes a contact sub-layer coupled to the first layer and an interface sub-layer formed between the contact sub-layer and the solder pads.

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