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(54) **Title**: DOUBLE BROKEN SEAL RING

FIG. 1A

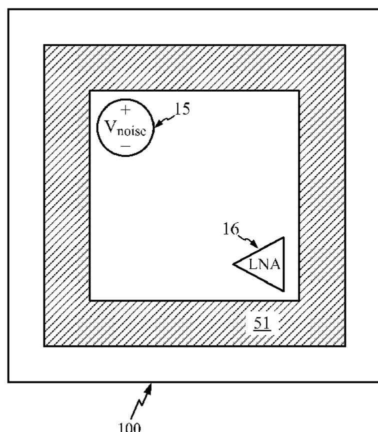
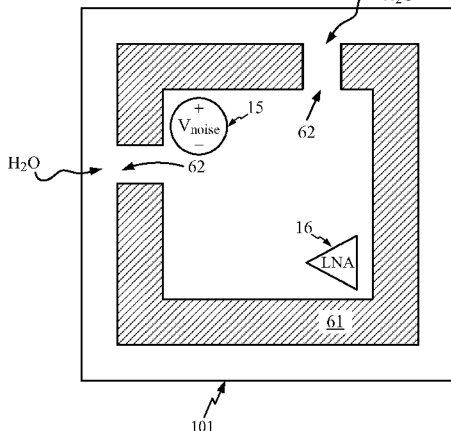


FIG. 1B



(57) **Abstract**: The amount of signal propagation and moisture penetration and corresponding reliability problems due to moisture penetration degradation in an IC can be reduced by fabricating two seal rings with non-adjacent gaps. In one embodiment, the same effect can be achieved by fabricating a wide seal ring with a channel having offset ingress and egress portions. Either of these embodiments can also have grounded seal ring segments which further reduce signal propagation.

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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DOUBLE BROKEN SEAL RING

TECHNICAL FIELD

[0001] The present disclosure generally relates to integrated circuits (ICs). More specifically, this disclosure relates to seal rings configurations to reduce signal propagation and to reduce moisture penetration.

BACKGROUND

[0002] Seal rings, which are rings composed of metals such as copper, aluminum, or gold, are fabricated around the perimeter of ICs to prevent IC cracking during the dicing process. An additional benefit in using a seal ring is that it serves as a barrier to moisture. That is, over time, as the IC is exposed to moisture, the IC performance may degrade without the use of a seal ring.

[0003] However, use of these seal rings also has disadvantages, including unwanted noise/signal propagation. Many times, a noise source, such as a digital signal input/output pad, clock input pad, power amplifier, etc., located on the IC causes noise to propagate along the seal ring, which subsequently can interfere with the operation of other devices on the IC. This is problematic because the devices on the IC are not then isolated from each other as may otherwise be intended and designed.

[0004] Conventionally, seal rings have taken two forms. First, single seal rings have been used that are composed of one solid piece of metal. The substrate below the seal ring is usually doped and then connected with vias to the bottom of the metal to make the best substrate connection to the metal seal ring. This helps reduce moisture contamination of the IC, but However, this type of ring allows for noise signals to propagate from a noise source along the seal ring to other devices on the IC.

[0005] To alleviate this noise propagation issue, a single seal ring has been used which incorporates several “breaks,” or intermittent interruptions. This helps to reduce the noise propagation problem, but poses a risk to reliability because moisture can enter the IC through these breaks in the seal ring and degrade the device performance over time.

BRIEF SUMMARY

[0006] The present disclosure is directed to a method of fabricating a broken seal ring that will reduce noise propagation by breaking the seal ring conduction path while also minimizing the amount of moisture penetrating the IC.

[0007] Specifically, the present disclosure is directed to a sealing system for an integrated circuit, where a first seal ring circumscribes the integrated circuit, and has at least one gap. A second seal ring circumscribes the first seal ring and has at least one gap offset from the gap of the first seal ring.

[0008] The present disclosure is further directed to a sealing system for an integrated circuit that contains a seal ring circumscribing the integrated circuit with at least one channel. The channel includes an ingress portion and an egress portion. The ingress portion is offset from the egress portion.

[0009] The present disclosure is further directed to an integrated circuit with a sealing system, where a first seal ring circumscribes the integrated circuit, and has at least one gap. A second seal ring circumscribes the first seal ring.

[0010] The present disclosure is further directed to a method for forming a sealing system for an integrated circuit by forming a first seal ring circumscribing the integrated circuit. The first seal ring includes at least one gap. The method also includes forming a second seal ring circumscribing the first seal ring, where the second seal ring includes at least one gap offset from the gap of the first seal ring.

[0011] The foregoing has outlined rather broadly the features and technical advantages of the present disclosure in order that the detailed description of the disclosure that follows may be better understood. Additional features and advantages of the disclosure will be described hereinafter which form the subject of the claims of the disclosure. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the disclosure as set forth in the appended claims. The novel features which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly

understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGURES 1A and 1B are schematic drawings of an IC device with conventional seal rings.

[0013] FIGURE 2 is a schematic diagram of an exemplary dual broken seal ring.

[0014] FIGURES 3A and 3B are schematic diagrams of alternate configurations of a dual broken seal ring.

[0015] FIGURE 4 is a schematic diagram of an alternate embodiment of a dual broken seal ring.

[0016] FIGURE 5 is a schematic diagram showing a wireless communication system in which an embodiment of the disclosure may be advantageously employed.

DETAILED DESCRIPTION

[0017] FIGURE 1A is a schematic drawing of an IC 100, such as a radio frequency (RF) IC, with a conventional seal ring 51. The seal ring 51 has no breaks or interruptions. As discussed above, a signal produced by a noise source 15 may propagate along the seal ring 51 and interfere with the performance of other devices on the IC. For example, the IC 100 includes a low noise amplifier (LNA) 16, which is a device that is susceptible to the effects of noise. Because the LNA 16 is susceptible to noise, it has been located as far away on the IC 100 from the noise source 15 as possible. However, those having skill in the art would understand the LNA 16 will nevertheless be subject to the adverse effects of noise created by the noise source 15 due to propagation of noise through the seal ring 51.

[0018] FIGURE 1B is a schematic drawing of an IC 101 with a different conventional seal ring 61. As discussed above, the seal ring 61 incorporates breaks, or openings, 62 in the seal ring 61. Such openings 62 may be created during the fabrication process to reduce noise created by the noise source 15 from propagating through the seal ring 61 to the LNA 16. However, while the seal ring 61 has improved

noise propagation characteristics as compared with the seal ring 51, the IC 101 is more susceptible to moisture (as illustrated by H_2O in FIGURE 1B) penetration through the openings 62.

[0019] FIGURE 2 is a schematic drawing of an IC 10 that includes a dual broken seal ring. The IC 10 includes two seal rings: an outer ring 11 circumscribing an inner ring 12. Noise coupling between inner and outer seal rings 11, 12 can be reduced in several ways. For example, it is possible to block doping of the substrate between these two seal rings 11, 12, creating a highly resistive path through the substrate.. Another option is to block doping of the substrate within each seal break, creating a highly resistive path through the substrate. Alternatively or in addition, it is possible to place ground connections on segments of each seal ring to reduce noisy currents or signals. If the number of ground connects are limited, one embodiment connects grounds to all segments of the inner seal ring 12.

[0020] In one embodiment, the substrate is a semiconductor, such as silicon. In another embodiment, the substrate is a ceramic. For convenience, the substrate will be referred to as silicon, although other substrates (such as Galium-Arsinide) are contemplated.

[0021] It is noted that the outer seal ring 11 circumscribes the inner seal ring 12 by overlapping with portions of the inner seal ring 12 to reduce moisture penetration. As can be seen in FIGURE 2, the outer ring 11 has an opening 13 and the inner ring 12 has an opening 14. The openings 13 and 14 are not aligned with one another and are, in fact, offset from each other. This offset is better illustrated by FIGURE 3A. The offset between the openings 13 and 14 reduces the possibility of moisture from the atmosphere penetrating into the IC 10. As shown in FIGURE 2, while moisture (illustrated by H_2O) may be able to penetrate through the opening 13 the moisture does not immediately penetrate into the IC 10 which could damage components, such as the transistors 17, in the IC 10. The moisture is blocked by the inner seal ring 12.

[0022] The openings 13 and 14 may be fabricated anywhere along the perimeter of the outer ring 11 and the inner ring 12 . In one embodiment, the openings 13 and 14 include a separation staggered about 100um (or more),to reduce the likelihood of moisture penetration into the IC 10. One purpose of the openings 13 and 14 is to stop noise conduction along the perimeter. In one embodiment, the openings

are cut through the metal layers as well as the substrate layers of each seal ring 11 and 12. An exemplary width for the openings 13, 14 is 20um to 50um.

[0023] Although FIGURE 2 illustrates three openings on the outer seal ring 11 and three openings on the inner seal ring 12, additional openings may be added to each ring. Moreover, each seal ring 11 and 12 may only have a single opening. In one embodiment, the outer seal ring 11 has no openings, while the inner seal ring 12 has openings. Additionally, the inner ring 12 may include more openings than the outer ring 11 to reduce noise propagation in the IC 10 while still increasing moisture resistance. Furthermore, multiple openings may be added to the inner ring 12 in the general vicinity of devices on the IC 10 that are particularly susceptible to noise (e.g., the LNA 16). When the inner ring 12 includes multiple openings, the outer ring 11 is preferably positioned such that the opening 13 is offset from the nearest openings on the inner ring 12.

[0024] In one embodiment, openings 14 are provided in the inner seal ring in the vicinity of (or on each side of) a noise producing element 15 or noise sensitive component (e.g., an LNA 16). The seal ring segment is then provided with a dedicated ground (FIGURE 4). Although not shown in the FIGURES, the LNA 16 could be provided in the lower left (as opposed to the lower right as depicted in FIGURE 2). In this case, the L-shaped seal ring segment would have a dedicated ground.

[0025] In another embodiment, only a single opening is provided on the seal ring in the vicinity of the noise producing/sensitive component. In this case, the opening interrupts the shortest path between the noise producing element and the noise sensitive element.

[0026] Staggering the gaps increases the mean path moisture travels to penetrate into the IC and causes a large percentage of moisture to stay between the double seal rings. A single seal ring with a single cut, would allow a hair line crack to create a moisture path directly from the outside to the inside of the IC. Staggered cuts on a double seal ring make it difficult for a continuous hairline crack to develop from outside to inside.

[0027] In one embodiment, the substrate (e.g., silicon) beneath the openings 13, 14 can be heavily doped. To make the openings 13, 14 as resistive to noise as possible, the silicon doping is typically blocked. The resistivity to noise within each

gap 13, 14 is therefore increased by changing the doping profile or blocking it altogether within the substrate under the gap 13, 14 so that signal propagation across the gaps 13, 14 is reduced.

[0028] In another embodiment, a dielectric is provided above the substrate inside the openings 13, 14. In yet another embodiment, a region which contains the electrical circuits is also filled with dielectric up to the height of the top metal of the inner seal ring 12. An outer region also can be provided with a dielectric. This outer region occurs when there is some space on the substrate between the outer metal ring 11 and the substrate edge.

[0029] FIGURE 3B illustrates an alternate embodiment. As can be seen, it is possible to achieve moisture reduction and reduced noise propagation by fabricating a single wide seal ring 20 and then fabricating a channel 23 through the wide seal ring 20. The ingress and egress portions of this channel 23 are offset from each other. Preferably, the ingress and egress portions of the channel 23 are separated by at least 100 um to about 200 um. More generally speaking, the offset is smaller than the circuit block size. The configuration illustrated in FIGURE 3B makes it difficult for moisture to penetrate into the IC, similar to the configuration shown in FIGURE 3A.

[0030] Forming the channel 23 also reduces noise propagation because the wide seal ring 20 is broken into two parts, 21 and 22. The gap between the seal ring is much more resistant to noise current/signal than the metal of the seal ring 20. In one embodiment, the silicon beneath the channel is doped to the same resistivity as under the seal ring. For example, a p+ dopant can be added to the channel, which is the same dopant as under the seal ring. The channel can be aproximately 200 um to 300 um to avoid moisture issues. The longer the channel 23, the more resistant to moisture; however less noise blocking results with longer dimensions. To make the opening as resistive as possible to noise signal transmission, silicon doping can be reduced or completely blocked.

[0031] FIGURE 4 illustrates another embodiment that can be used with either the parallel seal ring embodiment illustrated in FIGURE 3A or the wide seal ring embodiment illustrated in FIGURE 3B. FIGURE 4 shows two parallel seal rings 11, 12 with non-adjacent openings. However, the device of FIGURE 4 also incorporates pads 41 and 42 connecting to each portion of the broken inner seal ring 12. The pads 41 and 42 can be connected to a ground either outside of the package, on the board or through a

pin originating from the IC 401. The pads 41, 42 allows portions of the seal ring 12 to be grounded and therefore further reduce noise propagation. Alternatively, a pad may be added to only a single portion of the broken seal ring, or, in a two ring embodiment, a pad may be added to only one of the rings. It is beneficial to utilize as much grounding as possible. In one embodiment, ground pads are located very close to the seal ring. In another embodiment, a grounding pad is located on both sides of the broken seal ring segment. For example, by forming a segment proximate to the LNA 16 with breaks on both sides of the LNA 16, a grounding pad could be added to the seal ring on both sides of this LNA 16. However, when grounding is very limited, one ground can be applied to only the critical segments.

[0032] FIG. 5 shows an exemplary wireless communication system 500 in which an embodiment of the disclosure may be advantageously employed. For purposes of illustration, FIG. 5 shows three remote units 120, 130, and 150 and two base stations 140. It will be recognized that typical wireless communication systems may have many more remote units and base stations. Remote units 120, 130, and 150 include ICs having dual broken seal rings 125A, 125B, and 125C, respectively, which are embodiments of the disclosure as discussed further below. FIG. 1 shows forward link signals 180 from the base stations 140 and the remote units 120, 130, and 150 and reverse link signals 190 from the remote units 120, 130, and 150 to base stations 140.

[0033] In FIG. 5, remote unit 120 is shown as a mobile telephone, remote unit 130 is shown as a portable computer, and remote unit 150 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be cell phones, hand-held personal communication systems (PCS) units, portable data units such as personal data assistants, or fixed location data units such as meter reading equipment. Although FIG. 5 illustrates remote units according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. The disclosure may be suitably employed in any device which includes ICs having dual broken seal rings.

[0034] Thus, it can be seen, the disclosed seal ring configurations reduce substrate coupling of noise, thereby improving isolation of IC devices from substrate noise. Circuit performance is improved, for example improving low noise amplifier sensitivity and noise figure, enables better radio receiver system sensitivity.

[0035] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. For example, although two seal rings have been described, more than two seal rings are contemplated. Similarly, although the preceding description was with respect to a die including analog components, an all digital die for example a microprocessor, could include the disclosed seal rings to isolate digital signals. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A sealing system for an integrated circuit, comprising:

a first seal ring circumscribing the integrated circuit, the first seal ring including at least one gap; and

a second seal ring circumscribing the first seal ring, the second seal ring including at least one gap offset from the at least one gap of the first seal ring.

2. The sealing system of claim 1, further comprising a less heavily doped area under each gap, increasing resistivity to signal propagation across the gap .

3. The sealing system of claim 1 further comprising at least one grounded pad connected to the first seal ring.

4. The sealing system of claim 1 wherein the first seal ring comprises at least two gaps and the second seal ring comprises at least two gaps.

5. The sealing system of claim 1 further comprising at least one grounded pad connected to the second seal ring.

6. A sealing system for an integrated circuit (IC), comprising:

a first seal means circumscribing the integrated circuit, the first seal means including at least one gap; and

a second seal means circumscribing the first seal means, the second seal means including at least one gap offset from the at least one gap of the first seal means.

7. The sealing system of claim 6, further comprising a less heavily doped area under each gap, increasing resistivity to signal propagation across the gaps.

8. The sealing system of claim 6 further comprising a grounding means connected to the first seal means.

9. The sealing system of claim 6 wherein the first seal means comprises at least two gaps and the second seal means comprises at least two gaps.

10.The sealing system of claim 6 further comprising a grounding means connected to the second seal means.

11. The sealing system of claim 10, where the grounding means is grounded via a pin on the IC.

12. A sealing system for an integrated circuit, comprising:

a seal ring circumscribing the integrated circuit, the seal ring including at least one channel having an ingress portion and an egress portion, the ingress portion being offset from the egress portion.

13.The sealing system of claim 12, further comprising a less heavily doped area within the channel, whereby resistivity to signal propagation across the channel is increased.

14. The sealing system of claim 12, where the ingress is separated from the egress by at least 100 um.

15. A sealing system for an integrated circuit, comprising:

a seal means circumscribing the integrated circuit, the seal means including at least one separation means having an ingress portion and an egress portion, the ingress portion being offset from the egress portion.

16.The sealing system of claim 15, further comprising a less heavily doped area within the separation means, whereby resistivity to signal propagation across the separation means is increased.

17. An integrated circuit with a sealing system, comprising:

a first seal ring circumscribing the integrated circuit, the first seal ring including at least one gap; and

a second seal ring circumscribing the first seal ring.

18. A method for forming a sealing system for an integrated circuit, comprising:

forming a first seal ring circumscribing the integrated circuit, the first seal ring including at least one gap; and

forming a second seal ring circumscribing the first seal ring, the second seal ring including at least one gap offset from the at least one gap of the first seal ring.

19. The method for forming a sealing system of claim 18, further comprising forming a less heavily doped area under each gap, whereby resistivity to signal propagation across the gaps is increased.

FIG. 1A

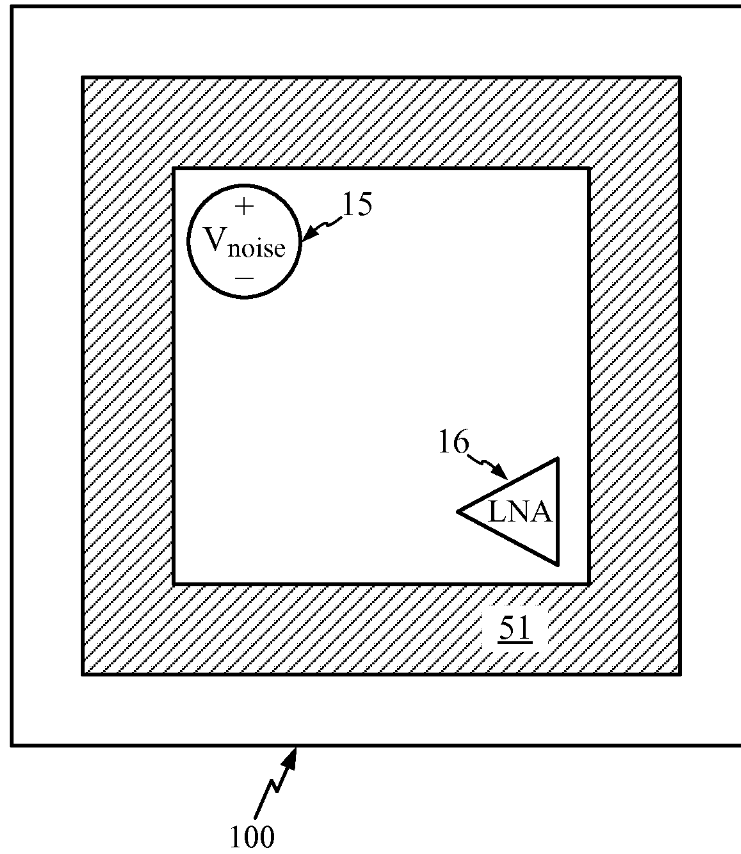

FIG. 1B

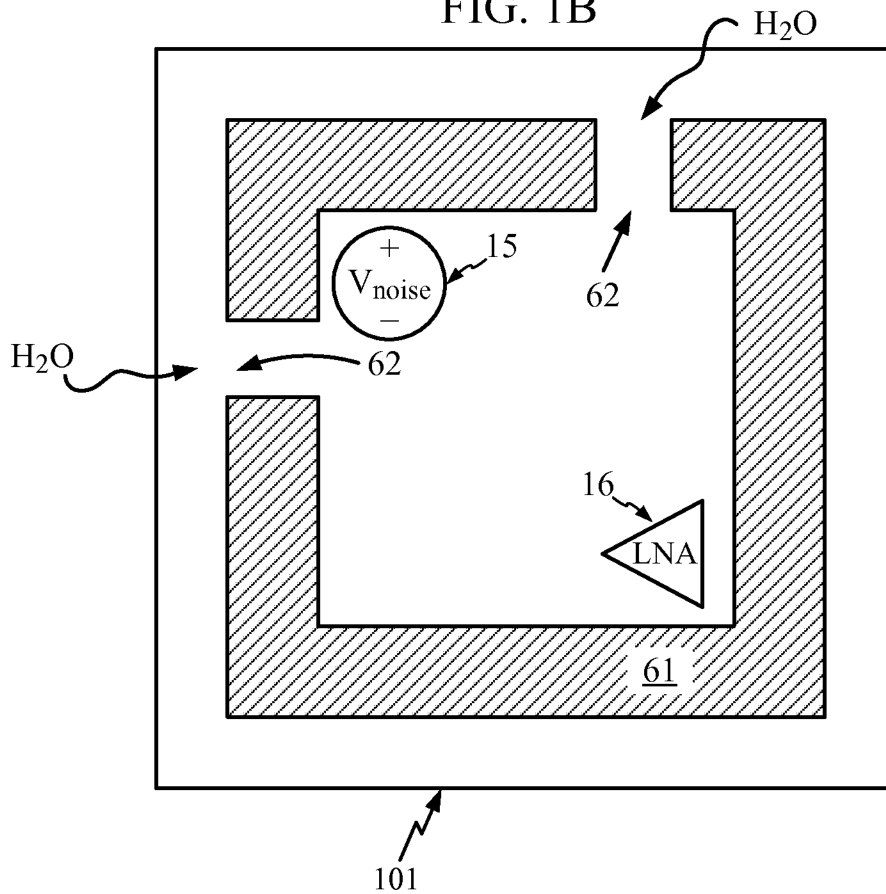

FIG. 2

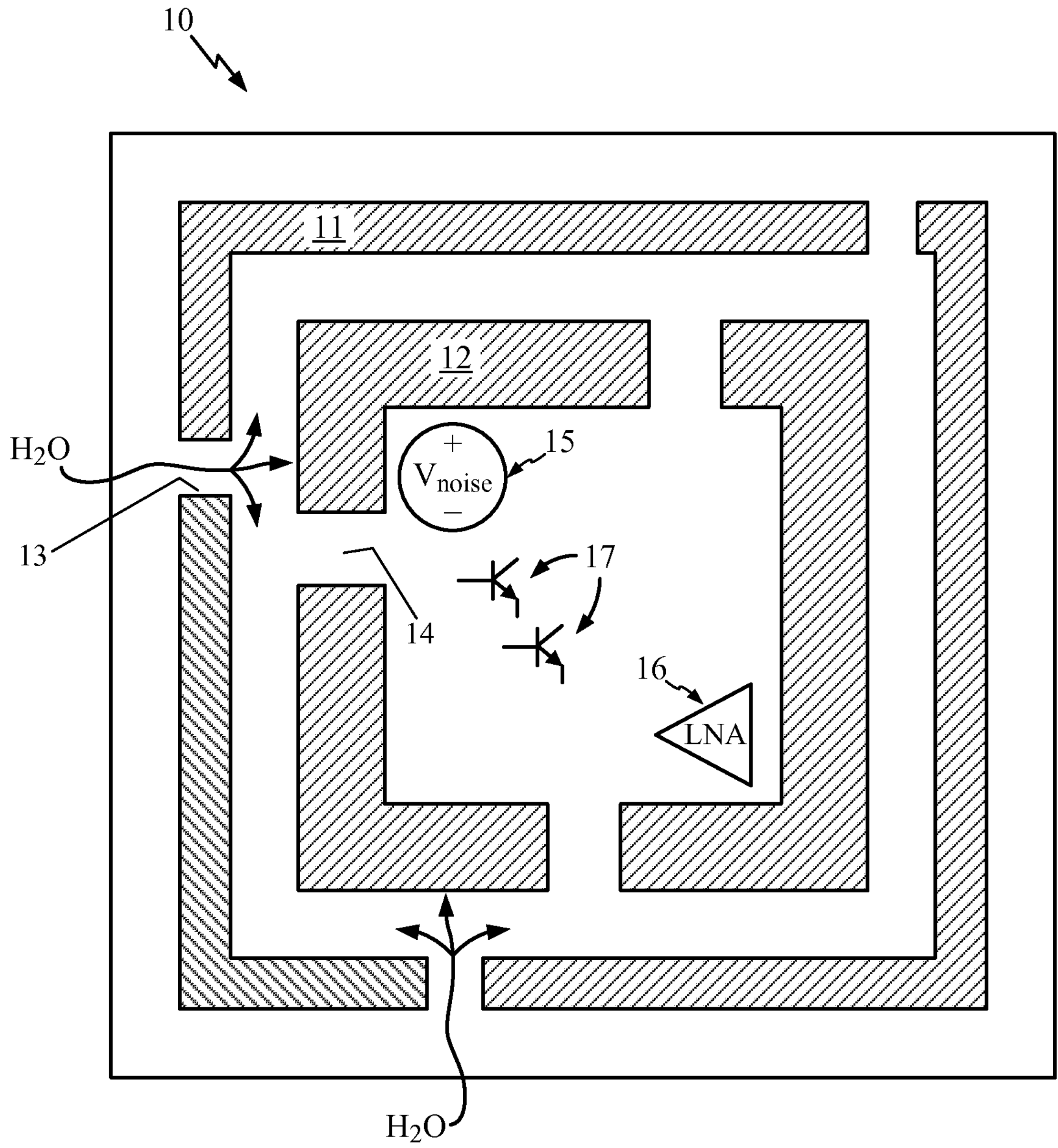

FIG. 3A

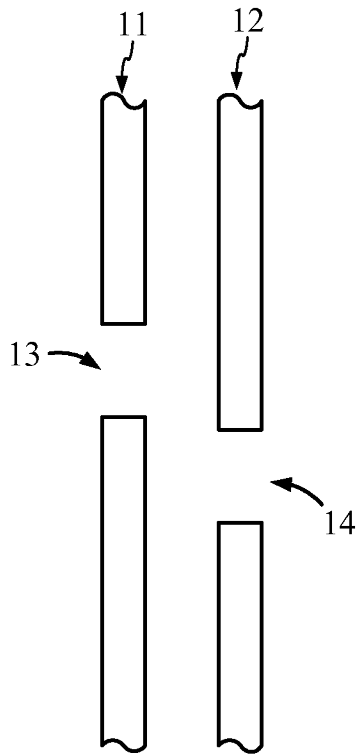

FIG. 3B

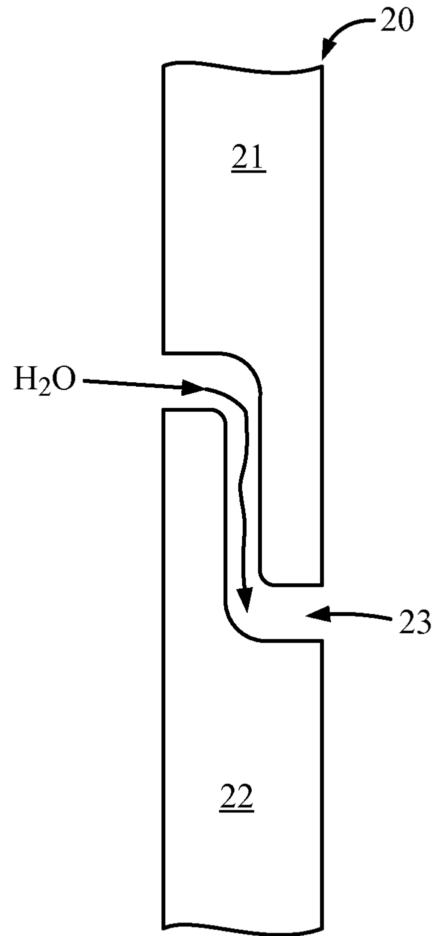

FIG. 4

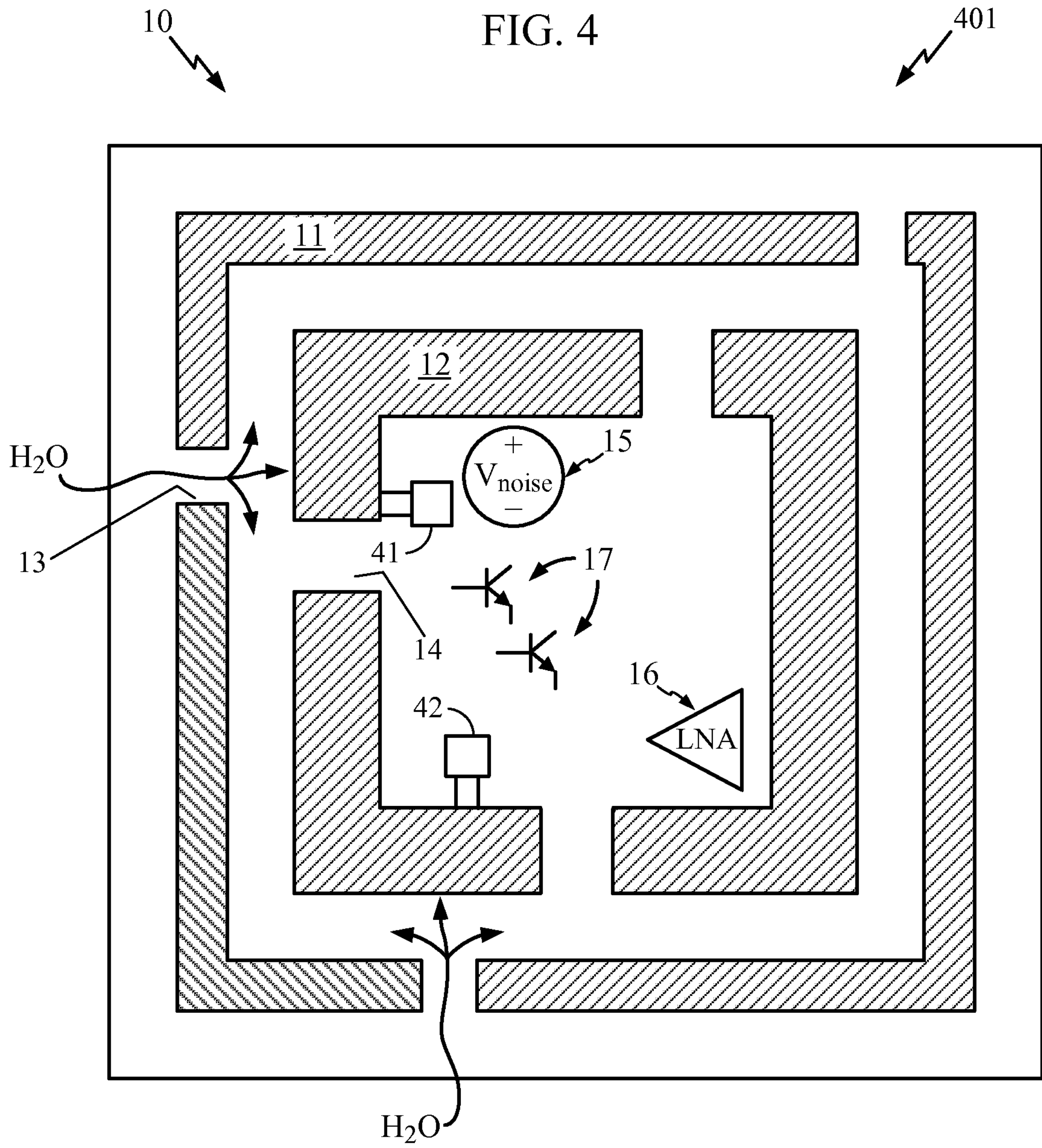

FIG. 5