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(54) **INTEGRATED CIRCUIT STRUCTURES HAVING BACKSIDE CAPACITORS**

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(52) **U.S. Cl.**

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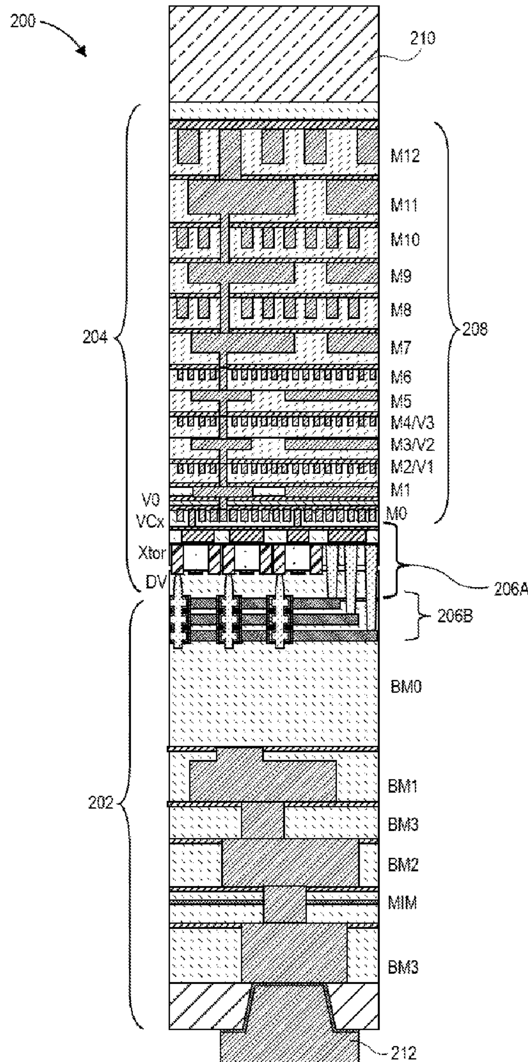
(57) **ABSTRACT**

Structures having backside capacitors are described. In an example, an integrated circuit structure includes a front side structure including a device layer having a plurality of select transistors, a plurality of metallization layers above the plurality of select transistors, and a plurality of vias below and coupled to the plurality of select transistors. A backside structure is below the plurality of vias of the device layer. The backside structure includes a memory layer coupled to the plurality of select transistors by the plurality of vias.



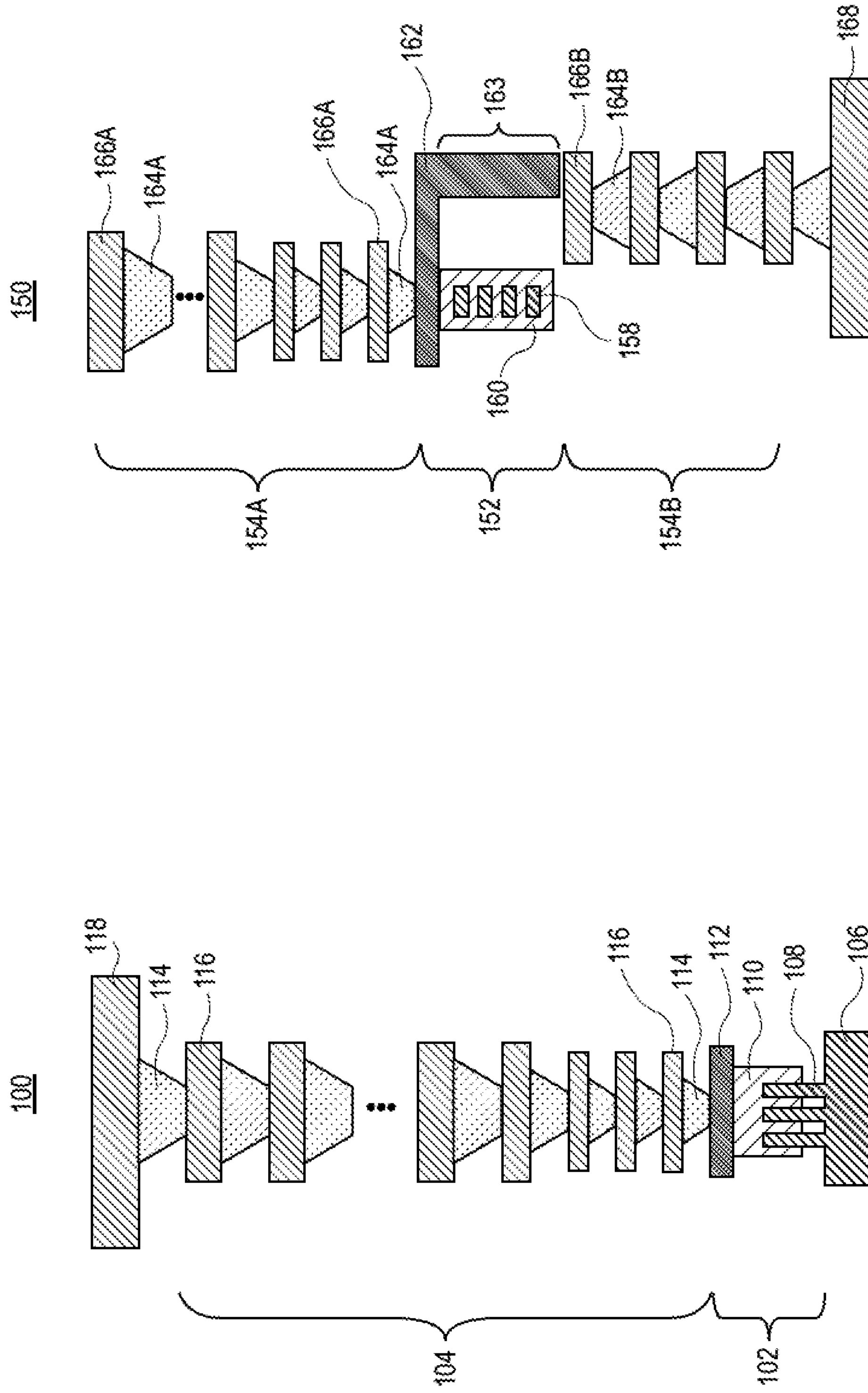


FIG. 1

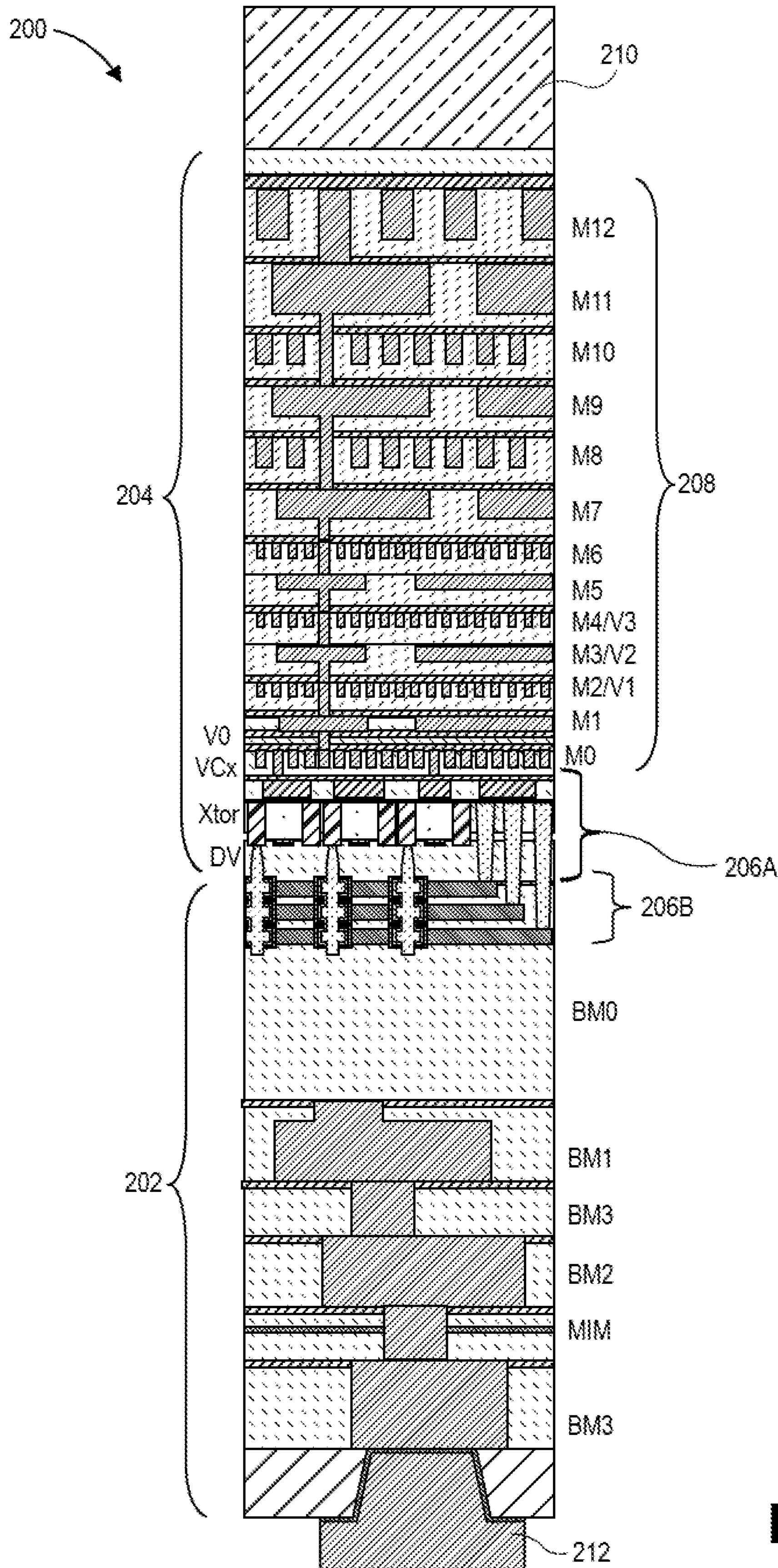


FIG. 2A

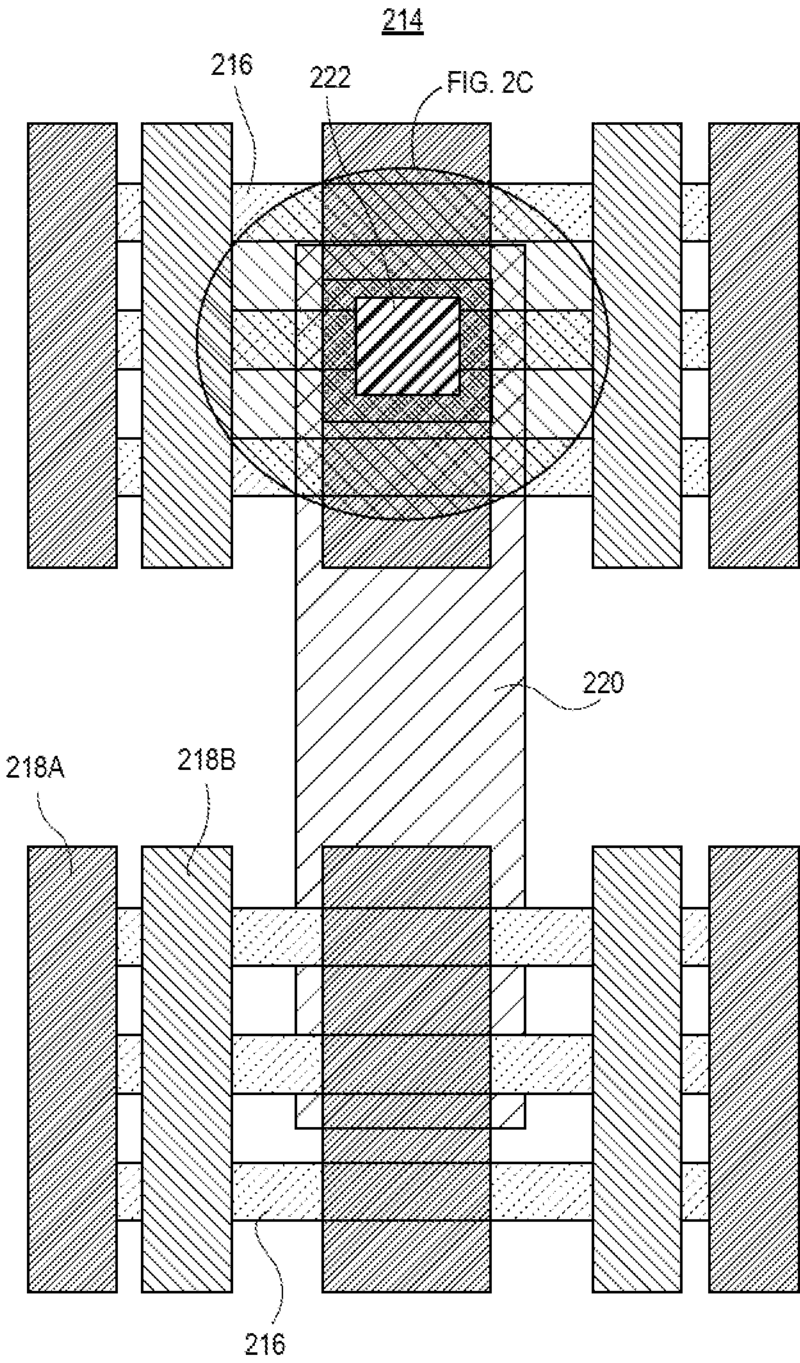


FIG. 2B

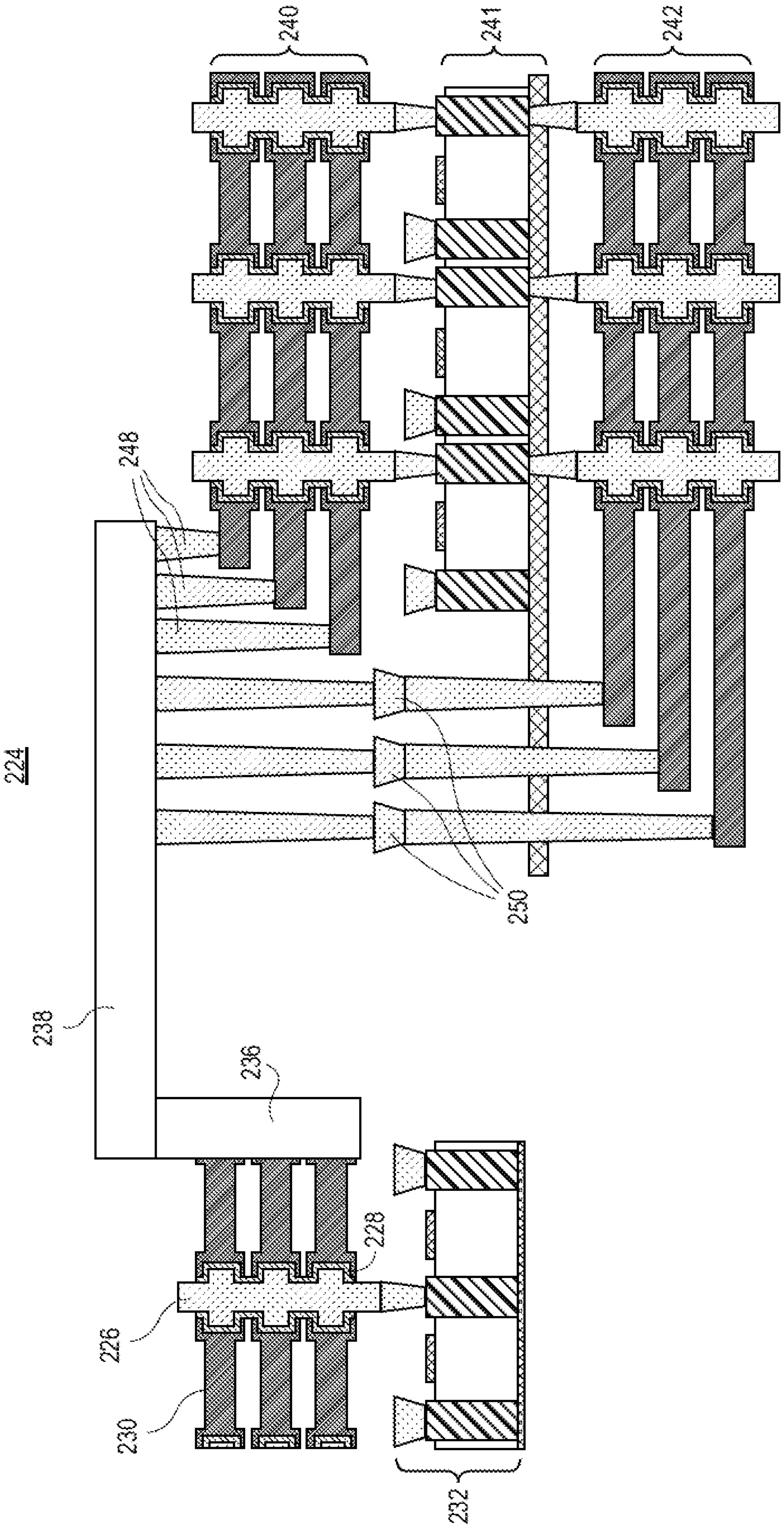


FIG. 2C

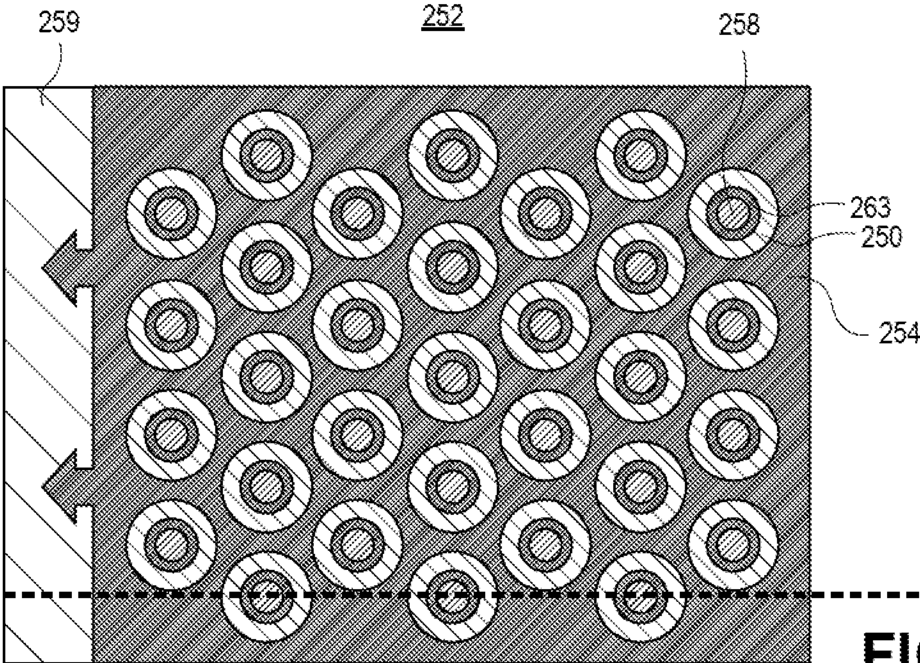


FIG. 2D

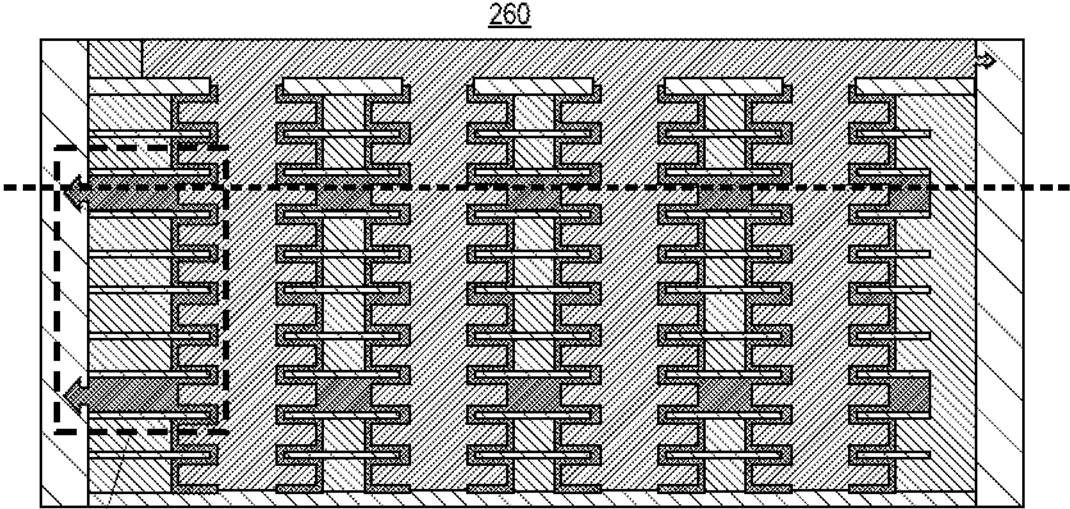


FIG. 2E

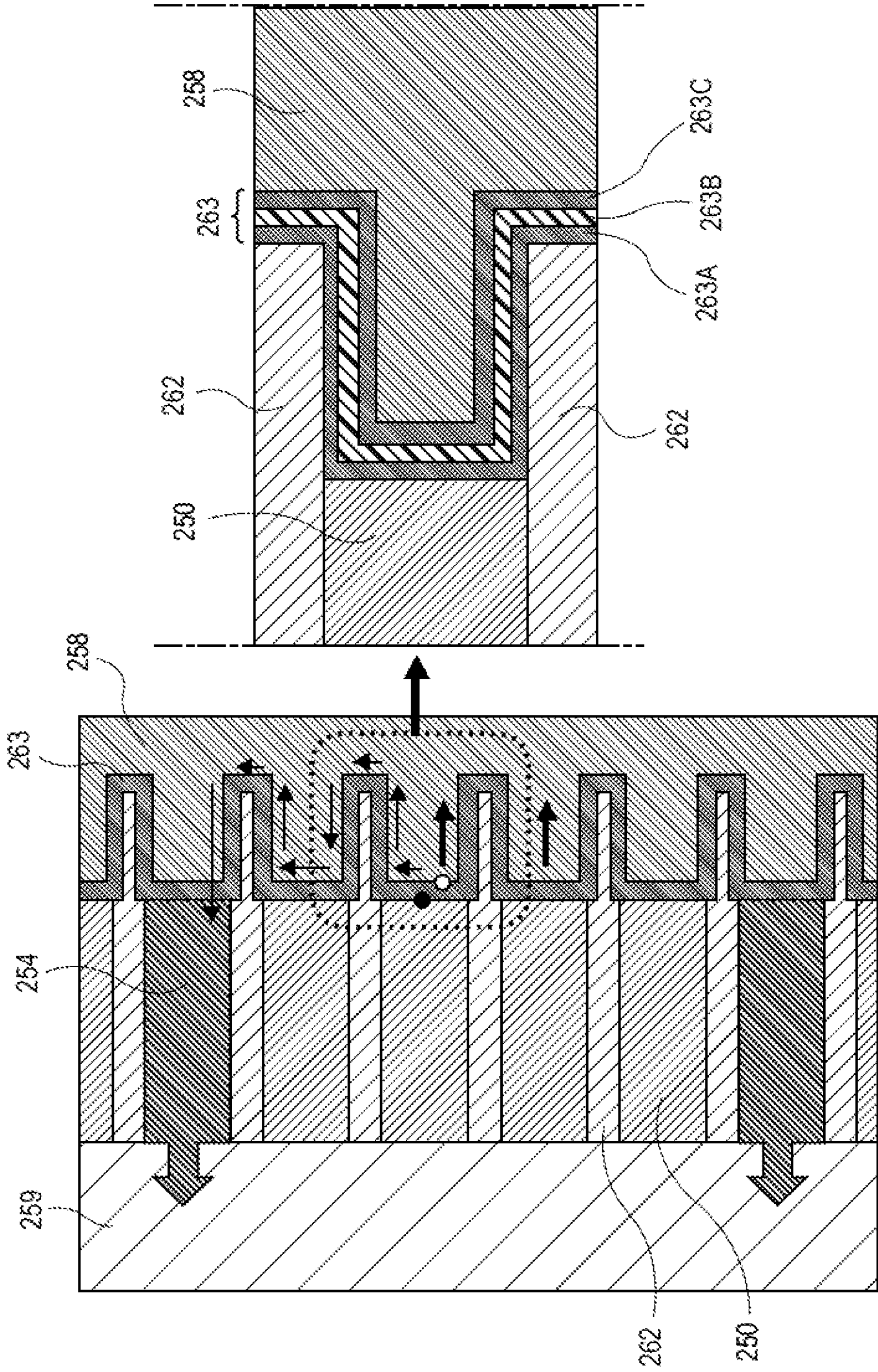


FIG. 2F

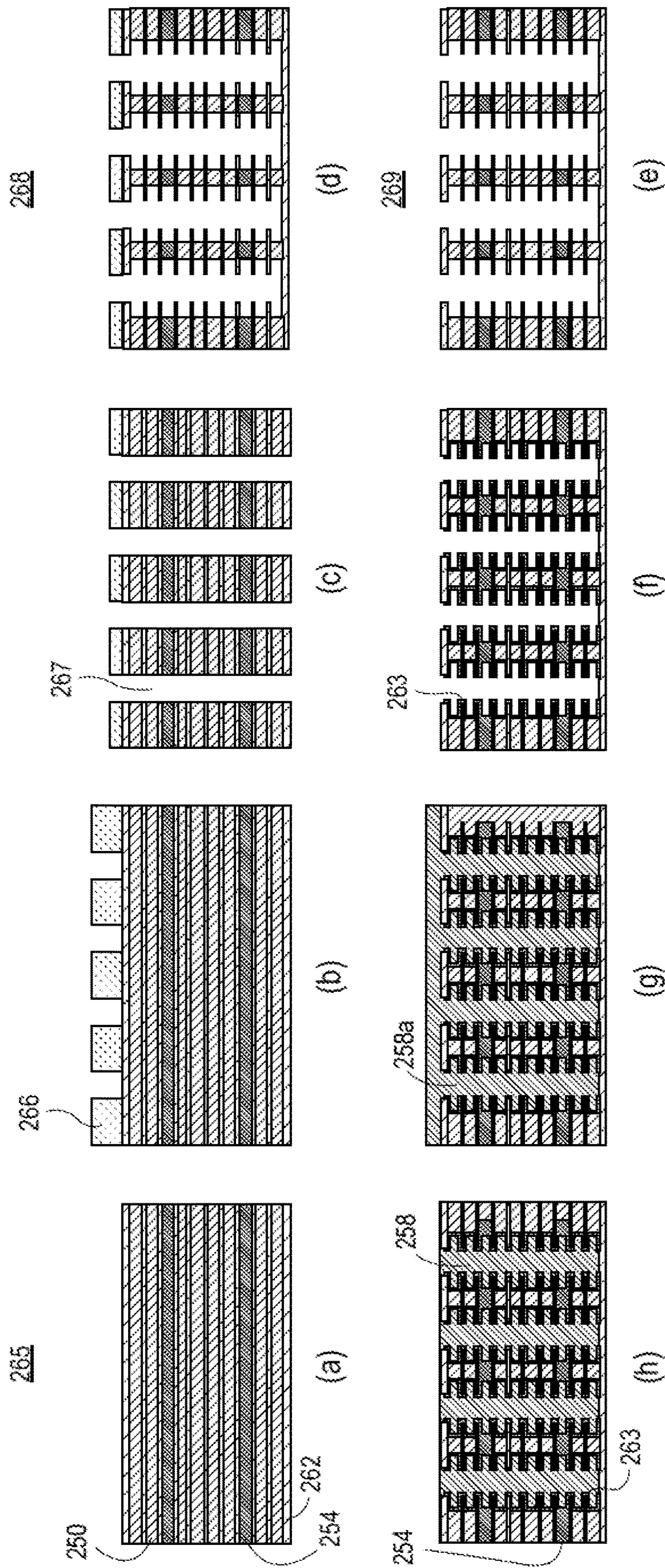


FIG. 2G

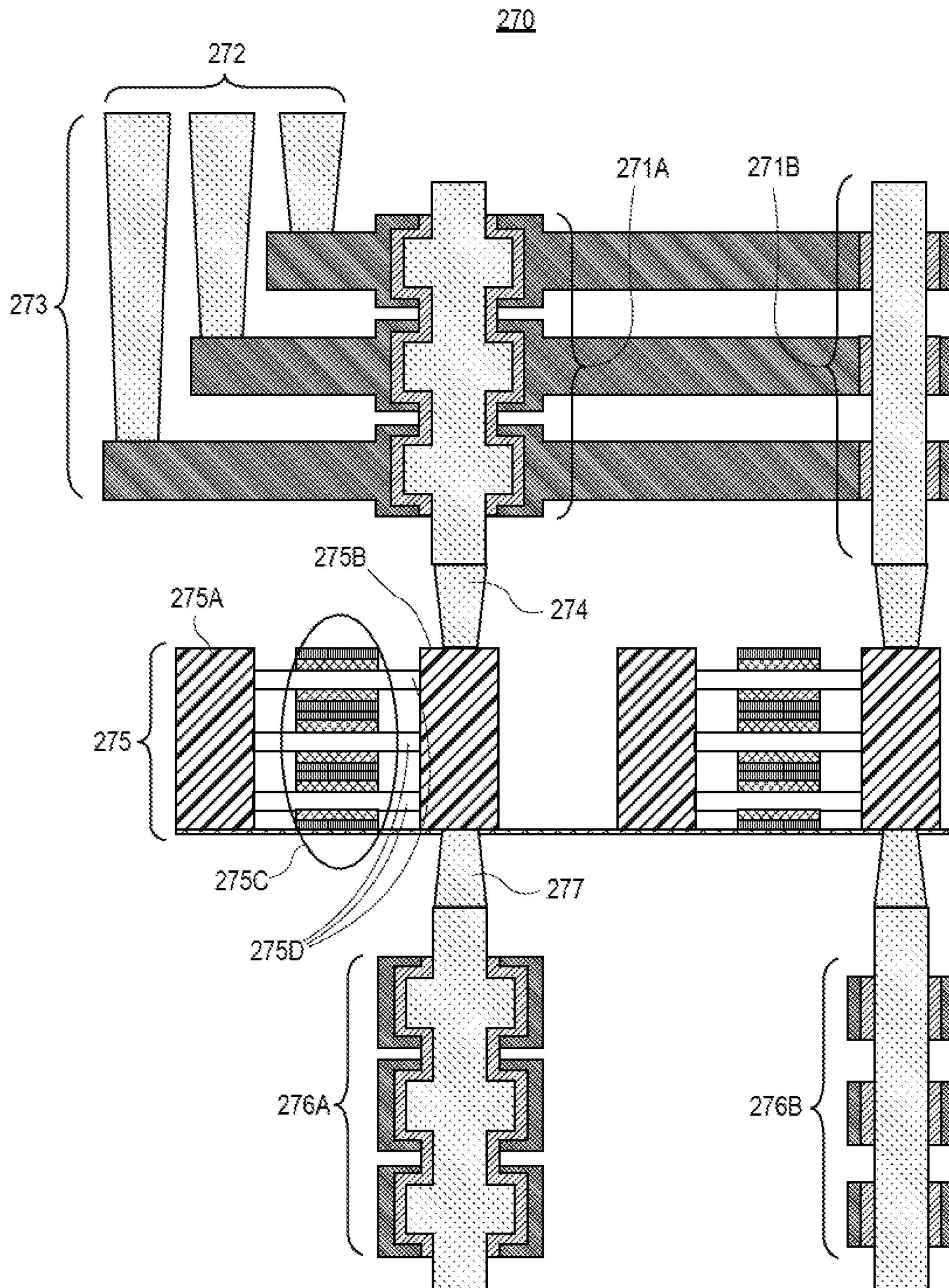


FIG. 2H

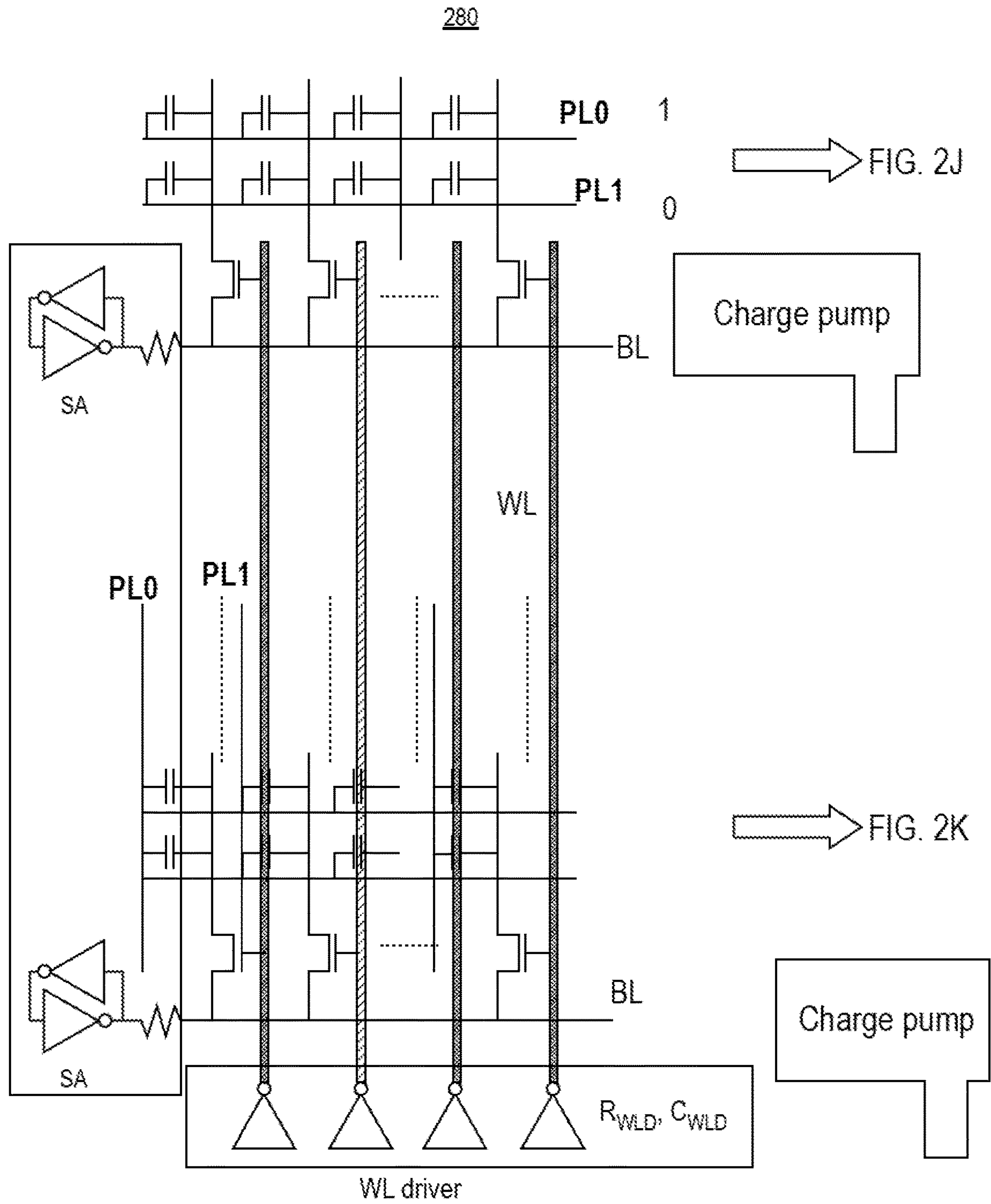


FIG. 2I

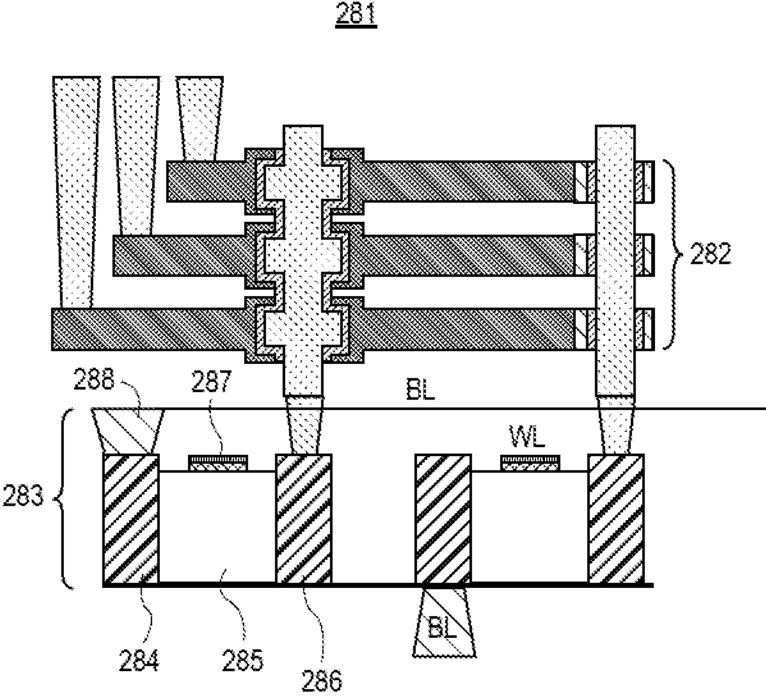


FIG. 2J

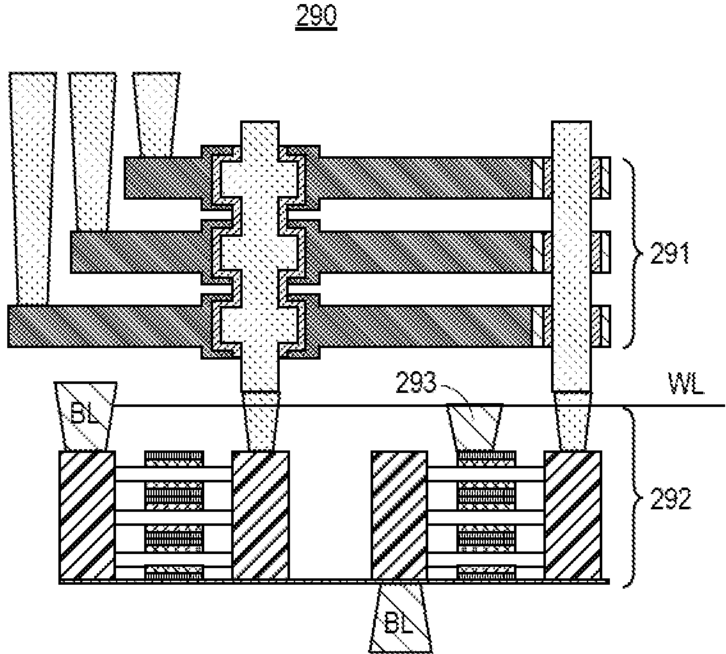


FIG. 2K

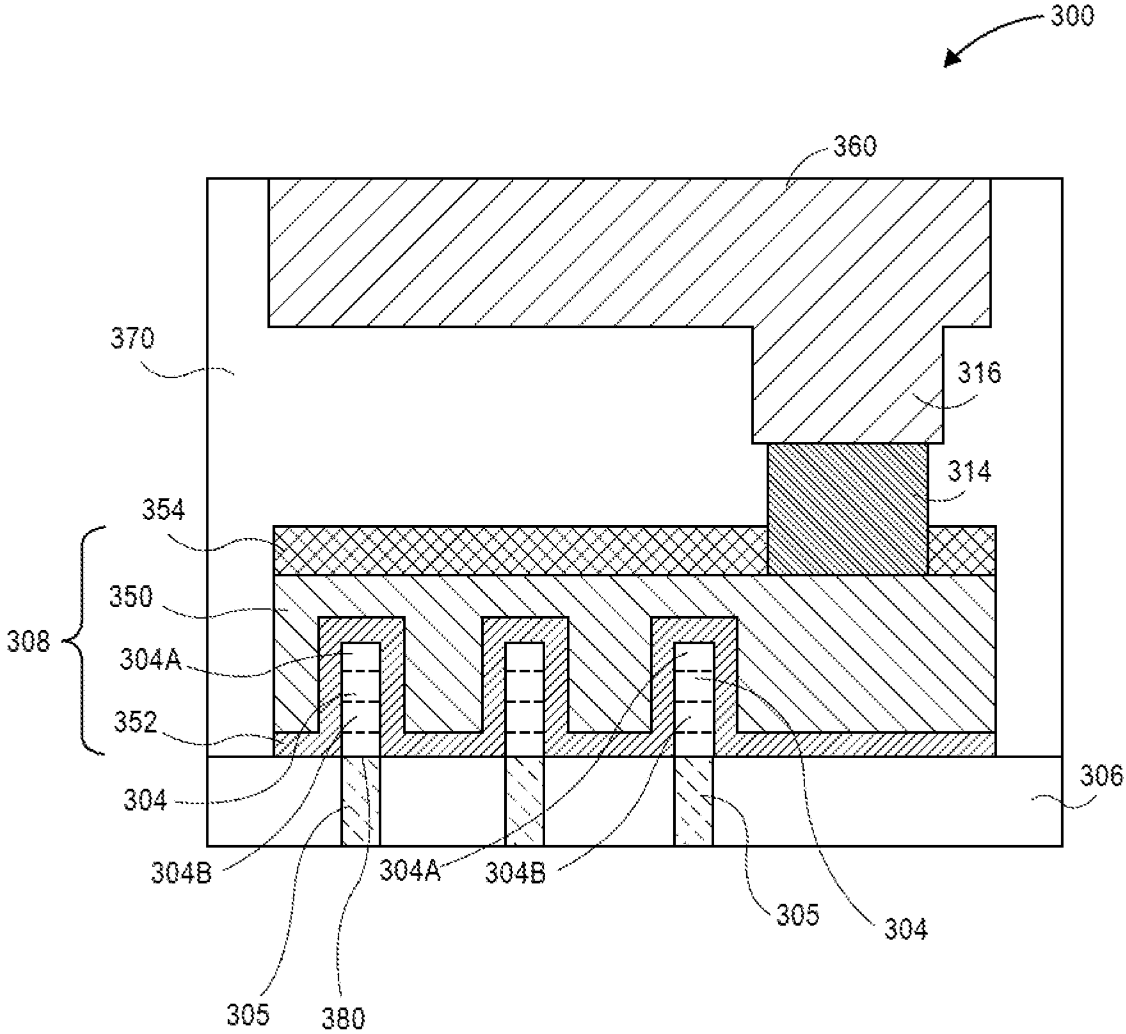


FIG. 3

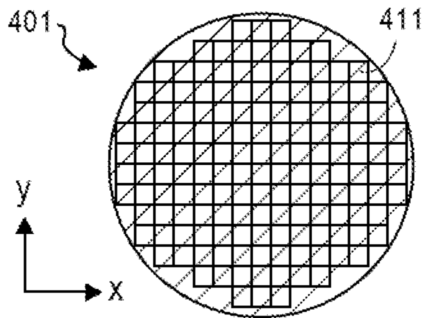


FIG. 4A

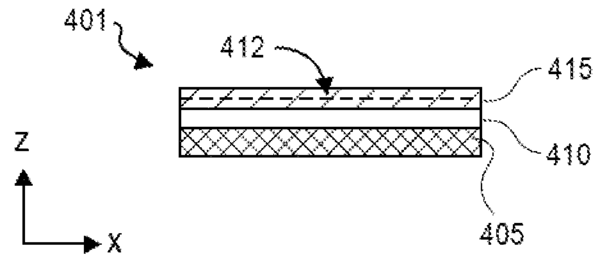


FIG. 5A

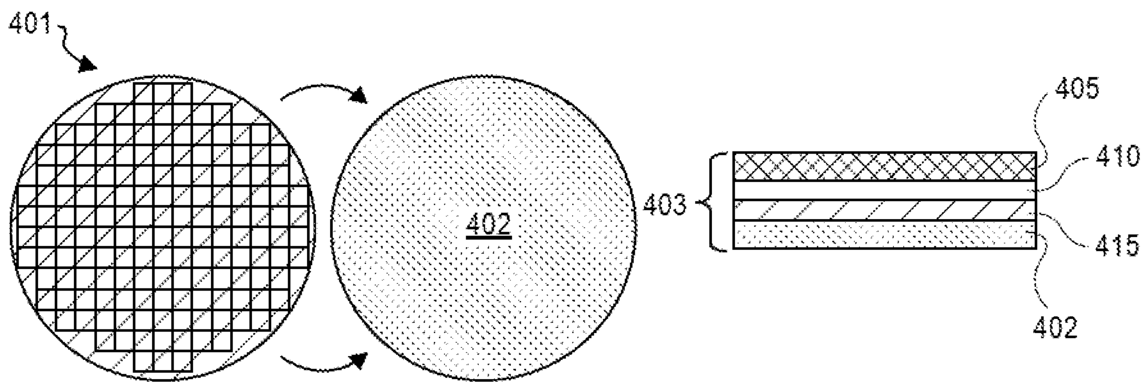


FIG. 4B

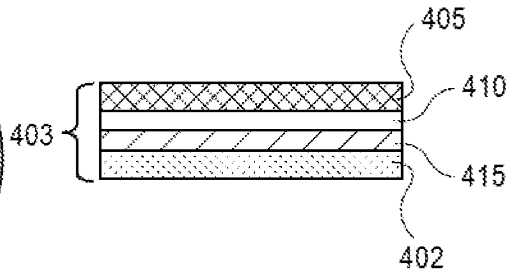


FIG. 5B

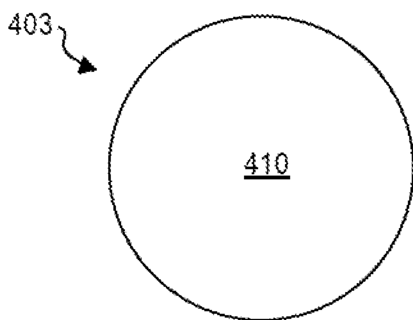


FIG. 4C

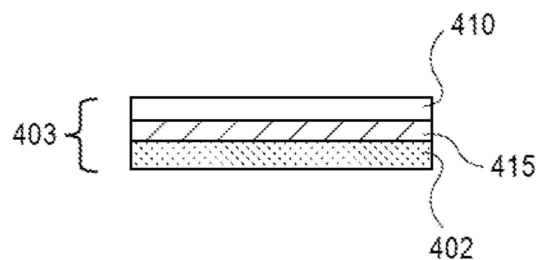


FIG. 5C

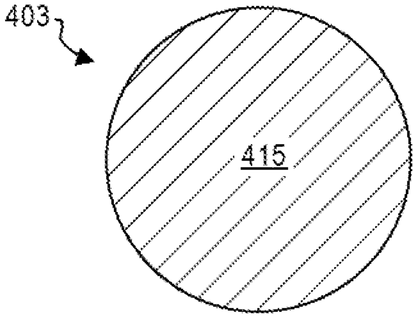


FIG. 4D

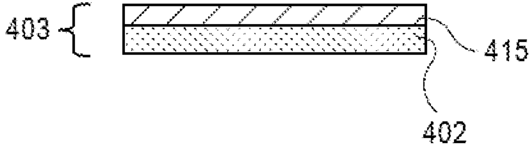


FIG. 5D

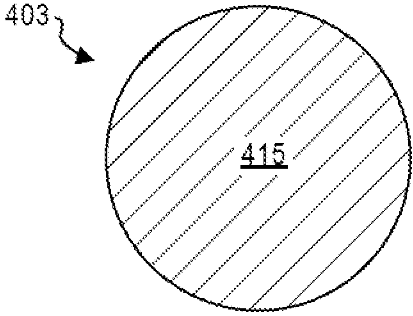


FIG. 4E

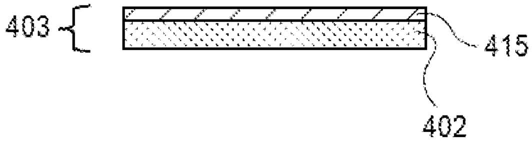


FIG. 5E

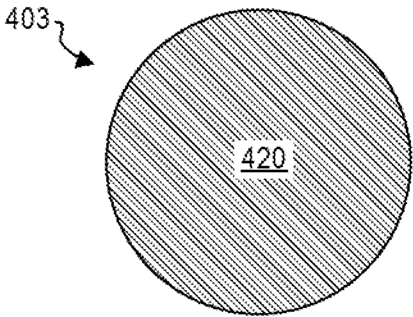


FIG. 4F

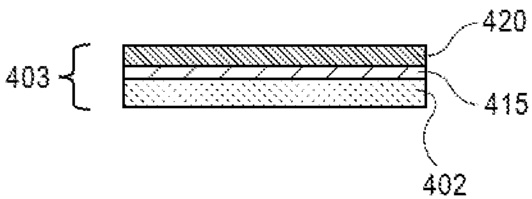


FIG. 5F

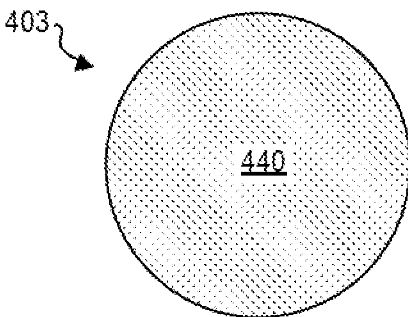


FIG. 4G

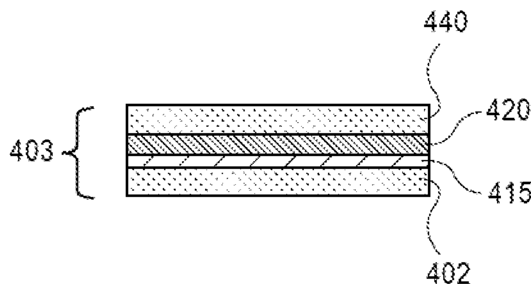


FIG. 5G

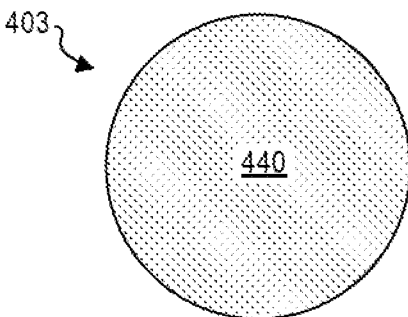


FIG. 4H

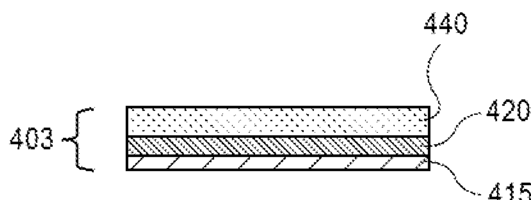


FIG. 5H

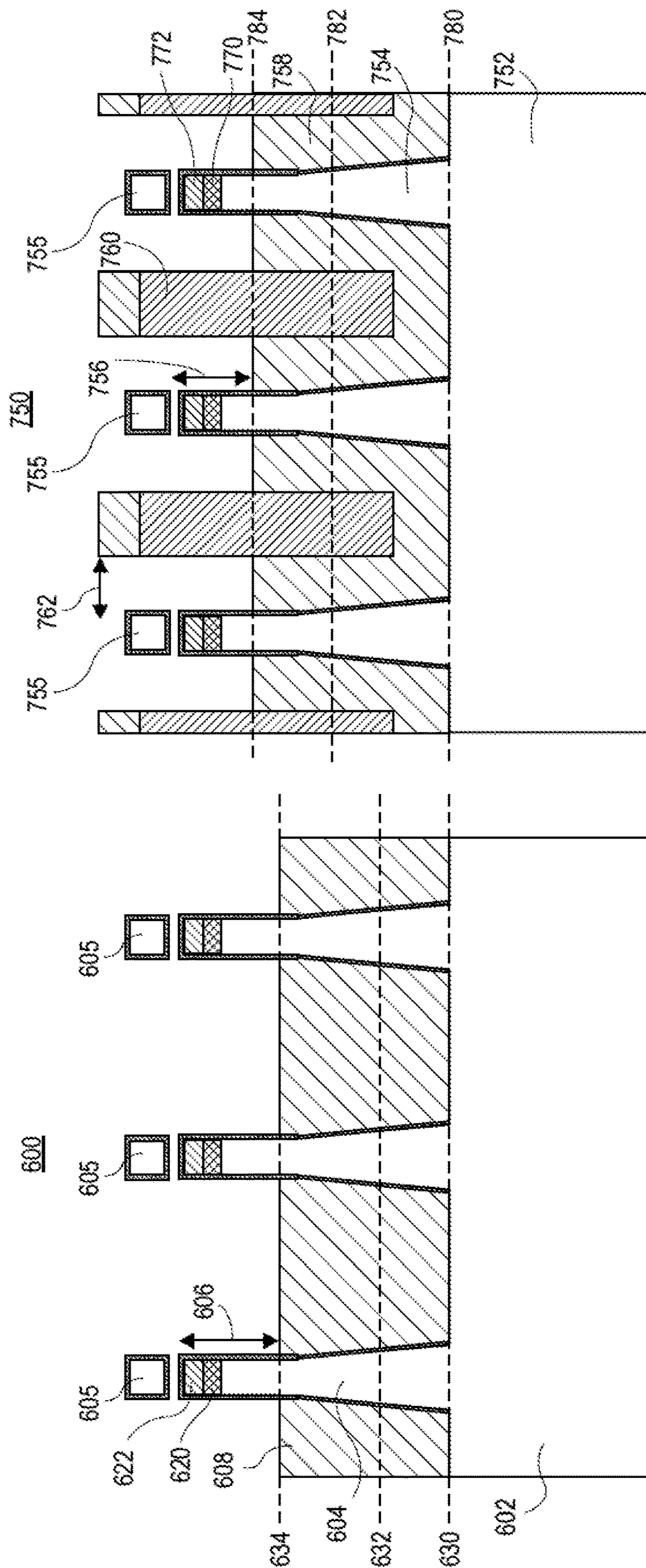


FIG. 7

FIG. 6

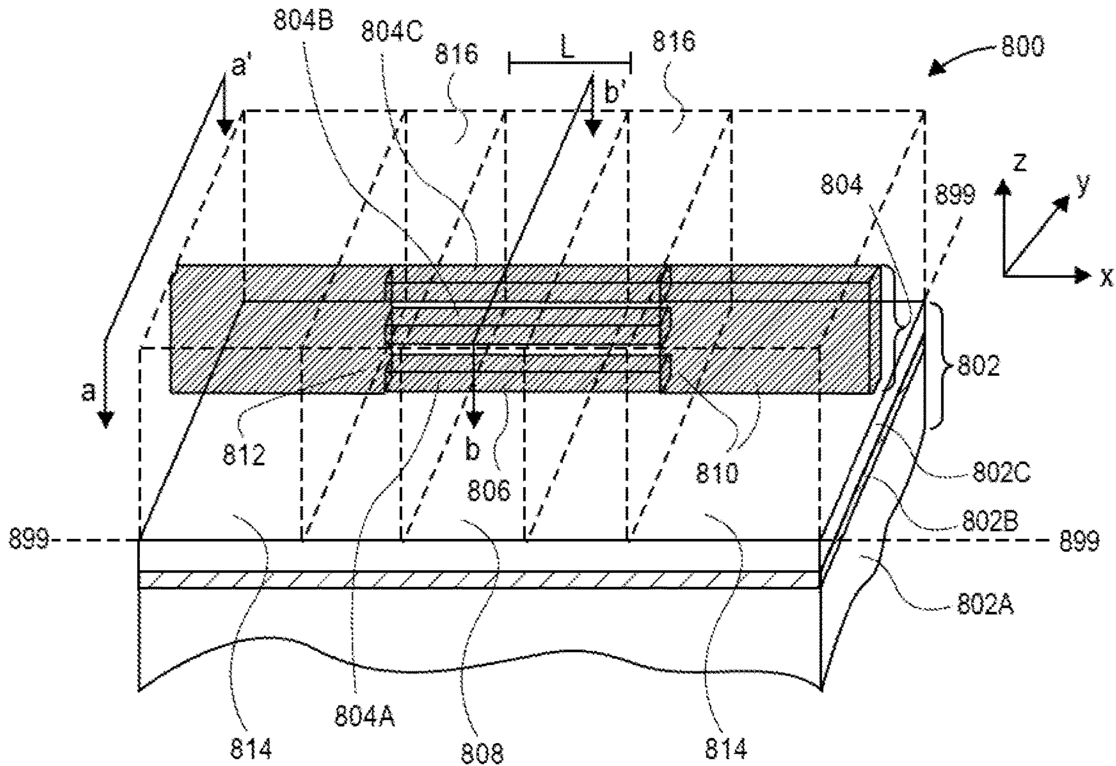


FIG. 8A

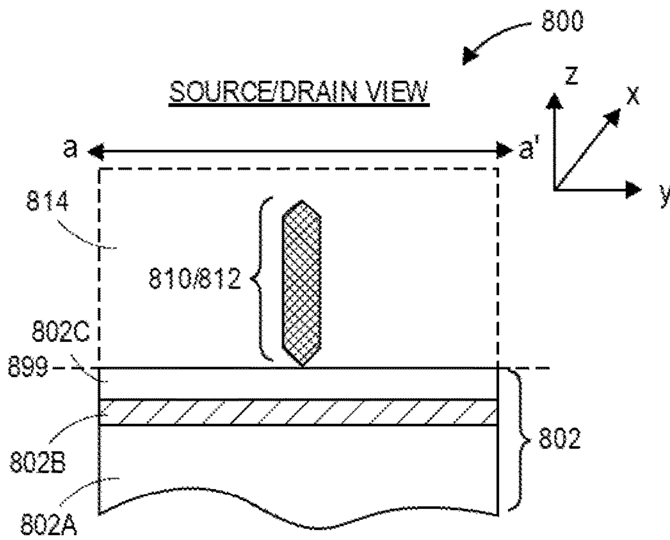


FIG. 8B

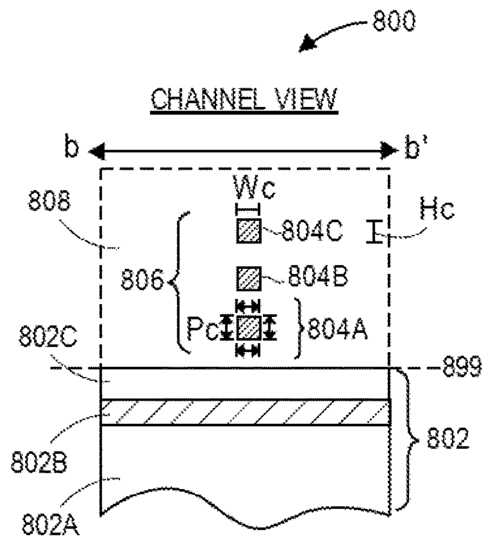


FIG. 8C

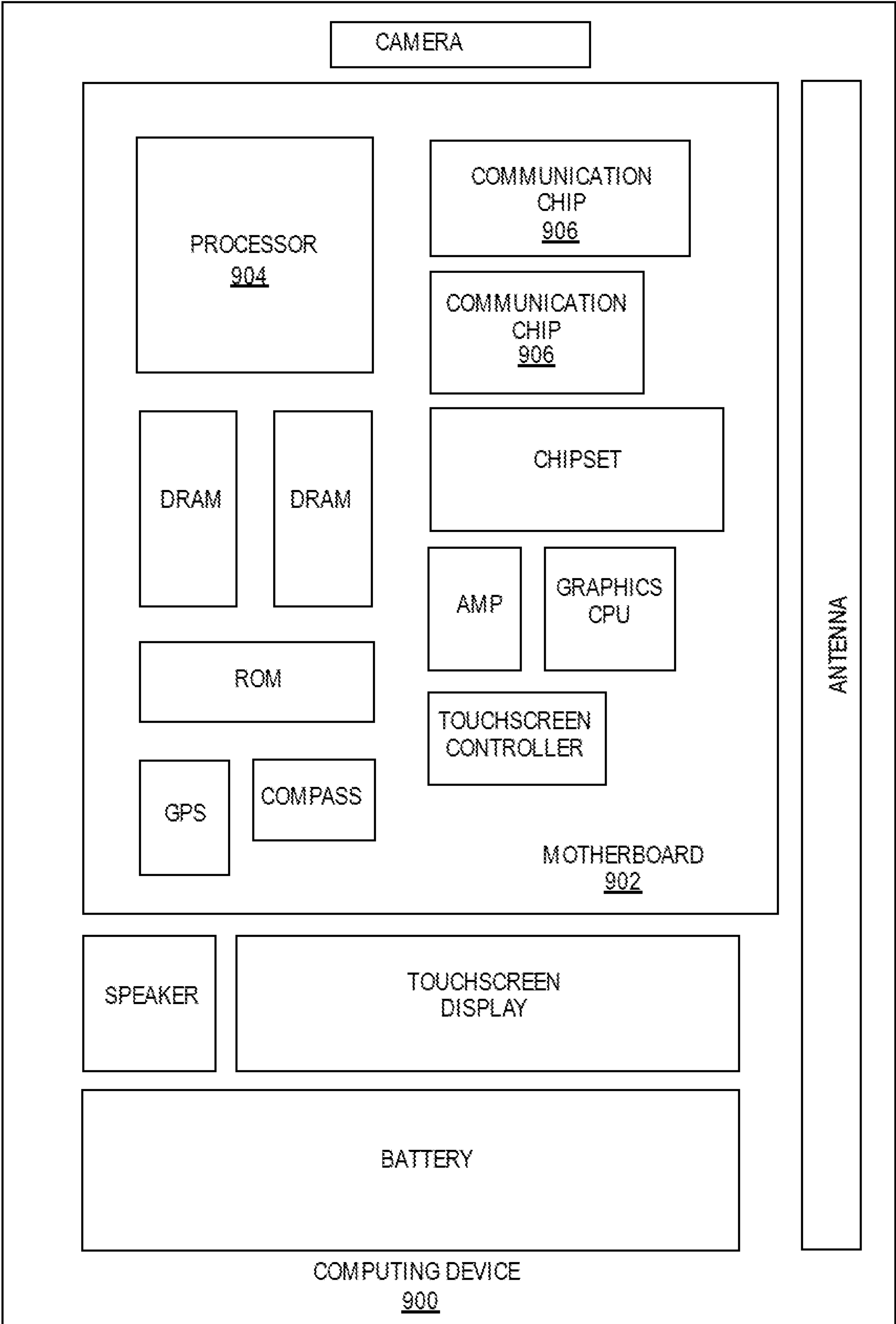


FIG. 9

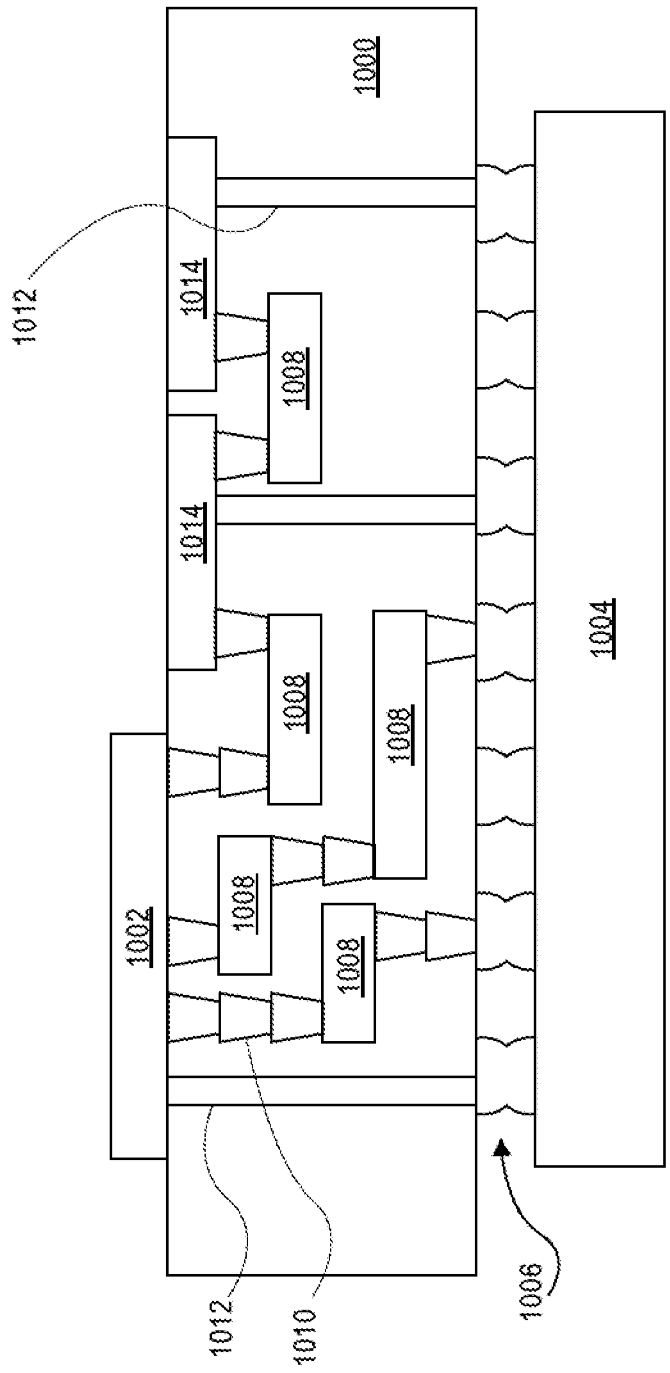


FIG. 10

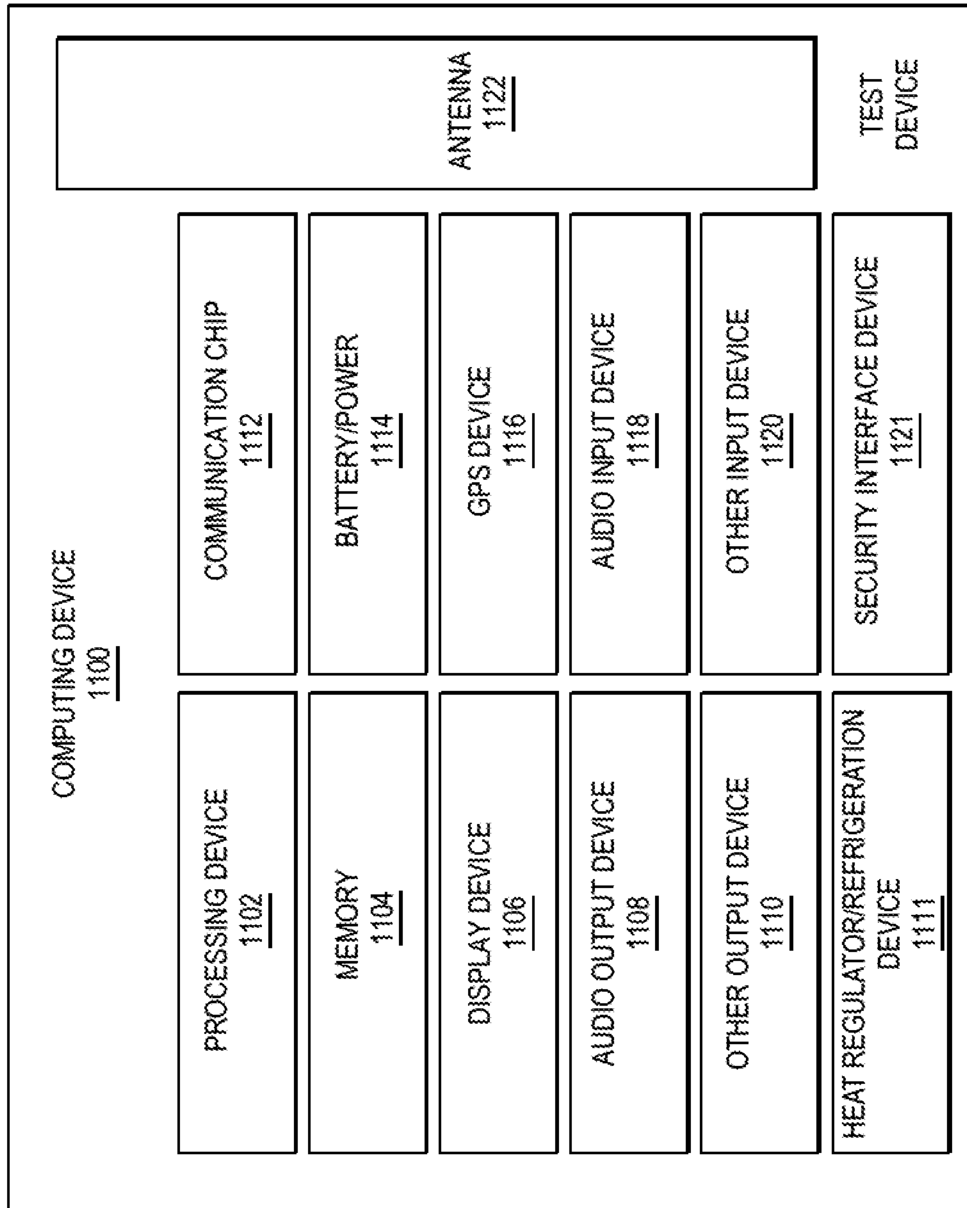


FIG. 11A

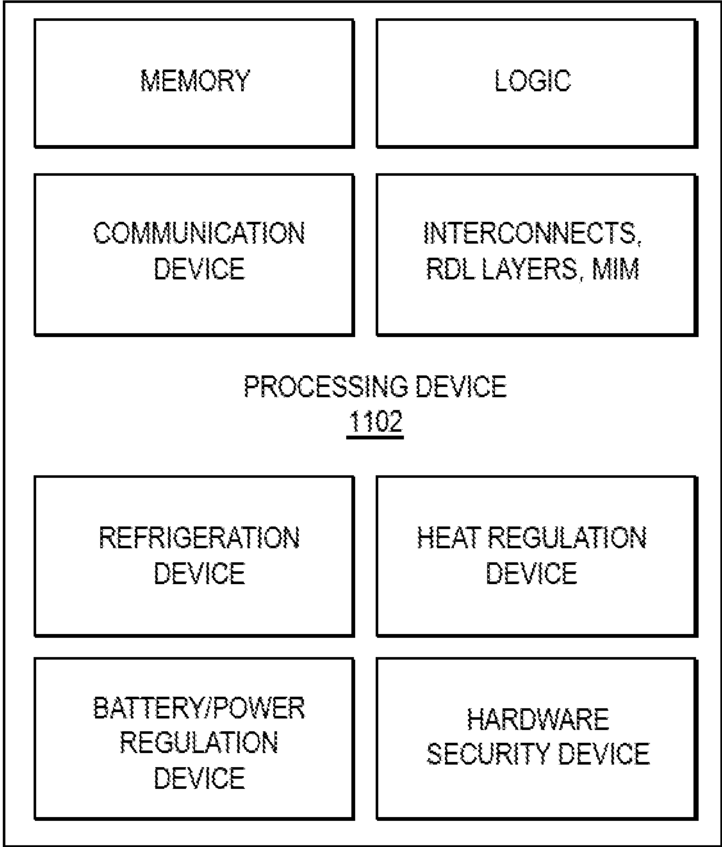


FIG. 11B

INTEGRATED CIRCUIT STRUCTURES HAVING BACKSIDE CAPACITORS

TECHNICAL FIELD

[0001] Embodiments of the disclosure are in the field of integrated circuit structures and processing and, in particular, integrated circuit structures having backside capacitors and methods of fabricating integrated circuit structures having backside capacitors.

BACKGROUND

[0002] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0003] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process. In another aspect, maintaining mobility improvement and short channel control as microelectronic device dimensions scale below the 10 nanometer (nm) node provides a challenge in device fabrication. Nanowires used to fabricate devices provide improved short channel control.

[0004] Scaling multi-gate and nanowire transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the lithographic processes used to pattern these building blocks have become overwhelming. In particular, there may be a trade-off between the smallest dimension of a feature patterned in a semiconductor stack (the critical dimension) and the spacing between such features.

[0005] Another aspect driving innovation is the drive for high bandwidth (HBW) computing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. **1** illustrates cross-sectional views of an interconnect stack having front side power delivery and of an interconnect stack having backside power delivery, in accordance with an embodiment of the present disclosure.

[0007] FIG. **2**A illustrates a cross-sectional view of an integrated circuit structure having a front side transistor layer and backside capacitor structure, in accordance with an embodiment of the present disclosure.

[0008] FIG. **2**B illustrates a plan view of a charge pump including a hysteretic capacitor, in accordance with an embodiment of the present disclosure.

[0009] FIG. **2**C illustrates a cross-sectional view of a hysteretic capacitor of FIG. **2**B, in accordance with an embodiment of the present disclosure.

[0010] FIGS. **2**D and **2**E illustrates a plan view and corresponding cross-sectional view of a capacitor array, respectively, in accordance with an embodiment of the present disclosure.

[0011] FIG. **2**F illustrates magnified cross-sectional views of the capacitor array of FIGS. **2**D and **2**E, in accordance with an embodiment of the present disclosure.

[0012] FIG. **2**G illustrates cross-sectional views representing various operations in a method of fabricating a capacitor array, in accordance with an embodiment of the present disclosure.

[0013] FIG. **2**H illustrates a cross-sectional view of a layered multi-capacitor system, in accordance with an embodiment of the present disclosure.

[0014] FIG. **2**I is a layout of a capacitor array system, in accordance with an embodiment of the present disclosure.

[0015] FIG. **2**J illustrates a cross-sectional view of a charge pump associated with the capacitor array system of FIG. **2**I, in accordance with an embodiment of the present disclosure.

[0016] FIG. **2**K illustrates a cross-sectional view of another charge pump associated with the capacitor array system of FIG. **2**I, in accordance with an embodiment of the present disclosure.

[0017] FIG. **3** illustrates a cross-sectional view of a non-planar integrated circuit structure as taken along a gate line, in accordance with an embodiment of the present disclosure.

[0018] FIGS. **4**A-**4**H illustrate plan views of a substrate processed with double-sided device processing methods, in accordance with some embodiments.

[0019] FIGS. **5**A-**5**H illustrate cross-sectional views of a substrate processed with double-sided device processing methods, in accordance with some embodiments.

[0020] FIG. **6** illustrates a cross-sectional view taken through nanowires and fins for a non-endcap architecture, in accordance with an embodiment of the present disclosure.

[0021] FIG. **7** illustrates a cross-sectional view taken through nanowires and fins for a self-aligned gate endcap (SAGE) architecture, in accordance with an embodiment of the present disclosure.

[0022] FIG. **8**A illustrates a three-dimensional cross-sectional view of a nanowire-based integrated circuit structure, in accordance with an embodiment of the present disclosure.

[0023] FIG. **8**B illustrates a cross-sectional source or drain view of the nanowire-based integrated circuit structure of FIG. **8**A, as taken along the a-a' axis, in accordance with an embodiment of the present disclosure.

[0024] FIG. **8**C illustrates a cross-sectional channel view of the nanowire-based integrated circuit structure of FIG. **8**A, as taken along the b-b' axis, in accordance with an embodiment of the present disclosure.

[0025] FIG. **9** illustrates a computing device in accordance with one implementation of an embodiment of the disclosure.

[0026] FIG. **10** illustrates an interposer that includes one or more embodiments of the disclosure.

[0027] FIG. **11**A illustrates a computing device in accordance with one implementation of an embodiment of the present disclosure.

[0028] FIG. 11B illustrates a processing device in accordance with one implementation of an embodiment of the present disclosure.

DESCRIPTION OF THE EMBODIMENTS

[0029] Integrated circuit structures having backside capacitors, and methods of fabricating integrated circuit structures having backside capacitors, are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be appreciated that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0030] Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as "upper", "lower", "above", and "below" refer to directions in the drawings to which reference is made. Terms such as "front", "back", "rear", and "side" describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0031] Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

[0032] Embodiments described herein may be directed to back-end-of-line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

[0033] Embodiments described below may be applicable to FEOL processing and structures, BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

[0034] One or more embodiments described herein are directed to ferroelectric capacitor processing on backside with hybrid manufacturing. One or more embodiments described herein are directed to low-temperature enabled dense charge pumps using hysteretic capacitors. One or more embodiments described herein are directed to approaches for using backside reveal for layering multi-capacitor systems.

[0035] In an embodiment, structures described herein are suitable for use as high bandwidth (HBW) devices which may be operated at a low temperature, e.g., in a range of −77 degrees Celsius to 0 degrees Celsius. In one embodiment, a heat regulator/refrigeration device is coupled to a common board having a device with structures such as those described herein coupled thereto. In one embodiment, a heat regulator device and/or refrigeration device is included on a processing device having structures such as those described herein. In an embodiment, structures described herein enable a zetta-unit of compute (Zuoc), e.g., to enable operation at low temperature, etc.

[0036] To provide further context, in standard cell design, the diffusion placement and metal routing layers are designed around a power delivery scheme. It can be through front side bump to the M0 and the diffusion contact or in the newer architectures it can be through wafer backside metals would be tapped through a via that would contact the diffusion contact on the front side. When these are performed, either on the front side metals or the diffusion there is a space allocation for the delivery of power.

[0037] Traditionally, power is delivered from a front side interconnect. At standard cell level, power can be delivered right on top of transistors or from a top and bottom cell boundary. Power delivered from a top and bottom cell boundary enables relatively shorter standard cell height with slightly higher power network resistance. However, a front side power network shares interconnect stack with signal routing and reduces signal routing tracks. In addition, for high performance design, top and bottom cell boundary power metal wires must be wide enough to reduce power network resistance and improve performance. This normally results in a cell height increase. In accordance with one or more embodiments of the present disclosure, delivering power from a wafer or substrate backside can be implemented to solve area and performance problems. At the cell level, wider metal 0 power at the top and bottom cell boundary may no longer be needed and, hence, cell height can be reduced. In addition, power network resistance can be significantly reduced resulting in performance improvement. At block and chip level, front side signal routing tracks are increased due to removed power routing and power network resistance is significantly reduced due to very wide wires, large vias and reduced interconnect layers.

[0038] In earlier technologies, a power delivery network from bump to the transistor required significant block resources. Such resource usage on the metal stack expressed itself in some process nodes as Standard Cell architectures with layout versioning or cell placement restrictions in the block level. In an embodiment, eliminating the power delivery network from the front side metal stack allows free sliding cell placement in the block without power delivery complications and placement related delay timing variation.

[0039] As a comparison, FIG. 1 illustrates cross-sectional views of an interconnect stack having front side power

delivery and of an interconnect stack having backside power delivery, in accordance with an embodiment of the present disclosure.

[0040] Referring to FIG. **1**, an interconnect stack **100** having front side power delivery includes a transistor **102** and signal and power delivery metallization **104**. The transistor **102** includes a bulk substrate **106**, semiconductor fins **108**, a terminal **110**, and a device contact **112**. The signal and power delivery metallization **104** includes conductive vias **114**, conductive lines **116**, and a metal bump **118**.

[0041] Referring again to FIG. **1**, an interconnect stack **150** having backside power delivery includes a transistor **152**, front side signal metallization **154**A, and power delivery metallization **154**B. The transistor **152** includes semiconductor nanowires or nanoribbons **158**, a terminal **160**, and a device contact **162**, and a boundary deep via **163**. The front side signal metallization **154**A includes conductive vias **164**A and conductive lines **166**A. The power delivery metallization **154**B includes conductive vias **164**B, conductive lines **166**B, and a metal bump **168**.

[0042] To provide further context, one of the ultimate goals in Standard Cell design is to minimize the impact of the power delivery to the signal routing in terms of area, while maintaining a robust power delivery scheme which would have minimum voltage drop from the supply. With front side power delivery, commercialized Standard Cell architectures had to allocate routing tracks for power and ground from the top of the front side stack to the first metal routing layer, M0. This approach would exploit metal routing tracks. That means tighter metal pitches are required to deliver power while routing signals. Tighter metal pitches cause higher cap and resistance resulting in higher power consumption. Furthermore, due to the resistance greater voltage drop occurs from the top of the stack to the transistor source.

[0043] In a first aspect, ferroelectric capacitor processing on backside with hybrid manufacturing is described.

[0044] To provide context, state-of the art DRAM manufacturing involves the fabrication of dense patterns for transistor arrays with front side processing. By contrast, in accordance with one or more embodiments of the present disclosure, select transistors are fabricated on a front side, and memory elements are fabricated on a backside. In a particular embodiment, a minimum pitch needed is about 100 nm by 100 nm, with 4× capacitors or MRAM devices.

[0045] As an exemplary structure, FIG. **2**A illustrates a cross-sectional view of an integrated circuit structure having a front side transistor layer and backside capacitor structure, in accordance with an embodiment of the present disclosure.

[0046] Referring to FIG. **2**A, an integrated circuit structure **200** includes a front side structure **204** on a backside structure **202**. The front side structure **204** includes a device layer **206**A, and a plurality of metallization layers **208** on the device layer **206**A. The structure **200** may be supported by a carrier wafer **210** on the front side structure **204**. The backside structure **202** includes a memory layer **206**B, and a stack of backside conductive structures that terminate at a conductive bump **212**.

[0047] In an embodiment, the device layer **206**A includes Field Effect Transistors (FETs), Xtor, such as nanowire-based or fin-based transistors. It is to be appreciated that, unless indicated otherwise, reference to nanowires herein can indicate nanowires or nanoribbons or even nanosheets. In one such, embodiment, the FETs are used for as select transistors for an underlying backside memory structure coupled thereto. In an embodiment, the device layer **206**A further includes trench contacts, gate contacts and contact vias (VCx). In an embodiment, the device layer **206**A includes a deep via (DV) layer of the front side structure **204**, as is depicted. In an embodiment, the plurality of metallization layers **208** includes increasing metal layer (e.g., M0-M12) and associated via layers (e.g., V0-V3 called out in FIG. **2**A).

[0048] In an embodiment, the memory layer **206**B of the backside structure **202** includes a plurality of capacitor structures in the form of a capacitor array, as is depicted. In one such embodiment, the capacitor array is a ferroelectric capacitor array. In another embodiment, the memory layer **206**B of the backside structure **202** includes a plurality of magnetic random access memory (MRAM) devices. In an embodiment, the memory layer **206**B of the backside structure **202** is coupled to the deep vias (DV) of the device layer **206**A of the front side structure **204**, e.g., which are coupled to select transistors of the device layer **206**A of the front side structure **204**.

[0049] In an embodiment, the backside structure **202** further includes a plurality of backside metal layers (e.g., BM0-BM3) and associated vias. In an embodiment, the backside structure **202** includes one or more power structures, such as ground metal lines. In an embodiment, the backside structure **202** includes one or more non-memory capacitor structures, such as a metal-insulator-metal (MIM) capacitor, as is depicted between backside metal 2 (BM2) and backside metal 3 (BM3), as an exemplary location.

[0050] In a second aspect, low-temperature enabled dense charge pumps using hysteretic capacitors are described.

[0051] To provide context, state-of-the art dense charge pumps involve the use of front-end congested dense capacitors an meta-insulator-metal (MIM) structures for charge pumps, which requires relatively large area.

[0052] In accordance with one or more embodiments of the present disclosure, hysterics capacitors are used for fabricating multi-phase charge pumps. Embodiments may be implemented to alleviate the need for MIM structures, which reduces signal routing. The charge can be stored in the material. Additionally, embodiments can be implemented for SRAM structures as well.

[0053] As an exemplary structure, FIG. **2**B illustrates a plan view of a charge pump including a hysteretic capacitor, in accordance with an embodiment of the present disclosure. FIG. **2**C illustrates a cross-sectional view of a hysteretic capacitor of FIG. **2**B, in accordance with an embodiment of the present disclosure.

[0054] Referring to FIG. **2**B, a charge pump **214** includes various layers of routing **216**, **218**A, **218**B and **220**. A hysteretic capacitor **222** is coupled to the routing **220**. An exemplary embodiments of the structure of the hysteretic capacitor **222** is described in association with FIG. **2**C, as hysteretic capacitor **224**.

[0055] Referring to FIG. **2**C, a hysteretic capacitor **224** includes a front side capacitor structure including electrode layers **226** and **230**, and an intervening dielectric layer **228**, which can be a ferroelectric dielectric layer in one embodiment. The front side capacitor structure **226**/**228**/**230** is coupled to a front side device structure **232**, e.g., a planar, a Fin-FET, or a nanowire structure. Interconnect/via structures **236**/**238** couple the front side capacitor structure **226**/**228**/**230** to a second front side capacitor structure **240** and to a

backside capacitor structure **242** by interconnects and vias **248/250**. A second front side device structure **241** is intervening between the second front side capacitor structure **240** and the backside capacitor structure **242**.

[0056] As an exemplary structure, FIGS. **2**D and **2**E illustrates a plan view and corresponding cross-sectional view of a capacitor array, respectively, in accordance with an embodiment of the present disclosure. FIG. **2**F illustrates magnified cross-sectional views of the capacitor array of FIGS. **2**D and **2**E, in accordance with an embodiment of the present disclosure.

[0057] Referring to FIG. **2**D, a plan view **252** of a capacitor array includes a plurality of cylindrical capacitors each including an outer electrode **250** and an inner electrode **258**, with an intervening dielectric layer **263**. Each of the plurality of cylindrical capacitors is surrounded by a metal strap layer **254**. The metal strap layer **254** is coupled to a collector **259**. Referring to FIG. **2**E, the cross-sectional view **260** is taken through the dashed line of the plan view **252**. The plan view **252** is taken at a location along the dashed line of the cross-sectional view **260**. Details of the structure are provided in the magnified views of FIG. **2**F.

[0058] Referring to the left-hand side of FIG. **2**F, a magnified view of the dashed box of FIG. **2**D illustrated. The magnified view shows the metal strap layer **254**, the collector **259**, and the outer electrode **250**, inner electrode **258**, and intervening dielectric layer **263**. Vertically intervening dielectric material **262** is also depicted.

[0059] Referring to the right-hand side of FIG. **2**F, a magnified view of the dashed box of the left-hand side of FIG. **2**F illustrated. The magnified view shows the outer electrode **250**, inner electrode **258**, and intervening dielectric layer **263**. Vertically intervening dielectric material **262** is also depicted. In an embodiment, as is depicted, the intervening dielectric layer **263** of the capacitor includes three layers **263**A, **263**B and **263**C. In one embodiment, the outer layers **263**A and **263**C are relatively lower dielectric constant but reactively more stable dielectrics, and the central layer **263**B is a relatively higher dielectric constant material, which may be a non-ferroelectric dielectric or a ferroelectric dielectric.

[0060] As an exemplary processing scheme, FIG. **2**G illustrates cross-sectional views representing various operations in a method of fabricating a capacitor array, in accordance with an embodiment of the present disclosure.

[0061] Referring to part (a) of FIG. **2**G, a starting super lattice **265** includes a stack of layers including outer electrode layers **250**, metal strap layers **254**, and dielectric layers **262**.

[0062] Referring to part (b) of FIG. **2**G, a patterned hardmask **266** is formed on the structure **265**.

[0063] Referring to part (c) of FIG. **2**G, the hardmask **266** is used as a mask to pattern trenches **267** in the stack of layers.

[0064] Referring to part (d) of FIG. **2**G, the outer electrode layers **250** and metal strap layers **254** are laterally recessed relative to the dielectric layers **262** to provide a structure **268**.

[0065] Referring to part (e) of FIG. **2**G, the hardmask **266** is removed to provide a structure **269**.

[0066] Referring to part (f) of FIG. **2**G, a capacitor dielectric layer **263** (or layers) is formed on the structure **269**.

[0067] Referring to part (g) of FIG. **2**G, an electrode material **258*a*** is formed on the capacitor dielectric layer **263**.

[0068] Referring to part (h) of FIG. **2**G, the electrode material **258*a*** is planarized to form inner electrode layers **258**, and to complete the capacitor array.

[0069] In a third aspect, approaches for using backside reveal for layering multi-capacitor systems are described.

[0070] To provide context, current approaches involve SRAM macro stacking without array level disaggregation with shared access, which requires a repeat of word lines across layers.

[0071] In accordance with one or more embodiments of the present disclosure, a deep backend via (DBV) or deep via bar mask is used to make word line to word line connections across tiers from front versus back to stack SRAM. Embodiments can be implemented to enable two times local array bandwidth, which can be further funneled out by a MUX.

[0072] As an exemplary structure, FIG. **2**H illustrates a cross-sectional view of a layered multi-capacitor system, in accordance with an embodiment of the present disclosure.

[0073] Referring to FIG. **2**H, a capacitor array **270** includes a front side capacitor structure **271**A and front side deep via bar **271**B, and associated contacts **272** and staggered electrodes **273**. The front side capacitor structure **271**A and front side deep via bar **271**B are coupled to a front side device structure **275**, e.g., a planar, a Fin-FET, or a nanowire structure (with nanowire structures being shown), by vias **274**. Each device includes source/drain structures **275**A and **275**B, gate-all-around structures **275**C, and nanowires **275**D. A backside capacitor structure **276**A and backside deep via bar **276**B are coupled to the front side device structure **275** by vias **277**.

[0074] FIG. **2**I is a layout of a capacitor array system, in accordance with an embodiment of the present disclosure. FIG. **2**J illustrates a cross-sectional view of a charge pump associated with the capacitor array system of FIG. **2**I, in accordance with an embodiment of the present disclosure. FIG. **2**K illustrates a cross-sectional view of another charge pump associated with the capacitor array system of FIG. **2**I, in accordance with an embodiment of the present disclosure.

[0075] Referring to FIG. **2**I, layout **280** includes word lines (WL), bit lines (BL), sense amplifiers (SA), capacitor structures (C), resistors (R), and phase locked loops (PL). The system **280** can have associated power delivery, such as backside power delivery. The system **280** can have associated voltage regulation, level shifters, and charge pumps. The system **280** can have associated array logic (decoders, sense amplifiers, multiplexers). The system **280** can have an associated bit cell array (WLs, BLs, and PLs).

[0076] Referring to FIG. **2**J, a charge pump **281** includes a front side capacitor structure and front side deep via bar (shown collectively as **282**), and associated contacts and staggered electrodes. The front side capacitor structure and front side deep via bar **282** are coupled to a front side device structure **283**, e.g., a planar, a Fin-FET, or a nanowire structure (with Fin-FET structures being shown), by vias. Each device includes source/drain structures **284** and **286**, gate structures **287**, and fins **285**. A front side contact **288** and a backside bit line, BL, are shown as coupled to the front side device structure **283**.

[0077] Referring to FIG. **2**K, a charge pump **290** includes a front side capacitor structure and front side deep via bar (shown collectively as **291**), and associated contacts and staggered electrodes. The front side capacitor structure and front side deep via bar **291** are coupled to a front side device

structure **292**, e.g., a planar, a Fin-FET, or a nanowire structure (with nanowire structures being shown), by vias. Each device includes source/drain structures, gate structures, and nanowires. A front side gate contact **293**, front side bit line (BL) and a backside bit line (BL) are shown as coupled to the front side device structure **292**.

[0078] In accordance with an embodiment of the present disclosure, conductive deep via structures are used between a front side structure and a backside structure, and are fabricated prior to performing epitaxial source or drain formation. To provide context, via structures that extend beneath source or drain structures may be referred to as deep via structures. Embodiments described herein may be directed to deep via formation prior to epitaxial source or drain growth. Embodiments described herein may be directed to back-side power solution for scaled sell sizes. In accordance with an embodiment of the present disclosure, a vertical transistor is fabricated in a location where a deep via structure or backside contact would otherwise be fabricated.

[0079] It is to be appreciated that, as used throughout the disclosure, a sub-fin, a nanowire, a nanoribbon, or a fin described herein may be a silicon sub-fin, a silicon nanowire, a silicon nanoribbon, or a silicon fin. As used throughout, a silicon layer or structure may be used to describe a silicon material composed of a very substantial amount of, if not all, silicon. However, it is to be appreciated that, practically, 100% pure Si may be difficult to form and, hence, could include a tiny percentage of carbon, germanium or tin. Such impurities may be included as an unavoidable impurity or component during deposition of Si or may "contaminate" the Si upon diffusion during post deposition processing. As such, embodiments described herein directed to a silicon layer or structure may include a silicon layer or structure that contains a relatively small amount, e.g., "impurity" level, non-Si atoms or species, such as Ge, C or Sn. It is to be appreciated that a silicon layer or structure as described herein may be undoped or may be doped with dopant atoms such as boron, phosphorous or arsenic.

[0080] It is to be appreciated that, as used throughout the disclosure, a sub-fin, a nanowire, a nanoribbon, or a fin described herein may be a silicon germanium sub-fin, a silicon germanium nanowire, a silicon germanium nanoribbon, or a silicon germanium fin. As used throughout, a silicon germanium layer or structure may be used to describe a silicon germanium material composed of substantial portions of both silicon and germanium, such as at least 5% of both. In some embodiments, the amount of germanium is greater than the amount of silicon. In particular embodiments, a silicon germanium layer or structure includes approximately 60% germanium and approximately 40% silicon ($Si_{40}Ge_{60}$). In other embodiments, the amount of silicon is greater than the amount of germanium. In particular embodiments, a silicon germanium layer or structure includes approximately 30% germanium and approximately 70% silicon ($Si_{70}Ge_{30}$). It is to be appreciated that, practically, 100% pure silicon germanium (referred to generally as SiGe) may be difficult to form and, hence, could include a tiny percentage of carbon or tin. Such impurities may be included as an unavoidable impurity or component during deposition of SiGe or may "contaminate" the SiGe upon diffusion during post deposition processing. As such, embodiments described herein directed to a silicon germanium layer or structure may include a silicon germanium layer or structure that contains a relatively small amount, e.g., "impurity" level, non-Ge and non-Si atoms or species, such as carbon or tin. It is to be appreciated that a silicon germanium layer or structure as described herein may be undoped or may be doped with dopant atoms such as boron, phosphorous or arsenic.

[0081] It is to be appreciated that the integrated circuit structures described above in association with FIGS. **2**A-**2**K can be co-integrated with other backside revealed integrated circuit structures. Additionally or alternatively, other integrated circuit structures can be fabricated using processes described in association with FIGS. **2**A-**2**K. As an example of a backside revealed device, FIG. **3** illustrate a cross-sectional view of a non-planar integrated circuit structure as taken along a gate line, in accordance with an embodiment of the present disclosure.

[0082] Referring to FIG. **3**, a semiconductor structure or device **300** includes a non-planar active region (e.g., a solid fin structure including protruding fin portion **304** and sub-fin region **305**) within a trench isolation region **306**. In another embodiment, instead of a solid fin, the non-planar active region is separated into nanowires (such as nanowires **304**A and **304**B) above sub-fin region **305**, as is represented by the dashed lines. In either case, for ease of description for non-planar integrated circuit structure **300**, a non-planar active region **304** is referenced below as a protruding fin portion. It is to be appreciated that, in one embodiment, there is no bulk substrate coupled to the sub-fin region **305**.

[0083] A gate line **308** is disposed over the protruding portions **304** of the non-planar active region (including, if applicable, surrounding nanowires **304**A and **304**B), as well as over a portion of the trench isolation region **306**. As shown, gate line **308** includes a gate electrode **350** and a gate dielectric layer **352**. In one embodiment, gate line **308** may also include a dielectric cap layer **354**. A gate contact **314**, and overlying gate contact via **316** are also seen from this perspective, along with an overlying metal interconnect **360**, all of which are disposed in inter-layer dielectric stacks or layers **370**. Also seen from the perspective of FIG. **3**, the gate contact **314** is, in one embodiment, disposed over trench isolation region **306**, but not over the non-planar active regions.

[0084] In an embodiment, the semiconductor structure or device **300** is a non-planar device such as, but not limited to, a fin-FET device, a tri-gate device, a nano-ribbon device, or a nano-wire device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines **308** surround at least a top surface and a pair of sidewalls of the three-dimensional body.

[0085] As is also depicted in FIG. **3**, in an embodiment, an interface **380** exists between a protruding fin portion **304** and sub-fin region **305**. The interface **380** can be a transition region between a doped sub-fin region **305** and a lightly or undoped upper fin portion **304**. In one such embodiment, each fin is approximately 10 nanometers wide or less, and sub-fin dopants are supplied from an adjacent solid state doping layer at the sub-fin location. In a particular such embodiment, each fin is less than 10 nanometers wide. In another embodiment, the sub-fin region is a dielectric material, formed by recessing the fin through a wet or dry etch, and filling the recessed cavity with a conformal or flowable dielectric.

[0086] Although not depicted in FIG. **3**, it is to be appreciated that source or drain regions of or adjacent to the protruding fin portions **304** are on either side of the gate line **308**, i.e., into and out of the page. In one embodiment, the source or drain regions are doped portions of original material of the protruding fin portions **304**. In another embodiment, the material of the protruding fin portions **304** is removed and replaced with another semiconductor material, e.g., by epitaxial deposition to form discrete epitaxial nubs or non-discrete epitaxial structures. In either embodiment, the source or drain regions may extend below the height of dielectric layer of trench isolation region **306**, i.e., into the sub-fin region **305**. In accordance with an embodiment of the present disclosure, the more heavily doped sub-fin regions, i.e., the doped portions of the fins below interface **380**, inhibits source to drain leakage through this portion of the bulk semiconductor fins.

[0087] With reference again to FIG. **3**, in an embodiment, fins **304/305** (and, possibly nanowires **304**A and **304**B) are composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof. In one embodiment, the concentration of silicon atoms is greater than 93%. In another embodiment, fins **304/305** are composed of a group III-V material, such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide, or a combination thereof. Trench isolation region **306** may be composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0088] Gate line **308** may be composed of a gate electrode stack which includes a gate dielectric layer **352** and a gate electrode layer **350**. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-k material. For example, in one embodiment, the gate dielectric layer is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer may include a layer of native oxide formed from the top few layers of the substrate fin **304**. In an embodiment, the gate dielectric layer is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride. In some implementations, a portion of the gate dielectric is a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate.

[0089] In one embodiment, the gate electrode is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides. In a specific embodiment, the gate electrode is composed of a non-workfunction-setting fill material formed above a metal workfunction-setting layer. The gate electrode layer may consist of a P-type workfunction metal or an N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a conductive fill layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV. In some implementations, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0090] Spacers associated with the gate electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0091] Gate contact **314** and overlying gate contact via **316** may be composed of a conductive material. In an embodiment, one or more of the contacts or vias are composed of a metal species. The metal species may be a pure metal, such as tungsten, nickel, or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material).

[0092] In an embodiment (although not shown), a contact pattern which is essentially perfectly aligned to an existing gate pattern **308** is formed while eliminating the use of a lithographic step with exceedingly tight registration budget. In one such embodiment, the self-aligned approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in conventional

approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

[0093] In an embodiment, providing structure **300** involves fabrication of the gate stack structure **308** by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF_6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH_4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

[0094] Referring again to FIG. **3**, the arrangement of semiconductor structure or device **300** places the gate contact over isolation regions. Such an arrangement may be viewed as inefficient use of layout space. In another embodiment, however, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region, e.g., over a sub-fin **305**, and in a same layer as a trench contact via.

[0095] It is to be appreciated that not all aspects of the processes described above need be practiced to fall within the spirit and scope of embodiments of the present disclosure. For example, in one embodiment, dummy gates need not ever be formed prior to fabricating gate contacts over active portions of the gate stacks. The gate stacks described above may actually be permanent gate stacks as initially formed. Also, the processes described herein may be used to fabricate one or a plurality of semiconductor devices. The semiconductor devices may be transistors or like devices. For example, in an embodiment, the semiconductor devices are a metal-oxide semiconductor (MOS) transistors for logic or memory, or are bipolar transistors. Also, in an embodiment, the semiconductor devices have a three-dimensional architecture, such as a trigate device, an independently accessed double gate device, a gate-all-around (GAA) device, a nanowire device, a nanoribbon device, or a FIN-FET. One or more embodiments may be particularly useful for fabricating semiconductor devices at a sub-10 nanometer (10 nm) technology node.

[0096] In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

[0097] In an embodiment, as is also used throughout the present description, metal lines or interconnect line material (and via material) is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers (e.g., layers including one or more of Ta, TaN, Ti or TiN), stacks of different metals or alloys, etc. Thus, the interconnect lines may be a single material layer, or may be formed from several layers, including conductive liner layers and fill layers. Any suitable deposition process, such as electroplating, chemical vapor deposition or physical vapor deposition, may be used to form interconnect lines. In an embodiment, the interconnect lines are composed of a conductive material such as, but not limited to, Cu, Al, Ti, Zr, Hf, V, Ru, Co, Ni, Pd, Pt, W, Ag, Au or alloys thereof. The interconnect lines are also sometimes referred to in the art as traces, wires, lines, metal, or simply interconnect.

[0098] In an embodiment, as is also used throughout the present description, hardmask materials, capping layers, or plugs are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, different hardmask, capping or plug materials may be used in different regions so as to provide different growth or etch selectivity to each other and to the underlying dielectric and metal layers. In some embodiments, a hardmask layer, capping or plug layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. Other hardmask, capping or plug layers known in the arts may be used depending upon the particular implementation. The hardmask, capping or plug layers maybe formed by CVD, PVD, or by other deposition methods.

[0099] In an embodiment, as is also used throughout the present description, lithographic operations are performed using 193 nm immersion lithography (i193), EUV and/or EBDW lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a trilayer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

[0100] In another aspect, integrated circuit structures described herein may be fabricated using a backside reveal of front side structures fabrication approach. In some exemplary embodiments, reveal of the backside of a transistor or other device structure entails wafer-level backside processing. In contrast to a conventional TSV-type technology, a reveal of the backside of a transistor as described herein may be performed at the density of the device cells, and even within sub-regions of a device. Furthermore, such a reveal of the backside of a transistor may be performed to remove substantially all of a donor substrate upon which a device layer was disposed during front side device processing. As such, a microns-deep TSV becomes unnecessary with the thickness of semiconductor in the device cells following a reveal of the backside of a transistor potentially being only tens or hundreds of nanometers.

[0101] Reveal techniques described herein may enable a paradigm shift from "bottom-up" device fabrication to "center-out" fabrication, where the "center" is any layer that is employed in front side fabrication, revealed from the backside, and again employed in backside fabrication. Processing of both a front side and revealed backside of a device structure may address many of the challenges associated with fabricating 3D ICs when primarily relying on front side processing.

[0102] A reveal of the backside of a transistor approach may be employed for example to remove at least a portion of a carrier layer and intervening layer of a donor-host substrate assembly, for example as illustrated in FIGS. **4**A-**4**H and **5**A-**5**H, described below. The process flow begins with an input of a donor-host substrate assembly. A thickness of a carrier layer in the donor-host substrate is polished (e.g., CMP) and/or etched with a wet or dry (e.g., plasma) etch process. Any grind, polish, and/or wet/dry etch process known to be suitable for the composition of the carrier layer may be employed. For example, where the carrier layer is a group IV semiconductor (e.g., silicon) a CMP slurry known to be suitable for thinning the semiconductor may be employed. Likewise, any wet etchant or plasma etch process known to be suitable for thinning the group IV semiconductor may also be employed.

[0103] In some embodiments, the above is preceded by cleaving the carrier layer along a fracture plane substantially parallel to the intervening layer. The cleaving or fracture process may be utilized to remove a substantial portion of the carrier layer as a bulk mass, reducing the polish or etch time needed to remove the carrier layer. For example, where a carrier layer is 400-900 μm in thickness, 100-700 μm may be cleaved off by practicing any blanket implant known to promote a wafer-level fracture. In some exemplary embodiments, a light element (e.g., H, He, or Li) is implanted to a uniform target depth within the carrier layer where the fracture plane is desired. Following such a cleaving process, the thickness of the carrier layer remaining in the donor-host substrate assembly may then be polished or etched to complete removal. Alternatively, where the carrier layer is not fractured, the grind, polish and/or etch operation may be employed to remove a greater thickness of the carrier layer.

[0104] Next, exposure of an intervening layer is detected. Detection is used to identify a point when the backside surface of the donor substrate has advanced to nearly the device layer. Any endpoint detection technique known to be suitable for detecting a transition between the materials employed for the carrier layer and the intervening layer may be practiced. In some embodiments, one or more endpoint criteria are based on detecting a change in optical absorbance or emission of the backside surface of the donor substrate during the polishing or etching performed. In some other embodiments, the endpoint criteria are associated with a change in optical absorbance or emission of byproducts during the polishing or etching of the donor substrate backside surface. For example, absorbance or emission wavelengths associated with the carrier layer etch byproducts may change as a function of the different compositions of the carrier layer and intervening layer. In other embodiments, the endpoint criteria are associated with a change in mass of species in byproducts of polishing or etching the backside surface of the donor substrate. For example, the byproducts of processing may be sampled through a quadrupole mass analyzer and a change in the species mass may be correlated to the different compositions of the carrier layer and intervening layer. In another exemplary embodiment, the endpoint criteria is associated with a change in friction between a backside surface of the donor substrate and a polishing surface in contact with the backside surface of the donor substrate.

[0105] Detection of the intervening layer may be enhanced where the removal process is selective to the carrier layer relative to the intervening layer as non-uniformity in the carrier removal process may be mitigated by an etch rate delta between the carrier layer and intervening layer. Detection may even be skipped if the grind, polish and/or etch operation removes the intervening layer at a rate sufficiently below the rate at which the carrier layer is removed. If an endpoint criteria is not employed, a grind, polish and/or etch operation of a predetermined fixed duration may stop on the intervening layer material if the thickness of the intervening layer is sufficient for the selectivity of the etch. In some examples, the carrier etch rate: intervening layer etch rate is 3:1-10:1, or more.

[0106] Upon exposing the intervening layer, at least a portion of the intervening layer may be removed. For example, one or more component layers of the intervening layer may be removed. A thickness of the intervening layer may be removed uniformly by a polish, for example. Alternatively, a thickness of the intervening layer may be removed with a masked or blanket etch process. The process may employ the same polish or etch process as that employed to thin the carrier, or may be a distinct process with distinct process parameters. For example, where the intervening layer provides an etch stop for the carrier removal process, the latter operation may employ a different polish or etch process that favors removal of the intervening layer over removal of the device layer.

[0107] Where less than a few hundred nanometers of intervening layer thickness is to be removed, the removal process may be relatively slow, optimized for across-wafer uniformity, and more precisely controlled than that employed for removal of the carrier layer. A CMP process employed may, for example employ a slurry that offers very high selectively (e.g., 100:1-300:1, or more) between semiconductor (e.g., silicon) and dielectric material (e.g., SiO) surrounding the device layer and embedded within the intervening layer, for example, as electrical isolation between adjacent device regions.

[0108] For embodiments where the device layer is revealed through complete removal of the intervening layer, backside processing may commence on an exposed backside of the device layer or specific device regions there in. In some embodiments, the backside device layer processing includes a further polish or wet/dry etch through a thickness of the device layer disposed between the intervening layer and a device region previously fabricated in the device layer, such as a source or drain region.

[0109] In some embodiments where the carrier layer, intervening layer, or device layer backside is recessed with a wet and/or plasma etch, such an etch may be a patterned etch or a materially selective etch that imparts significant non-planarity or topography into the device layer backside surface. As described further below, the patterning may be within a device cell (i.e., "intra-cell" patterning) or may be across device cells (i.e., "inter-cell" patterning). In some patterned etch embodiments, at least a partial thickness of the intervening layer is employed as a hard mask for

backside device layer patterning. Hence, a masked etch process may preface a correspondingly masked device layer etch.

[0110] The above described processing scheme may result in a donor-host substrate assembly that includes IC devices that have a backside of an intervening layer, a backside of the device layer, and/or backside of one or more semiconductor regions within the device layer, and/or front side metallization revealed. Additional backside processing of any of these revealed regions may then be performed during downstream processing.

[0111] In accordance with one or more embodiments of the present disclosure, in order to enable backside access to a partitioned source or drain contact structure, a double-sided device processing scheme may be practiced at the wafer-level. In some exemplary embodiments, a large formal substrate (e.g., 300 or 450 mm diameter) wafer may be processed. In an exemplary processing scheme, a donor substrate including a device layer is provided. In some embodiments, the device layer is a semiconductor material that is employed by an IC device. As one example, in a transistor device, such as a field effect transistor (FET), the channel semiconductor is formed from the semiconductor device layer. As another example, for an optical device, such as a photodiode, the drift and/or gain semiconductor is formed from the device layer. The device layer may also be employed in a passive structure with an IC device. For example, an optical waveguide may employ semiconductor patterned from the device layer.

[0112] In some embodiments, the donor substrate includes a stack of material layers. Such a material stack may facilitate subsequent formation of an IC device stratum that includes the device layer but lacks other layers of the donor substrate. In an exemplary embodiment, the donor substrate includes a carrier layer separated from the device layer by one or more intervening material layers. The carrier layer is to provide mechanical support during front side processing of the device layer. The carrier may also provide the basis for crystallinity in the semiconductor device layer. The intervening layer(s) may facilitate removal of the carrier layer and/or the reveal of the device layer backside.

[0113] Front side fabrication operations are then performed to form a device structure that includes one or more regions in the device layer. Any known front side processing techniques may be employed to form any known IC device and exemplary embodiments are further described elsewhere herein. A front side of the donor substrate is then joined to a host substrate to form a device-host assembly. The host substrate is to provide front side mechanical support during backside processing of the device layer. The host substrate may also entail integrated circuitry with which the IC devices fabricated on the donor substrate are interconnected. For such embodiments, joining of the host and donor substrate may further entail formation of 3D interconnect structures through hybrid (dielectric/metal) bonding. Any known host substrate and wafer-level joining techniques may be employed.

[0114] The process flow continues where the backside of the device stratum is revealed by removing at least a portion of the carrier layer. In some further embodiments, portions of any intervening layer and/or front side materials deposited over the device layer may also be removed during the reveal operation. As described elsewhere herein in the context of some exemplary embodiments, an intervening layer(s) may facilitate a highly-uniform exposure of the device stratum backside, for example serving as one or more of an etch marker or etch stop employed in the wafer-level backside reveal process. Device stratum surfaces exposed from the backside are processed to form a double-side device stratum. Native materials, such as any of those of the donor substrate, which interfaced with the device regions may then be replaced with one or more non-native materials. For example, a portion of a semiconductor device layer or intervening layer may be replaced with one or more other semiconductor, metal, or dielectric materials. In some further embodiments, portions of the front side materials removed during the reveal operation may also be replaced. For example, a portion of a dielectric spacer, gate stack, or contact metallization formed during front side device fabrication may be replaced with one or more other semiconductor, metal, or dielectric materials during backside deprocessing/reprocessing of the front side device. In still other embodiments, a second device stratum or metal interposer is bonded to the reveal backside.

[0115] The above process flow provides a device stratum-host substrate assembly. The device stratum-host assembly may then be further processed. For example, any known technique may be employed to singulate and package the device stratum-host substrate assembly. Where the host substrate is entirely sacrificial, packaging of the device stratum-host substrate may entail separation of the host substrate from the device stratum. Where the host substrate is not entirely sacrificial (e.g., where the host substrate also includes a device stratum), the device stratum-host assembly output may be fed back as a host substrate input during a subsequent iteration of the above process flow.

[0116] Iteration of the above approach may thus form a wafer-level assembly of any number of double-side device strata, each only tens or hundreds of nanometers in thickness, for example. In some embodiments, and as further described elsewhere herein, one or more device cells within a device stratum are electrically tested, for example as a yield control point in the fabrication of a wafer-level assembly of double-side device strata. In some embodiments, the electrical test entails backside device probing.

[0117] FIGS. **4**A-**4**H illustrate plan views of a substrate processed with double-sided device processing methods, in accordance with some embodiments. FIGS. **5**A-**5**H illustrate cross-sectional views of a substrate processed with double-sided device processing methods, in accordance with some embodiments.

[0118] As shown in FIGS. **4**A and **5**A, donor substrate **401** includes a plurality of IC die **411** in an arbitrary spatial layout over a front side wafer surface. Front side processing of IC die **411** may have been performed following any techniques to form any device structures. In exemplary embodiments, die **411** include one or more semiconductor regions within device layer **415**. An intervening layer **410** separates device layer **415** from carrier layer **405**. In the exemplary embodiment, intervening layer **410** is in direct contact with both carrier layer **405** and device layer **415**. Alternatively, one or more spacer layers may be disposed between intervening layer **410** and device layer **415** and/or carrier layer **405**. Donor substrate **401** may further include other layers, for example disposed over device layer **415** and/or below carrier layer **405**.

[0119] Device layer **415** may include one or more layers of any device material composition known to be suitable for a

particular IC device, such as, but not limited to, transistors, diodes, and resistors. In some exemplary embodiments, device layer **415** includes one or more group IV (i.e., IUPAC group 14) semiconductor material layers (e.g., Si, Ge, SiGe), group III-V semiconductor material layers (e.g., GaAs, InGaAs, InAs, InP), or group III-N semiconductor material layers (e.g., GaN, AlGaN, InGaN). Device layer **415** may also include one or more semiconductor transition metal dichalcogenide (TMD or TMDC) layers. In other embodiments, device layer **415** includes one or more graphene layer, or a graphenic material layer having semiconductor properties. In still other embodiments, device layer **415** includes one or more oxide semiconductor layers. Exemplary oxide semiconductors include oxides of a transition metal (e.g., IUPAC group 4-10) or post-transition metal (e.g., IUPAC groups 11-14). In advantageous embodiments, the oxide semiconductor includes at least one of Cu, Zn, Sn, Ti, Ni, Ga, In, Sr, Cr, Co, V, or Mo. The metal oxides may be suboxides (A_2O) monoxides (AO), binary oxides (AO_2), ternary oxides (ABO_3), and mixtures thereof. In other embodiments, device layer **415** includes one or more magnetic, ferromagnetic, ferroelectric material layer. For example device layer **415** may include one or more layers of any material known to be suitable for an tunneling junction device, such as, but not limited to a magnetic tunneling junction (MTJ) device.

[0120] In some embodiments, device layer **415** is substantially monocrystalline. Although monocrystalline, a significant number of crystalline defects may nonetheless be present. In other embodiments, device layer **415** is amorphous or nanocrystalline. Device layer **415** may be any thickness (e.g., z-dimension in FIG. **5**A). In some exemplary embodiments, device layer **415** has a thickness greater than a z-thickness of at least some of the semiconductor regions employed by die **411** as functional semiconductor regions of die **411** built on and/or embedded within device layer **415** need not extend through the entire thickness of device layer **415**. In some embodiments, semiconductor regions of die **411** are disposed only within a top-side thickness of device layer **415** demarked in FIG. **5**A by dashed line **412**. For example, semiconductor regions of die **411** may have a z-thickness of 200-300 nm, or less, while device layer may have a z-thickness of 700-1000 nm, or more. As such, around 600 nm of device layer thickness may separate semiconductor regions of die **411** from intervening layer **410**.

[0121] Carrier layer **405** may have the same material composition as device layer **415**, or may have a material composition different than device layer **415**. For embodiments where carrier layer **405** and device layer **415** have the same composition, the two layers may be identified by their position relative to intervening layer **410**. In some embodiments where device layer **415** is a crystalline group IV, group III-V or group III-N semiconductor, carrier layer **405** is the same crystalline group IV, group III-V or group III-N semiconductor as device layer **415**. In alternative embodiments, where device layer **415** is a crystalline group IV, group III-V or group III-N semiconductor, carrier layer **405** is a different crystalline group IV, group III-V or group III-N semiconductor than device layer **415**. In still other embodiments, carrier layer **405** may include, or be, a material onto which device layer **415** transferred, or grown upon. For example, carrier layer may include one or more amorphous oxide layers (e.g., glass) or crystalline oxide layer (e.g., sapphire), polymer sheets, or any material(s) built up or laminated into a structural support known to be suitable as a carrier during IC device processing. Carrier layer **405** may be any thickness (e.g., z-dimension in FIG. **5**A) as a function of the carrier material properties and the substrate diameter. For example, where the carrier layer **405** is a large format (e.g., 300-450 mm) semiconductor substrate, the carrier layer thickness may be 700-1000 μm, or more.

[0122] In some embodiments, one or more intervening layers **410** are disposed between carrier layer **405** and device layer **415**. In some exemplary embodiments, an intervening layer **410** is compositionally distinct from carrier layer **405** such that it may serve as a marker detectable during subsequent removal of carrier layer **405**. In some such embodiments, an intervening layer **410** has a composition that, when exposed to an etchant of carrier layer **405** will etch at a significantly slower rate than carrier layer **405** (i.e., intervening layer **410** functions as an etch stop for a carrier layer etch process). In further embodiments, intervening layer **410** has a composition distinct from that of device layer **415**. Intervening layer **410** may be a metal, semiconductor, or dielectric material, for example.

[0123] In some exemplary embodiments where at least one of carrier layer **405** and device layer **415** are crystalline semiconductors, intervening layer **410** is also a crystalline semiconductor layer. Intervening layer **410** may further have the same crystallinity and crystallographic orientation as carrier layer **405** and/or device layer **415**. Such embodiments may have the advantage of reduced donor substrate cost relative to alternative embodiments where intervening layer **410** is a material that necessitates bonding (e.g., thermal-compression bonding) of intervening layer **410** to intervening layer **410** and/or to carrier layer **405**.

[0124] For embodiments where intervening layer **410** is a semiconductor, one or more of the primary semiconductor lattice elements, alloy constituents, or impurity concentrations may vary between at least carrier layer **405** and intervening layer **410**. In some embodiments where at least carrier layer **405** is a group IV semiconductor, intervening layer **410** may also be a group IV semiconductor, but of a different group IV element or alloy and/or doped with an impurity species to an impurity level different than that of carrier layer **405**. For example, intervening layer **410** may be a silicon-germanium alloy epitaxially grown on a silicon carrier. For such embodiments, a pseudomorphic intervening layer may be grown heteroepitaxially to any thickness below the critical thickness. Alternatively, the intervening layer **410** may be a relaxed buffer layer having a thickness greater than the critical thickness.

[0125] In other embodiments, where at least carrier layer **405** is a group III-V semiconductor, intervening layer **410** may also be a group III-V semiconductor, but of a different group III-V alloy and/or doped with an impurity species to an impurity level different than that of carrier layer **405**. For example, intervening layer **410** may be an AlGaAs alloy epitaxially grown on a GaAs carrier. In some other embodiments where both carrier layer **405** and device layer **415** are crystalline semiconductors, intervening layer **410** is also a crystalline semiconductor layer, which may further have the same crystallinity and crystallographic orientation as carrier layer **405** and/or device layer **415**.

[0126] In embodiments where both carrier layer **405** and intervening layer **410** are of the same or different primary semiconductor lattice elements, impurity dopants may dif-

ferentiate the carrier and intervening layer. For example, intervening layer **410** and carrier layer **405** may both be silicon crystals with intervening layer **410** lacking an impurity present in carrier layer **405**, or doped with an impurity absent from carrier layer **405**, or doped to a different level with an impurity present in carrier layer **405**. The impurity differentiation may impart etch selectivity between the carrier and intervening layer, or merely introduce a detectable species.

[0127] Intervening layer **410** may be doped with impurities that are electrically active (i.e., rendering it an n-type or p-type semiconductor), or not, as the impurity may provide any basis for detection of the intervening layer **410** during subsequent carrier removal. Exemplary electrically active impurities for some semiconductor materials include group III elements (e.g., B), group IV elements (e.g., P). Any other element may be employed as a non-electrically active species. Impurity dopant concentration within intervening layer **410** need only vary from that of carrier layer **405** by an amount sufficient for detection, which may be predetermined as a function of the detection technique and detector sensitivity.

[0128] As described further elsewhere herein, intervening layer **410** may have a composition distinct from device layer **415**. In some such embodiments, intervening layer **410** may have a different band gap than that of device layer **415**. For example, intervening layer **410** may have a wider band-gap than device layer **415**.

[0129] In embodiments where intervening layer **410** includes a dielectric material, the dielectric material may be an inorganic material (e.g., SiO, SiN, SiON, SiOC, hydrogen silsesquioxane, methyl silsesquioxane) or organic material (polyimide, polynorbornenes, benzocyclobutene). For some dielectric embodiments, intervening layer **410** may be formed as an embedded layer (e.g., SiOx through implantation of oxygen into a silicon device and/or carrier layer). Other embodiments of a dielectric intervening layer may necessitate bonding (e.g., thermal-compression bonding) of carrier layer **405** to device layer **415**. For example, where donor substrate **401** is a semiconductor-on-oxide (SOI) substrate, either or both of carrier layer **405** and device layer **415** may be oxidized and bonded together to form a SiO intervening layer **410**. Similar bonding techniques may be employed for other inorganic or organic dielectric materials.

[0130] In some other embodiments, intervening layer **410** includes two or more materials laterally spaced apart within the layer. The two or more materials may include a dielectric and a semiconductor, a dielectric and a metal, a semiconductor and a metal, a dielectric and a metal, two different dielectric, two different semiconductors, or two different metals. Within such an intervening layer, a first material may surround islands of the second material that extend through the thickness of the intervening layer. For example, an intervening layer may include a field isolation dielectric that surrounds islands of semiconductor, which extend through the thickness of the intervening layer. The semiconductor may be epitaxially grown within openings of a patterned dielectric or the dielectric material may be deposited within openings of a patterned semiconductor.

[0131] In some exemplary embodiments, semiconductor features, such as fins or mesas, are etched into a front side surface of a semiconductor device layer. Trenches surrounding these features may be subsequently backfilled with an isolation dielectric, for example following any known shallow trench isolation (STI) process. One or more of the semiconductor feature or isolation dielectric may be employed for terminating a backside carrier removal process, for example as a backside reveal etch stop. In some embodiments, a reveal of trench isolation dielectric may stop, significantly retard, or induce a detectable signal for terminating a backside carrier polish. For example, a CMP polish of carrier semiconductor employing a slurry that has high selectivity favoring removal of carrier semiconductor (e.g., Si) over removal of isolation dielectric (e.g., SiO) may be significantly slowed upon exposure of a (bottom) surface of the trench isolation dielectric surrounding semiconductor features including the device layer. Because the device layer is disposed on a front side of intervening layer, the device layer need not be directly exposed to the backside reveal process.

[0132] Notably, for embodiments where the intervening layer includes both semiconductor and dielectric, the intervening layer thickness may be considerably greater than the critical thickness associated with the lattice mismatch of the intervening layer and carrier. Whereas an intervening layer below critical thickness may be an insufficient thickness to accommodate non-uniformity of a wafer-level backside reveal process, embodiments with greater thickness may advantageously increase the backside reveal process window. Embodiments with pin-holed dielectric may otherwise facilitate subsequent separation of carrier and device layers as well as improve crystal quality within the device layer.

[0133] Semiconductor material within intervening layers that include both semiconductor and dielectric may also be homoepitaxial. In some exemplary embodiments, a silicon epitaxial device layer is grown through a pin-holed dielectric disposed over a silicon carrier layer.

[0134] Continuing with description of FIGS. **4**A and **5**A, intervening layer **410** may also be a metal. For such embodiments, the metal may be of any composition known to be suitable for bonding to carrier layer **405** or device layer **415**. For example, either or both of carrier layer **405** and device layer **415** may be finished with a metal, such as, but not limited to Au or Pt, and subsequently bonded together, for example to form an Au or Pt intervening layer **410**. Such a metal may also be part of an intervening layer that further includes a patterned dielectric surrounding metal features.

[0135] Intervening layer **410** may be of any thickness (e.g., z-height in FIG. **5**A). The intervening layer should be sufficiently thick to ensure the carrier removal operation can be reliably terminated before exposing device regions and/or device layer **415**. Exemplary thicknesses for intervening layer **410** range from a few hundred nanometers to a few micrometers and may vary as a function of the amount of carrier material that is to be removed, the uniformity of the carrier removal process, and the selectivity of the carrier removal process, for example. For embodiments where the intervening layer has the same crystallinity and crystallographic orientation as carrier layer **405**, the carrier layer thickness may be reduced by the thickness of intervening layer **410**. In other words, intervening layer **410** may be a top portion of a 700-1000 μm thick group IV crystalline semiconductor substrate also employed as the carrier layer. In pseudomorphic heteroepitaxial embodiments, intervening layer thickness may be limited to the critical thickness. For heteroepitaxial intervening layer embodiments employing aspect ratio trapping (ART) or another fully relaxed buffer architecture, the intervening layer may have any thickness.

[0136] As further illustrated in FIGS. 4B and 5B, donor substrate **401** may be joined to a host substrate **402** to form a donor-host substrate assembly **403**. In some exemplary embodiments, a front side surface of donor substrate **401** is joined to a surface of host substrate **402** such that device layer **415** is proximal host substrate **402** and carrier layer **405** is distal from host substrate **402**. Host substrate **402** may be any substrate known to be suitable for joining to device layer **415** and/or a front side stack fabricated over device layer **415**. In some embodiments, host substrate **402** includes one or more additional device strata. For example, host substrate **402** may further include one or more device layer (not depicted). Host substrate **402** may include integrated circuitry with which the IC devices fabricated in a device layer of host substrate **402** are interconnected, in which case joining of device layer **415** to host substrate **402** may further entail formation of 3D interconnect structures through the wafer-level bond.

[0137] Although not depicted in detail by FIG. 5B, any number of front side layers, such as interconnect metallization levels and interlayer dielectric (ILD) layers, may be present between device layer **415** and host substrate **402**. Any technique may be employed to join host substrate **402** and donor substrate **401**. In some exemplary embodiments further described elsewhere herein, the joining of donor substrate **401** to host substrate **402** is through metal-metal, oxide-oxide, or hybrid (metal/oxide-metal/oxide) thermal compression bonding.

[0138] With host substrate **402** facing device layer **415** on a side opposite carrier layer **405**, at least a portion of carrier layer **405** may be removed as further illustrated in FIGS. 4C and 5C. Where the entire carrier layer **405** is removed, donor-host substrate assembly **403** maintains a highly uniform thickness with planar backside and front side surfaces. Alternatively, carrier layer **405** may be masked and intervening layer **410** exposed only in unmasked sub-regions to form a non-planar backside surface. In the exemplary embodiments illustrated by FIGS. 4C and 5C, carrier layer **405** is removed from the entire backside surface of donor-host substrate assembly **403**. Carrier layer **405** may be removed, for example by cleaving, grinding, and/or polishing (e.g., chemical-mechanical polishing), and/or wet chemical etching, and/or plasma etching through a thickness of the carrier layer to expose intervening layer **410**. One or more operations may be employed to remove carrier layer **405**. Advantageously, the removal operation(s) may be terminated based on duration or an endpoint signal sensitive to exposure of intervening layer **410**.

[0139] In further embodiments, for example as illustrated by FIGS. 4D and 5D, intervening layer **410** is also at least partially etched to expose a backside of device layer **415**. At least a portion of intervening layer **410** may be removed subsequent to its use as a carrier layer etch stop and/or carrier layer etch endpoint trigger. Where the entire intervening layer **410** is removed, donor-host substrate assembly **403** maintains a highly uniform device layer thickness with planar backside and front side surfaces afforded by the intervening layer **410** being much thinner than the carrier layer. Alternatively, intervening layer **410** may be masked and device layer **415** exposed only in unmasked sub-regions, thereby forming a non-planar backside surface. In the exemplary embodiments illustrated by FIGS. 4D and 5D, intervening layer **410** is removed from the entire backside surface of donor-host substrate assembly **403**. Intervening layer **410** may be so removed, for example, by polishing (e.g., chemical-mechanical polishing), and/or blanket wet chemical etching, and/or blanket plasma etching through a thickness of the intervening layer to expose device layer **415**. One or more operations may be employed to remove intervening layer **410**. Advantageously, the removal operation(s) may be terminated based on duration or an endpoint signal sensitive to exposure of device layer **415**.

[0140] In some further embodiments, for example as illustrated by FIGS. 4E and 5E, device layer **415** is partially etched to expose a backside of a device structure previously formed from during front side processing. At least a portion of device layer **415** may be removed subsequent to its use in fabricating one or more of the device semiconductor regions, and/or its use as an intervening layer etch stop or endpoint trigger. Where device layer **415** is thinned over the entire substrate area, donor-host substrate assembly **403** maintains a highly uniform reduced thickness with planar back and front surfaces. Alternatively, device layer **415** may be masked and device structures (e.g., device semiconductor regions) selectively revealed only in unmasked sub-regions, thereby forming a non-planar backside surface. In the exemplary embodiments illustrated by FIGS. 4E and 5E, device layer **415** is thinned over the entire backside surface of donor-host substrate assembly **403**. Device layer **415** may be thinned, for example by polishing (e.g., chemical-mechanical polishing), and/or wet chemical etching, and/or plasma etching through a thickness of the device layer to expose one or more device semiconductor regions, and/or one or more other device structures (e.g., front side device terminal contact metallization, spacer dielectric, etc.) previously formed during front side processing. One or more operations may be employed to thin device layer **415**. Advantageously, the device layer thinning may be terminated based on duration or an endpoint signal sensitive to exposure of patterned features within device layer **415**. For example, where front side processing forms device isolation features (e.g., shallow trench isolation), backside thinning of device layer **415** may be terminated upon exposing the isolation dielectric material.

[0141] A non-native material layer may be deposited over a backside surface of an intervening layer, device layer, and/or specific device regions within device layer **415**, and/or over or more other device structures (e.g., front side device terminal contact metallization, spacer dielectric, etc.). One or more materials exposed (revealed) from the backside may be covered with non-native material layer or replaced with such a material. In some embodiments, illustrated by FIGS. 4F and 5F, non-native material layer **420** is deposited on device layer **415**. Non-native material layer **420** may be any material having a composition and/or microstructure distinct from that of the material removed to reveal the backside of the device stratum. For example, where intervening layer **410** is removed to expose device layer **415**, non-native material layer **420** may be another semiconductor of different composition or microstructure than that of intervening layer **410**. In some such embodiments where device layer **415** is a group III-N semiconductor, non-native material layer **420** may also be a group III-N semiconductor of the same or different composition that is regrown upon a revealed backside surface of a group III-N device region. This material may be epitaxially regrown from the revealed group III-N device region, for example, to have better crystal quality than that of the material removed,

and/or to induce strain within the device layer and/or device regions within the device layer, and/or to form a vertical (e.g., z-dimension) stack of device semiconductor regions suitable for a stacked device.

[0142] In some other embodiments where device layer **415** is a group III-V semiconductor, non-native material layer **420** may also be a group III-V semiconductor of the same or different composition that is regrown upon a revealed backside surface of a group III-V device region. This material may be epitaxially regrown from the revealed group III-V device region, for example, to have relatively better crystal quality than that of the material removed, and/or to induce strain within the device layer or a specific device region within the device layer, and/or to form a vertical stack of device semiconductor regions suitable for a stacked device.

[0143] In some other embodiments where device layer **415** is a group IV semiconductor, non-native material layer **420** may also be a group IV semiconductor of the same or different composition that is regrown upon a revealed backside surface of a group IV device region. This material may be epitaxially regrown from the revealed group IV device region, for example, to have relatively better crystal quality than that of the material removed, and/or to induce strain within the device region, and/or to form a stack of device semiconductor regions suitable for a stacked device.

[0144] In some other embodiments, non-native material layer **420** is a dielectric material, such as, but not limited to SiO, SiON, SiOC, hydrogen silsesquioxane, methyl silsesquioxane, polyimide, polynorbornenes, benzocyclobutene, or the like. Deposition of such a dielectric may serve to electrically isolate various device structures, such as semiconductor device regions, that may have been previously formed during front side processing of donor substrate **401**.

[0145] In some other embodiments, non-native material layer **420** is a conductive material, such as any elemental metal or metal alloy known to be suitable for contacting one or more surfaces of device regions revealed from the backside. In some embodiments, non-native material layer **420** is a metallization suitable for contacting a device region revealed from the backside, such as a transistor source or drain region. In embodiments, intermetallic contacts such as NixSiy, TixSiy, Ni:Si:Pt, TiSi, CoSi, etc. may be formed. Additionally, implants may be used to enable robust contacts (e.g., P, Ge, B etc.).

[0146] In some embodiments, non-native material layer **420** is a stack of materials, such as a FET gate stack that includes both a gate dielectric layer and a gate electrode layer. As one example, non-native material layer **420** may be a gate dielectric stack suitable for contacting a semiconductor device region revealed from the backside, such as a transistor channel region. Any of the other the materials described as options for device layer **415** may also be deposited over a backside of device layer **415** and/or over device regions formed within device layer **415**. For example, non-native material layer **420** may be any of the oxide semiconductors, TMDC, or tunneling materials described above, which may be deposited on the backside, for example, to incrementally fabricate vertically-stacked device strata.

[0147] Backside wafer-level processing may continue in any manner known to be suitable for front side processing. For example, non-native material layer **420** may be patterned into active device regions, device isolation regions, device contact metallization, or device interconnects using any known lithographic and etch techniques. Backside wafer-level processing may further fabricate one or more interconnect metallization levels coupling terminals of different devices into an IC. In some embodiments further described elsewhere herein, backside processing may be employed to interconnect a power bus to various device terminals within an IC.

[0148] In some embodiments, backside processing includes bonding to a secondary host substrate. Such bonding may employ any layer transfer process to join the backside (e.g., non-native) material layer to another substrate. Following such joining, the former host substrate may be removed as a sacrificial donor to re-expose the front side stack and/or the front side of the device layer. Such embodiments may enable iterative side-to-side lamination of device strata with a first device layer serving as the core of the assembly. In some embodiments illustrated in FIGS. **4**G and **5**G, secondary host substrate **440** joined to non-native material layer **420** provides at least mechanical support while host substrate **402** is removed.

[0149] Any bonding, such as, but not limited to, thermal-compression bonding may be employed to join secondary host substrate **440** to non-native material layer **420**. In some embodiments, both a surface layer of secondary host substrate **440** and non-native material layer **420** are continuous dielectric layers (e.g., SiO), which are thermal-compression bonded. In some other embodiments, both a surface layer of secondary host substrate **440** and non-native material layer **420** include a metal layer (e.g., Au, Pt, etc.), which are thermal-compression bonded. In other embodiments, at least one of surface layer of secondary host substrate **440** and non-native material layer **420** are patterned, including both patterned metal surface (i.e., traces) and surrounding dielectric (e.g., isolation), which are thermal-compression bonded to form a hybrid (e.g., metal/oxide) joint. For such embodiments, structural features in the secondary host substrate **440** and the patterned non-native material layer **420** are aligned (e.g., optically) during the bonding process. In some embodiments, non-native material layer **420** includes one or more conductive backside traces coupled to a terminal of a transistor fabricated in device layer **415**. The conductive backside trace may, for example, be bonded to metallization on secondary host substrate **440**.

[0150] Bonding of device strata may proceed from the front side and/or backside of a device layer before or after front side processing of the device layer has been completed. A backside bonding process may be performed after front side fabrication of a device (e.g., transistor) is substantially complete. Alternatively, backside bonding process may be performed prior to completing front side fabrication of a device (e.g., transistor), in which case the front side of the device layer may receive additional processing following the backside bonding process. As further illustrated in FIGS. **4**H and **5**H, for example, front side processing includes removal of host substrate **402** (as a second donor substrate) to re-expose the front side of device layer **415**. At this point, donor-host substrate assembly **403** includes secondary host **440** joined to device layer **415** through non-native material layer **420**.

[0151] In another aspect, the integrated circuit structures described above in association with FIGS. **2**A-**2**K can be co-integrated with other backside revealed integrated circuit structures such as neighboring semiconductor structures or devices separated by self-aligned gate endcap (SAGE) struc-

tures. Particular embodiments may be directed to integration of multiple width (multi-Wsi) nanowires and nanoribbons in a SAGE architecture and separated by a SAGE wall. In an embodiment, nanowires/nanoribbons are integrated with multiple Wsi in a SAGE architecture portion of a front-end process flow. Such a process flow may involve integration of nanowires and nanoribbons of different Wsi to provide robust functionality of next generation transistors with low power and high performance. Associated epitaxial source or drain regions may be embedded (e.g., portions of nanowires removed and then source or drain (S/D) growth is performed).

[0152] To provide further context, advantages of a self-aligned gate endcap (SAGE) architecture may include the enabling of higher layout density and, in particular, scaling of diffusion-to-diffusion spacing. To provide illustrative comparison, FIG. **6** illustrates a cross-sectional view taken through nanowires and fins for a non-endcap architecture, in accordance with an embodiment of the present disclosure. FIG. **7** illustrates a cross-sectional view taken through nanowires and fins for a self-aligned gate endcap (SAGE) architecture, in accordance with an embodiment of the present disclosure.

[0153] Referring to FIG. **6**, an integrated circuit structure **600** includes a substrate **602** having fins **604** protruding there from by an amount **606** above an isolation structure **608** laterally surrounding lower portions of the fins **604**. Upper portions of the fins may include a local isolation structure **622** and a growth enhancement layer **620**, as is depicted. Corresponding nanowires **605** are over the fins **604**. A gate structure may be formed over the integrated circuit structure **600** to fabricate a device. However, breaks in such a gate structure may be accommodated for by increasing the spacing between fin **604**/nanowire **605** pairs.

[0154] Referring to FIG. **6**, in an embodiment, following gate formation, the lower portions of the structure **600** can be planarized and/or etched to level **634** in order to leave a backside surface including exposed bottom surfaces of gate structures and epitaxial source or drain structures. It is to be appreciated that backside (bottom) contacts may be formed on the exposed bottom surfaces of the epitaxial source or drain structures. It is also to be appreciated that planarization and/or etching could be to other levels such as **630** or **632**.

[0155] By contrast, referring to FIG. **7**, an integrated circuit structure **750** includes a substrate **752** having fins **754** protruding therefrom by an amount **756** above an isolation structure **758** laterally surrounding lower portions of the fins **754**. Upper portions of the fins may include a local isolation structure **772** and a growth enhancement layer **770**, as is depicted. Corresponding nanowires **755** are over the fins **754**. Isolating SAGE walls **760** (which may include a hardmask thereon, as depicted) are included within the isolation structure **758** and between adjacent fin **754**/nanowire **755** pairs. The distance between an isolating SAGE wall **760** and a nearest fin **754**/nanowire **755** pair defines the gate endcap spacing **762**. A gate structure may be formed over the integrated circuit structure **750**, between insolating SAGE walls to fabricate a device. Breaks in such a gate structure are imposed by the isolating SAGE walls. Since the isolating SAGE walls **760** are self-aligned, restrictions from conventional approaches can be minimized to enable more aggressive diffusion-to-diffusion spacing. Furthermore, since gate structures include breaks at all locations, individual gate structure portions may be layer connected by local interconnects formed over the isolating SAGE walls **760**. In an embodiment, as depicted, the isolating SAGE walls **760** each include a lower dielectric portion and a dielectric cap on the lower dielectric portion.

[0156] Referring to FIG. **7**, in an embodiment, following gate formation, the lower portions of the structure **750** can be planarized and/or etched to level **784** in order to leave a backside surface including exposed bottom surfaces of gate structures and epitaxial source or drain structures. It is to be appreciated that backside (bottom) contacts may be formed on the exposed bottom surfaces of the epitaxial source or drain structures. It is also to be appreciated that planarization and/or etching could be to other levels such as **780** or **782**.

[0157] A self-aligned gate endcap (SAGE) processing scheme involves the formation of gate/trench contact endcaps self-aligned to fins without requiring an extra length to account for mask mis-registration. Thus, embodiments may be implemented to enable shrinking of transistor layout area. Embodiments described herein may involve the fabrication of gate endcap isolation structures, which may also be referred to as gate walls, isolation gate walls or self-aligned gate endcap (SAGE) walls.

[0158] In an embodiment, as described throughout, self-aligned gate endcap (SAGE) isolation structures may be composed of a material or materials suitable to ultimately electrically isolate, or contribute to the isolation of, portions of permanent gate structures from one another. Exemplary materials or material combinations include a single material structure such as silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride. Other exemplary materials or material combinations include a multi-layer stack having lower portion silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride and an upper portion higher dielectric constant material such as hafnium oxide.

[0159] It is to be appreciated that the integrated circuit structures described above in association with FIGS. **2**A-**2**K can be co-integrated with other backside revealed integrated circuit structures such as nanowire or nanoribbon based devices. Additionally or alternatively, other integrated circuit structures can be fabricated using processes described in association with FIGS. **2**A-**2**K. To highlight an exemplary integrated circuit structure having three vertically arranged nanowires, FIG. **8**A illustrates a three-dimensional cross-sectional view of a nanowire-based integrated circuit structure, in accordance with an embodiment of the present disclosure. FIG. **8**B illustrates a cross-sectional source or drain view of the nanowire-based integrated circuit structure of FIG. **8**A, as taken along the a-a' axis. FIG. **8**C illustrates a cross-sectional channel view of the nanowire-based integrated circuit structure of FIG. **8**A, as taken along the b-b' axis.

[0160] Referring to FIG. **8**A, an integrated circuit structure **800** includes one or more vertically stacked nanowires (**804** set) above a substrate **802**. In an embodiment, as depicted, a local isolation structure **802**C, a growth enhancement layer **802**B, and a lower substrate portion **802**A are included in substrate **802**, as is depicted. An optional fin below the bottommost nanowire and formed from the substrate **802** is not depicted for the sake of emphasizing the nanowire portion for illustrative purposes. Embodiments herein are targeted at both single wire devices and multiple wire devices. As an example, a three nanowire-based devices having nanowires **804**A, **804**B and **804**C is shown for

illustrative purposes. For convenience of description, nanowire **804**A is used as an example where description is focused on one of the nanowires. It is to be appreciated that where attributes of one nanowire are described, embodiments based on a plurality of nanowires may have the same or essentially the same attributes for each of the nanowires.

[0161] Each of the nanowires **804** includes a channel region **806** in the nanowire. The channel region **806** has a length (L). Referring to FIG. **8**C, the channel region also has a perimeter (Pc) orthogonal to the length (L). Referring to both FIGS. **8**A and **8**C, a gate electrode stack **808** surrounds the entire perimeter (Pc) of each of the channel regions **806**. The gate electrode stack **808** includes a gate electrode along with a gate dielectric layer between the channel region **806** and the gate electrode (not shown). In an embodiment, the channel region is discrete in that it is completely surrounded by the gate electrode stack **808** without any intervening material such as underlying substrate material or overlying channel fabrication materials. Accordingly, in embodiments having a plurality of nanowires **804**, the channel regions **806** of the nanowires are also discrete relative to one another.

[0162] Referring to both FIGS. **8**A and **8**B, integrated circuit structure **800** includes a pair of non-discrete source or drain regions **810/812**. The pair of non-discrete source or drain regions **810/812** is on either side of the channel regions **806** of the plurality of vertically stacked nanowires **804**. Furthermore, the pair of non-discrete source or drain regions **810/812** is adjoining for the channel regions **806** of the plurality of vertically stacked nanowires **804**. In one such embodiment, not depicted, the pair of non-discrete source or drain regions **810/812** is directly vertically adjoining for the channel regions **806** in that epitaxial growth is on and between nanowire portions extending beyond the channel regions **806**, where nanowire ends are shown within the source or drain structures. In another embodiment, as depicted in FIG. **8**A, the pair of non-discrete source or drain regions **810/812** is indirectly vertically adjoining for the channel regions **806** in that they are formed at the ends of the nanowires and not between the nanowires.

[0163] In an embodiment, as depicted, the source or drain regions **810/812** are non-discrete in that there are not individual and discrete source or drain regions for each channel region **806** of a nanowire **804**. Accordingly, in embodiments having a plurality of nanowires **804**, the source or drain regions **810/812** of the nanowires are global or unified source or drain regions as opposed to discrete for each nanowire. That is, the non-discrete source or drain regions **810/812** are global in the sense that a single unified feature is used as a source or drain region for a plurality (in this case, 3) of nanowires **804** and, more particularly, for more than one discrete channel region **806**. In one embodiment, from a cross-sectional perspective orthogonal to the length of the discrete channel regions **806**, each of the pair of non-discrete source or drain regions **810/812** is approximately rectangular in shape with a bottom tapered portion and a top vertex portion, as depicted in FIG. **8**B. In other embodiments, however, the source or drain regions **810/812** of the nanowires are relatively larger yet discrete non-vertically merged epitaxial structures such as nubs.

[0164] In accordance with an embodiment of the present disclosure, and as depicted in FIGS. **8**A and **8**B, integrated circuit structure **800** further includes a pair of contacts **814**, each contact **814** on one of the pair of non-discrete source or drain regions **810/812**. In one such embodiment, in a vertical sense, each contact **814** completely surrounds the respective non-discrete source or drain region **810/812**. In another aspect, the entire perimeter of the non-discrete source or drain regions **810/812** may not be accessible for contact with contacts **814**, and the contact **814** thus only partially surrounds the non-discrete source or drain regions **810/812**, as depicted in FIG. **8**B. In a contrasting embodiment, not depicted, the entire perimeter of the non-discrete source or drain regions **810/812**, as taken along the a-a' axis, is surrounded by the contacts **814**.

[0165] Referring again to FIG. **8**A, in an embodiment, integrated circuit structure **800** further includes a pair of spacers **816**. As is depicted, outer portions of the pair of spacers **816** may overlap portions of the non-discrete source or drain regions **810/812**, providing for "embedded" portions of the non-discrete source or drain regions **810/812** beneath the pair of spacers **816**. As is also depicted, the embedded portions of the non-discrete source or drain regions **810/812** may not extend beneath the entirety of the pair of spacers **816**.

[0166] Substrate **802** may be composed of a material suitable for integrated circuit structure fabrication. In one embodiment, substrate **802** includes a lower bulk substrate composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium, germanium-tin, silicon-germanium-tin, or a group III-V compound semiconductor material. An upper insulator layer composed of a material which may include, but is not limited to, silicon dioxide, silicon nitride or silicon oxy-nitride is on the lower bulk substrate. Thus, the structure **800** may be fabricated from a starting semiconductor-on-insulator substrate. Alternatively, the structure **800** is formed directly from a bulk substrate and local oxidation is used to form electrically insulative portions in place of the above described upper insulator layer. In another alternative embodiment, the structure **800** is formed directly from a bulk substrate and doping is used to form electrically isolated active regions, such as nanowires, thereon. In one such embodiment, the first nanowire (i.e., proximate the substrate) is in the form of an omega-FET type structure.

[0167] In an embodiment, the nanowires **804** may be sized as wires or ribbons, as described below, and may have squared-off or rounder corners. In an embodiment, the nanowires **804** are composed of a material such as, but not limited to, silicon, germanium, or a combination thereof. In one such embodiment, the nanowires are single-crystalline. For example, for a silicon nanowire **804**, a single-crystalline nanowire may be based from a (100) global orientation, e.g., with a <100> plane in the z-direction. As described below, other orientations may also be considered. In an embodiment, the dimensions of the nanowires **804**, from a cross-sectional perspective, are on the nano-scale. For example, in a specific embodiment, the smallest dimension of the nanowires **804** is less than approximately 20 nanometers. In an embodiment, the nanowires **804** are composed of a strained material, particularly in the channel regions **806**.

[0168] Referring to FIGS. **8**C, in an embodiment, each of the channel regions **806** has a width (Wc) and a height (Hc), the width (Wc) approximately the same as the height (Hc). That is, in both cases, the channel regions **806** are square-like or, if corner-rounded, circle-like in cross-section profile. In another aspect, the width and height of the channel region need not be the same, such as the case for nanoribbons as described throughout.

[0169] Referring again to FIGS. **8**A, **8**B and **8**C, in an embodiment, the lower portions of the structure **800** can be planarized and/or etched to level **899** in order to leave a backside surface including exposed bottom surfaces of gate structures and epitaxial source or drain structures. It is to be appreciated that backside (bottom) contacts may be formed on the exposed bottom surfaces of the epitaxial source or drain structures.

[0170] In an embodiment, as described throughout, an integrated circuit structure includes non-planar devices such as, but not limited to, a finFET or a tri-gate structure with corresponding one or more overlying nanowire structures, and an isolation structure between the finFET or tri-gate structure and the corresponding one or more overlying nanowire structures. In some embodiments, the finFET or tri-gate structure is retained. In other embodiments, the finFET or tri-gate structure is may ultimately be removed in a substrate removal process.

[0171] Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

[0172] FIG. **9** illustrates a computing device **900** in accordance with one implementation of an embodiment of the present disclosure. The computing device **900** houses a board **902**. The board **902** may include a number of components, including but not limited to a processor **904** and at least one communication chip **906**. The processor **904** is physically and electrically coupled to the board **902**. In some implementations the at least one communication chip **906** is also physically and electrically coupled to the board **902**. In further implementations, the communication chip **906** is part of the processor **904**.

[0173] Depending on its applications, computing device **900** may include other components that may or may not be physically and electrically coupled to the board **902**. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0174] The communication chip **906** enables wireless communications for the transfer of data to and from the computing device **900**. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip **906** may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device **900** may include a plurality of communication chips **906**. For instance, a first communication chip **906** may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip **906** may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0175] The processor **904** of the computing device **900** includes an integrated circuit die packaged within the processor **904**. The integrated circuit die of the processor **904** may include one or more structures, such as integrated circuit structures built in accordance with implementations of embodiments of the present disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0176] The communication chip **906** also includes an integrated circuit die packaged within the communication chip **906**. The integrated circuit die of the communication chip **906** may include one or more structures, such as integrated circuit structures built in accordance with implementations of embodiments of the present disclosure.

[0177] In further implementations, another component housed within the computing device **900** may contain an integrated circuit die that includes one or structures, such as integrated circuit structures built in accordance with implementations of embodiments of the present disclosure.

[0178] In various implementations, the computing device **900** may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device **900** may be any other electronic device that processes data.

[0179] FIG. **10** illustrates an interposer **1000** that includes one or more embodiments of the present disclosure. The interposer **1000** is an intervening substrate used to bridge a first substrate **1002** to a second substrate **1004**. The first substrate **1002** may be, for instance, an integrated circuit die. The second substrate **1004** may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer **1000** is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer **1000** may couple an integrated circuit die to a ball grid array (BGA) **1006** that can subsequently be coupled to the second substrate **1004**. In some embodiments, the first and second substrates **1002/1004** are attached to opposing sides of the interposer **1000**. In other embodiments, the first and second substrates **1002/1004** are attached to the same side of the

interposer **1000**. And, in further embodiments, three or more substrates are interconnected by way of the interposer **1000**.

[0180] The interposer **1000** may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer **1000** may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0181] The interposer **1000** may include metal interconnects **1008** and vias **1010**, including but not limited to through-silicon vias (TSVs) **1012**. The interposer **1000** may further include embedded devices **1014**, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer **1000**. In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer **1000** or in the fabrication of components included in the interposer **1000**.

[0182] It is to be appreciated that structures described herein may be operated at a low temperature, e.g., in a range of −77 degrees Celsius to 0 degrees Celsius. In one embodiment, a heat regulator/refrigeration device is coupled to a common board having a device with structures such as those described herein coupled thereto, such as described below in association with FIG. **11**A. In one embodiment, a heat regulator device and/or refrigeration device is included on a processing device having structures such as those described herein, such as described below in association with FIG. **11**B.

[0183] FIG. **11**A illustrates a computing device **1100** in accordance with one implementation of an embodiment of the present disclosure. The computing device **1100** houses a board. The board may include a number of components, including but not limited to a processing device **1102**. The computing device **1100** can also include communication chip **1112**. In one embodiment, the processing device **1102** is physically and electrically coupled to the board. In some implementations the communication chip **1112** is also physically and electrically coupled to the board. In further implementations, the communication chip **1112** is part of the processing device **1102**.

[0184] Depending on its applications, computing device **1100** may include other components that may or may not be physically and electrically coupled to the board. These other components can include, but are not limited to, memory **1104**, such as volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), or flash memory, an antenna **1122**, a display device **1106**, a battery/power **1114**, an audio output device **1108**, an audio input device **1118**, a global positioning system (GPS) device **1116**, another output device **1110** (such as video output), and other input device **1120** (such as video input), a security interface device **1121**, and/or a test device. In one embodiment, a heat regulation/refrigeration device **1111** is included and is coupled to the board, e.g., a device including actively cooled copper channels.

[0185] The communication chip **1112** enables wireless communications for the transfer of data to and from the computing device **1100**. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip **1112** may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device **1100** may include a plurality of communication chips **1112**. For instance, a first communication chip **1112** may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip **1112** may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0186] The processing device **1102** of the computing device **1100** can include an integrated circuit die in a package. The processing device **1102** may include one or more structures, such as gate-all-around integrated circuit structures having backside capacitors, built in accordance with implementations of embodiments of the present disclosure. The term "processing device" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0187] FIG. **11**B illustrates a processing device in accordance with one implementation of an embodiment of the present disclosure. Referring to FIG. **11**B, an exemplary processing device **1102** includes a memory region, a logic region, a communication device region, an interconnects and redistribution layer (RDL) and metal-insulator-metal (MIM) region, a refrigeration device region, a heat regulation device region, a batter/power regulation device region and a hardware security device region. In one embodiment, the refrigeration device region and/or the heat regulation device region is a region including actively cooled copper channels.

[0188] Thus, embodiments of the present disclosure include integrated circuit structures having backside capacitors, and methods of fabricating integrated circuit structures having backside capacitors.

[0189] The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0190] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

[0191] Example embodiment 1: An integrated circuit structure includes a front side structure including a device layer having a plurality of fin-based select transistors, a plurality of metallization layers above the plurality of fin-based select transistors, and a plurality of vias below and coupled to the plurality of fin-based select transistors. A backside structure is below the plurality of vias of the device layer. The backside structure includes a memory layer coupled to the plurality of fin-based select transistors by the plurality of vias.

[0192] Example embodiment 2: The integrated circuit structure of example embodiment 1, wherein the memory layer includes a plurality of capacitor structures.

[0193] Example embodiment 3: The integrated circuit structure of example embodiment 2, wherein the plurality of capacitor structures is a ferroelectric capacitor array.

[0194] Example embodiment 4: The integrated circuit structure of example embodiment 1, 2 or 3, wherein the memory layer includes a plurality of magnetic random access memory devices.

[0195] Example embodiment 5: The integrated circuit structure of example embodiment 1, 2, 3 or 4, wherein the backside structure further includes a non-memory metal-insulator-metal (MIM capacitor).

[0196] Example embodiment 6: An integrated circuit structure includes a front side structure including a device layer having a plurality of nanowire-based select transistors, a plurality of metallization layers above the plurality of nanowire-based select transistors, and a plurality of vias below and coupled to the plurality of nanowire-based select transistors. A backside structure is below the plurality of vias of the device layer. The backside structure includes a memory layer coupled to the plurality of nanowire-based select transistors by the plurality of vias.

[0197] Example embodiment 7: The integrated circuit structure of example embodiment 6, wherein the memory layer includes a plurality of capacitor structures.

[0198] Example embodiment 8: The integrated circuit structure of example embodiment 7, wherein the plurality of capacitor structures is a ferroelectric capacitor array.

[0199] Example embodiment 9: The integrated circuit structure of example embodiment 6, 7 or 8, wherein the memory layer includes a plurality of magnetic random access memory devices.

[0200] Example embodiment 10: The integrated circuit structure of example embodiment 6, 7, 8 or 9, wherein the backside structure further includes a non-memory metal-insulator-metal (MIM capacitor).

[0201] Example embodiment 11: A computing device includes a board, and a component coupled to the board. The component includes an integrated circuit structure including a front side structure including a device layer having a plurality of fin-based select transistors, a plurality of metallization layers above the plurality of fin-based select transistors, and a plurality of vias below and coupled to the plurality of fin-based select transistors. A backside structure is below the plurality of vias of the device layer. The backside structure includes a memory layer coupled to the plurality of fin-based select transistors by the plurality of vias.

[0202] Example embodiment 12: The computing device of example embodiment 11, further including a memory coupled to the board.

[0203] Example embodiment 13: The computing device of example embodiment 11 or 12, further including a communication chip coupled to the board.

[0204] Example embodiment 14: The computing device of example embodiment 11, 12 or 13, wherein the component is a packaged integrated circuit die.

[0205] Example embodiment 15: The computing device of example embodiment 11, 12, 13 or 14, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

[0206] Example embodiment 16: A computing device includes a board, and a component coupled to the board. The component includes an integrated circuit structure including a front side structure including a device layer having a plurality of nanowire-based select transistors, a plurality of metallization layers above the plurality of nanowire-based select transistors, and a plurality of vias below and coupled to the plurality of nanowire-based select transistors. A backside structure is below the plurality of vias of the device layer. The backside structure includes a memory layer coupled to the plurality of nanowire-based select transistors by the plurality of vias.

[0207] Example embodiment 17: The computing device of example embodiment 16, further including a memory coupled to the board.

[0208] Example embodiment 18: The computing device of example embodiment 16 or 17, further including a communication chip coupled to the board.

[0209] Example embodiment 19: The computing device of example embodiment 16, 17 or 18, wherein the component is a packaged integrated circuit die.

[0210] Example embodiment 20: The computing device of example embodiment 16, 17, 18 or 19, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

What is claimed is:

1. An integrated circuit structure, comprising:

a front side structure comprising:

a device layer having a plurality of fin-based select transistors;

a plurality of metallization layers above the plurality of fin-based select transistors; and

a plurality of vias below and coupled to the plurality of fin-based select transistors; and

a backside structure below the plurality of vias of the device layer, the backside structure including a memory layer coupled to the plurality of fin-based select transistors by the plurality of vias.

2. The integrated circuit structure of claim **1**, wherein the memory layer comprises a plurality of capacitor structures.

3. The integrated circuit structure of claim **2**, wherein the plurality of capacitor structures is a ferroelectric capacitor array.

4. The integrated circuit structure of claim **1**, wherein the memory layer comprises a plurality of magnetic random access memory devices.

5. The integrated circuit structure of claim **1**, wherein the backside structure further comprises a non-memory metal-insulator-metal (MIM capacitor).

6. An integrated circuit structure, comprising:

a front side structure comprising:

a device layer having a plurality of nanowire-based select transistors;

a plurality of metallization layers above the plurality of nanowire-based select transistors; and
a plurality of vias below and coupled to the plurality of nanowire-based select transistors; and
a backside structure below the plurality of vias of the device layer, the backside structure including a memory layer coupled to the plurality of nanowire-based select transistors by the plurality of vias.

7. The integrated circuit structure of claim **6**, wherein the memory layer comprises a plurality of capacitor structures.

8. The integrated circuit structure of claim **7**, wherein the plurality of capacitor structures is a ferroelectric capacitor array.

9. The integrated circuit structure of claim **6**, wherein the memory layer comprises a plurality of magnetic random access memory devices.

10. The integrated circuit structure of claim **6**, wherein the backside structure further comprises a non-memory metal-insulator-metal (MIM capacitor).

11. A computing device, comprising:
a board; and
a component coupled to the board, the component including an integrated circuit structure, comprising:
a front side structure comprising:
a device layer having a plurality of fin-based select transistors;
a plurality of metallization layers above the plurality of fin-based select transistors; and
a plurality of vias below and coupled to the plurality of fin-based select transistors; and
a backside structure below the plurality of vias of the device layer, the backside structure including a memory layer coupled to the plurality of fin-based select transistors by the plurality of vias.

12. The computing device of claim **11**, further comprising:
a memory coupled to the board.

13. The computing device of claim **11**, further comprising:
a communication chip coupled to the board.

14. The computing device of claim **11**, wherein the component is a packaged integrated circuit die.

15. The computing device of claim **11**, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

16. A computing device, comprising:
a board; and
a component coupled to the board, the component including an integrated circuit structure, comprising:
a front side structure comprising:
a device layer having a plurality of nanowire-based select transistors;
a plurality of metallization layers above the plurality of nanowire-based select transistors; and
a plurality of vias below and coupled to the plurality of nanowire-based select transistors; and
a backside structure below the plurality of vias of the device layer, the backside structure including a memory layer coupled to the plurality of nanowire-based select transistors by the plurality of vias.

17. The computing device of claim **16**, further comprising:
a memory coupled to the board.

18. The computing device of claim **16**, further comprising:
a communication chip coupled to the board.

19. The computing device of claim **16**, wherein the component is a packaged integrated circuit die.

20. The computing device of claim **16**, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

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