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(54) METHOD AND SYSTEM FOR LOW NOISE AMPLIFIER (LNA) AND POWER AMPLIFIER (PA) GAIN CONTROL

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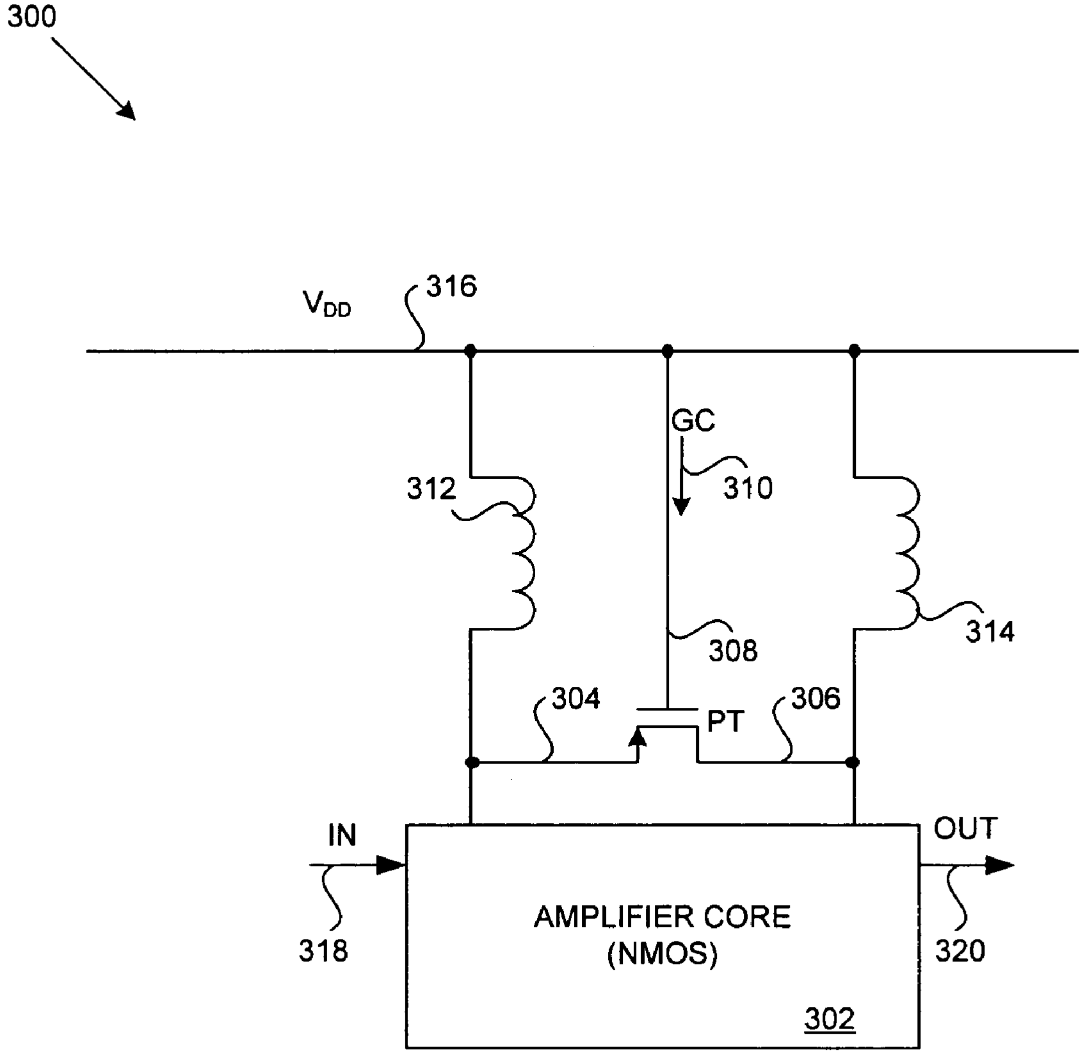
(57) **ABSTRACT**

Methods and systems for processing signals are disclosed herein. In one aspect of the invention a circuit for processing signals may comprise a triple well (TW) NMOS transistor coupled to an amplifier core. The TW NMOS transistor may track process and temperature variations (PVT) of at least one NMOS transistor within the amplifier core. A drain of the TW NMOS transistor may be coupled to a first inductor and the first inductor may be coupled to a first voltage source. The first voltage source may generate a standard voltage of about 1.2V. A source of the TW NMOS transistor may be coupled to a second inductor and the second inductor may be coupled to the first voltage source. A gate of the TW NMOS transistor may be coupled to a second voltage source, where the second voltage source may generate a standard voltage of about 2.5V.



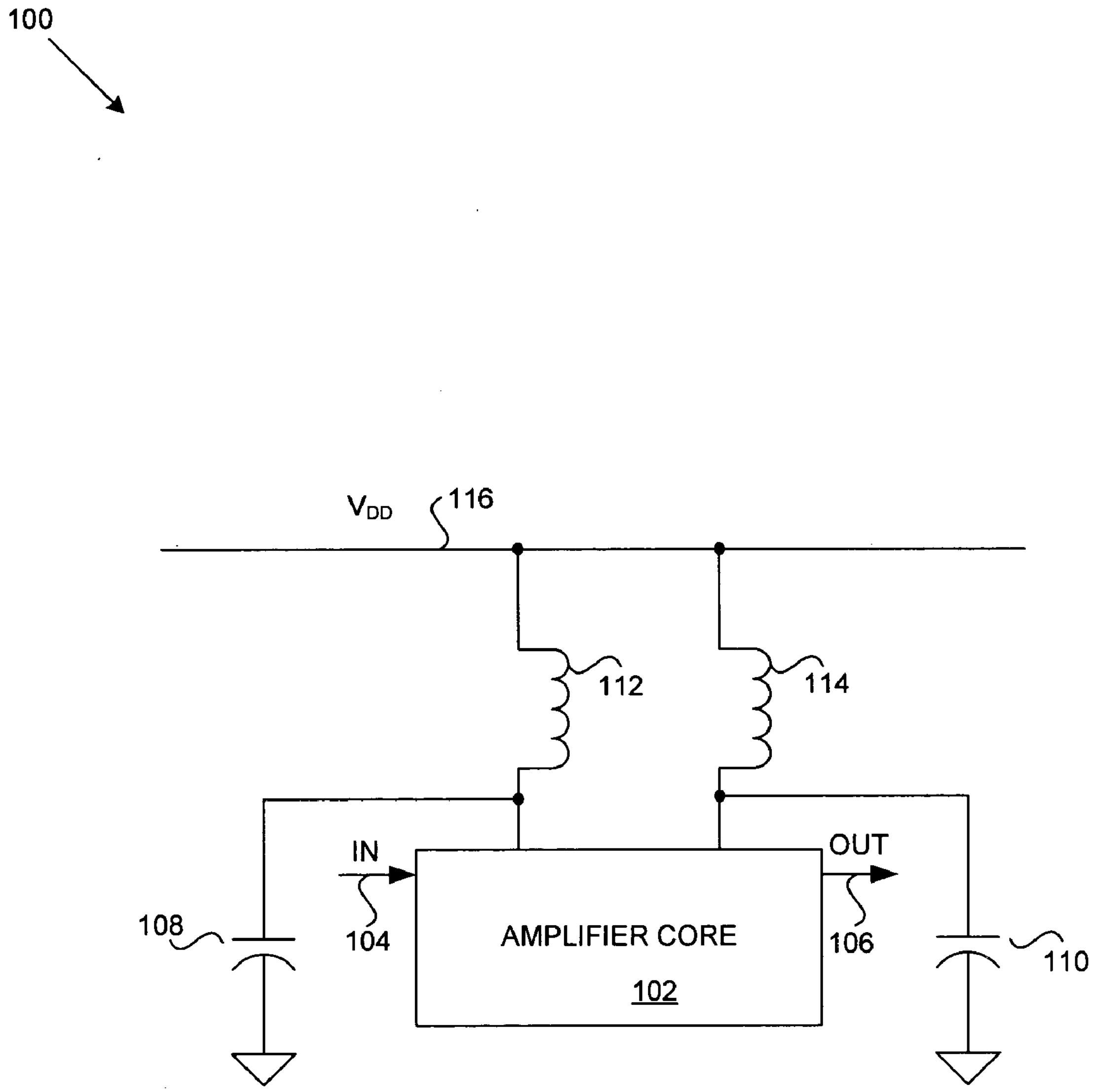


FIG. 1

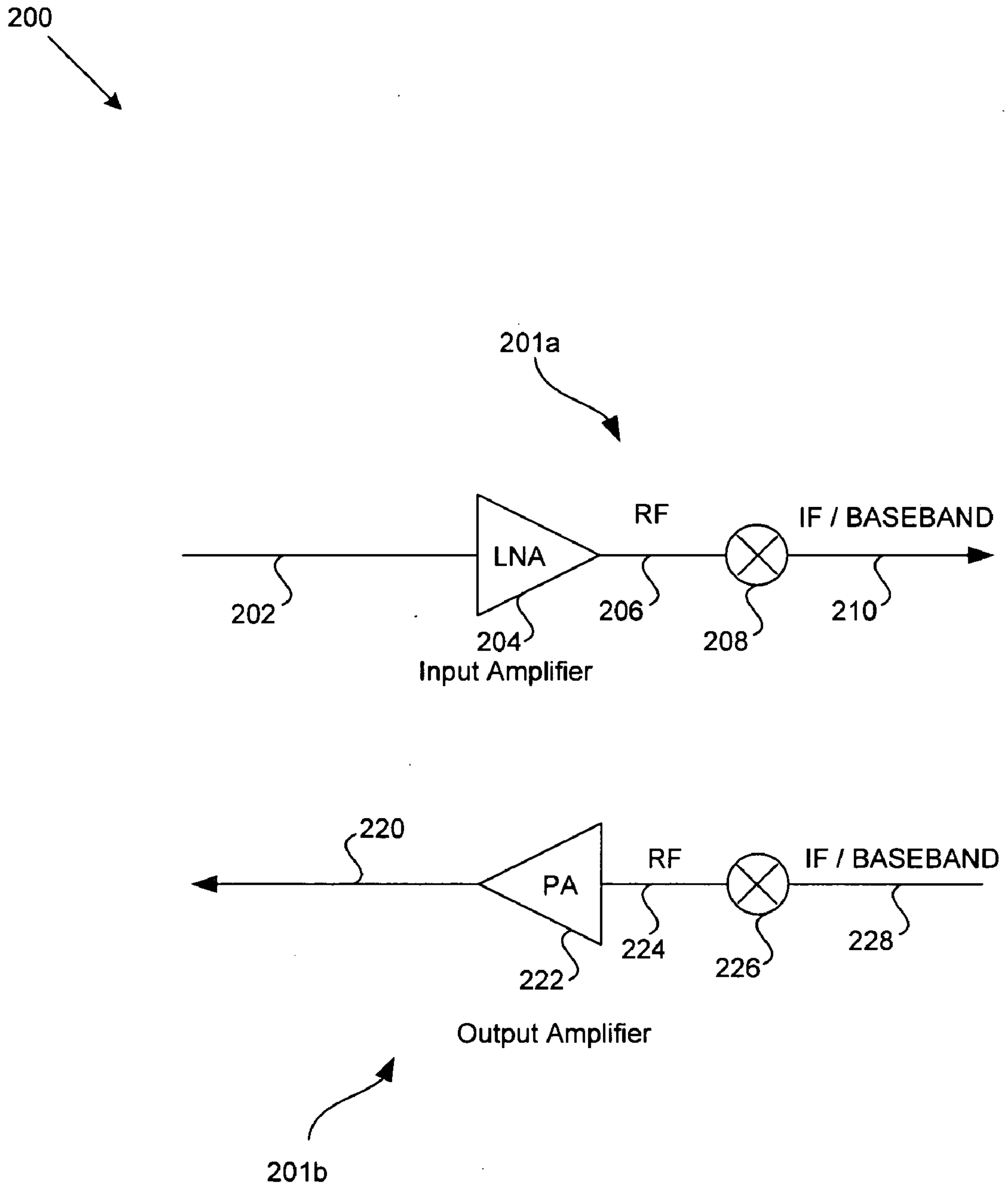

200
201a
RF
IF / BASEBAND
LNA
202
206
210
204
208
Input Amplifier
220
RF
IF / BASEBAND
PA
224
228
222
226
Output Amplifier
201b

FIG. 2

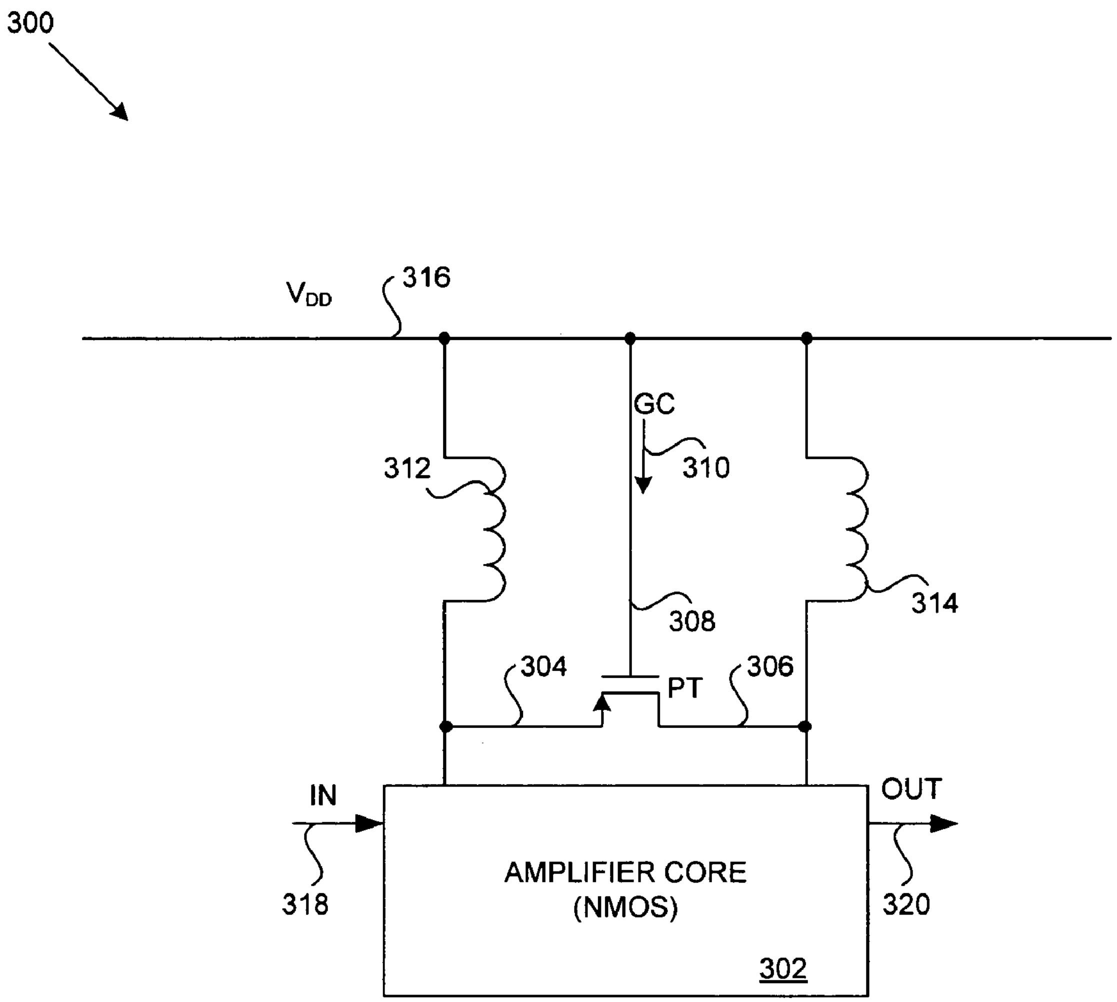

300
V_{DD}
316
GC
310
312
314
308
304
306
PT
IN
OUT
AMPLIFIER CORE
(NMOS)
302
318
320

FIG. 3

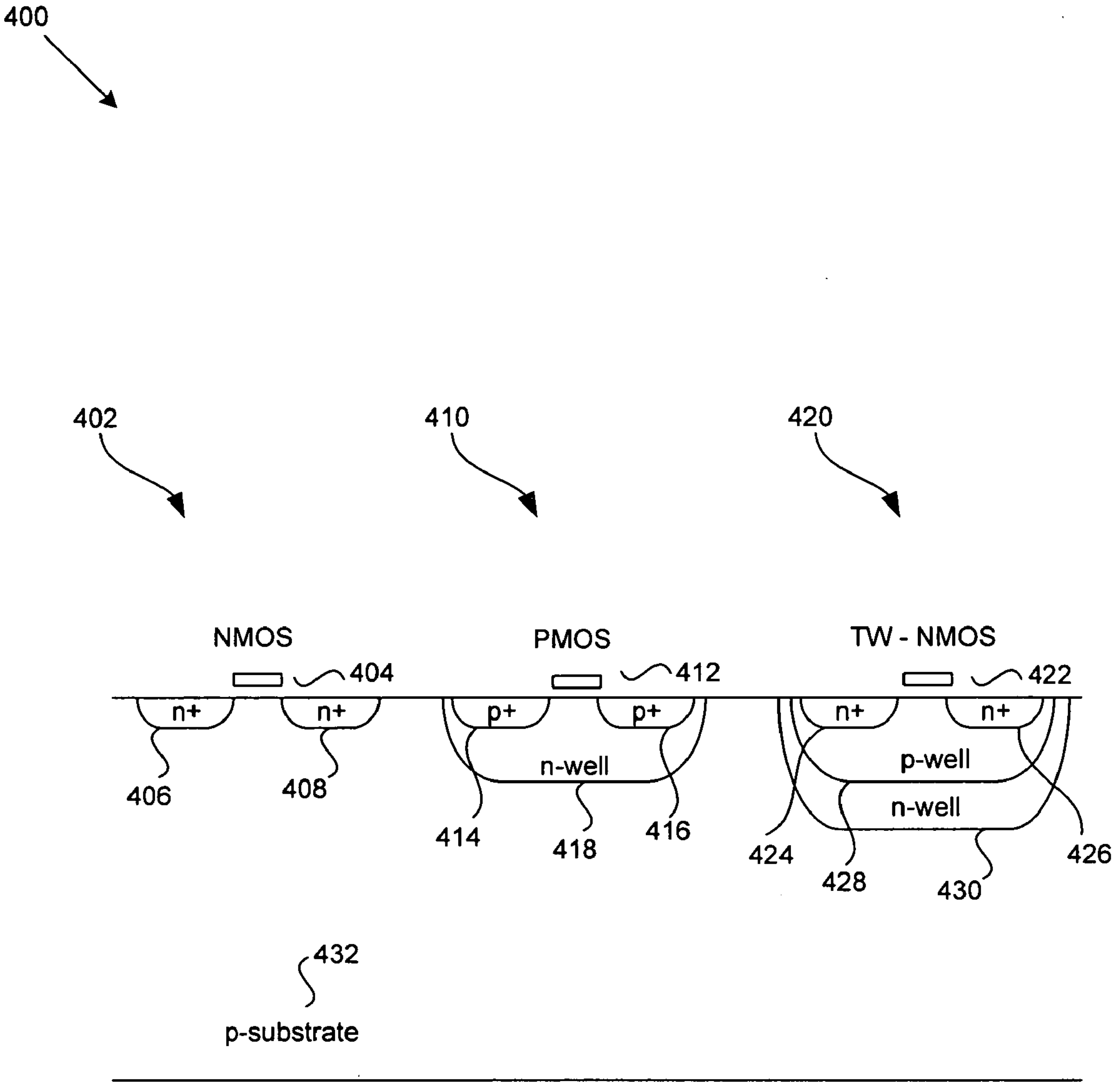

400
402
410
420
NMOS
404
n+
n+
406
408
PMOS
412
p+
p+
n-well
414
418
416
TW - NMOS
422
n+
n+
p-well
n-well
424
428
430
426
432
p-substrate

FIG. 4

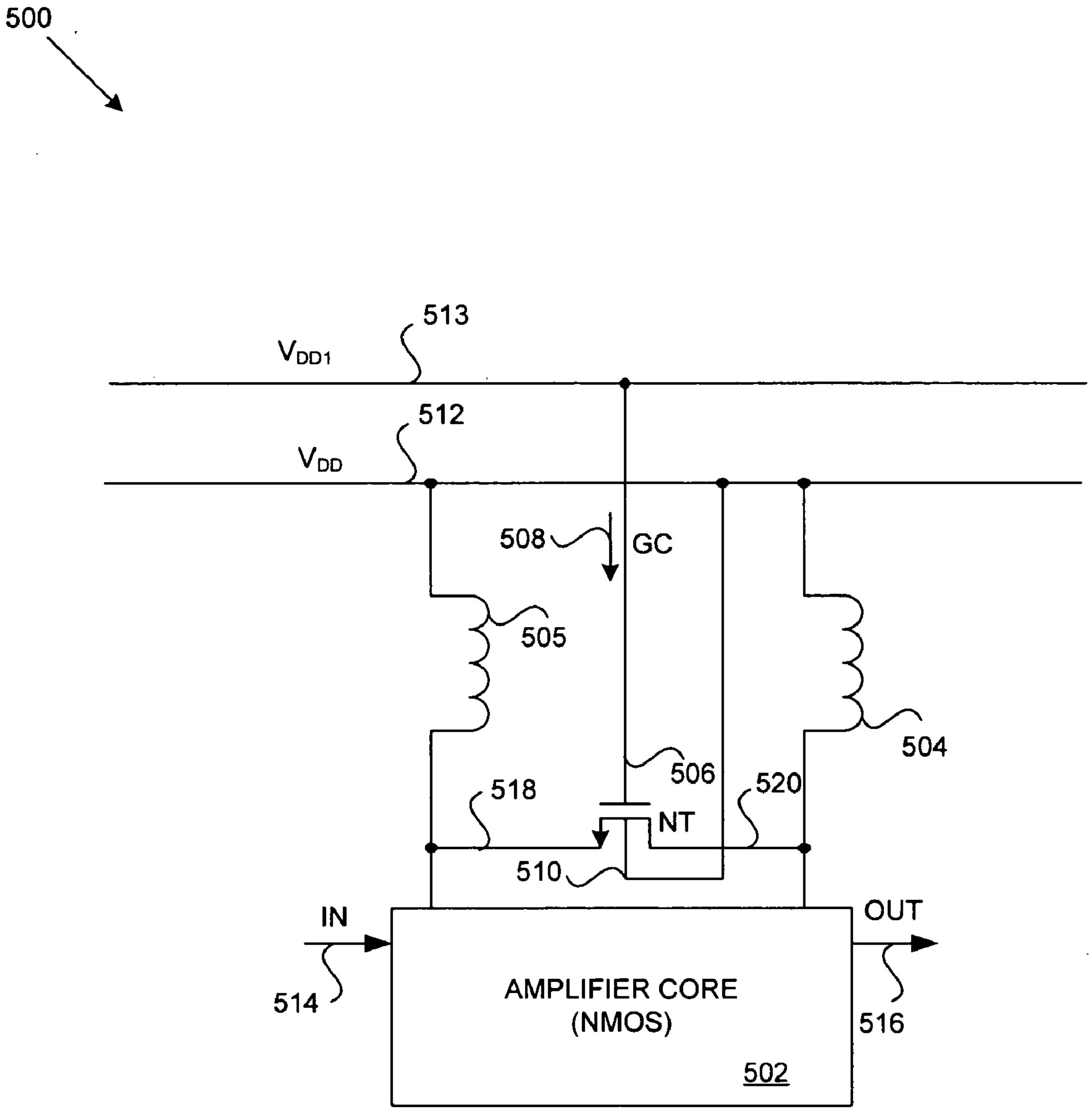

500
513
V_{DD1}
512
V_{DD}
508
GC
505
504
506
518
520
NT
510
IN
OUT
514
516
AMPLIFIER CORE
(NMOS)
502

FIG. 5A

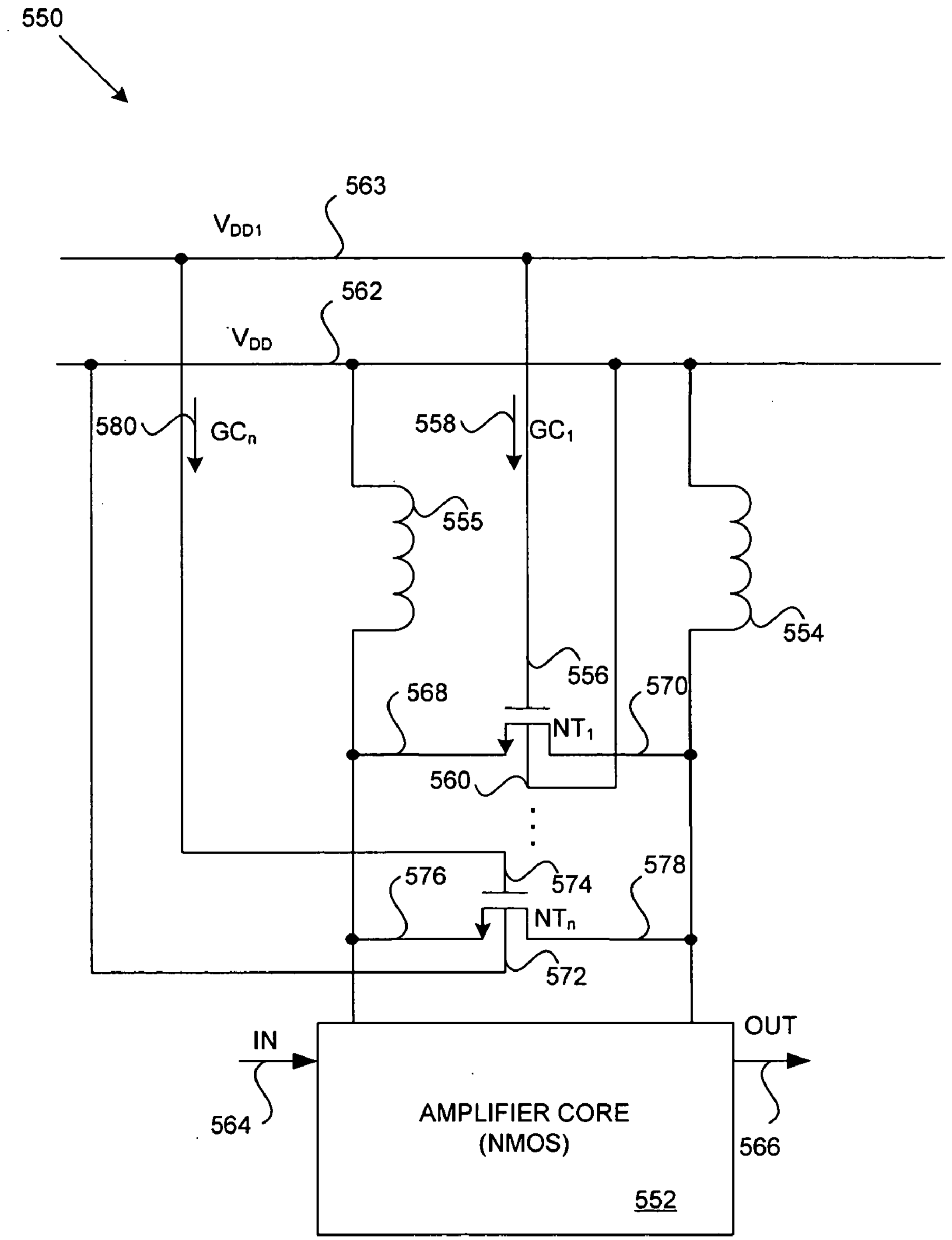

550
563
V_{DD1}
562
V_{DD}
580
GC_n
558
GC_1
555
554
556
568
570
NT_1
560
576
574
578
NT_n
572
IN
OUT
564
AMPLIFIER CORE
(NMOS)
552
566

FIG. 5B

METHOD AND SYSTEM FOR LOW NOISE AMPLIFIER (LNA) AND POWER AMPLIFIER (PA) GAIN CONTROL

RELATED APPLICATIONS

[0001] This application is related to the following applications, each of which is incorporated herein by reference in its entirety for all purposes:

[0002] U.S. patent application Ser. No. ______ (Attorney Docket No. 16149US01) filed ______, 2004;

[0003] U.S. patent application Ser. No. ______ (Attorney Docket No. 16150US01) filed ______, 2004;

[0004] U.S. patent application Ser. No. ______ (Attorney Docket No. US01) filed ______, 2004;

[0005] U.S. patent application Ser. No. ______ (Attorney Docket No. 16152US01) filed ______, 2004;

[0006] U.S. patent application Ser. No. ______ (Attorney Docket No. 16153US01) filed ______, 2004;

[0007] U.S. patent application Ser. No. ______ (Attorney Docket No. 16155US01) filed ______, 2004;

[0008] U.S. patent application Ser. No. ______ (Attorney Docket No. 16156US01) filed ______, 2004;

[0009] U.S. patent application Ser. No. ______ (Attorney Docket No. 16157US01) filed ______, 2004;

[0010] U.S. patent application Ser. No. ______ (Attorney Docket No. 16158US01) filed ______, 2004;

[0011] U.S. patent application Ser. No. ______ (Attorney Docket No. 16162US01) filed ______, 2004;

[0012] U.S. patent application Ser. No. ______ (Attorney Docket No. 16228US01) filed ______, 2004;

[0013] U.S. patent application Ser. No. ______ (Attorney Docket No. 16229US01) filed ______, 2004;

[0014] U.S. patent application Ser. No. ______ (Attorney Docket No. 16230US01) filed ______, 2004;

[0015] U.S. patent application Ser. No. ______ (Attorney Docket No. 16234US01) filed ______, 2004;

[0016] U.S. patent application Ser. No. ______ (Attorney Docket No. 16236US01) filed ______, 2004; and

[0017] U.S. patent application Ser. No. ______ (Attorney Docket No. 16237US01) filed ______, 2004.

FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0018] [Not Applicable]

MICROFICHE/COPYRIGHT REFERENCE

[0019] [Not Applicable]

FIELD OF THE INVENTION

[0020] Certain embodiments of the invention relate to the processing of radio signals in a transceiver. More specifically, certain embodiments of the invention relate to a method and system for low noise amplifier (LNA) and power amplifier (PA) gain control.

BACKGROUND OF THE INVENTION

[0021] Modern communication devices, such as radio frequency (RF) communication devices, process electromagnetic wave signals with variable signal strength. The variable signal strength varies depending on distance between a transmitter and a receiver, as well as environmental factors and process, temperature etc. variations (PVT). A power amplifier (PA) is utilized prior to signal transmission by a transmitter, for example, and a variable gain low noise amplifier (LNA) is utilized after a signal is received by a receiver, to amplify the signal and adjust the signal gain accordingly. Conventional gain control circuits in a signal amplifying device, however, do not improve the linearity of the PA and/or LNA that is utilized for signal amplification.

[0022] Different gain control techniques are utilized by conventional gain control circuits in signal amplifying devices without accounting for PVT. For example, amplifier gain in a conventional LNA or PA devices is varied by changing the resistance of one or more resonance tanks in the conventional LNA or PA. A resonance tank may comprise one or more LC circuits, for example, adapted to resonate at a determined frequency. By changing the inductance (L) and/or capacitance (C) of the LC tank, the overall tank resistance may be changed and, as a result, the LNA's or PA's gain may be changed as well. This technique, however, does not compensate for gain variations in the core amplifier circuit due to PVT.

[0023] Other conventional gain control techniques utilize PMOS transistor switches to implement low gain and high gain amplification within an exemplary LNA or PA. For example, if the PMOS transistor is turned off, high gain control may be applied by the exemplary LNA or PA. Similarly, if the PMOS transistor is turned on, low gain control may be applied by the LNA or PA. PMOS transistors utilized in conventional variable gain LNA and PA devices, however, cause high parasitic capacitance and increase overall device non-linearity since variations, such as PVT, in the core amplifying circuit are not tracked during an operation cycle. As a result, non-linearity decreases amplifier sensitivity and contributes to the creation of intermodulation (IM) products in the desired signal passband.

[0024] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of ordinary skill in the art through comparison of such systems with the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF SUMMARY OF THE INVENTION

[0025] Certain embodiments of the invention may be found in a circuit for processing signals. The circuit may comprise a triple well (TW) NMOS transistor coupled to an amplifier core. The TW NMOS transistor may track process and temperature variations (PVT) of at least one NMOS transistor within the amplifier core. A drain of the TW NMOS transistor may be coupled to a first inductor and the first inductor may be coupled to a first voltage source. The first voltage source may generate a standard voltage of about 1.2V. A source of the TW NMOS transistor may be coupled to a second inductor and the second inductor may be coupled to the first voltage source. A gate of the TW NMOS transistor may be coupled to a second voltage source, where the second voltage source may generate a standard voltage of about 2.5V. The gate may receive a control signal associated with a power status of the TW NMOS transistor. A third well of the TW NMOS transistor may be coupled to the first voltage source.

[0026] Certain embodiments of the invention may also be found in a method for processing signals. The method may comprise tracking process and temperature variations (PVT) of at least one NMOS transistor within an amplifier core utilizing a triple well (TW) NMOS transistor coupled to the amplifier core. A drain of the TW NMOS transistor may be coupled to a first inductor and the first inductor may be coupled to a first voltage source. The first voltage source may generate a standard voltage of about 1.2V. A source of the TW NMOS transistor may be coupled to a second inductor and the second inductor may be coupled to the first voltage source. A gate of the TW NMOS transistor may be coupled to a second voltage source, where the second voltage source may generate a standard voltage of about 2.5V. The gate may receive a control signal associated with a power status of the TW NMOS transistor. A third well of the TW NMOS transistor may be coupled to the first voltage source.

[0027] Another embodiment of the invention may be found in a circuit for processing signals. The circuit may comprise a triple well (TW) NMOS transistor coupled to an amplifier core. The TW NMOS transistor may be adapted to track process and temperature variations (PVT) of at least one NMOS transistor within the amplifier core. A source of the TW NMOS transistor may be coupled to a first terminal of a first inductor. The first terminal of the first inductor may be coupled to the amplifier core. A second terminal of the first inductor may be coupled to a first voltage source. A gate of the TW NMOS transistor may be coupled to a second voltage source and a drain of the TW NMOS transistor may be coupled to a first terminal of a second inductor. The first terminal of the second inductor may be coupled to the amplifier core. A second terminal of the second inductor may be coupled to the first voltage source. A third well of the TW NMOS transistor may be coupled to the first voltage source.

[0028] These and other features and advantages of the present invention may be appreciated from a review of the following detailed description of the present invention, along with the accompanying figures in which like reference numerals refer to like parts throughout.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0029] **FIG. 1** is a circuit illustrating an amplifier circuit that may be utilized in connection with an embodiment of the invention.

[0030] **FIG. 2** is a circuit illustrating exemplary low noise amplifier (LNA) and power amplifier (PA) circuits that may be utilized in connection with an embodiment of the invention.

[0031] **FIG. 3** is a circuit illustrating an exemplary amplifier circuit with a PMOS transistor switch that may be utilized in connection with an embodiment of the invention.

[0032] **FIG. 4** is an exemplary circuit illustrating NMOS, PMOS, and triple well (TW) NMOS transistors that may be utilized in connection with an embodiment of the invention.

[0033] **FIG. 5A** is a circuit illustrating an amplifier circuit with a triple well (TW) NMOS transistor, in accordance with an embodiment of the invention.

[0034] **FIG. 5B** is a circuit illustrating an amplifier circuit with a plurality of triple well (TW) NMOS transistors, in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0035] Certain embodiments of the invention may be found in a circuit for processing signals, such as a signal amplifying circuit. The signal amplifying circuit may comprise an amplifier core and one or more NMOS transistors, such as triple well (TW) NMOS transistors, which may be coupled to the core and utilized for gain control. In accordance with an aspect of the invention, a TW NMOS transistor may be utilized to track process and temperature variations (PVT) of at least one NMOS transistor within the amplifier core in a LNA and/or a PA. Since a LNA and/or PA amplifier core may comprise NMOS transistors, an NMOS transistor utilized as a switch outside the core, may be utilized to track the transconductance g_m as well as other variations, such as PVT, within the core NMOS transistors.

[0036] A LNA or a PA utilizing an NMOS transistor switch, such as TW NMOS, is characterized by a well defined high and low gain as the TW NMOS may be adapted to track PVT within core NMOS devices. By using TW NMOS switch in a LNA and/or a PA, parasitic capacitance may be decreased, amplifier sensitivity may be significantly improved, and gain values may be well defined. For example, a minimum gain may be well defined for a large interference/blocker signal and maximum gain may be well defined for a small desired signal. In another aspect of the invention, multiple NMOS transistors may be utilized as switches resulting in multiple well-defined gain values for a LNA and/or a PA.

[0037] **FIG. 1** is a circuit illustrating an amplifier circuit **100** that may be utilized in connection with an embodiment of the invention. Referring to **FIG. 1**, the amplifier circuit **100** may comprise an amplifier core **102**, inductors **112** and **114**, capacitors **108** and **110**, and a voltage supply rail **116**. In operation, the LC-tank comprising inductor **112** and capacitor **108** and/or the LC-tank comprising inductor **114** and capacitor **110** may be tuned to a resonance frequency f_0 and may limit the bandwidth of the incoming signal **104**. For example, the LC-tank comprising inductor **112** and capacitor **108** and/or the LC-tank comprising inductor **114** and capacitor **110** may be tuned to resonate at approximately 900 MHz for an incoming GSM signal **104**. The amplifier core **102** may comprise suitable circuitry or logic and may be adapted to amplify the incoming signal **104** to generate an output signal **106**.

[0038] In one aspect of the invention, the LC-tank comprising inductor **112** and capacitor **108** and/or the LC-tank comprising inductor **114** and capacitor **110** may be replaced by corresponding load resistors and gain within the amplifier core **102** may be changed by proportionally changing the resistance of the load resistors. For example, high gain may be achieved with a high load resistance and lower gain may be achieved by a lower load resistance. High amplifier sensitivity and well defined gain of the amplifier circuit **100**

may be achieved by using a triple well (TW) NMOS transistor as a load, as further explained herein below.

[0039] The amplifier circuit **100** may be utilized for signal amplification immediately after a signal is received by a receiver, for example. In addition, the amplifier circuit **100** may also be utilized to amplify a signal prior to transmission. Depending on the particular application, the amplifier core **102** may be utilized with additional circuitry, such as a mixer, to downconvert or upconvert a signal, if the amplifier circuit **100** is used in a receiver LNA or a transmitter PA, respectively.

[0040] **FIG. 2** is a circuit **200** illustrating exemplary low noise amplifier (LNA) **201***a* and power amplifier (PA) **201***b* circuits that may be utilized in connection with an embodiment of the invention. Referring to **FIG. 2**, the exemplary LNA amplifier circuit **201***a* may comprise a LNA **204** and a downconversion mixer **208**. The exemplary PA amplifier circuit **201***b* may comprise a PA **222** and an upconversion mixer **226**.

[0041] The LNA **204** in the LNA amplifier circuit **201***a* may comprise suitable circuitry and/or code and may be adapted to receive an input signal **202** and generate an amplified RF signal **206**. The LNA **204** may be also adapted to adjust the gain of the input signal **202** in accordance with one or more gain control signals, for example. In one aspect of the invention, the LNA **204** may comprise one or more NMOS transistors, such as TW NMOS transistors, that may be utilized by the amplifier core as a switch for triggering different gain levels. For example, a TW NMOS transistor utilized by the LNA **204** may be adapted to be turned on and off in accordance with the gain control signal, triggering low and high gain, respectively.

[0042] The downconversion mixer **208** may comprise suitable circuitry and/or logic and may be adapted to receive the RF signal **206** and downconvert it to an intermediate frequency (IF)/baseband signal **210**. The IF/baseband signal **210** may then be further filtered and/or amplified.

[0043] In operation, the LNA **204** may receive the incoming signal **202** and may amplify it in accordance with one or more gain control signals communicated to the LNA **204**. Well defined gain levels and reduced parasitic capacitance within the LNA **204** may be achieved by using a TW NMOS transistor as a switch. In this manner, by utilizing a gain control signal corresponding to a power status of the TW NMOS transistor, the LNA **204** may apply a maximum gain, if the input signal **202** comprises a weak desired signal, or a minimum gain, if the input signal **202** comprises a strong interference/blocker signal. After the LNA **204** amplifies the input signal **202** and generates the RF signal **206**, the downconversion mixer **208** may downconvert the RF signal **206** to IF/baseband signal **210**. The IF/baseband signal **210** may then be further processed by additional filtering and/or amplifying, for example.

[0044] The PA **222** in the PA amplifier circuit **201***b* may comprise suitable circuitry and/or code and may be adapted to receive an upconverted RF signal **224** and generate an amplified output signal **220**. The PA **222** may be also adapted to adjust the gain of the RF signal **224** in accordance with one or more gain control signals, for example. In another aspect of the invention, the PA **222** may comprise one or more NMOS transistors, such as TW NMOS transistors, that may be utilized by the amplifier core as a switch for triggering different gain levels. For example, a TW NMOS transistor utilized by the PA **222** may be adapted to be turned on and off in accordance with the gain control signal, triggering low and high gain, respectively.

[0045] The upconversion mixer **226** may comprise suitable circuitry and/or logic and may be adapted to receive an IF/baseband signal **228** and upconvert it to an RF signal **224**. After the RF signal **224** is amplified by the PA **222**, it may be transmitted as an output signal **220**.

[0046] In operation, an IF/baseband signal **228** may be upconverted by the upconversion mixer **226** to generate RF signal **224**. The PA **222** may receive the incoming RF signal **224** and may amplify it in accordance with one or more gain control signals communicated to the PA **222**. Well defined gain levels and reduced parasitic capacitance within the PA **222** may be achieved by using a TW NMOS transistor as a switch. In this manner, by utilizing a gain control signal corresponding to a power status of the TW NMOS transistor, the PA **222** may apply a maximum gain, if the input RF signal **224** comprises a weak desired signal, or a minimum gain, if the input RF signal **224** comprises a strong interference/blocker signal.

[0047] **FIG. 3** is a circuit illustrating an exemplary amplifier circuit with a PMOS transistor switch that may be utilized in connection with an embodiment of the invention. Referring to **FIG. 3**, the amplifier circuit **300** may comprise inductors **312** and **314**, PMOS transistor PT, and amplifier core **302**. The amplifier core **302** may comprise suitable circuitry and/or logic and may be adapted to receive an incoming signal **318**, amplify the received signal, and generate an output signal **320**. For example, the amplifier core **302** may comprise one or more NMOS transistors that may be utilized for amplifying the input signal **318**.

[0048] In one aspect of the invention, the amplifier core **302** may utilize PMOS transistor PT to control one or more gain levels of the amplifier core **302**. The source **304** and drain **306** of transistor PT may be coupled to inductors **312** and **314**, respectively. The gate **308** of transistor PT may be coupled to voltage rail **316**. A gain control signal **310** may be asserted on the gate **308** to enable or disable the transistor PT and to assert low or high gain on the incoming signal **318**.

[0049] In operation, the amplifier core **302** may receive the incoming signal **318**. If the incoming signal **318** comprises a weak desired signal, the gain control (GC) signal **310** may be asserted, for example, GC set to logic **1**, by connecting the gate **308** of transistor PT to voltage rail **316** with voltage V_{DD}. If the gain control signal **310** is asserted, the PMOS transistor PT will be turned off and the amplifier core **302** may assert high gain on the incoming signal **318**. If the incoming signal **318** comprises a strong interference/blocker signal, the gain control signal **310** may be de-asserted, for example, GC set to logic **0**, by disconnecting the gate **308** of transistor PT from voltage rail **316** with voltage V_{DD}. If the gain control signal **310** is de-asserted, the PMOS transistor PT will be turned on and the amplifier core **302** may assert low gain on the incoming signal **318**.

[0050] In one aspect of the invention, parasitic capacitance within the amplifier circuit **300** may be reduced and sensitivity of the amplifier core **302** may be increased by utilizing an NMOS transistor, such as a triple well NMOS transistor, in place of the PMOS transistor PT as further explained with regard to **FIGS. 5A and 5B**.

[0051] **FIG. 4** is an exemplary diagram **400** illustrating NMOS, PMOS, and triple well (TW) NMOS transistors that may be utilized in connection with an embodiment of the invention. Referring to **FIG. 4**, there is illustrated an exemplary NMOS transistor **402**, a PMOS transistor **410**, and a TW NMOS transistor **420**.

[0052] The NMOS transistor **402** may comprise a gate **404**, a source **406**, and a drain **408**. The source **406** and the drain **408** may be implemented in a p-substrate **432**. The PMOS transistor **410** may comprise a gate **412**, a source **414**, and a drain **416**. The source **414** and the drain **416** may be implemented in an n-well **418**, and the n-well **418** may be implemented in the p-substrate **432**. The TW NMOS transistor **420** may comprise a gate **422**, a source **424**, and a drain **426**. The source **424** and the drain **426** may be implemented in a p-well **428**. The p-well **428** may be implemented in an n-well **430**, and the n-well **430** may be implemented in the p-substrate **432**.

[0053] The NMOS transistor **402**, PMOS transistor **410**, and TW NMOS transistor **420** may each be utilized as gain control switches in accordance with an amplifier circuit, such as a LNA and/or a PA circuit. The TW NMOS transistor **420**, however, may be utilized to achieve low parasitic capacitance within the amplifier circuit, as well as increased gain control sensitivity. As a result, an amplifier circuit utilizing TW NMOS switch for gain control may be characterized with well defined high and/or low gain and improved amplifier linearity.

[0054] **FIG. 5A** is a circuit illustrating an amplifier circuit with a triple well (TW) NMOS transistor, in accordance with an embodiment of the invention. Referring to **FIG. 5A**, the amplifier circuit **500** may comprise inductors **505** and **504**, a TW NMOS transistor NT, and an amplifier core **502**. The amplifier core **502** may comprise suitable circuitry and/or logic and may be adapted to receive an incoming signal **514**, amplify the received signal, and generate an output signal **516**. For example, the amplifier core **502** may comprise one or more NMOS transistors that may be utilized for amplifying the input signal **514**.

[0055] In one aspect of the invention, the amplifier core **502** may utilize the TW NMOS transistor TW to control one or more gain levels of the amplifier core **502**. The source **518** and drain **520** of transistor NT may be coupled to inductors **505** and **504**, respectively. The inductors **505** and **504** may be coupled to voltage rail **512** with supply voltage V_{DD}. Since transistor NT is an NMOS transistor, the gate voltage V_G for gate **506** may be represented as $V_G=V_{DD}+V_T$, where V_T is a determined threshold voltage. The gate **506**, therefore, may be connected to a different supply voltage rail **513** in order for transistor NT to operate as a switch. The supply voltage rail **513** may utilize supply voltage V_{DD1}, where $V_{DD1}>V_{DD}$. In an exemplary aspect of the invention, V_{DD} may be approximately 1.2V and V_{DD1} may be approximately 2.5V, for example. A gain control signal **508** may be asserted on the gate **506** to enable or disable the transistor NT and to assert low or high gain on the incoming signal **514**. The third well **510** of transistor NT may be connected to voltage supply rail **512** with voltage V_{DD}.

[0056] In operation, the amplifier core **502** may receive the incoming signal **514**. If the incoming signal **514** comprises a strong interference/blocker signal, the gain control (GC) signal **508** may be asserted, for example, GC set to logic **1**, by connecting the gate **506** of transistor NT to voltage rail **513** with voltage VDD_1 and the third well **510** to supply voltage rail **512** with voltage V_{DD}. If the gain control signal **508** is asserted, or GC is set to logic **1**, the TW NMOS transistor NT will be turned on and the amplifier core **502** may assert low gain on the incoming signal **514**. If the incoming signal **514** comprises a weak desired signal, the gain control signal **508** may be de-asserted, for example, GC set to logic **0**, by disconnecting the gate **506** of transistor NT from voltage rail **513** with voltage V_{DD1}. If the gain control signal **508** is de-asserted, or GC is set to logic **0**, the TW NMOS transistor NT will be turned off and the amplifier core **502** may assert high gain on the incoming signal **514**.

[0057] In a different aspect of the invention, an amplifying circuit may utilize several TW NMOS transistors in order to achieve a well defined gain at more than two gain levels. For example, an amplifying circuit utilizing more than one TW NMOS transistors as gain control switches, may be characterized by a well defined high gain, low gain, as well as several well defined mid-gains, for example.

[0058] **FIG. 5B** is a circuit illustrating an amplifier circuit with a plurality of triple well (TW) NMOS transistors, in accordance with an embodiment of the invention. Referring to **FIG. 5B**, the amplifier circuit **550** may comprise inductors **555** and **554**, TW NMOS transistors NT_1 through NT_n, and an amplifier core **552**. The amplifier core **552** may comprise suitable circuitry and/or logic and may be adapted to receive an incoming signal **564**, amplify the received signal, and generate an output signal **566**. For example, the amplifier core **552** may comprise one or more NMOS transistors that may be utilized for amplifying the input signal **564**.

[0059] In one aspect of the invention, the amplifier core **552** may utilize the TW NMOS transistors NT_1 through NT_n to control a plurality of gain levels of the amplifier core **552**. Source connections **568** through **576**, and drain connections **570** through **578** of transistors NT_1 through NT_n may be coupled to inductors **555** and **554**, respectively. Inductors **555** and **554** may be coupled to voltage rail **562** with supply voltage V_{DD}. Since transistors NT_1 through NT_n are NMOS transistors, the respective gate voltages V_G for gates **556** through **574** may be represented as $V_G=V_{DD}+V_T$, where V_T is a determined threshold voltage.

[0060] Gates **556** through **574**, therefore, may be connected to a different supply voltage rail **563** in order for transistors NT_1 through NT_n to operate as a switches for different gain levels of the amplifier core **552**. The supply voltage rail **563** may utilize supply voltage V_{DD1}, where $V_{DD1}>V_{DD}$. In an exemplary aspect of the invention, V_{DD} may be approximately 1.2V and V_{DD1} may be approximately 2.5V, for example. Gain control signals **558** through **580** may be asserted on gates **556** through **574**, respectively, to enable or disable transistors NT_1 through NT_n and to assert low or high gain on the incoming signal **564**. Third well connections **560** through **572** of transistors NT_1 through NT_n, respectively, may be connected to voltage supply rail **562** with voltage V_{DD}.

[0061] In operation, the amplifier core **552** may receive the incoming signal **564**. If the incoming signal **564** comprises a weak desired signal, the gain control (GC) signals

558 through **580** may be asserted, for example, GC set to logic **1**, by connecting the gates **556** through **574** of transistors NT_1 through NT_n to voltage rail **563** with voltage V_{DD1}. Third well connections **560** through **572** may be connected to supply voltage rail **562** with voltage V_{DD}. If gain control signals **558** through **580** are asserted, TW NMOS transistors NT_1 through NT_n will be turned off and the amplifier core **552** may assert high gain on the incoming signal **564**. If the incoming signal **564** comprises a strong interference/blocker signal, gain control signals **558** through **580** may be de-asserted, for example, GC set to logic **0**, by disconnecting gates **556** through **574** of transistors NT_1 through NT_n from voltage rail **563** with voltage V_{DD1}. If gain control signals **558** through **580** are de-asserted, TW NMOS transistors NT_1 through NT_n will be turned on and the amplifier core **552** may assert low gain on the incoming signal **564**.

[**0062**] In a different aspect of the invention, one or more well defined gains within the amplifier core **552** may be asserted by utilizing different number of TW NMOS transistors. For example, by asserting different number of gain control signals and connecting different combination of gates from the plurality of gates **556** through **574**, the amplifier core **552** may be characterized by several well defined mid gain levels, for example.

[**0063**] Accordingly, aspects of the invention may be realized in hardware, software, firmware or a combination thereof. The invention may be realized in a centralized fashion in at least one computer system, or in a distributed fashion where different elements are spread across several interconnected computer systems. Any kind of computer system or other apparatus adapted for carrying out the methods described herein is suited. A typical combination of hardware, software and firmware may be a general-purpose computer system with a computer program that, when being loaded and executed, controls the computer system such that it carries out the methods described herein.

[**0064**] One embodiment of the present invention may be implemented as a board level product, as a single chip, application specific integrated circuit (ASIC), or with varying levels integrated on a single chip with other portions of the system as separate components. The degree of integration of the system will primarily be determined by speed and cost considerations. Because of the sophisticated nature of modern processors, it is possible to utilize a commercially available processor, which may be implemented external to an ASIC implementation of the present system. Alternatively, if the processor is available as an ASIC core or logic block, then the commercially available processor may be implemented as part of an ASIC device with various functions implemented as firmware.

[**0065**] The invention may also be embedded in a computer program product, which comprises all the features enabling the implementation of the methods described herein, and which when loaded in a computer system is able to carry out these methods. Computer program in the present context may mean, for example, any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following: a) conversion to another language, code or notation; b) reproduction in a different material form. However, other meanings of computer program within the understanding of those skilled in the art are also contemplated by the present invention.

[**0066**] While the invention has been described with reference to certain embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present invention without departing from its scope. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the present invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A circuit for processing signals, comprising a triple well (TW) NMOS transistor coupled to an amplifier core, said TW NMOS transistor tracks process and temperature variations (PVT) of at least one NMOS transistor within said amplifier core.

2. The circuit according to claim 1, wherein a drain of said TW NMOS transistor is coupled to a first inductor.

3. The circuit according to claim 2, wherein said first inductor is coupled to a first voltage source.

4. The circuit according to claim 3, wherein said first voltage source generates a standard voltage of about 1.2V.

5. The circuit according to claim 1, wherein a source of said TW NMOS transistor is coupled to a second inductor.

6. The circuit according to claim 5, wherein said second inductor is coupled to said first voltage source.

7. The circuit according to claim 1, wherein a gate of said TW NMOS transistor is coupled to a second voltage source.

8. The circuit according to claim 7, wherein said second voltage source generates a standard voltage of about 2.5V.

9. The circuit according to claim 7, wherein said gate receives a control signal associated with a power status of said TW NMOS transistor.

10. The circuit according to claim 1, wherein a third well of said TW NMOS transistor is coupled to said first voltage source.

11. A method for processing signals, comprising tracking process and temperature variations (PVT) of at least one NMOS transistor within an amplifier core utilizing a triple well (TW) NMOS transistor coupled to said amplifier core.

12. The method according to claim 11, further comprising coupling a drain of said TW NMOS transistor to a first inductor.

13. The method according to claim 12, further comprising coupling said first inductor to a first voltage source.

14. The method according to claim 13, wherein said first voltage source generates a standard voltage of about 1.2V.

15. The method according to claim 11, further comprising coupling a source of said TW NMOS transistor to a second inductor.

16. The method according to claim 15, further comprising coupling said second inductor to said first voltage source.

17. The method according to claim 11, further comprising coupling a gate of said TW NMOS transistor to a second voltage source.

18. The method according to claim 17, wherein said second voltage source generates a standard voltage of about 2.5V.

19. The method according to claim 17, further comprising receiving by said gate a control signal associated with a power status of said TW NMOS transistor.

20. The method according to claim 11, further comprising coupling a third well of said TW NMOS transistor to said first voltage source.

21. A circuit for processing signals, comprising a triple well (TW) NMOS transistor coupled to an amplifier core, said TW NMOS transistor tracks process and temperature variations (PVT) of at least one NMOS transistor within said amplifier core, wherein

a source of said TW NMOS transistor is coupled to a first terminal of a first inductor;

said first terminal of said first inductor is coupled to said amplifier core;

a second terminal of said first inductor is coupled to a first voltage source;

a gate of said TW NMOS transistor is coupled to a second voltage source;

a drain of said TW NMOS transistor is coupled to a first terminal of a second inductor;

said first terminal of said second inductor is coupled to said amplifier core; and

a second terminal of said second inductor is coupled to said first voltage source.

22. The circuit according to claim 21, wherein a third well of said TW NMOS transistor is coupled to said first voltage source.

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