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(54) **TRENCH FORMATION SCHEME FOR PROGRAMMABLE METALLIZATION CELL TO PREVENT METAL REDEPOSIT**

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsin-Chu (TW)

(72) Inventors: **Fu-Ting Sung**, Yangmei City (TW); **Chung-Chiang Min**, Zhubei City (TW); **Yuan-Tai Tseng**, Zhubei City (TW)

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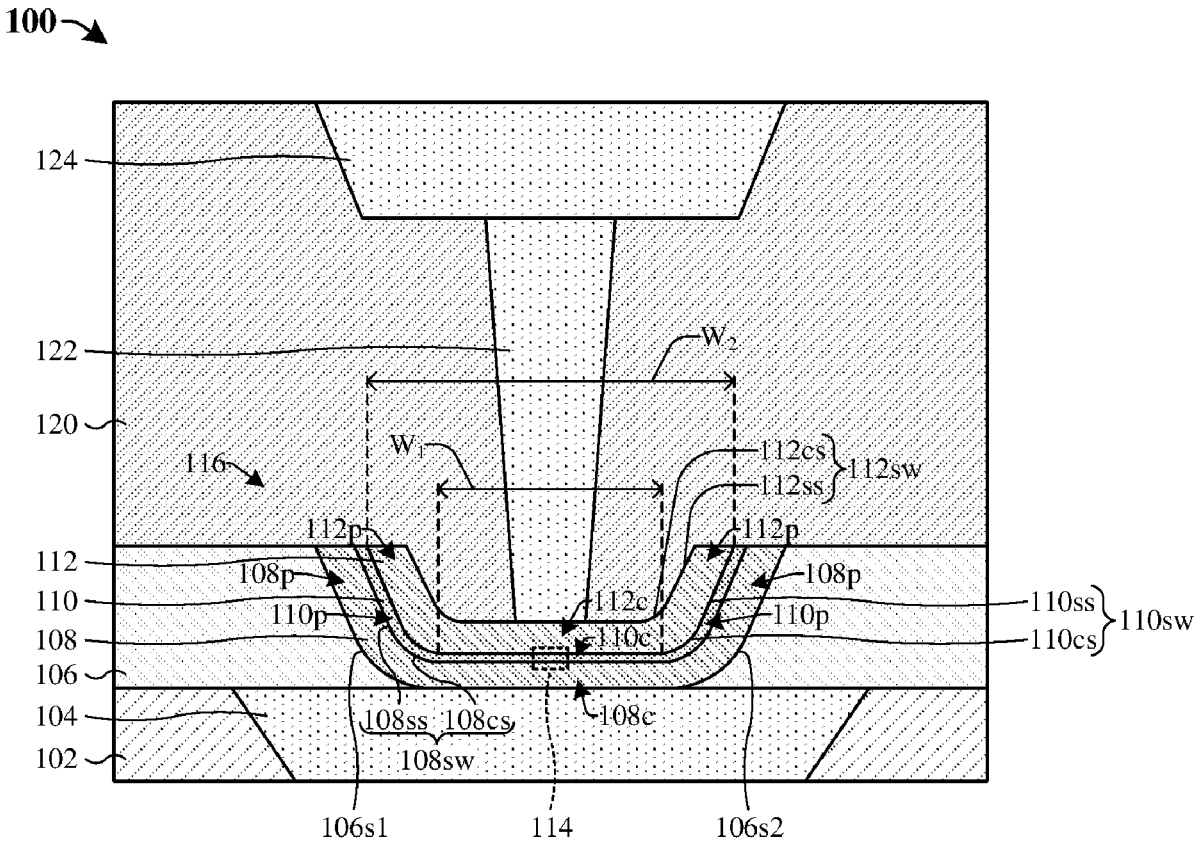
(57) **ABSTRACT**

Some embodiments relate to a memory device. The memory device includes a top electrode overlying a bottom electrode. A data storage layer overlies the bottom electrode. The bottom electrode cups an underside of the data storage layer. The top electrode overlies the data storage layer. A top surface of the bottom electrode is aligned with a top surface of the top electrode.



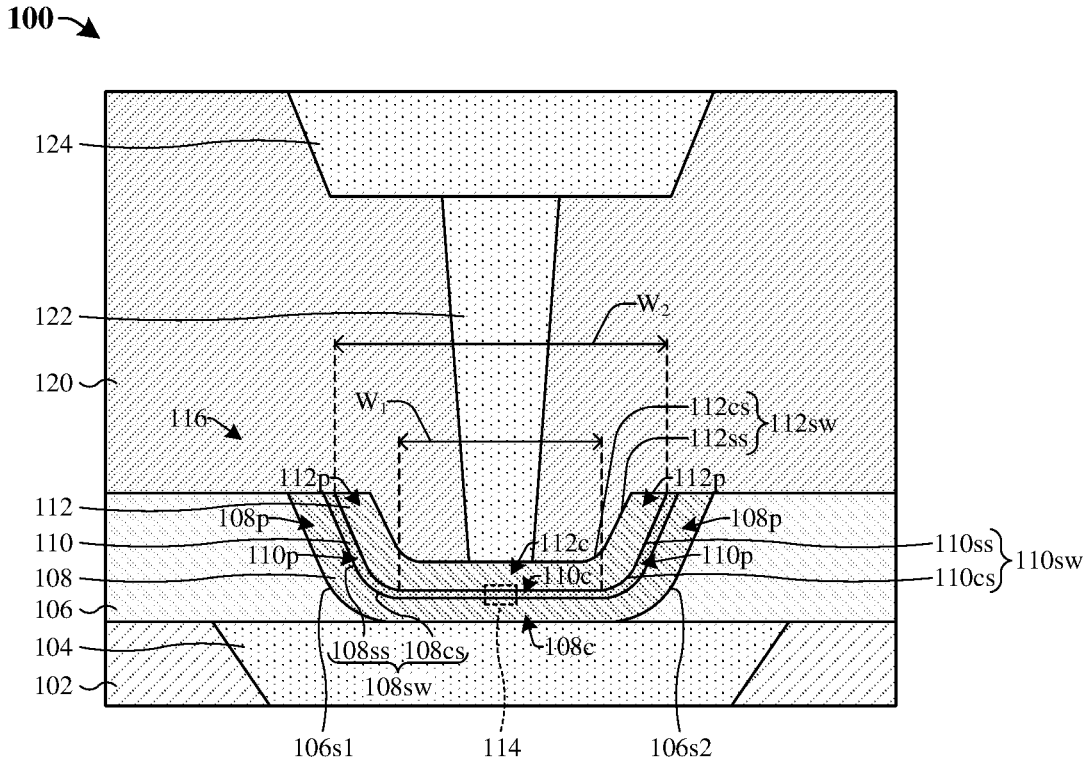

100
124
122
120
116
112
110
108
106
104
102
W_2
W_1
112cs
112ss
112sw
112p
112p
108p
108p
110p
110p
112c
110c
110ss
110cs
110sw
108ss
108cs
108sw
108c
106s1
114
106s2

Fig. 1

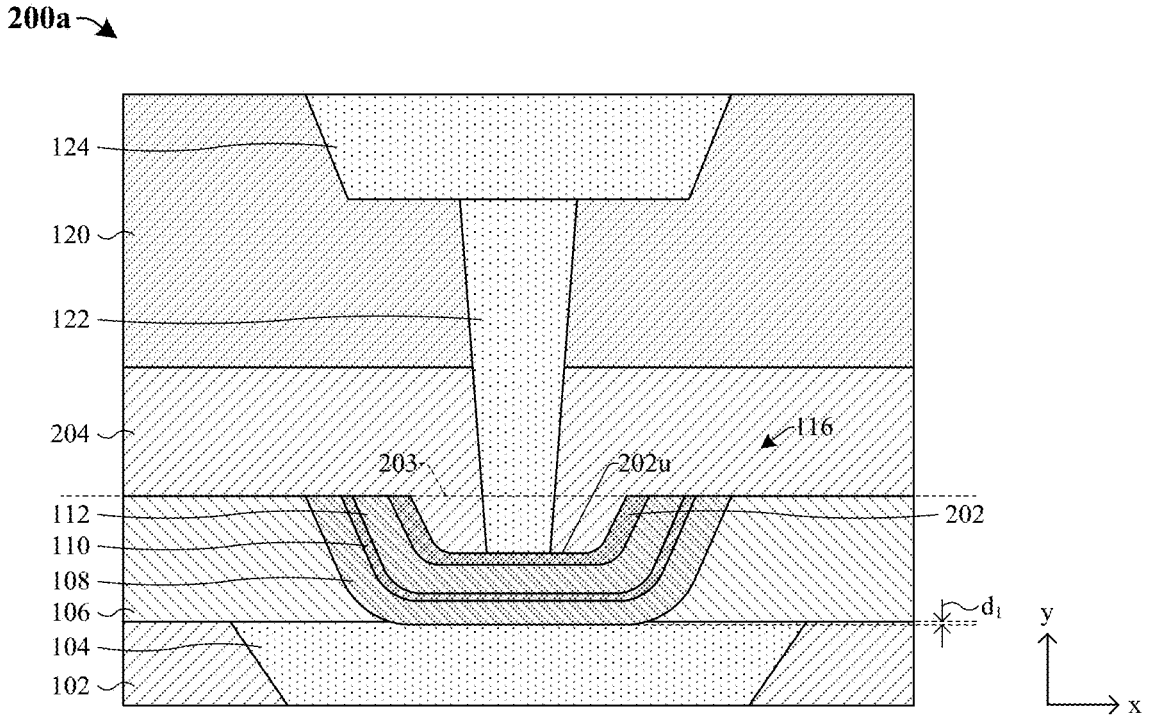

200a
124
120
122
204
116
203
202u
202
112
110
108
106
104
102
d_1
y
x

Fig. 2A

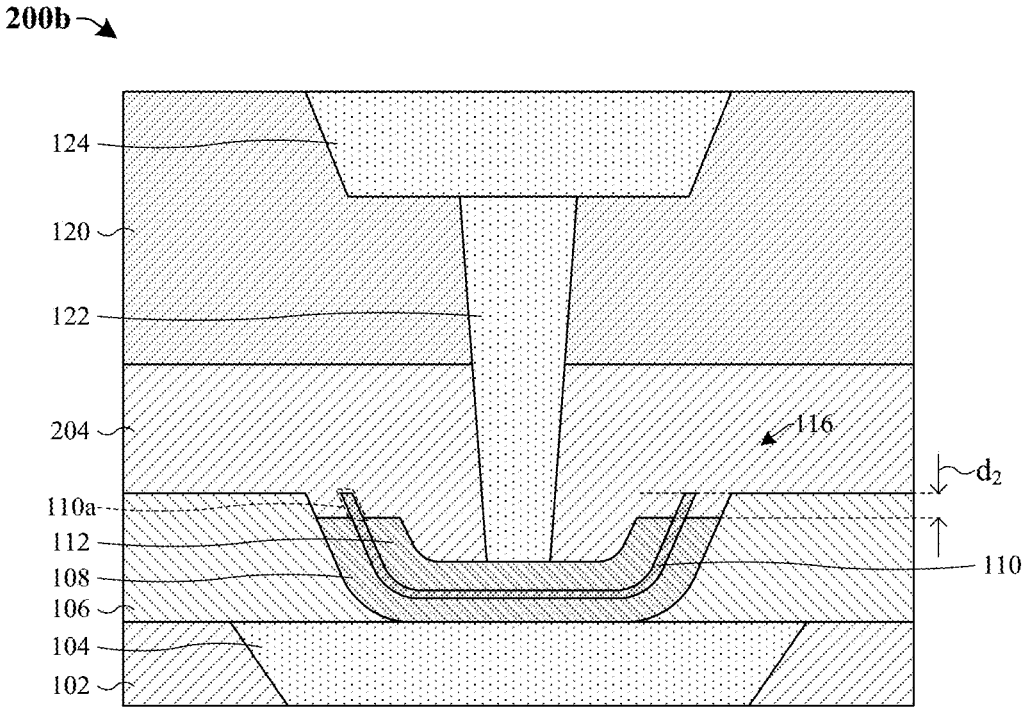

200b
124
120
122
204
116
d_2
110a
112
110
108
106
104
102

Fig. 2B

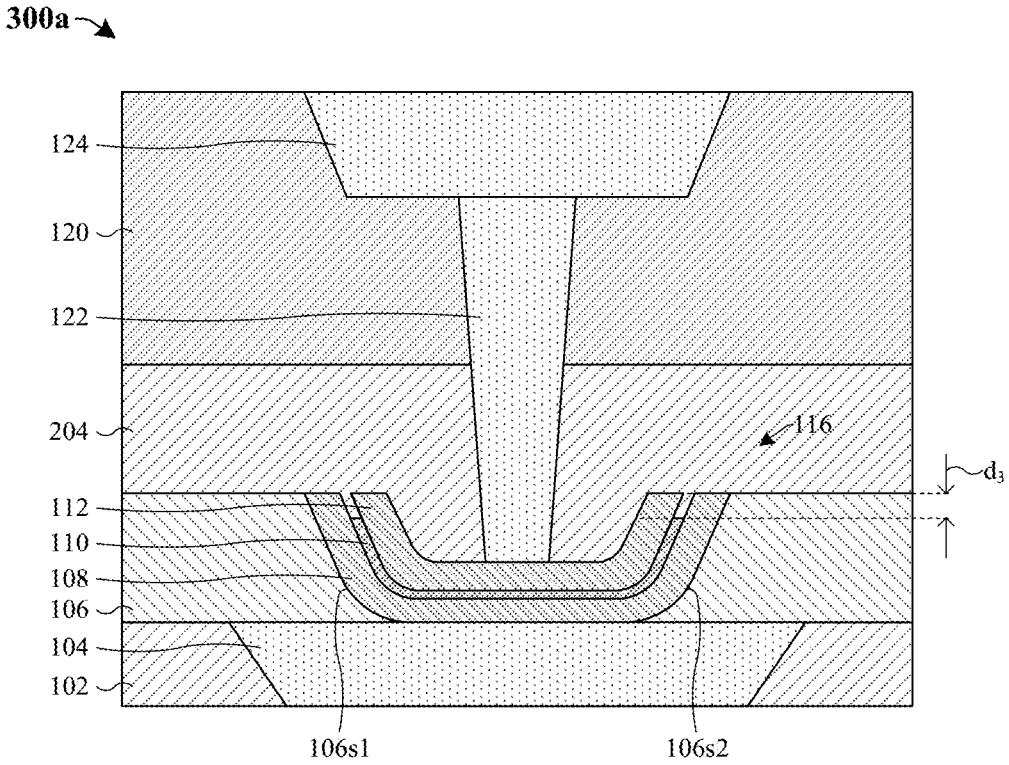

300a
124
120
122
204
116
d_3
112
110
108
106
104
102
106s1
106s2

Fig. 3A

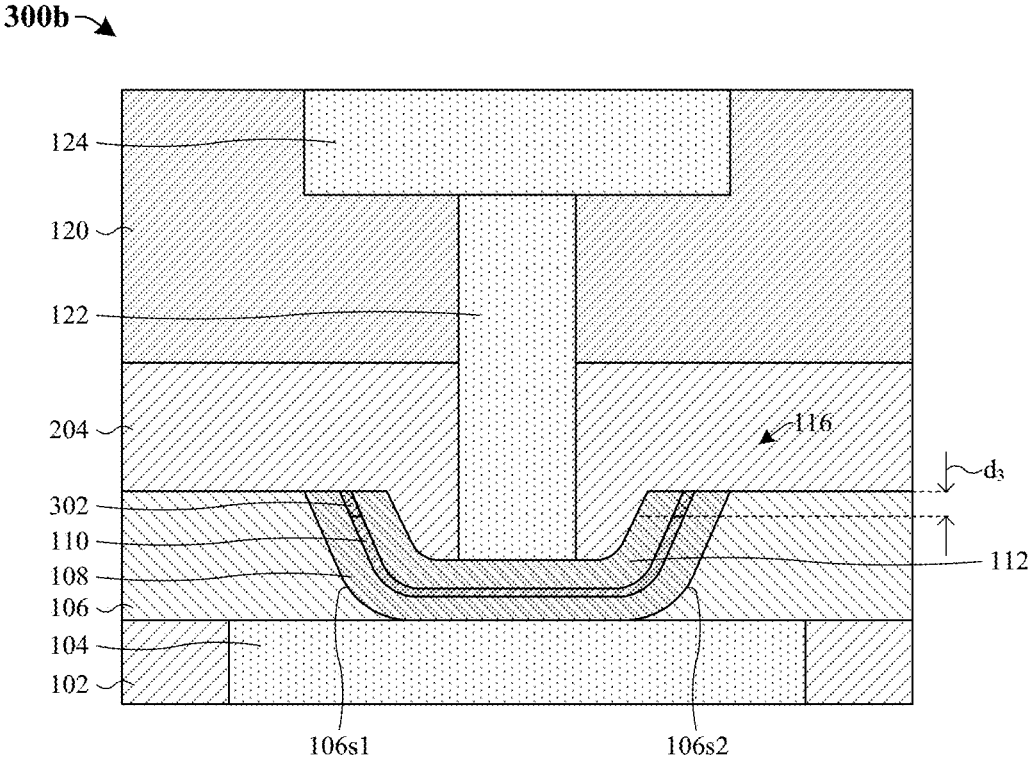

300b
124
120
122
204
116
d_3
302
110
112
108
106
104
102
106s1
106s2

Fig. 3B

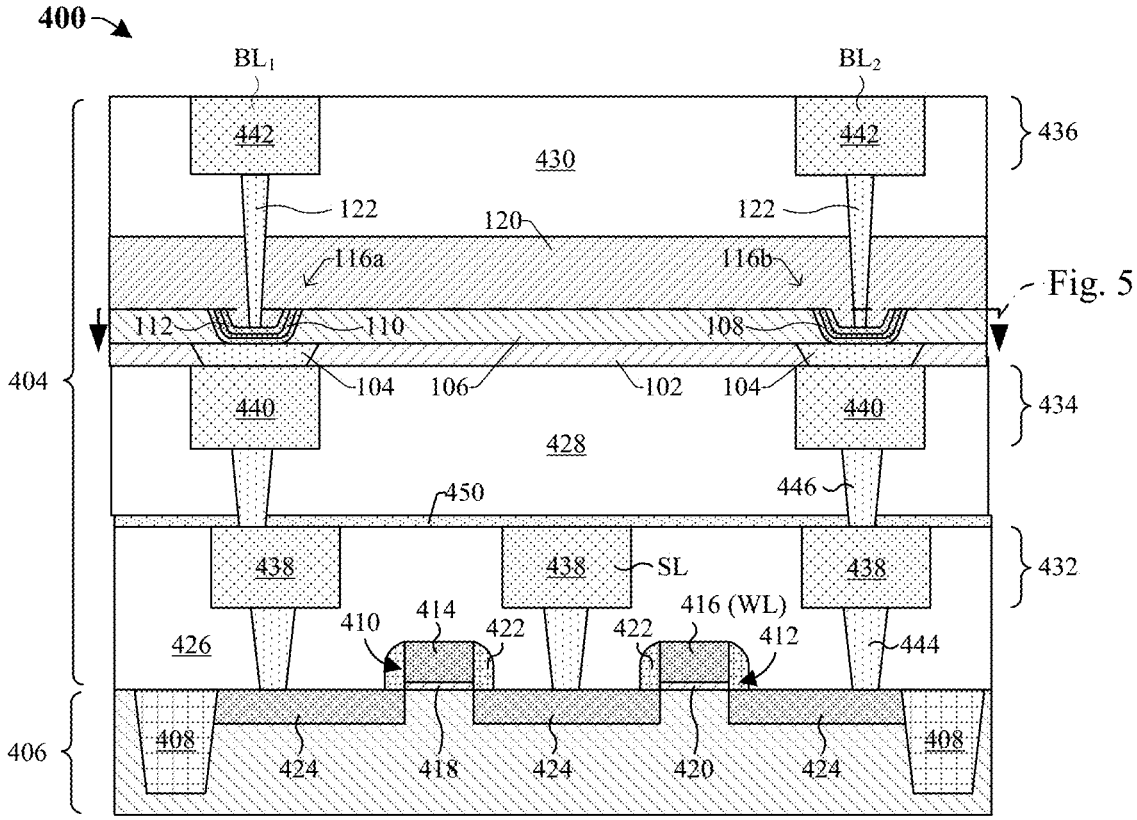

400
BL1
BL2
442
442
436
430
122
120
122
116a
116b
Fig. 5
112
110
108
404
104
106
102
104
440
440
434
428
450
446
438
438
SL
438
432
410
414
422
422
416 (WL)
412
426
444
406
408
424
418
424
420
424
408

Fig. 4

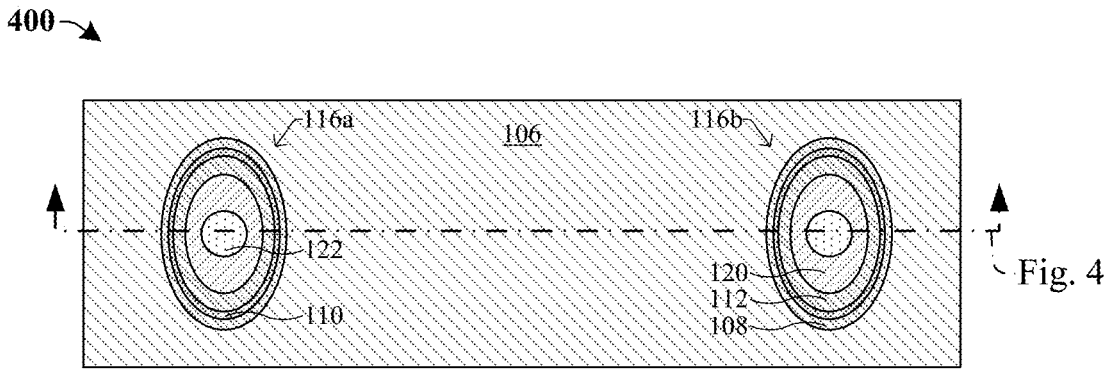

400
116a
106
116b
122
120
112
110
108
Fig. 4

Fig. 5

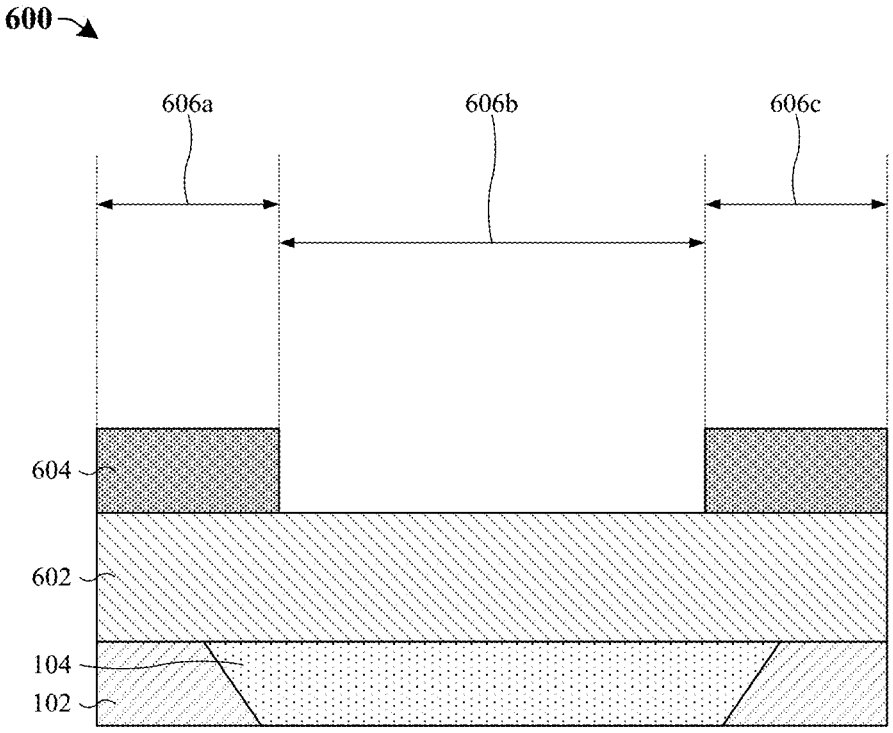

600
606a
606b
606c
604
602
104
102

Fig. 6

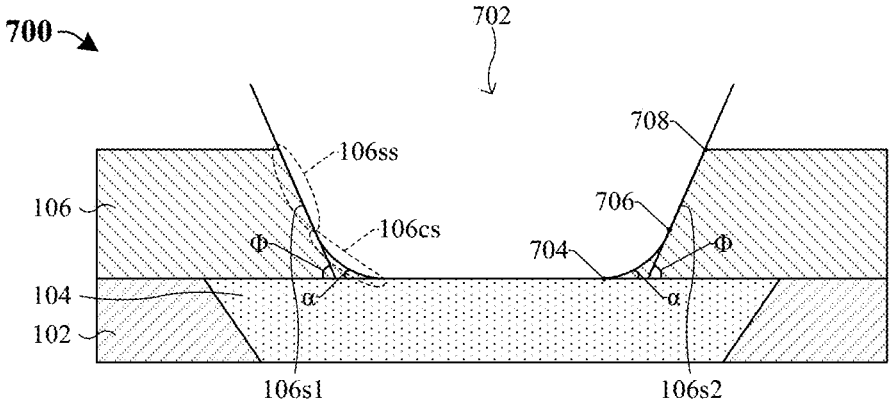

700
702
708
106ss
106
706
106cs
Φ
704
Φ
104
α
α
102
106s1
106s2

Fig. 7

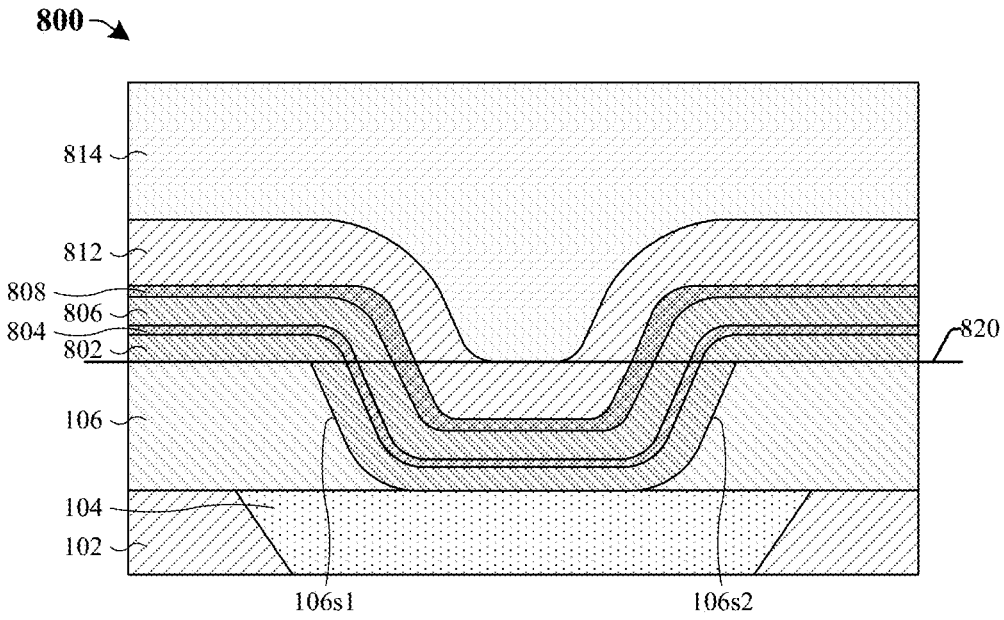

800
814
812
808
806
804
802
820
106
104
102
106s1
106s2

Fig. 8

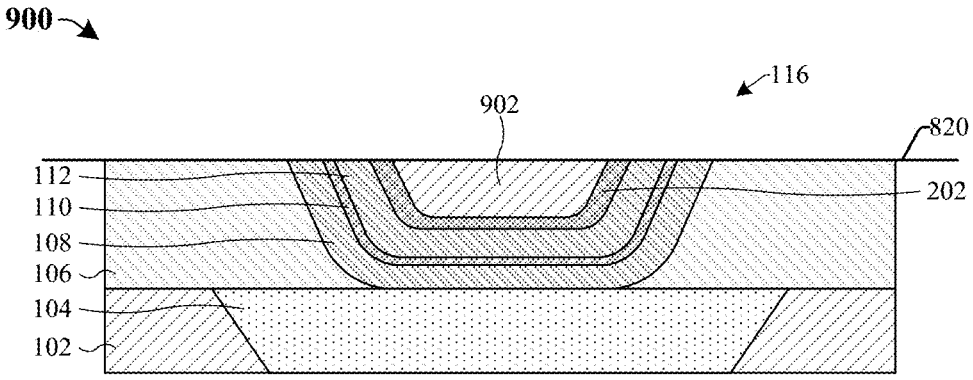

900
116
902
820
112
110
108
106
104
102
202

Fig. 9

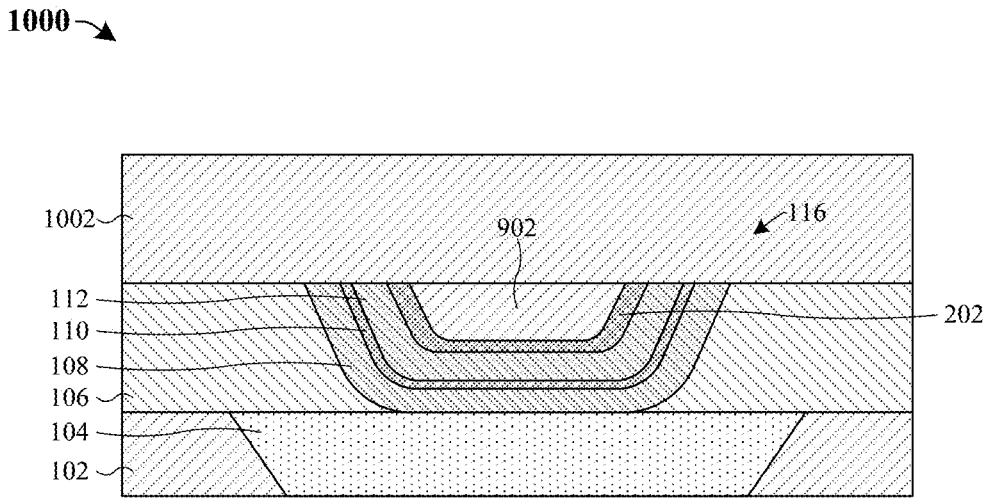

1000
1002
902
116
112
110
108
106
104
102
202

Fig. 10

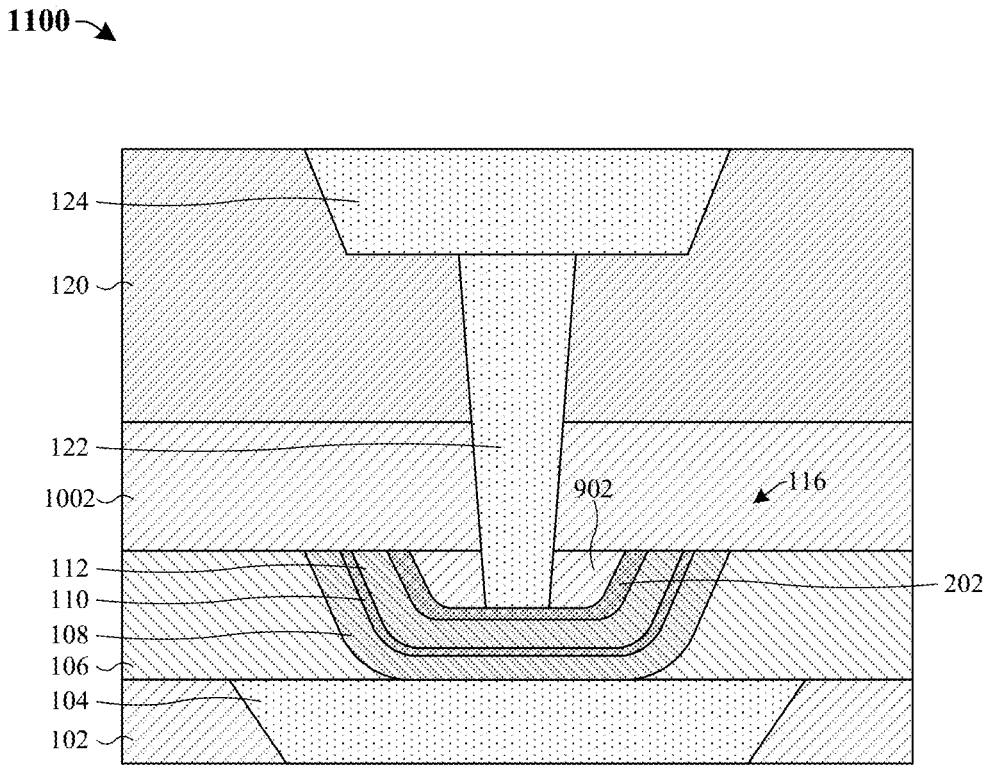

1100
124
120
122
1002
902
116
112
110
108
106
104
102
202

Fig. 11

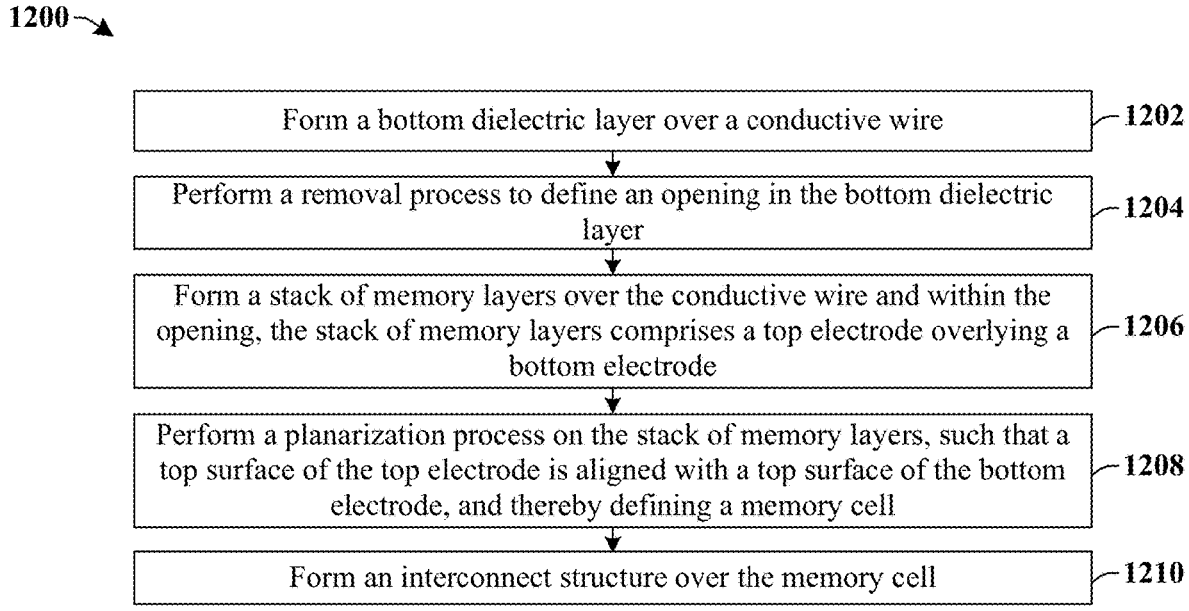

1200
Form a bottom dielectric layer over a conductive wire
1202
Perform a removal process to define an opening in the bottom dielectric layer
1204
Form a stack of memory layers over the conductive wire and within the opening, the stack of memory layers comprises a top electrode overlying a bottom electrode
1206
Perform a planarization process on the stack of memory layers, such that a top surface of the top electrode is aligned with a top surface of the bottom electrode, and thereby defining a memory cell
1208
Form an interconnect structure over the memory cell
1210

Fig. 12

TRENCH FORMATION SCHEME FOR PROGRAMMABLE METALLIZATION CELL TO PREVENT METAL REDEPOSIT

BACKGROUND

[0001] Many modern day electronic devices contain electronic memory. Electronic memory may be volatile memory or non-volatile memory. Non-volatile memory is able to retain its stored data in the absence of power, whereas volatile memory loses its stored data when power is lost. Programmable metallization cell (PMC) random access memory (RAM), which may also be referred to as conductive bridging RAM, CBRAM, Nanobridge, or electrolytic memory, is one promising candidate for next generation non-volatile electronic memory due to advantages over current electronic memory. Compared to current non-volatile memory, such as flash random-access memory, PMCRAM typically has better performance and reliability. Compared to current volatile memory, such as dynamic random-access memory (DRAM) and static random-access memory (SRAM), PMCRAM typically has better performance and density, with lower power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0003] FIG. **1** illustrates a cross-sectional view of some embodiments of a memory device including a programmable metallization cell.

[0004] FIGS. **2**A-**2**B and **3**A-**3**B illustrate cross-sectional views of various alternative embodiments of the memory device of FIG. **1**.

[0005] FIG. **4** illustrates a cross-sectional view of some embodiments of a memory device including two programmable metallization cells.

[0006] FIG. **5** illustrates a top view of some embodiments of the memory device of FIG. **4**, as indicated by the cut-lines in FIGS. **4** and **5**.

[0007] FIGS. **6-11** illustrate cross-sectional views of some embodiments of a method of forming a memory device including a programmable metallization cell.

[0008] FIG. **12** illustrates a methodology in flowchart format that illustrates some embodiments of a method of forming a memory device including a programmable metallization cell.

DETAILED DESCRIPTION

[0009] The present disclosure provides many different embodiments, or examples, for implementing different features of this disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0010] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0011] A programmable metallization cell generally includes a data storage layer arranged between a top electrode and a bottom electrode. When a set voltage is applied across the top and bottom electrodes, a conductive bridge is formed within the data storage layer (resulting in a low resistance state). When a reset voltage is applied across the top and bottom electrodes, the conductive bridge is erased within the data storage layer (resulting in a high resistance state).

[0012] During fabrication of the programmable metallization cell, a memory cell stack is formed over a substrate. The memory cell stack comprises a data storage layer disposed between a top electrode layer and a bottom electrode layer. A hard mask layer is formed over the top electrode layer. Separate etch processes are subsequently performed to define top and bottom electrodes. For example, a first etch process (e.g., a first plasma etch process) is performed to define a top electrode by patterning the top electrode layer. During the first etch process, material (e.g., titanium nitride) from the top electrode layer will re-deposit onto sidewalls of the hard mask layer. During a second etch process (e.g., a second plasma etch process) used to define the bottom electrode, material from the top electrode and/or the bottom electrode layer may be etched and redistributed onto sidewalls of the data storage layer. Since the material is conductive, the material may electrically short the top and bottom electrodes, thereby rendering the programmable metallization cell inoperable. Additionally, a wet clean process (e.g., using cleaning solution(s) such as hydrofluoric acid and/or deionized water) utilized after the separate etch processes (e.g., to reduce the re-deposited conductive material) may damage an interface(s) between the top and/or bottom electrode and the data storage layer, thereby leading to peeling between the layers. This, in part, may impair a stability, endurance, and/or switching time of the programmable metallization cell.

[0013] In some embodiments of the present disclosure, to eliminate the re-deposition of material from the top electrode and/or bottom electrode layer onto sidewalls of the memory cell stack, the memory cell stack may be formed by a planarization process (e.g., a chemical-mechanical planarization (CMP) process) instead of separate etch processes. In such embodiments, a dielectric layer is formed over a conductive wire and a masking layer is formed over outer regions of the dielectric layer. An etch process is performed to define an opening in the dielectric layer directly above a center portion of the conductive wire. The

memory cell stack is formed within the opening such that an upper surface of the memory cell stack is recessed below a top surface of the dielectric layer. A planarization process is performed on the memory cell stack until the top surface of the dielectric layer is reached, thereby defining a programmable metallization cell. By virtue of the planarization process, layers within the programmable metallization cell respectively have a U-shaped profile. After forming the programmable metallization cell, the wet clean process (e.g., the wet clean process described above) is performed on the programmable metallization cell. The U-shaped profile of the layers in the programmable metallization cell mitigates and/or prevents peeling between the layers. The memory cell stack is not formed by a plasma etch process, thereby mitigating and/or eliminating a re-deposition of conductive material on the top and/or bottom electrodes. Thus, this method facilities formation of the programmable metallization cell without etching the memory cell stack, and thereby prevents the top and bottom electrodes from being shorted together. Additionally, replacing the separate etch processes with the planarization process reduces costs and time associated with forming the programmable metallization cell, and mitigates peeling at the interface(s) between the top and/or bottom electrode and the data storage layer. This, in part, increases a stability, endurance, and/or switching time of the programmable metallization cell.

[0014] Referring to FIG. **1**, a cross-sectional view of some embodiments of a memory device **100** including a memory cell **116** is provided.

[0015] The memory cell **116** includes a bottom electrode **108** and a top electrode **112**, with a data storage layer **110** (in some embodiments, also known as an insulator layer or an electrolyte) disposed between the top and bottom electrode **112**, **108**. The memory cell **116** is disposed within a bottom dielectric layer **106**, such that a top surface of the memory cell **116** is aligned with a top surface of the bottom dielectric layer **106**, and a bottom surface of the memory cell **116** is aligned with a bottom surface of the bottom dielectric layer **106**. In some embodiments, the memory cell **116** is configured as a programmable metallization cell (PMC) random access memory (RAM), which may also be referred to as conductive bridging RAM, CBRAM, Nanobridge, or electrolytic memory.

[0016] The memory cell **116** is often disposed over an inter-level dielectric (ILD) layer **102** with a bottom conductive wire **104** disposed within the ILD layer **102**. The bottom conductive wire **104** electrically couples the bottom electrode **108** to underlying metal layers and/or complementary metal-oxide-semiconductor (CMOS) devices (e.g., transistors, diodes, etc.) that may overlie a semiconductor substrate (not shown). A conductive via **122** overlies the top electrode **112**, and electrically couples the top electrode **112** to upper conductive layers (e.g., an upper conductive wire **124**. The conductive via **122** extends through an upper ILD structure **120**. The upper conductive wire **124** extends past sidewalls of the conductive via **122** and may be electrically coupled to an overlying bit line (not shown).

[0017] The bottom electrode **108** includes a central bottom electrode region **108***c* and a peripheral bottom electrode region **108***p* that extends upwardly from the central bottom electrode region **108***c*. Similarly, the data storage layer **110** and top electrode **112** include central regions **110***c*, **112***c*, respectively, over the bottom electrode central region **108***c*, and include peripheral regions **110***p*, **112***p*, respectively, over the bottom electrode peripheral region **108***p*.

[0018] In some embodiments, the bottom dielectric layer **106** has a pair of sidewalls **106***s***1**, **106***s***2** that are in direct contact with outer sidewalls of the bottom electrode **108**. The pair of sidewalls **106***s***1**, **106***s***2** respectively have a slanted segment overlying a curved segment, such that sidewalls (e.g., outer sidewalls and/or inner sidewalls) of the bottom electrode **108** respectively have a slanted segment overlying a curved segment. Further, sidewalls (e.g., outer sidewalls and/or inner sidewalls) of the data storage layer **110** respectively have a slanted segment overlying a curved segment, and sidewalls (e.g., outer sidewalls and/or inner sidewalls) of the top electrode **112** respectively have a slanted segment overlying a curved segment. The bottom electrode **108** underlies and cups a bottom surface and outer sidewalls of the data storage layer **110**. The data storage layer **110** underlies and cups a bottom surface and outer sidewalls of the top electrode **112**. A top surface of the bottom electrode **108**, a top surface of the data storage layer **110**, a top surface of the top electrode **112**, and a top surface of the bottom dielectric layer **106** are aligned. It may be appreciated, aligned as used herein contemplates that some small misalignments, such as due to tolerances (e.g., during a chemical-mechanical planarization (CMP) process used to form a device), may be present in the surfaces and/or parts of layers and/or structures that are aligned.

[0019] In some embodiments, the pair of sidewalls **106***s***1**, **106***s***2**, outer sidewalls of the bottom electrode **108**, outer sidewalls of the data storage layer **110**, and outer sidewalls of the top electrode **112** are defined from a cross-sectional view. For example, if when viewed from above the memory cell **116** is circular or elliptical then the pair of sidewalls **106***s***1**, **106***s***2** is a single continuous sidewall when viewed from above, therefore the "pair" of sidewalls **106***s***1**, **106***s***2** refers to the nature of this single continuous sidewall when depicted in in a cross-sectional view. Additionally, if when viewed from above the memory cell **116** is circular or elliptical then any length and/or width associated with a cross-sectional view of the layers comprising the memory cell **116** respectively correspond to diameters of a circle or lengths defined between two vertices on the major axis of an ellipse.

[0020] In some embodiments, an inner sidewall **112***sw* of the top electrode **112** has a slanted segment **112***ss* overlying a curved segment **112***cs*, such that a first width W_1 of the top electrode **112** is less than a second width W_2 of the top electrode **112**. As seen in FIG. **1**, the width of the top electrode **112** continuously increases from the first width W_1 to the second with W_2. Further, an inner sidewall **110***sw* of the data storage layer **110** has a slanted segment **110***ss* overlying a curved segment **110***cs*. Furthermore, an inner sidewall **108***sw* of the bottom electrode **108** has a slanted segment **108***ss* overlying a curved segment **108***cs*.

[0021] During operation, the memory cell **116** relies on redox reactions to form and dissolve a conductive bridge in a conductive bridge region **114** of the data storage layer **110** between the top and bottom electrodes **112**, **108**. The existence of a conductive bridge in conductive bridge region **114** between the top and bottom electrodes **112**, **108** produces a low resistance state, while the absence of a conductive bridge in conductive bridge region **114** results in a high resistance state. Thus, the memory cell **116** can be switched between the high resistance state and low resistance state by

applying appropriate biases between the top and bottom electrodes **112**, **108** to produce or dissolve a conductive bridge in conductive bridge region **114**.

[0022] In some embodiments, top and bottom electrodes **112**, **108** are made of silver. In these and/or other embodiments, to facilitate this switching, one of the top or bottom electrodes **112**, **108** is electrochemically inert, while the other is electrochemically active to help facilitate switching. For example, in some embodiments, the top electrode **112** can be relatively electrochemically inert and may comprise titanium nitride, tantalum nitride, silver, tantalum, titanium, platinum, nickel, hafnium, zirconium, and/or tungsten, among others; and/or the bottom electrode **108** can be electrochemically active and can be made of silver, copper, aluminum, or tellurium, among others. In other embodiments the compositions of the top and bottom electrodes **112**, **108** can be flipped relative to what is described above, such that the top electrode **112** is electrochemically active and the bottom electrode **108** is inert. In some embodiments, the data storage layer **110** can manifest as a thin film of solid electrolyte, which is a solid material with highly mobile ions. For example, in some embodiments the data storage layer **110** can be made of hafnium oxide (HfO_2), zirconium oxide (ZrO_2), Aluminum oxide (Al_2O_3), amorphous silicon, or silicon nitride (Si_3N_4), among others.

[0023] In some embodiments, such as illustrated in FIG. **2**A which is described further herein, the top electrode **112** comprises a conductive barrier layer overlying an electrochemically inert or active layer. For example, in FIG. **1** the top electrode **112** may comprise a titanium nitride layer (i.e. conductive barrier layer) overlying a silver layer (i.e., electrochemically inert layer), such that the titanium nitride layer provides a stable interface for overlying conductive vias and/or wires (e.g., the conductive via **122**). In some embodiments, if the conductive barrier layer (e.g., titanium nitride layer) is omitted and a conductive via and/or wire is disposed directly on the electrochemically inert or active layer (e.g., silver layer), then migration of the conductive material (e.g., silver) in the electrochemically inert or active layer may occur. This, in part, may cause a short circuit between the top and bottom electrodes **112**, **108** and/or cause a non-ohmic contact between the overlying conductive vias and/or wires (e.g., the conductive via **122**) and the top electrode **112**.

[0024] By overlying the memory cell **116** along the pair of sidewalls **106***s***1**, **106***s***2** of the bottom dielectric layer **106**, a re-deposition of conductive material(s) from the top and/or bottom electrode **112**, **108** to the data storage layer **110** is mitigated during fabrication of the memory cell **116**. By mitigating the re-deposition of conductive material(s) from the top and/or bottom electrodes **112**, **108**, the top and bottom electrodes **112**, **108** are not electrically shorted together by the conductive material(s), and thus the memory cell **116** can change between a high resistance state and a low resistance state.

[0025] Although FIG. **1** describes the memory cell **116** as being a programmable metallization cell (PMC) random access memory (RAM) cell, it will be appreciated that the memory cell **116** is not limited to such a device. Rather, in alternative embodiments, the memory cell **116** may be a phase-change random-access memory (PCRAM) cell, a resistive random-access memory (RRAM) cell, a magnetoresistive random-access memory (MRAM) cell, a spin-transfer torque magnetoresistive random-access memory (STT-MRAM) cell, or the like. In such embodiments, the memory cell **116** can be formed to have a top surface of a top electrode, a top surface of a bottom electrode, and a top surface of a data storage layer respectively aligned with a substantially straight horizontal line such that the top and bottom electrodes are not electrically coupled together (e.g., by re-deposited conductive materials).

[0026] Referring to FIG. **2**A, a cross-sectional view of a memory device **200***a* according to some alternative embodiments of the memory device **100** of FIG. **1** is provided in which a conductive barrier layer **202** overlies the top electrode **112**.

[0027] The memory device **200***a* includes a top dielectric layer **204** overlying the memory cell **116**. The memory cell **116** comprises a conductive barrier layer **202** overlying a top electrode **112**, and a data storage layer **110** disposed between the top electrode **112** and a bottom electrode **108**. In some embodiments, the conductive barrier layer **202** is a part of the top electrode **112**, such that the conductive barrier layer **202** is a topmost layer in the top electrode **112**. The conductive barrier layer **202** is configured to prevent migration of a material (e.g., silver) from the top electrode **112** to the bottom electrode **108** (and/or to overlying metal layers), thereby mitigating electrical shorting between the top and bottom electrodes **112**, **108** and/or preventing a non-ohmic contact with overlying metal layers (e.g., the conductive via **122**). In further embodiments, a top surface of the conductive barrier layer **202**, a top surface of the top electrode **112**, a top surface of the data storage layer **110**, a top surface of the bottom electrode **108**, and a top surface of the bottom dielectric layer **106** are respectively aligned with a horizontal plane **203** (e.g., x-z plane). In further embodiments, the horizontal plane **203** is parallel with a top surface of an underlying semiconductor substrate (not shown). A bottom surface of the conductive via **122** is below the horizontal plane **203**. An upper surface **202***u* of the conductive barrier layer **202** is below the horizontal plane **203**. A lower portion of the top dielectric layer **204** extends below the horizontal plane **203**. In further embodiments, the top surface of the conductive barrier layer **202**, the top surface of the top electrode **112**, the top surface of the data storage layer **110**, the top surface of the bottom electrode **108**, and the top surface of the bottom dielectric layer **106** are respectively in direct contact with a lower surface of the top dielectric layer **204**. In some embodiments, a bottom surface of the bottom electrode **108** is recessed below a top surface of the bottom conductive wire **104** by a distance d_1 that may, for example, be within a range of about 1 to 130 Angstroms. In further embodiments the bottom surface of the bottom electrode **108** is aligned with the top surface of the bottom conductive wire **104**, such that the distance d_1 is 0 Angstroms (not shown).

[0028] In some embodiments, the bottom dielectric layer **106** may be one or more dielectric layers and may, for example, be or comprise silicon nitride, silicon carbide, or the like with a thickness within a range of approximately 300 to 1000 Angstroms. In further embodiments, the bottom electrode **108** may be one or more conductive layers and may, for example, be or comprise silver, copper, aluminum, tellurium, or the like with a thickness within a range of approximately 75 to 300 Angstroms. In yet further embodiments, the data storage layer **110** may be one or more dielectric layers and may, for example, be or comprise hafnium oxide, zirconium oxide, aluminum oxide, tantalum oxide, another metal oxide, or the like with a thickness

within a range of approximately 20 to 100 Angstroms. In some embodiments, the top electrode **112** may be one or more conductive layers and may, for example, be or comprise silver, copper, titanium nitride, tantalum nitride, or the like with a thickness within a range of approximately 100 to 600 Angstroms. In some embodiments, the conductive barrier layer **202** may be, for example, titanium nitride, tantalum nitride, or the like with a thickness within a range of approximately 10 to 200 Angstroms. In some embodiments, the top and bottom electrodes **112**, **108** comprise a same conductive material (e.g., silver) different than a material (e.g., titanium nitride) the conductive barrier layer **202** is comprised of. In some embodiments, the bottom conductive wire **104**, the conductive via **122**, and the upper conductive wire **124** may, for example, be or comprise aluminum, copper, or the like. In yet further embodiments, the top dielectric layer **204** may be one or more dielectric layers and may, for example, be or comprise silicon nitride, silicon carbide, or the like with a thickness within a range of 300 to 1500 Angstroms. In some embodiments, the top dielectric layer **204** is a same material and/or combination of materials as the bottom dielectric layer **106**. In yet further embodiments, the upper ILD structure **120** comprises one or more dielectric layers and may, for example, be or comprise silicon oxide, another oxide, a low-k dielectric, or the like with a thickness within a range of about 1250 to 2800 Angstroms. As used herein, a low-k dielectric is a dielectric material that has a dielectric constant less than 3.9.

[0029] Referring to FIG. **2**B, a cross-sectional view of a memory device **200***b* according to some alternative embodiments of the memory device **100** of FIG. **1** is provided in which a top surface of the top electrode **112** and a top surface of the bottom electrode **108** are recessed below a top surface of the data storage layer **110** by a distance d_2. An upper segment **110***a* of the data storage layer **110** is vertically above the top surfaces of the top and bottom electrodes **112**, **108**. This, in part, increases isolation between the top and bottom electrodes **112**, **108**, and thereby mitigates "leakage" (i.e., a flow of current) between the top and bottom electrodes **112**, **108**. By increasing isolation between the top and bottom electrodes **112**, **108**, an initial "leakage" of the memory cell **116** is reduced, and stability, endurance, and/or a set/reset voltage window of the memory cell **116** may be increased. In some embodiments, the top surface of the top electrode **112** is below the top surface of the bottom electrode **108**, or vice versa (not shown). This, in part, may be due to an over etch of either the top or bottom electrode **112**, **108** during formation of the memory device **200***b* (e.g., during an etch process used to from the recess).

[0030] In some embodiments, the distance d_2 is within a range of 20 to 200 Angstroms. In some embodiments, if the distance d_2 is greater than 20 Angstroms, then isolation between the top and bottom electrodes **112**, **108** is increased, thus mitigating "leakage" between the top and bottom electrodes **112**, **108**. In further embodiments, if the distance d_2 is less than 200 Angstroms, then the top and/or bottom electrode **112**, **108** are sufficiently large enough, such that the memory cell **116** has an enhanced stability, endurance, and/or switching time.

[0031] Referring to FIG. **3**A, a cross-sectional view of a memory device **300***a* according to some alternative embodiments of the memory device **100** of FIG. **1** is provided in which a top surface of the data storage layer **110** is recessed below a top surface of the top electrode **112** and a top surface of the bottom electrode **108** by a distance d_3. This, in part, increases isolation between the top and bottom electrodes **112**, **108**, and thereby mitigates "leakage" between the top and bottom electrodes **112**, **108**. By increasing isolation between the top and bottom electrodes **112**, **108**, an initial "leakage" of the memory cell **116** is reduced, and stability, endurance, and/or a set/reset voltage window of the memory cell **116** may be increased. An upper segment of the top electrode **112** and an upper segment of the bottom electrode **108** are respectively above the top surface of the data storage layer **110**. In some embodiments, the upper segments of the top and bottom electrodes **112**, **108** are laterally separated from one another by the top dielectric layer **204**. In further embodiments, a protrusion of the top dielectric layer **204** extends from the top surface of the top electrode **112** to the top surface of the data storage layer **110** by the distance d_3.

[0032] In some embodiments, the distance d_3 is within a range of 20 to 200 Angstroms. In some embodiments, if the distance d_3 is greater than 20 Angstroms, then isolation between the top and bottom electrodes **112**, **108** is increased, thus mitigating "leakage" between the top and bottom electrodes **112**, **108**. In further embodiments, if the distance d_3 is less than 200 Angstroms, then the top and/or bottom electrode **112**, **108** are sufficiently large enough, such that the memory cell **116** has an enhanced stability, endurance, and/or switching time.

[0033] Referring to FIG. **3**B, a cross-sectional view of a memory device **300***b* according to some alternative embodiments of the memory device **300***a* of FIG. **3**A is provided in which the upper segments of the top and bottom electrodes **112**, **108** are laterally separated from one another by a filling dielectric layer **302**. In some embodiments, the filling dielectric layer **302** may, for example, be or comprise silicon nitride, silicon carbide, or the like. In some embodiments, the filling dielectric layer **302** extends from the top surface of the top electrode **112** to the top surface of the data storage layer **110** by the distance d_3. In yet further embodiments, the filling dielectric layer **302** comprises a material different than the bottom dielectric layer **106** and/or the top dielectric layer **204**. In yet further embodiments, the filling dielectric layer **302** is omitted and a space occupied by the filling dielectric layer **302** is filled with empty space (e.g., air) (not shown).

[0034] Referring to FIG. **4**, a cross-sectional view of some embodiments of an integrated circuit **400**, which includes a first memory cell **116***a* and a second memory cell **116***b* disposed in an interconnect structure **404** of the integrated circuit **400** is provided. The first and second memory cells **116***a*, **116***b* are each as the memory cell **116** of FIG. **1** is illustrated and described.

[0035] The integrated circuit **400** includes a substrate **406**. The substrate **406** may be, for example, a bulk substrate (e.g., a bulk silicon substrate) or a silicon-on-insulator (SOI) substrate. The illustrated embodiment depicts one or more shallow trench isolation (STI) regions **408**, which may include a dielectric filled trench within the substrate **406**. A cut-line is disposed directly above a top surface of the top electrode **112**, a top surface of the data storage layer **110**, and a top surface of the bottom electrode **108** of both memory cells **116***a*, **116***b*.

[0036] Two access transistors **410**, **412** are disposed between the STI regions **408**. The access transistors **410**, **412** include access gate electrodes **414**, **416**, respectively; access gate dielectrics **418**, **420**, respectively; access sidewall spac-

ers **422**; and source/drain regions **424**. The source/drain regions **424** are disposed within the substrate **406** between the access gate electrodes **414**, **416** and the STI regions **408**, and are doped to have a first conductivity type which is opposite a second conductivity type of a channel region under the access gate dielectrics **418**, **420**, respectively. The access gate electrodes **414**, **416** may be, for example, doped polysilicon or a metal, such as aluminum, copper, or combinations thereof. The access gate dielectrics **418**, **420** may be, for example, an oxide, such as silicon dioxide, or a high-k dielectric material. As used herein, a high-k dielectric material is a dielectric material that has a dielectric constant greater than about **3.9**. The access sidewall spacers **422** can be made of silicon nitride (e.g., Si_3N_4), for example. In some embodiments, the access transistor **410** and/or the access transistor **412** may, for example, be electrically coupled to a word line (WL) such that an appropriate WL voltage can be applied to the access gate electrode **414** and/or the access gate electrode **416**.

[0037] The interconnect structure **404** is arranged over the substrate **406** and electrically couples devices (e.g., access transistors **410**, **412**) to one another. The interconnect structure **404** includes a plurality of inter-metal dielectric (IMD) layers **426**, **428**, **430**, and a plurality of metallization layers **432**, **434**, **436** which are layered over one another in an alternating fashion. The IMD layers **426**, **428**, **430** may be made, for example of a low-k dielectric layer, or an oxide, such as silicon dioxide. The metallization layers **432**, **434**, **436** include metal lines **438**, **440**, **442**, which are formed within trenches, and which may be made of a metal such as copper or aluminum. Contacts **444** extend from the bottom metallization layer **432** to the source/drain regions **424** and/or access gate electrodes **414**, **416**; and vias **446** extend between the metallization layers **432**, **434**, **436**. The vias **446** extend through dielectric-protection layer **450** (which can be made of a dielectric material and can act as an etch stop layer during manufacturing). The dielectric-protection layer **450** made be made of an extreme low-k dielectric material, for example. The contacts **444** and the vias **446** made be made of a metal, such as copper or tungsten, for example. In some embodiments, a metal line in the metal lines **438** may, for example, be electrically coupled to a source line (SL) such that an output of the access transistors **410**, **412** may be accessed at the SL.

[0038] The first and second memory cells **116***a*, **116***b*, which are configured to store respective data states, are arranged within the interconnect structure **404** between neighboring metal layers. The first and second memory cells **116***a*, **116***b* respectively include the bottom electrode **108**, the data storage layer **110**, and the top electrode **112**. The first and second memory cells **116***a*, **116***b* are respectively electrically coupled to a first bit-line BL_1 and a second bit-line BL_2 through the metal line **442**. In some embodiments, a conductive via is disposed between the bottom conductive wire **104** and the metal line **440** (not shown). In yet further embodiments, a top electrode via is respectively disposed between the first and second memory cells **116***a*, **116***b* and the conductive via **122** (not shown).

[0039] Referring to FIG. **5**, a top view of some embodiments of the integrated circuit **400** of FIG. **4** is provided.

[0040] As illustrated in FIG. **5**, the first and second memory cells **116***a*, **116***b* have a circular/elliptical shape. In some embodiments, when viewed from a top view, the first and second memory cells **116***a*, **116***b* may have a square and/or rectangular shape. In other embodiments, however, for example due to partialities of many etch processes, the corners of a square or rectangular shape can become rounded, resulting in the first and second memory cells **116***a*, **116***b* respectively having a square or rectangular shape with rounded corners, or having a circular or elliptical shape. The first and second memory cells **116***a*, **116***b* are arranged over metal lines (**440** of FIG. **4**), respectively, and have upper portions in direct electrical connection with the conductive via **122**. In some embodiments, an upper portion of the top electrode **112** is directly electrically coupled to a top electrode via disposed between the top electrode **112** and the metal line **442** (not shown).

[0041] FIGS. **6-11** illustrate cross-sectional views **600-1100** of some embodiments of a method of forming a memory device including a programmable metallization cell according to the present disclosure. Although the cross-sectional views **600-1100** shown in FIGS. **6-11** are described with reference to a method, it will be appreciated that the structures shown in FIGS. **6-11** are not limited to the method but rather may stand alone separate of the method. Although FIGS. **6-11** are described as a series of acts, it will be appreciated that these acts are not limiting in that the order of the acts can be altered in other embodiments, and the methods disclosed are also applicable to other structures. In other embodiments, some acts that are illustrated and/or described may be omitted in whole or in part.

[0042] As shown in cross-sectional view **600** of FIG. **6**, a bottom conductive wire **104** is formed within an inter-level dielectric (ILD) layer **102**. A dielectric film **602** is formed over the bottom conductive wire **104**. In some embodiments, the dielectric film **602** is comprised of one or more dielectric layers and may, for example, be or comprise silicon nitride, silicon carbide, or the like formed to a thickness within a range of about 300 to 1000 Angstroms. A masking layer **604** is formed over the dielectric film **602**, such that the masking layer **604** covers outer regions **606***a*, **606***c* of the dielectric film **602** and leaves a center region **606***b* of the dielectric film **602** uncovered and exposed. In some embodiments, the masking layer **604** includes a photoresist mask. In other embodiments, the masking layer **604** comprises a hardmask layer (e.g., comprising a nitride layer). In yet further embodiments, the masking layer **604** may comprise a multi-layer hard mask. In some embodiments, the bottom conductive wire **104** may, for example, be or comprise aluminum, copper, or the like.

[0043] As shown in cross-sectional view **700** of FIG. **7**, an etching process is performed to etch the dielectric film (**602** of FIG. **6**) and form an opening **702** in the dielectric film (**602** of FIG. **6**), thereby defining a bottom dielectric layer **106**. The etching process involves exposing the dielectric film (**602** of FIG. **6**) within the center region (**606***b* of FIG. **6**) to one or more etchants, and subsequently performing a removal process to remove the masking layer (**604** of FIG. **6**) (not shown). In some embodiments, the etching process may comprise one or more etchants such as difluoromethane (e.g., CH_2F_2, CHF_3), perfluorocyclobutane (C_4F_8), hydrofluoric acid, and/or nitric acid. In further embodiments, the etching process may comprise a dry etch process utilizing first etchants (e.g., difluoromethane (e.g., CH_2F_2, CHF_3), and/or perfluorocyclobutane (C_4F_8)), subsequently followed by a blanket etch back process utilizing second etchants different than the first etchants. In some embodiments, the etching process etches the bottom conductive wire **104**, such

that an upper surface of the bottom conductive wire **104** is below a bottom surface of the bottom dielectric layer **106** by a distance within a range of approximately 1 to 130 Angstroms (not shown).

[0044] In some embodiments, by virtue of the etching process, the bottom dielectric layer **106** has a pair of opposing sidewalls **106***s***1**, **106***s***2** that respectively comprise a slanted sidewall segment **106***ss* overlying a curved sidewall segment **106***cs*. For example, the dry etch process may form the slanted sidewall segment **106***ss* and the blanket etch back process may form the curved sidewall segment **106***cs*. In some embodiments, the curved sidewall segment **106***cs* is defined from a first point **704** (in which an edge of the bottom dielectric layer **106** directly contacts the bottom conductive wire **104**) to a second point **706** (in which the second point **706** is below a midpoint of the bottom dielectric layer **106** and above the first point **704** by a non-zero distance). In further embodiments, a slope of a curved surface of the bottom dielectric layer **106** continuously increases while moving along incremental segments of the curved surface from the first point **704** to the second point **706**. An angle a defined between the curved surface and the bottom conductive wire **104** may be within a range of about 1 to 60 degrees. In further embodiments, the slanted sidewall segment **106***ss* is defined from the second point **706** to a third point **708** (defined at an edge of the top surface of the bottom dielectric layer **106**). In some embodiments, the slanted sidewall segment **106***ss* is substantially straight and has an angle Φ from the top surface of the bottom conductive wire **104** to the sidewall **106***s***2** of the bottom dielectric layer **106**. The angle Φ may, for example, be within a range of about 30 to 75 degrees. In further embodiments, a sidewall **106***s***1** has a slanted sidewall segment **106***ss* overlying a curved sidewall segment **106***cs* configured as described above.

[0045] As shown in cross-sectional view **800** of FIG. **8**, a bottom electrode layer **802** is formed over the bottom dielectric layer **106**. A data storage film **804** is formed over the bottom electrode layer **802**. A top electrode layer **806** is formed over the data storage film **804**. A conductive barrier film **808** is formed over the top electrode layer **806**. A top dielectric film **812** is formed over the conductive barrier film **808**. A buffer layer **814** is formed over the top dielectric film **812**. In some embodiments, the conductive barrier film **808** is a part of the top electrode layer **806** (such that the top electrode layer **806** comprises a top layer directly overlying a bottom layer). A substantially straight horizontal line **820** is aligned with the top surface of the bottom dielectric layer **106**.

[0046] In some embodiments, the bottom electrode layer **802** may, for example, be or comprise silver, copper, or the like formed to a thickness within a range of approximately 75 to 300 Angstroms. In some embodiments, the data storage film **804** may, for example, be or comprise metal oxide such as hafnium oxide, aluminum oxide, tantalum oxide, or the like formed to a thickness within a range of approximately 20 to 100 Angstroms. In some embodiments, the top electrode layer **806** may, for example, be or comprise silver, titanium nitride, copper, or the like formed to a thickness within a range of approximately 100 to 600 Angstroms. In some embodiments, the conductive barrier film **808** may, for example, be or comprise titanium nitride, a nitride, tantalum nitride, or the like formed to a thickness within a range of approximately 25 to 250 Angstroms. In some embodiments, the top dielectric film **812** may, for example, be or comprise silicon nitride, silicon carbide, or the like formed to a thickness within a range of approximately 300 to 1500 Angstroms. In yet further embodiments, the top dielectric film **812** may comprise a same material as the bottom dielectric layer **106**. In some embodiments, the buffer layer **814** may, for example, be or comprise an oxide such as silicon oxide formed to a thickness within a range of approximately 1000 to 3000 Angstroms.

[0047] As shown in cross-sectional view **900** of FIG. **9**, a planarization process is performed until the top surface of the bottom dielectric layer **106** is reached, thereby defining a memory cell **116**. The planarization process removes the buffer layer **814** and removes portions of the bottom electrode layer **802**, the data storage film **804**, the top electrode layer **806**, the conductive barrier film **808**, and the top dielectric film **812**, thereby defining a bottom electrode **108**, an data storage **110**, a top electrode **112**, a conductive barrier layer **202**, and a dielectric segment **902**, respectively. The memory cell **116** includes the bottom electrode **108**, the data storage layer **110**, the top electrode **112** and the conductive barrier layer **202**. In some embodiments, the planarization process comprises performing a chemical-mechanical planarization (CMP) process along the substantially straight horizontal line **820**. In some embodiments, the planarization process comprises one or more slurry for a non-selective CMP. Thus, in some embodiments, the memory cell **116** is formed by, for example, a single CMP process, such that the top and bottom electrode **112**, **108** are electrically isolated from one another. Further, in some embodiments after performing the planarization process a cleaning process (e.g., a wet cleaning process utilizing hydrofluoric acid) is performed. In further embodiments, the cleaning process may remove conductive materials extending over the top and bottom electrodes **112**, **108** and the data storage layer **110**, thereby increasing isolation between the top and bottom electrodes **112**, **108**. In yet further embodiments, the top electrode **112**, the data storage layer **110**, the bottom electrode **108** respectively having a U-shaped profile mitigates peeling between the aforementioned layers, thereby increasing a stability and/or endurance of the memory cell **116**.

[0048] In some embodiments, after performing the planarization process and/or the cleaning process, a pullback etch process is performed. In some embodiments, the pullback etch process utilizes a dry etch (e.g., comprising methane (CH_4) and/or hydrogen (H_2) etchant(s)) configured to remove a portion of the top electrode **112**, conductive barrier layer **202**, and/or the bottom electrode **108** (e.g., please refer to FIG. **2**B). In further embodiments, the pullback etch process utilizes a dry etch (e.g., comprising a carbon tetrafluoride (CF_4) etchant) configured to remove a portion of the data storage layer **110** (e.g., please refer to FIG. **3**A). In yet further embodiments, the pullback etch process utilizes a wet etch (e.g., comprising a hydrochloric acid etchant) configured to remove a portion of the top electrode **112**, conductive barrier layer **202**, and/or the bottom electrode **108** (e.g., please refer to FIG. **2**B). In other embodiments, the pullback etch process utilizes a wet etch (e.g., comprising a dihydrofolic acid etchant) configured to remove a portion of the data storage layer **110** (e.g., please refer to FIG. **3**A).

[0049] As shown in cross-sectional view **1000** of FIG. **10**, a top dielectric film **1002** is formed over the memory cell **116**. In some embodiments, the top dielectric film **1002** may

comprise a same material as the dielectric segment **902** and/or the bottom dielectric layer **106**. In further embodiments, the top dielectric film **1002** may, for example, be or comprise an extreme low-k dielectric material, an oxide such as silicon oxide, or the like formed to a thickness within a range of approximately 300 to 1500 Angstroms.

[0050] As shown in cross-sectional view **1100** of FIG. **11**, an upper inter-level dielectric (ILD) structure **120** is formed over the top dielectric film **1002**. In some embodiments, the upper ILD structure **120** may comprise one or more dielectric materials and/or one or more dielectric layers. In further embodiments, the upper ILD structure **120** may, for example, be or comprise an extreme low-k dielectric material, an oxide such as silicon oxide, or the like formed to a thickness within a range of approximately 1250 to 2800 Angstroms. A conductive via **122** is formed over the memory cell **116**, such that the conductive via **122** electrically couples the conductive barrier layer **202** to overlying conductive wires. An upper conductive wire **124** is formed over the conductive via **122**.

[0051] In some embodiments, the conductive via **122** is formed by a single damascene process, and subsequently the upper conductive wire **124** is formed by the single damascene process. In further embodiments, the single damascene process comprises depositing a dielectric layer, patterning the dielectric layer with openings for a single layer of conductive features (e.g., a layer of contacts, vias, or wires), and filling the openings with conductive materials to form the single layer of conductive features. In some embodiments, the conductive via **122** and the upper conductive wire **124** may, for example, be or comprise copper, aluminum, or the like. In yet further embodiments, the conductive via **122**, the upper conductive wire **124**, the top dielectric film **1002**, and the upper ILD structure **120** are a part of an interconnect structure.

[0052] FIG. **12** illustrates a method **1200** of forming a memory device in accordance with some embodiments. Although the method **1200** is illustrated and/or described as a series of acts or events, it will be appreciated that the method is not limited to the illustrated ordering or acts. Thus, in some embodiments, the acts may be carried out in different orders than illustrated, and/or may be carried out concurrently. Further, in some embodiments, the illustrated acts or events may be subdivided into multiple acts or events, which may be carried out at separate times or concurrently with other acts or sub-acts. In some embodiments, some illustrated acts or events may be omitted, and other un-illustrated acts or events may be included.

[0053] At act **1202**, a bottom dielectric layer is formed over a conductive wire. FIG. **6** illustrates a cross-sectional view **600** corresponding to some embodiments of act **1202**.

[0054] At act **1204**, a removal process is performed on the bottom dielectric layer to define an opening in the bottom dielectric layer. FIG. **7** illustrates a cross-sectional view **700** corresponding to some embodiments of act **1204**.

[0055] At act **1206**, a stack of memory layers is formed over the conductive wire and within the opening. The stack of memory layers comprises a top electrode overlying a bottom electrode. FIG. **8** illustrates a cross-sectional view **800** corresponding to some embodiments of act **1206**.

[0056] At act **1208**, a planarization process is performed on the stack of memory layers such that a top surface of the top electrode is aligned with a top surface of the bottom electrode, thereby defining a memory cell. FIG. **9** illustrates a cross-sectional view **900** corresponding to some embodiments of act **1208**.

[0057] At act **1210**, an interconnect structure is formed over the memory cell. FIGS. **10** and **11** illustrates cross-sectional views **1000** and **1100** that correspond to some embodiments of act **1210**.

[0058] Accordingly, in some embodiments, the present disclosure relates to a method of forming a memory cell comprising a top electrode overlying a bottom electrode with a planarization process (e.g., a single CMP process), such that a top surface of the top electrode is aligned with a top surface of the bottom electrode.

[0059] In some embodiments, the present disclosure relates to a memory device including a bottom electrode; a data storage layer overlying the bottom electrode, wherein the bottom electrode cups an underside of the data storage layer; and a top electrode overlying the data storage layer, wherein a top surface of the bottom electrode is aligned with a top surface of the top electrode.

[0060] In other embodiments, the present disclosure relates to a programmable metallization cell including a bottom dielectric layer overlying a conductive wire; a bottom electrode disposed within the bottom dielectric layer, wherein the bottom electrode is U-shaped and contacts the conductive wire; a data storage layer overlying the bottom electrode, wherein the data storage layer is U-shaped, such that an upper surface of the bottom electrode continuously extends along a lower surface of the data storage layer; and a top electrode overlying the data storage layer.

[0061] In further embodiments, the present disclosure relates to a method for manufacturing a memory device. The method including forming a bottom dielectric layer over a conductive wire; patterning the bottom dielectric layer to form an opening above the conductive wire, wherein the opening has a curved sidewall such that a width of the opening continuously increases from a bottom surface of the bottom dielectric layer to a top surface of the bottom dielectric layer; forming a stack of memory layers over the conductive wire and within the opening, wherein the stack of memory layers comprise a top electrode overlying a bottom electrode; and performing a planarization process on the stack of memory layers, such that a top surface of the top electrode is aligned with a top surface of the bottom electrode.

[0062] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

1. A memory device, comprising:

a bottom electrode including a central bottom electrode region and a peripheral bottom electrode region that extends upwardly from the central bottom electrode region;

a data storage layer overlying the bottom electrode, wherein an upper surface of the bottom electrode cups an underside of the data storage layer; and

a top electrode overlying the data storage layer, wherein an upper surface of the data storage layer cups an underside of the top electrode and the data storage layer separates the top electrode from the bottom electrode, and-wherein a top surface of the bottom electrode is level with a top surface of the top electrode, and wherein a sidewall of the top electrode comprises a slanted segment at a height above a curved segment.

2. The memory device of claim **1**, wherein a width of the top electrode continuously increases from a bottom surface of the top electrode to the top surface of the top electrode.

3. The memory device of claim **1**, wherein the data storage layer comprises a conductive bridge region over the central bottom electrode region, and wherein the conductive bridge region includes a conductive bridge coupling the bottom electrode to the top electrode for a first data state.

4. The memory device of claim **1**, wherein the bottom electrode continuously extends along and directly contacts a sidewall of the data storage layer and a bottom surface of the data storage layer.

5. (canceled)

6. (canceled)

7. The memory device of claim **1**, wherein the top electrode comprises an upper layer overlying a bottom layer, such that the upper layer comprises a first material and the bottom layer comprises a second material that is different from the first material, and wherein the bottom electrode comprises the second material.

8. The memory device of claim **7**, wherein the first material is titanium nitride and the second material is silver.

9. The memory device of claim **1**, further comprising:

a dielectric segment disposed over the top electrode, wherein the top electrode cups an underside of the dielectric segment and has a top surface aligned with a top surface of the dielectric segment.

10. A programmable metallization cell, comprising:

a bottom dielectric layer overlying a conductive wire;

a bottom electrode disposed within the bottom dielectric layer, wherein the bottom electrode is U-shaped and contacts the conductive wire;

a data storage layer overlying the bottom electrode, wherein the data storage layer is U-shaped, such that an upper surface of the bottom electrode continuously extends along a lower surface of the data storage layer; and

a top electrode overlying the data storage layer, wherein the top electrode is U-shaped and an upper surface of the data storage layer continuously extends along a lower surface of the top electrode.

11. (canceled)

12. The programmable metallization cell of claim **10**, wherein the bottom dielectric layer has a sidewall that has a slanted segment at a height above a curved segment, such that a sidewall of the bottom electrode directly contacts the slanted segment and the curved segment.

13. The programmable metallization cell of claim **10**, wherein a dielectric segment overlies the top electrode, such that the top electrode continuously extends along a lower surface of the dielectric segment, and wherein a top surface of the dielectric segment is aligned with a top surface of the top electrode.

14. The programmable metallization cell of claim **13**, wherein the dielectric segment comprises a dielectric material different than the bottom dielectric layer.

15. The programmable metallization cell of claim **10**, wherein the top electrode comprises a titanium nitride layer directly overlying a silver layer.

16. The programmable metallization cell of claim **10**, wherein a bottommost surface of the bottom electrode is recessed below a topmost surface of the conductive wire.

17-20. (canceled)

21. A programmable metallization cell, comprising:

a bottom dielectric layer overlying a conductive wire, wherein the bottom dielectric layer comprises sidewalls defining a trench over the conductive wire;

a bottom electrode overlying the conductive wire, wherein the bottom electrode is disposed within the trench and contacts the sidewalls of the bottom dielectric layer, wherein the bottom electrode is U-shaped;

a data storage layer overlying the bottom electrode and disposed within the trench, wherein the data storage layer is U-shaped;

a top electrode overlying the data storage layer and disposed within the trench, wherein the top electrode is U-shaped and extends continuously along an upper surface of the data storage layer, wherein a top surface of the top electrode is aligned with a top surface of the bottom electrode; and

a conductive barrier layer overlying the top electrode and disposed within the trench, wherein the conductive barrier layer is U-shaped, wherein a top surface of the conductive barrier layer is aligned with the top surface of the top electrode.

22. The programmable metallization cell of claim **21**, wherein the top electrode comprises a first material and the conductive barrier layer comprises a second material different from the first material.

23. The programmable metallization cell of claim **21**, further comprising:

a conductive via overlying the conductive barrier layer, wherein a bottom surface of the conductive via extends below the top surface of the top electrode to contact an upper surface of the conductive barrier layer.

24. The programmable metallization cell of claim **21**, wherein the top surface of the top electrode is aligned with a top surface of the bottom dielectric layer.

25. The programmable metallization cell of claim **21**, wherein a bottom surface of the bottom electrode is disposed vertically below a bottom surface of the bottom dielectric layer.

26. The programmable metallization cell of claim **21**, wherein the bottom electrode, the data storage layer, the top electrode, and the conductive barrier layer respectively comprise a sidewall having a slanted sidewall segment at a height above a curved sidewall segment.

27. The memory device of claim **1**, further comprising:

a conductive via overlying the top electrode, wherein a bottom surface of the conductive via is vertically below the top surface of the bottom electrode.

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