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(54) **SEMICONDUCTOR DEVICES INCLUDING CONDUCTIVE STRUCTURES**

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(57) **ABSTRACT**

Semiconductor devices and fabrication methods thereof. For example, a semiconductor device may include a dielectric structure, and first conductive structures and second conductive structures. The dielectric structure may include a first dielectric layer that surrounds the first conductive structures and a second dielectric layer that surrounds the second conductive structures. The first dielectric layer may include a first intervention between the first conductive structures. The second dielectric layer may include a second intervention between the second conductive structures. A width in a first direction of the first intervention may decrease in a second direction from a top surface toward a bottom surface of the first intervention. A width in the first direction of the second intervention may increase in the second direction from a top surface toward a bottom surface of the second intervention. The first dielectric layer and the second dielectric layer may include different dielectric materials.

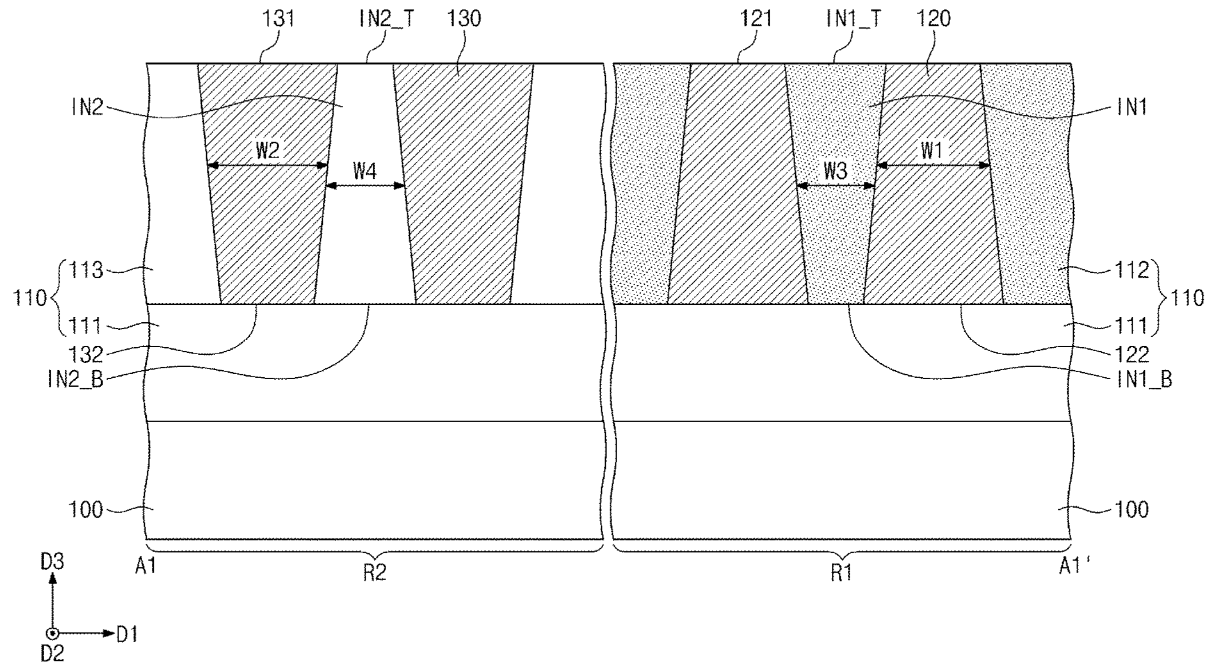


FIG. 1A

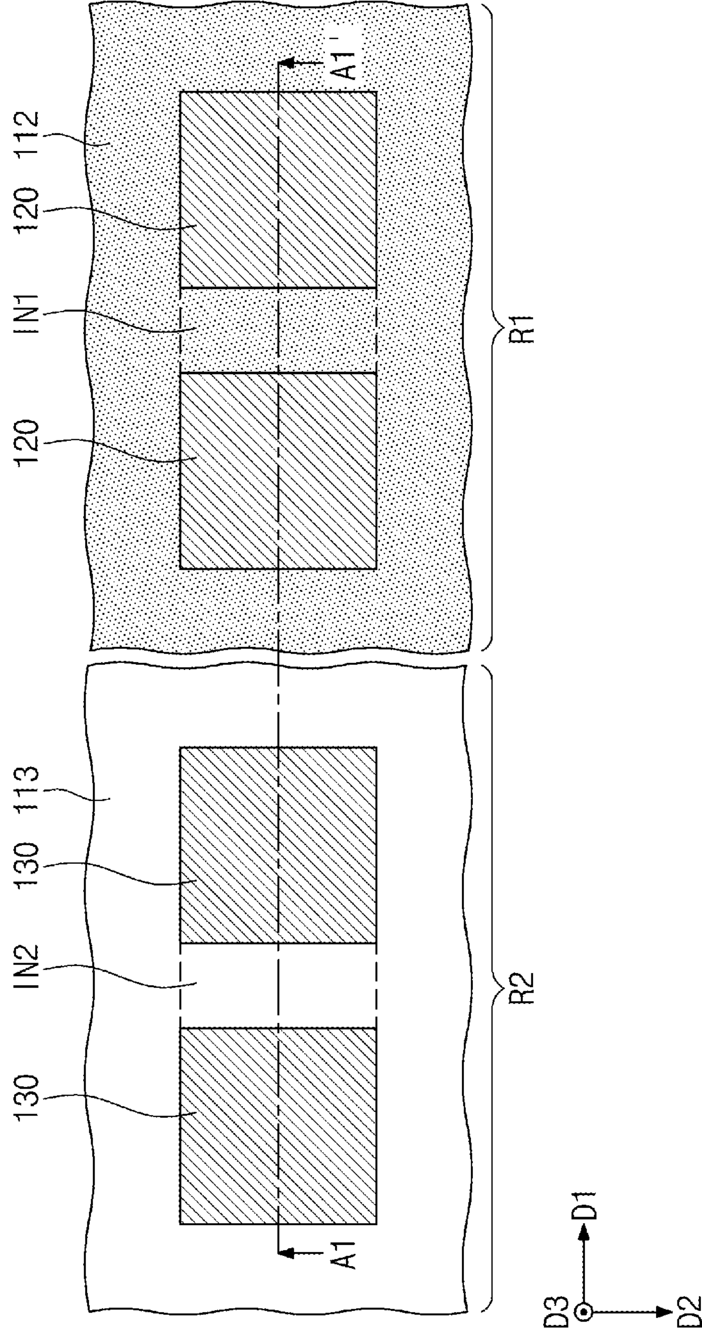


FIG. 1B

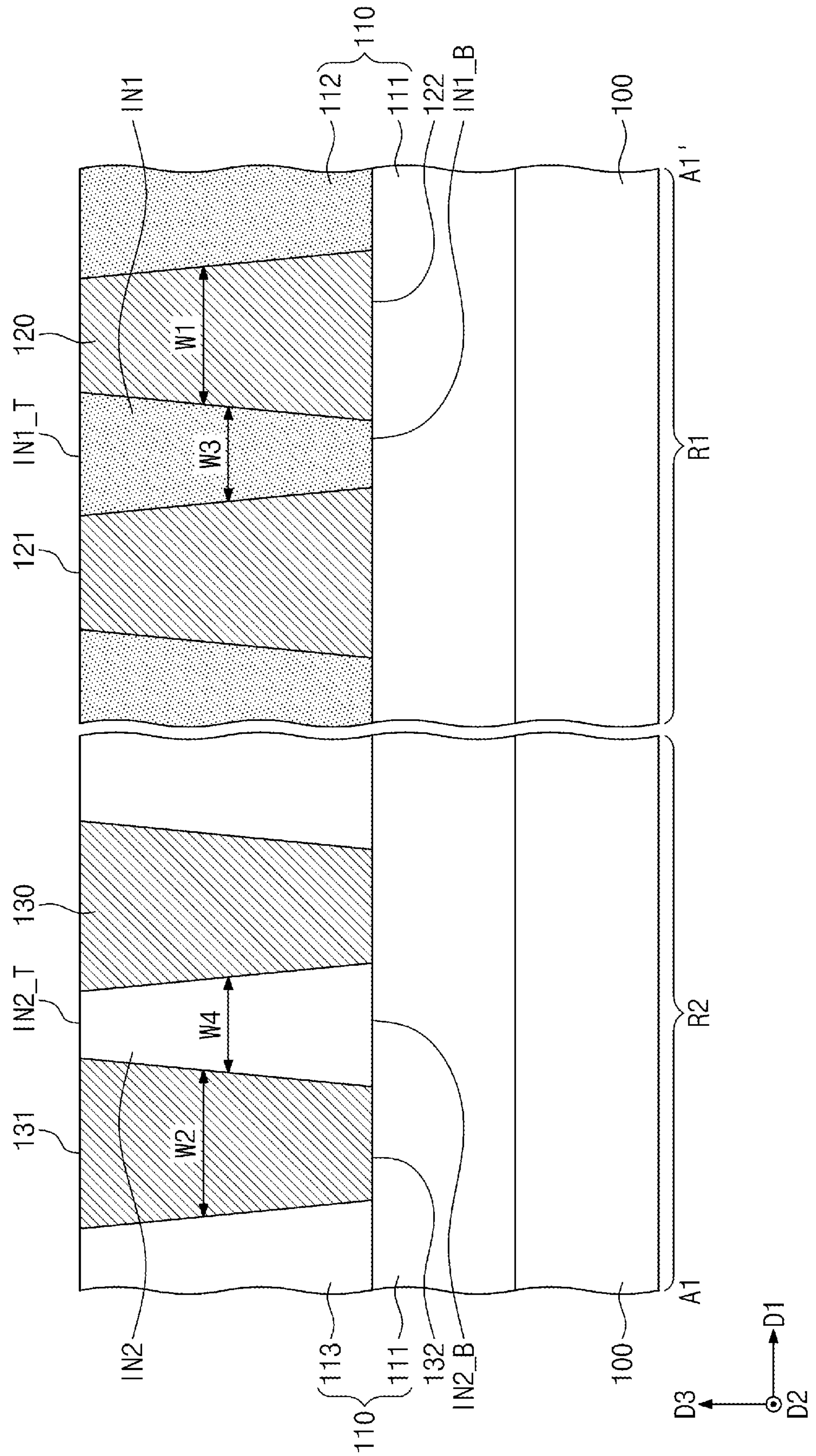
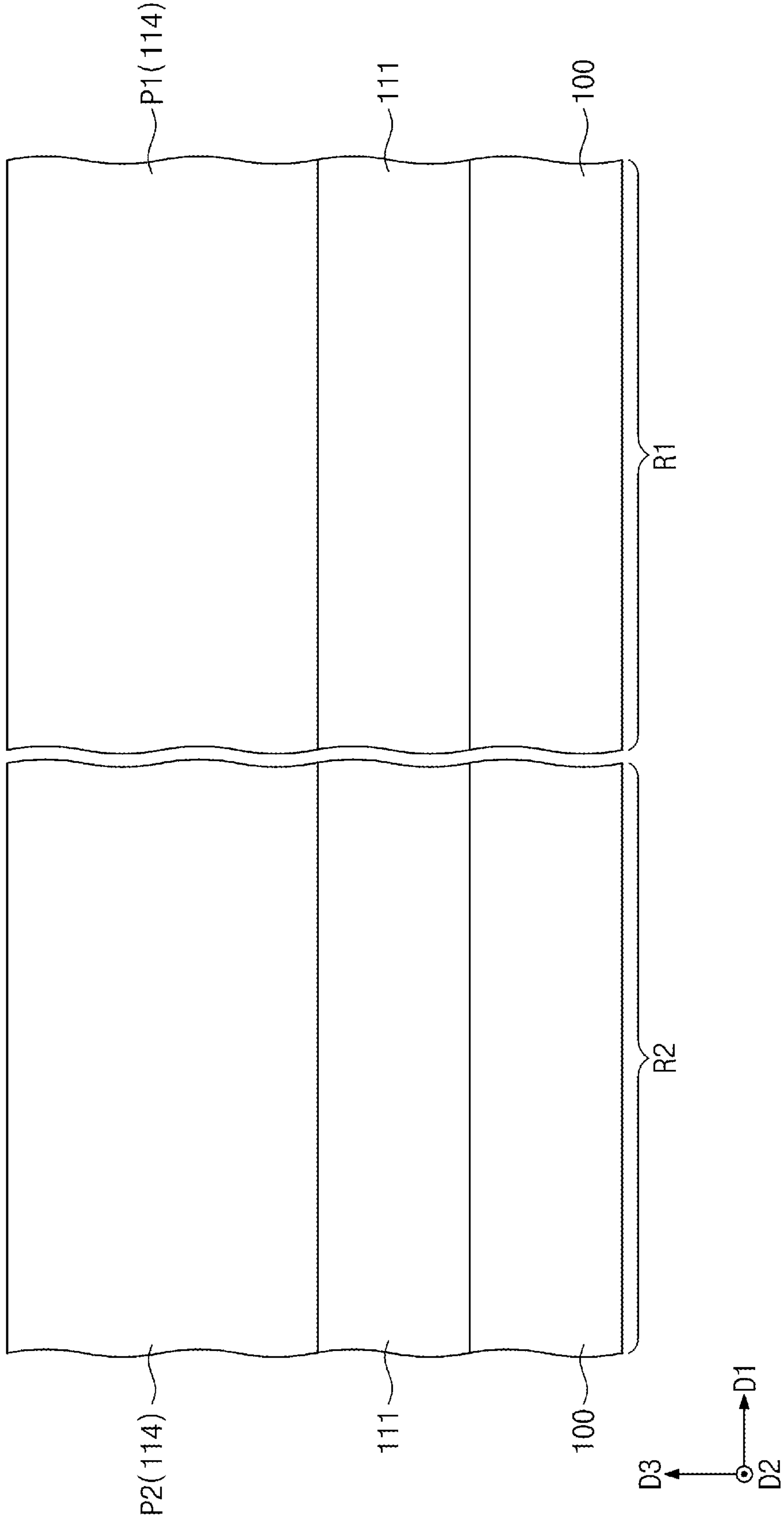


FIG. 2A



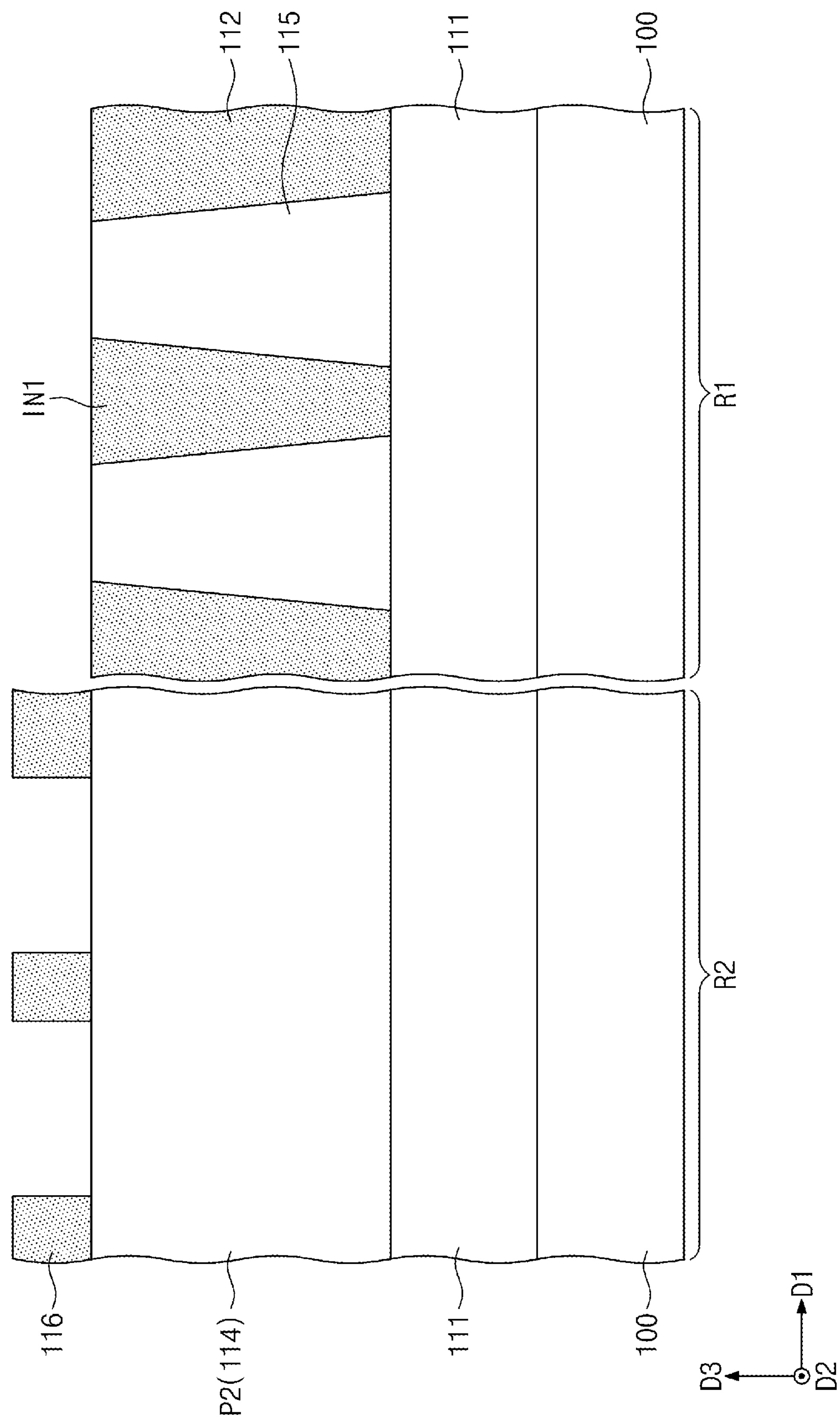


FIG. 2B
112
115
111
100
IN1
R1
R2
116
P2(114)
111
100
D1
D2
D3

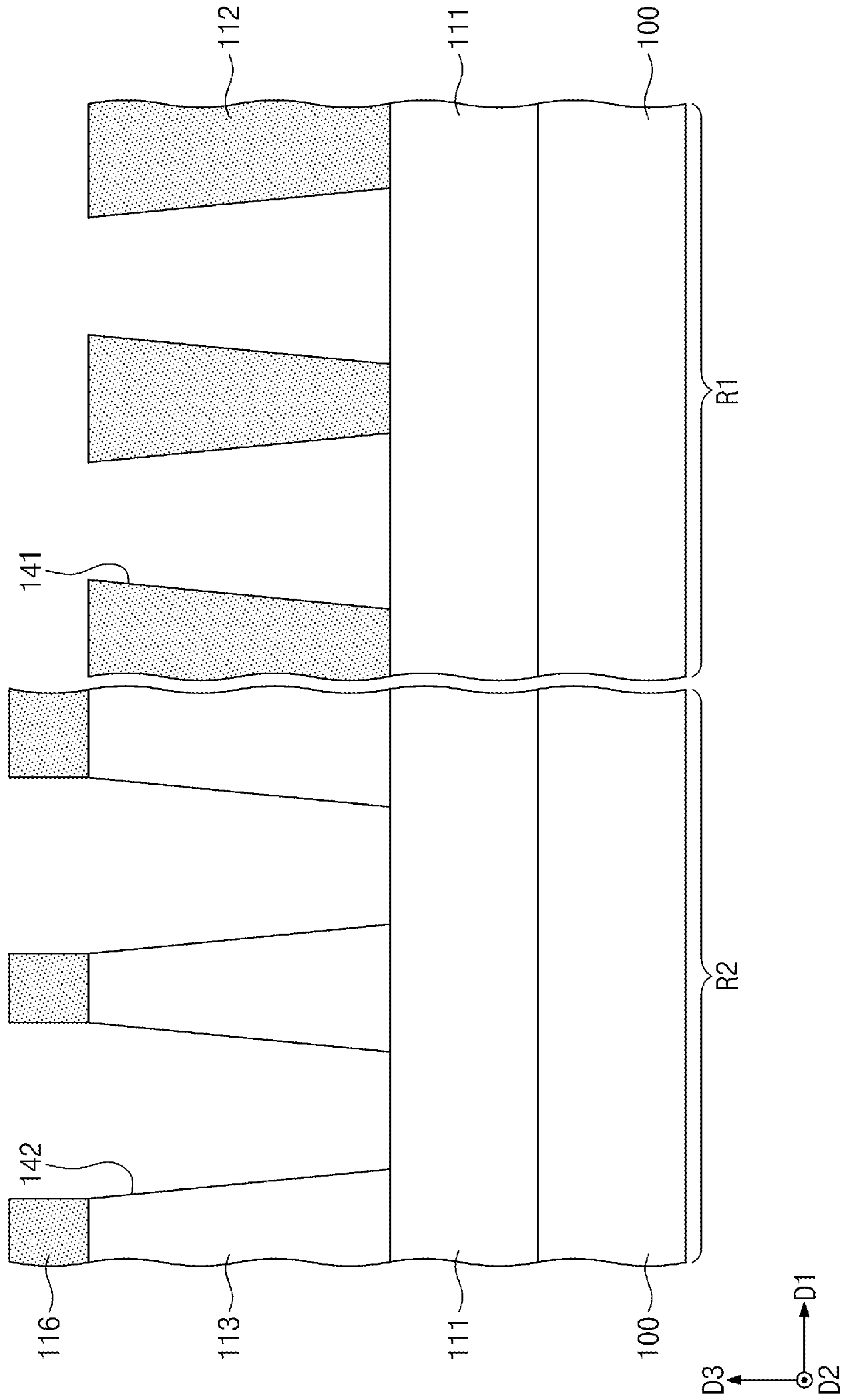


FIG. 2C
112
111
100
141
R1
R2
142
116
113
111
100
D1
D2
D3

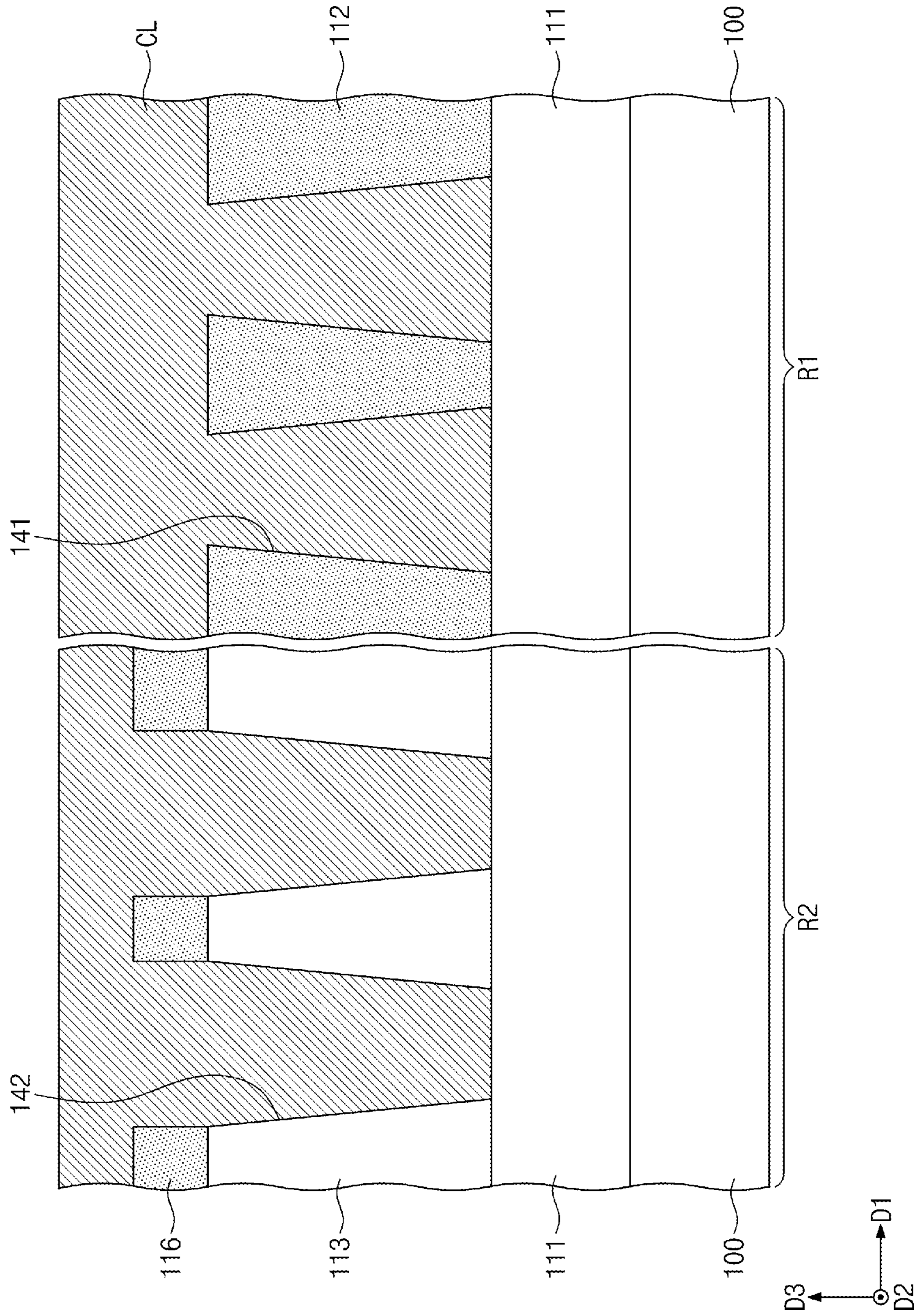


FIG. 2D

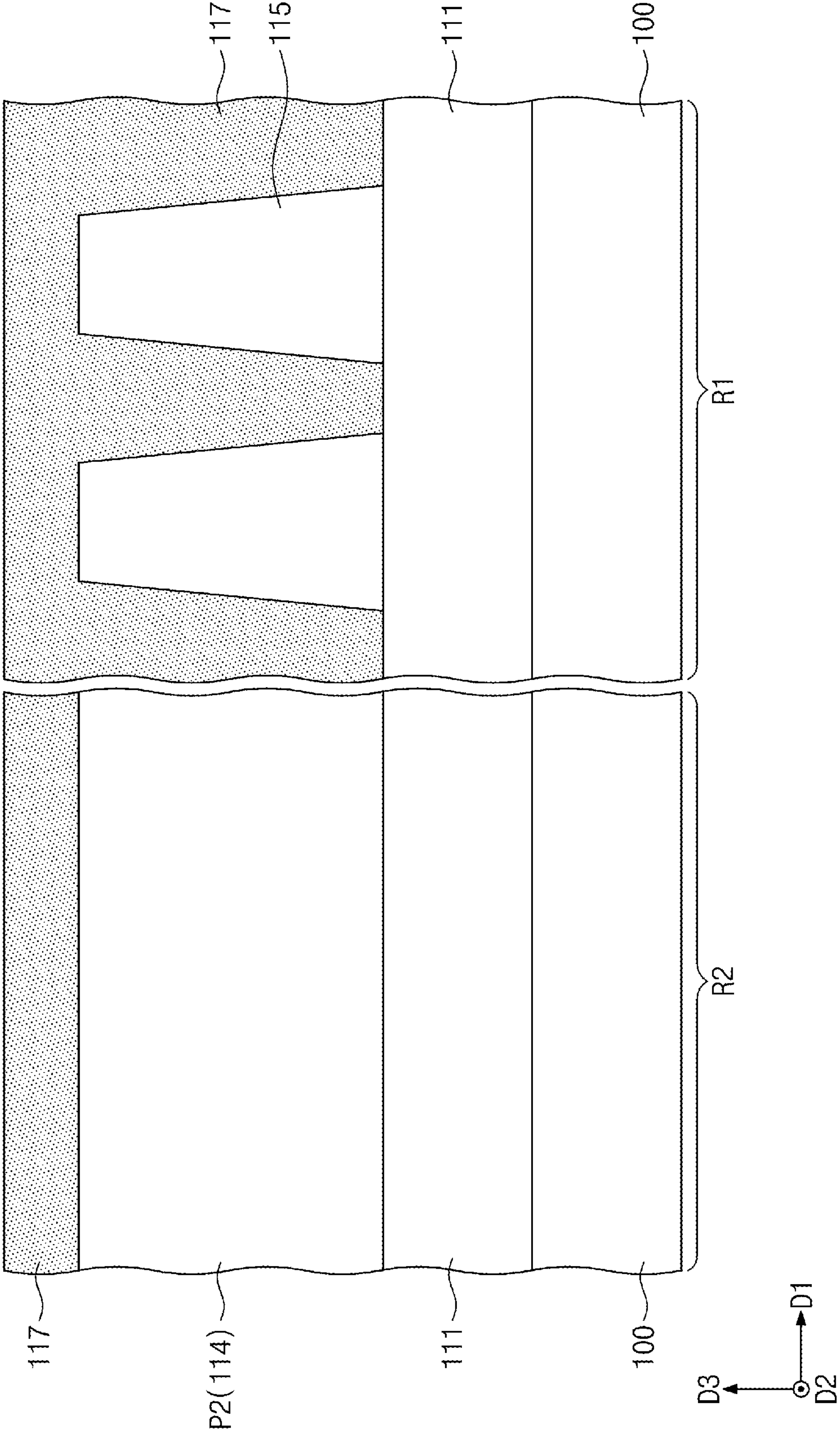
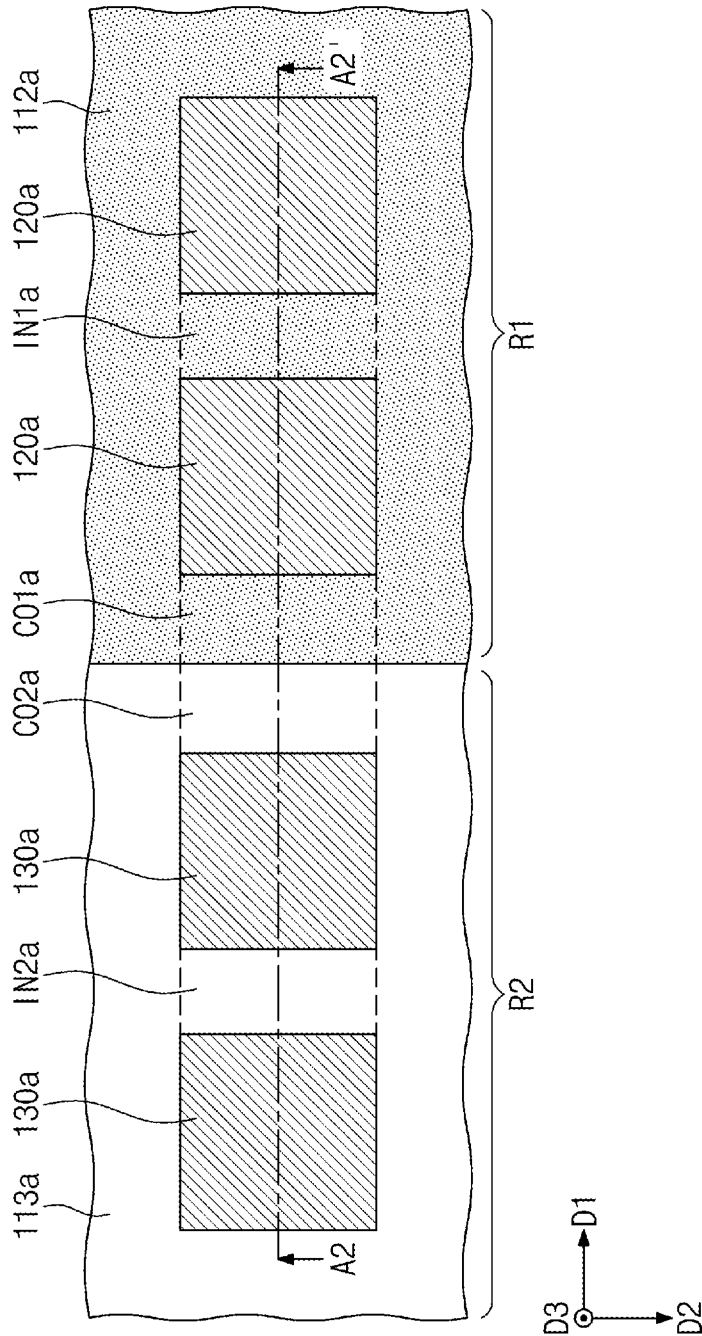


FIG. 3

FIG. 4A



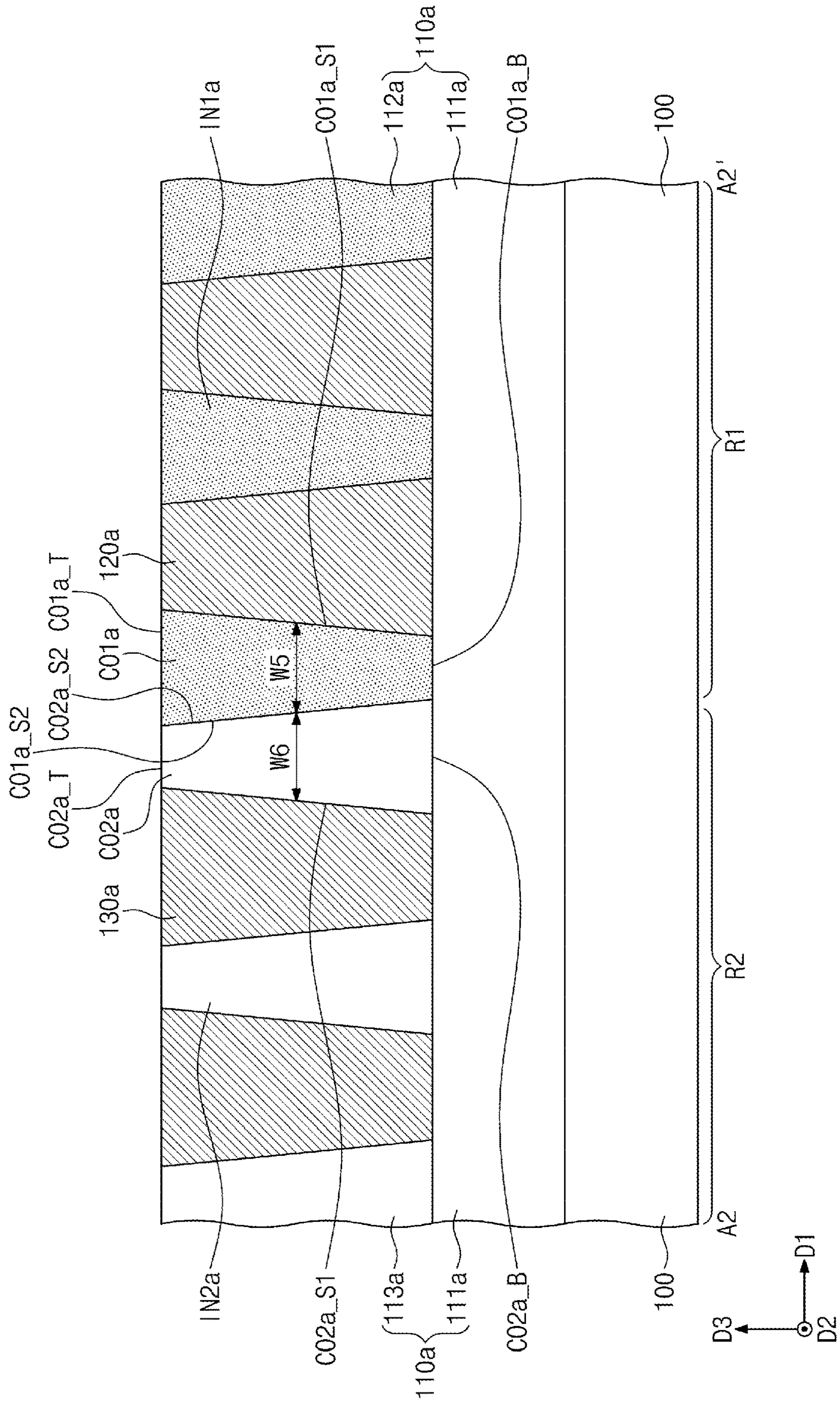


FIG. 4B
IN1a
C01a_S1
112a
111a
110a
C01a_B
100
A2'
R1
120a
C01a_T
C01a
C02a_S2
W5
C01a_S2
W6
C02a_T
C02a
130a
R2
A2
IN2a
C02a_S1
113a
111a
110a
C02a_B
100
D1
D2
D3

FIG. 5

FIG. 6A

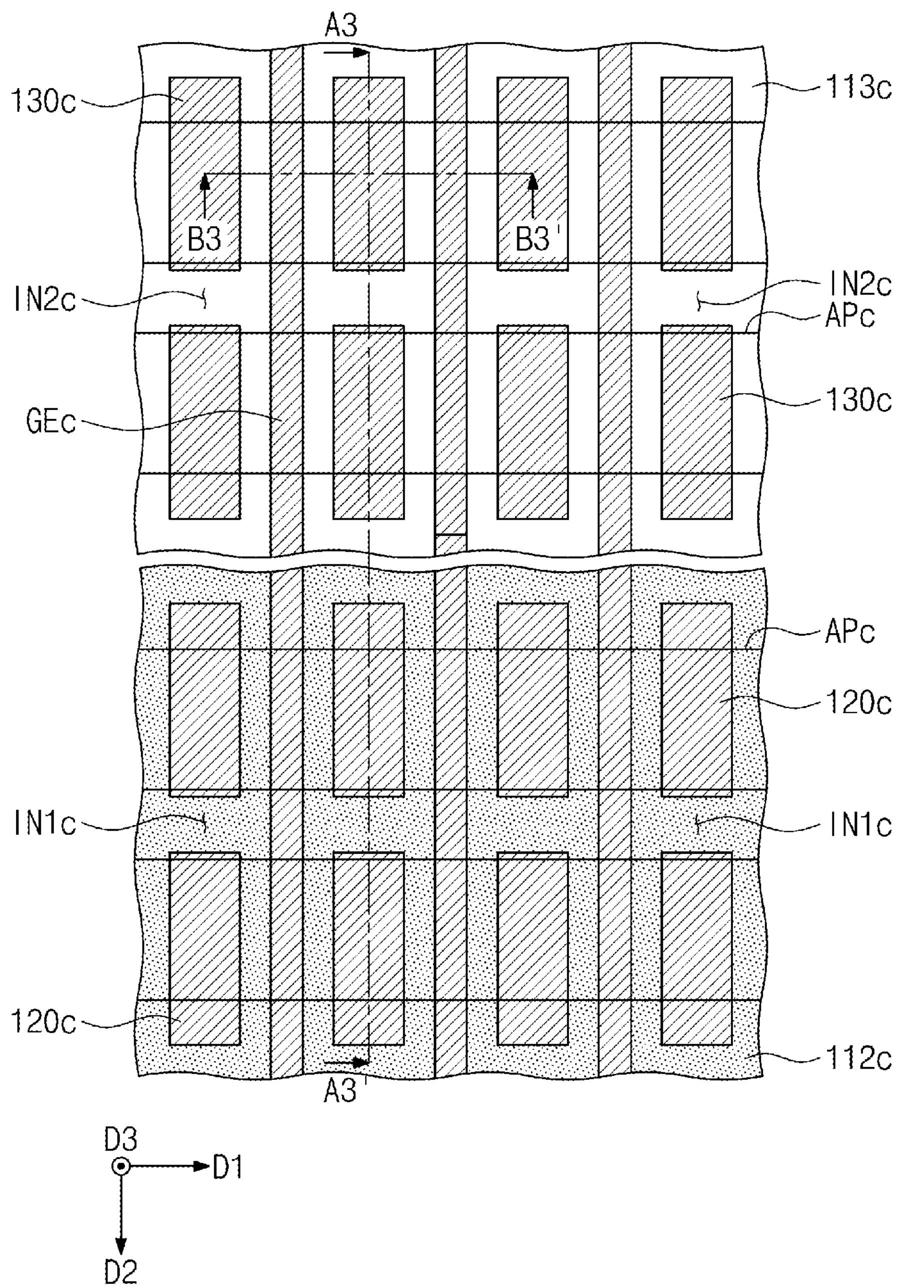
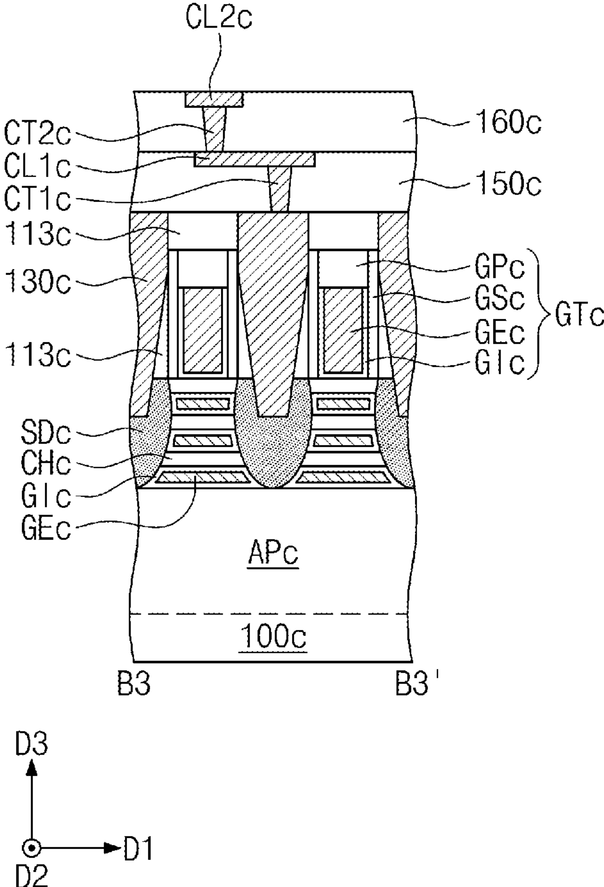


FIG. 6B

FIG. 6C



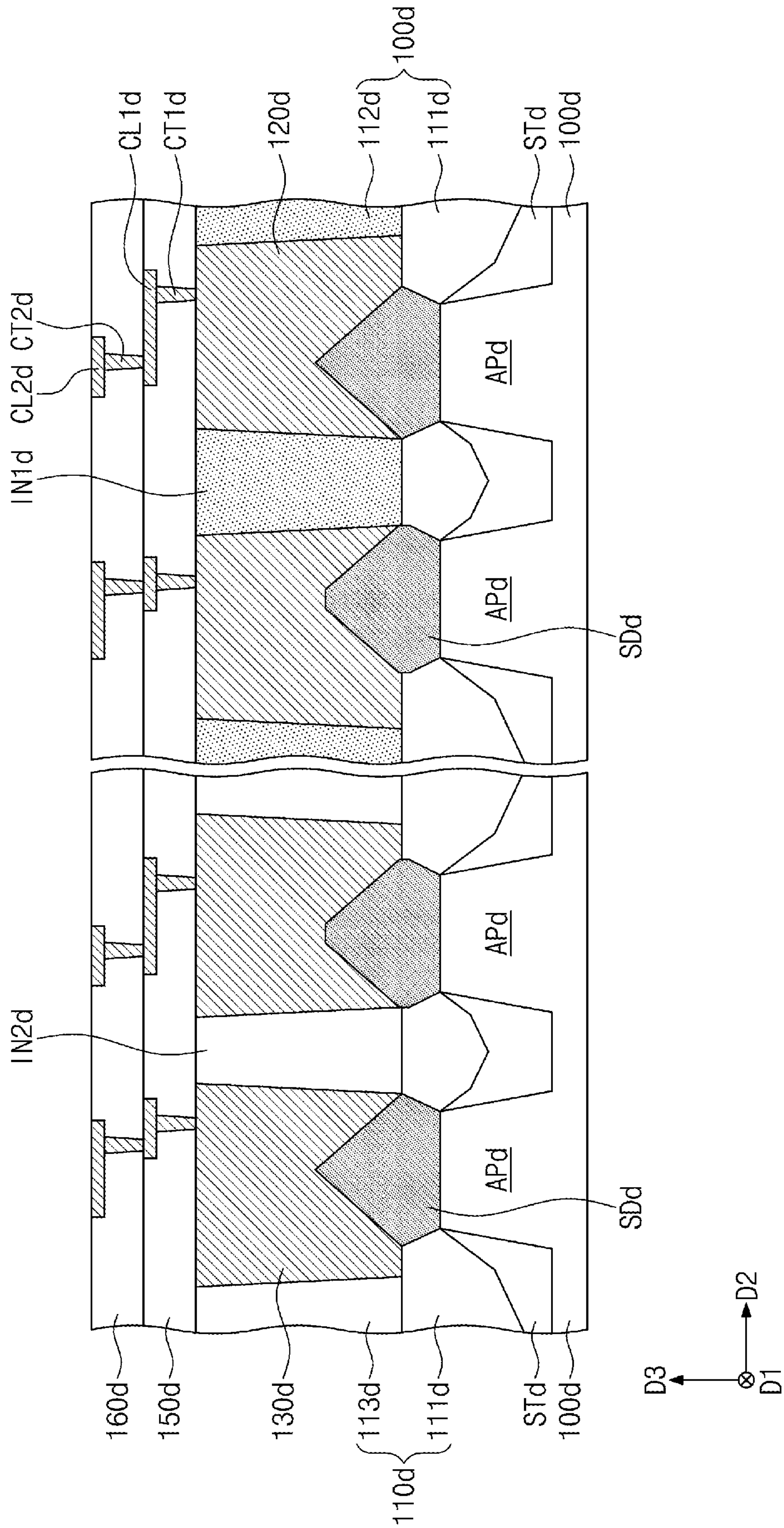


FIG. 7
CL1d
CT1d
CL2d
CT2d
IN1d
IN2d
120d
112d
111d
100d
STd
APd
SDd
160d
150d
130d
113d
110d
D1
D2
D3

SEMICONDUCTOR DEVICES INCLUDING CONDUCTIVE STRUCTURES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. nonprovisional application claims priority under 35 U.S.C § 119 to Korean Patent Application No. 10-2022-0070369 filed on Jun. 9, 2022 in the Korean Intellectual Property Office, and the entire contents of the above-identified application are incorporated by reference herein.

TECHNICAL FIELD

[0002] The present inventive concepts relate to semiconductor devices, and more particularly, relate to semiconductor devices that include conductive structures.

BACKGROUND

[0003] Semiconductor devices are beneficial in the electronics industry because of their small size, multi-functionality, and/or low fabrication cost. Semiconductor devices may be categorized as any one of semiconductor memory devices storing logic data, semiconductor logic devices processing operations of logic data, and hybrid semiconductor devices having both memory and logic elements.

[0004] Recently, desired characteristics for electronic products of increased speed and reduced power consumption have resulted in corresponding demand for semiconductor devices to be used or embedded in the electronic products to exhibit higher operating speeds and/or lower operating voltage. On the other hand, an increase in integration of the semiconductor device may induce a reduction in electrical properties and a reduction in a production yield of the semiconductor device. Hence, many studies have been conducted to increase or improve electrical properties and production yields of semiconductor devices.

SUMMARY

[0005] Some embodiments of the present inventive concepts provide semiconductor devices with increased or improved reliability and/or increased or improved electrical properties.

[0006] According to some embodiments of the present inventive concepts, a semiconductor device may comprise: a dielectric structure; and first conductive structures and second conductive structures in the dielectric structure. The dielectric structure may include a first dielectric layer that surrounds the first conductive structures and a second dielectric layer that surrounds the second conductive structures. The first dielectric layer may include a first intervention in contact with and between the first conductive structures. The second dielectric layer may include a second intervention in contact with and between the second conductive structures. A width in a first direction of the first intervention may decrease in a second direction from a top surface of the first intervention toward a bottom surface of the first intervention. A width in the first direction of the second intervention may increase in the second direction from a top surface of the second intervention toward a bottom surface of the second intervention. The first dielectric layer and the second dielectric layer may include different dielectric materials from each other.

[0007] According to some embodiments of the present inventive concepts, a semiconductor device may include: a substrate; a dielectric structure on the substrate; and first conductive structures and second conductive structures in the dielectric structure. The dielectric structure may include a first dielectric layer that surrounds the first conductive structures and a second dielectric layer that surrounds the second conductive structures. The first dielectric layer may include a first intervention between the first conductive structures. The second dielectric layer may include a second intervention between the second conductive structures. A width in a first direction of the first intervention may decrease with decreasing distance from a top surface of the substrate. A width in the first direction of the second intervention may increase with decreasing distance from the top surface of the substrate. The first dielectric layer and the second dielectric layer may include different dielectric materials from each other.

[0008] According to some embodiments of the present inventive concepts, a semiconductor device may comprise: a substrate that includes an active pattern; a source/drain region on the active pattern; a conductive structure connected to the source/drain region; and a dielectric structure that surrounds the conductive structure. The dielectric structure may include a first dielectric layer and a second dielectric layer that include different dielectric materials from each other. The conductive structure may include first conductive structures in the first dielectric layer and second conductive structures in the second dielectric layer. The first dielectric layer may include a first separation structure between the first conductive structures. The second dielectric layer may include a second separation structure between the second conductive structures. A width in a first direction of each of the first conductive structures may increase with decreasing distance from the substrate. A width in the first direction of each of the second conductive structures may decrease with decreasing distance from the substrate. A width in the first direction of the first separation structure may decrease with decreasing distance from the substrate. A width in the first direction of the second separation structure may increase with decreasing distance from the substrate.

[0009] According to some embodiments of the present inventive concepts, a method of fabricating a semiconductor device may include: forming a preliminary dielectric layer that includes a first section and a second section; forming a dielectric pattern by etching the first section of the preliminary dielectric layer; forming a first dielectric layer that surrounds the dielectric pattern; forming a mask pattern on the second section of the preliminary dielectric layer; etching the dielectric pattern and the second section of the preliminary dielectric layer using the mask pattern and the first dielectric layer as etching masks, wherein the etching of the second section of the preliminary dielectric layer results in a second dielectric layer; forming a first conductive structure that is surrounded by the first dielectric layer; and forming a second conductive structure that is surrounded by the second dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1**A illustrates a plan view showing a semiconductor device according to some embodiments.

[0011] FIG. **1**B illustrates a cross-sectional view taken along line **A1**-**A1'** of FIG. **1**A.

[0012] FIGS. **2**A, **2**B, **2**C, and **2**D illustrate cross-sectional views showing a method of fabricating the semiconductor device according to FIGS. **1**A and **1**B.

[0013] FIG. **3** illustrates a cross-sectional view showing a method of fabricating a semiconductor device according to some embodiments.

[0014] FIG. **4**A illustrates a plan view showing a semiconductor device according to some embodiments.

[0015] FIG. **4**B illustrates a cross-sectional view taken along line A**2**-A**2**' of FIG. **4**A.

[0016] FIG. **5** illustrates a cross-sectional view showing a semiconductor device according to some embodiments.

[0017] FIG. **6**A illustrates a plan view showing a semiconductor device according to some embodiments.

[0018] FIG. **6**B illustrates a cross-sectional view taken along line A**3**-A**3**' of FIG. **6**A.

[0019] FIG. **6**C illustrates a cross-sectional view taken along line B**3**-B**3**' of FIG. **6**A.

[0020] FIG. **7** illustrates a cross-sectional view showing a semiconductor device according to some embodiments.

DETAILED DESCRIPTION

[0021] The following will describe in detail a semiconductor device and its fabrication method according to some embodiments of the present inventive concepts with reference to the accompanying drawings.

[0022] FIG. **1**A illustrates a plan view showing a semiconductor device according to some embodiments. FIG. **1**B illustrates a cross-sectional view taken along line A**1**-A**1**' of FIG. **1**A.

[0023] Referring to FIGS. **1**A and **1**B, a semiconductor device may include a first region R**1** and a second region R**2**. As seen from the plan view of FIG. **1**A, the first region R**1** and the second region R**2** may be divided areas that are elongated in a first direction D**1** and a second direction D**2**. The first direction D**1** and the second direction D**2** may intersect each other. For example, the first direction D**1** and the second direction D**2** may be horizontal directions that are orthogonal to each other. The first region R**1** and the second region R**2** may be spaced apart from each other in the first direction D**1**.

[0024] The semiconductor device may include a substrate **100**. In some embodiments, the substrate **100** may be a semiconductor substrate. For example, the substrate **100** may include silicon, germanium, silicon-germanium, GaP, or GaAs. In some embodiments, the substrate **100** may be a silicon-on-insulator (SOI) substrate or a germanium-on-insulator (GOI) substrate. The substrate **100** may have a plate shape that extends along a plane that is elongated in the first direction D**1** and the second direction D**2**.

[0025] A dielectric structure **110** may be provided on the substrate **100**. The dielectric structure **110** may include a lower dielectric layer **111**, a first dielectric layer **112**, and a second dielectric layer **113**. The lower dielectric layer **111** may be provided on the substrate **100**. The first dielectric layer **112** and the second dielectric layer **113** may be provided on the lower dielectric layer **111**. The first dielectric layer **112** may be provided in the first region R**1**. The second dielectric layer **113** may be provided in the second region R**2**.

[0026] The lower dielectric layer **111** may include a dielectric material. For example, the lower dielectric layer **111** may include oxide. In some embodiments, the lower dielectric layer **111** may be a multi-layered structure that includes a plurality of dielectric layers. In some embodiments, the lower dielectric layer **111** may cover a semiconductor element (not shown) provided on the substrate **100**, and the lower dielectric layer **111** may be provided therein with conductive structures (not shown) that are electrically connected to the semiconductor element. The semiconductor element may include, for example, at least one selected from transistors, capacitors, and resistors. The conductive structures in the lower dielectric layer **111** may include, for example, conductive contacts and/or conductive lines.

[0027] The first dielectric layer **112** and the second dielectric layer **113** may include different dielectric materials from each other. The first dielectric layer **112** may include a first dielectric material, and the second dielectric layer **113** may include a second dielectric material having an etch selectivity with respect to the first dielectric material. For example, the first dielectric material may be nitride or carbonitride, and the second dielectric material may be oxide. The first dielectric layer **112** may include a dielectric material different from that of the lower dielectric layer **111**. The first dielectric material of the first dielectric layer **112** may have an etch selectivity with respect to a dielectric material included in the lower dielectric layer **111**.

[0028] The first dielectric layer **112** and the second dielectric layer **113** may be located at the same level as each other. For example, the first and second dielectric layers **112** and **113** may have their bottom surfaces that are coplanar with each other and are an equal distance from the substrate **100** (e.g., from a top surface of the substrate **100**). The first and second dielectric layers **112** and **113** may have their top surfaces that are coplanar with each other and are an equal distance from the substrate **100** (e.g., from the top surface of the substrate **100**).

[0029] In some embodiments, the second dielectric layer **113** and the lower dielectric layer **111** may include the same dielectric material, and may be connected to constitute a single unitary structure with no boundary therebetween. Stated differently, the second dielectric layer **113** and the lower dielectric layer **111** may be integral with each other.

[0030] First conductive structures **120** may be provided in the first dielectric layer **112** of the dielectric structure **110**. The first conductive structures **120** may be provided in the first region R**1**. The first conductive structures **120** may be surrounded by the first dielectric layer **112** of the dielectric structure **110**. The first conductive structures **120** may extend in a third direction D**3** and may extend through the first dielectric layer **112**. The third direction D**3** may intersect the first direction D**1** and the second direction D**2**. For example, the third direction D**3** may be a vertical direction that is perpendicular to the first direction D**1** and the second direction D**2**. The first conductive structures **120** may include a conductive material.

[0031] The first conductive structures **120** may be provided on the lower dielectric layer **111**. In some embodiments, the first conductive structure **120** may be connected to a conductive structure in the lower dielectric layer **111** (e.g., one or more of the conductive contacts and/or conductive lines discussed above), and may be electrically connected through the conductive structure in the lower dielectric layer **111** to a semiconductor element on the substrate **100** (e.g., one or more of the transistors, capacitors, and resistors discussed above). In some embodiments, the first conductive structures **120** may be provided on and directly connected to the substrate **100**.

[0032] Second conductive structures **130** may be provided in the second dielectric layer **113** of the dielectric structure **110**. The second conductive structures **130** may be provided in the second region R**2**. The second conductive structures **130** may be surrounded by the second dielectric layer **113** of the dielectric structure **110**. The second conductive structures **130** may extend in the third direction D**3** and may extend through the second dielectric layer **113**. The second conductive structures **130** may include a conductive material.

[0033] The second conductive structures **130** may be provided on the lower dielectric layer **111**. In some embodiments, the second conductive structure **130** may be connected to a conductive structure in the lower dielectric layer **111** (e.g., one or more of the conductive contacts and/or conductive lines discussed above), and may be electrically connected through the conductive structure in the lower dielectric layer **111** to the semiconductor element on the substrate **100** (e.g., one or more of the transistors, capacitors, and resistors discussed above). In some embodiments, the second conductive structures **130** may be provided on and directly connected to the substrate **100**.

[0034] The first and second conductive structures **120** and **130** may be located at the same level, or an equal distance from the substrate **100** (e.g., a top or bottom surface of the substrate **100**). The first and second conductive structures **120** and **130** may be located at the same level as that of the first and second dielectric layers **112** and **113**. In some embodiments, the top surfaces of the first and second dielectric layers **112** and **113** may be coplanar with top surfaces **121** of the first conductive structures **120** and with top surfaces **131** of the second conductive structures **130**. The bottom surfaces of the first and second dielectric layers **112** and **113** may be coplanar with bottom surfaces **122** of the first conductive structures **120** and with bottom surfaces **132** of the second conductive structures **130**.

[0035] In some embodiments, the first and second conductive structures **120** and **130** may be conductive contacts. In some embodiments, the first and second conductive structures **120** and **130** may be conductive lines that extend in the second direction D**2**.

[0036] The first conductive structure **120** may have inclined sidewalls. The first conductive structure **120** may have a width that increases with decreasing distance from the substrate **100** and the lower dielectric layer **111**. For example, a width W**1** in the first direction D**1** of the first conductive structure **120** may increase with decreasing distance from the substrate **100** (or a top surface thereof) and the lower dielectric layer **111**. The width of the first conductive structure **120** may increase in a direction from the top surface **121** toward the bottom surface **122** of the first conductive structure **120**. The first conductive structure **120** may have a width at the top surface **121** that is less than a width at the bottom surface **122**. Stated differently, the first conductive structure **120** may be wider in the first direction D**1** at the bottom surface **122** thereof than at the top surface **121** thereof.

[0037] The second conductive structure **130** may have inclined sidewalls. The second conductive structure **130** may have a width that decreases with decreasing distance from the substrate **100** and the lower dielectric layer **111**. For example, a width W**2** in the first direction D**1** of the second conductive structure **130** may decrease with decreasing distance from the substrate **100** (or a top surface thereof) and the lower dielectric layer **111**. The width of the second conductive structure **130** may decrease in a direction from the top surface **131** toward the bottom surface **132** of the second conductive structure **130**. The second conductive structure **130** may have a width at the top surface **131** that is greater than a width at the bottom surface **132**. Stated differently, the second conductive structure **130** may be wider in the first direction D**1** at the top surface **131** thereof than at the bottom surface **132** thereof.

[0038] The first dielectric layer **112** may include a first intervention IN**1** interposed between the first conductive structures **120**. The first intervention IN**1** may be a separation structure or insulating structure. The first intervention IN**1** may be in contact with the first conductive structures **120** adjacent to each other. The first intervention IN**1** may have opposite sidewalls that are correspondingly or respectively in contact with the sidewall of one of the first conductive structures **120** and with the sidewall of another of the first conductive structures **120**. The sidewalls of the first intervention IN**1** may be inclined corresponding to the sidewalls of the first conductive structure **120**.

[0039] The first intervention IN**1** may have a width that decreases with decreasing distance from the substrate **100**. For example, a width W**3** in the first direction D**1** of the first intervention IN**1** may decrease with decreasing distance from the substrate **100**. The width of the first intervention IN**1** may decrease in a direction from a top surface IN**1**_T toward a bottom surface IN**1**_B of the first intervention IN**1**. The first intervention IN**1** may have a width at the top surface IN**1**_T that is greater than a width at the bottom surface IN**1**_B.

[0040] The second dielectric layer **113** may include a second intervention IN**2** interposed between the second conductive structures **130**. The second intervention IN**2** may be a separation structure or insulating structure. The second intervention IN**2** may be in contact with the second conductive structures **130** adjacent to each other. The second intervention IN**2** may have opposite sidewalls that are correspondingly or respectively in contact with the sidewall of one of the second conductive structures **130** and with the sidewall of another of the second conductive structures **130**. The sidewalls of the second intervention IN**2** may be inclined corresponding to the sidewalls of the second conductive structure **130**.

[0041] The second intervention IN**2** may have a width that increases with decreasing distance from the substrate **100**. For example, a width W**4** in the first direction D**1** of the second intervention IN**2** may increase with decreasing distance from the substrate **100**. The width of the second intervention IN**2** may increase in a direction from a top surface IN**2**_T toward a bottom surface IN**2**_B of the second intervention IN**2**. The second intervention IN**2** may have a width at the top surface IN**2**_T that is less than a width at the bottom surface IN**2**_B.

[0042] A semiconductor device according to some embodiments may be configured such that the widths of the first conductive structures **120** on the first region R**1** may increase with decreasing distance from the substrate **100**, and that the widths of the second conductive structures **130** on the second region R**2** may decrease with decreasing distance from the substrate **100**. Therefore, the first and second conductive structures **120** and **130** may have different shapes and sizes, and may induce or result in a difference in resistance and capacitance. As the first and second regions

R**1** and R**2** that are different from each other are provided thereon with the first and second conductive structures **120** and **130** having different shapes and sizes, it may be possible to optimize electrical properties of the semiconductor device.

[0043] FIGS. **2**A, **2**B, **2**C, and **2**D illustrate cross-sectional views showing a method of fabricating the semiconductor device according to FIG. **1**.

[0044] Referring to FIG. **2**A, a substrate **100** may be provided. A lower dielectric layer **111** may be formed on the substrate **100**. A preliminary dielectric layer **114** may be formed on the lower dielectric layer **111**. In some embodiments, the preliminary dielectric layer **114** may include the same material as that of the lower dielectric layer **111**, and the preliminary dielectric layer **114** and the lower dielectric layer **111** may be connected to constitute a single unitary structure with no boundary therebetween.

[0045] The preliminary dielectric layer **114** may include a first section P**1** in the first region R**1** and a second section P**2** in the second region R**2**. The first section P**1** and the second section P**2** may be located at the same level. In some embodiments, the first section P**1** and the second section P**2** may be continuously connected into a single unitary structure with no boundary therebetween. In some embodiments, the first section P**1** and the second section P**2** may be contiguous. In some embodiments, the first section P**1** and the second section P**2** may be provided therebetween with a boundary and thus may be distinguished from each other.

[0046] Referring to FIG. **2**B, the first section P**1** of the preliminary dielectric layer **114** may be etched. The first section P**1** of the preliminary dielectric layer **114** may be etched to form dielectric patterns **115**. The first section P**1** of the preliminary dielectric layer **114** may have a portion that is not etched by the etching process, and the dielectric pattern **115** may be the non-etched portion of the first section P**1** of the preliminary dielectric layer **114**. The dielectric pattern **115** may have a width that increases with decreasing distance from the substrate **100**.

[0047] A first dielectric layer **112** may be formed to surround the dielectric pattern **115**. The first dielectric layer **112** may at least partially fill an empty space that is formed by etching the first section P**1** of the preliminary dielectric layer **114**. The first dielectric layer **112** may include a dielectric material having an etch selectivity with respect to the dielectric pattern **115**. For example, the first dielectric layer **112** may include nitride or carbonitride, and the dielectric pattern **115** may include oxide. The first dielectric layer **112** may include a first intervention IN**1** interposed between the dielectric patterns **115**.

[0048] A mask pattern **116** may be formed on the second section P**2** of the preliminary dielectric layer **114**. In some embodiments, the mask pattern **116** may be located at a higher level than that of the first dielectric layer **112**. The formation of the mask pattern **116** may include forming a mask layer on the second section P**2** of the preliminary dielectric layer **114**, and patterning the mask layer to form the mask pattern **116**. The mask pattern **116** may include a material having an etch selectivity with respect to the second section P**2** of the preliminary dielectric layer **114**. For example, the mask pattern **116** may include nitride or carbonitride, and the second section P**2** of the preliminary dielectric layer **114** may include oxide. In some embodiments, the mask pattern **116** may include the same material as that of the first dielectric layer **112**.

[0049] Referring to FIG. **2**C, the mask pattern **116** and the first dielectric layer **112** may be used as an etching mask to perform an etching process. The etching process may etch the dielectric patterns **115** and the second section P**2** of the preliminary dielectric layer **114**. The etching process may remove the dielectric patterns **115** and may form first spaces **141** surrounded by the first dielectric layer **112**. The first spaces **141** may expose the lower dielectric layer **111**. The etching process may form second spaces **142** surrounded by the second section P**2** of the preliminary dielectric layer **114**. The second spaces **142** may expose the lower dielectric layer **111**. A second dielectric layer **113** may be defined to indicate the etched second section P**2** of the preliminary dielectric layer **114**.

[0050] Referring to FIG. **2**D, a conductive layer CL may be formed. The conductive layer CL may include a conductive material. The conductive layer CL may at least partially fill the first spaces **141** and the second spaces **142**. The conductive layer CL may cover the mask pattern **116**, the first dielectric layer **112**, and the second dielectric layer **113**.

[0051] Referring to FIG. **1**B, a process may be performed to remove the mask pattern **116** and an upper portion of the conductive layer CL. For example, the mask pattern **116** and the upper portion of the conductive layer CL may be removed by a chemical mechanical polishing (CMP) process. The upper portion of the conductive layer CL may be removed, such that the conductive layer CL may be divided into first and second conductive structures **120** and **130**.

[0052] In a method of fabricating a semiconductor device according to some embodiments, the first and second conductive structures **120** and **130** having different shapes and sizes may be respectively formed on the first and second regions R**1** and R**2** that are different from each other, which may result in an optimization of electrical properties of the semiconductor device.

[0053] FIG. **3** illustrates a cross-sectional view showing a method of fabricating a semiconductor device according to some embodiments.

[0054] Referring to FIG. **3**, similar to the description of FIG. **2**A, a preliminary dielectric layer **114** may be formed which includes the substrate **100**, the lower dielectric layer **111**, the first section P**1**, and the second section P**2**. The first section P**1** of the preliminary dielectric layer **114** may be etched to form dielectric patterns **115**.

[0055] A mask layer **117** may be formed to cover the dielectric patterns **115** and the second section P**2** of the preliminary dielectric layer **114**. The mask layer **117** may at least partially fill an empty space that is formed by etching the first section P**1** of the preliminary dielectric layer **114**. The mask layer **117** may extend from the second region R**2** to the first region R**1**.

[0056] The mask layer **117** may be patterned to form a mask pattern **116** and a first dielectric layer **112** that are similar to those discussed with reference to FIG. **2**B. In some embodiments, a portion of the mask layer **117** in the first region R**1** may be patterned simultaneously with a portion of the mask layer **117** in the second region R**2**, and the first dielectric layer **112** may be formed in the first region R**1** simultaneously with the mask pattern **116** in the second region R**2**. In some embodiments, a portion of the mask layer **117** in the first region R**1** may be patterned independently of a portion of the mask layer **117** in the second region R**2**, and the first dielectric layer **112** may be formed in the first region R**1** independently of the mask pattern **116** in the

second region R**2**. For example, a portion of the mask layer **117** in the first region R**1** may be patterned to form the first dielectric layer **112** and thereafter a portion of the mask layer **117** in the second region R**2** may be patterned to form the mask pattern **116**.

[0057] Similar to the description of FIGS. **1**B, **2**C, and **2**D, a second dielectric layer **113** may be formed, and the first and second conductive structures **120** and **130** may be formed.

[0058] FIG. **4**A illustrates a plan view showing a semiconductor device according to some embodiments. FIG. **4**B illustrates a cross-sectional view taken along line A**2**-A**2**' of FIG. **4**A.

[0059] Referring to FIGS. **4**A and **4**B, a semiconductor device may include a substrate **100***a*, a dielectric structure **110***a* on the substrate **100***a*, first conductive structures **120***a* in the dielectric structure **110***a*, and second conductive structures **130***a* in the dielectric structure **110***a*.

[0060] The dielectric structure **110***a* may include a lower dielectric layer **111***a* on the substrate **100***a*, a first dielectric layer **112***a* on the lower dielectric layer **111***a*, and a second dielectric layer **113***a* on the lower dielectric layer **111***a*.

[0061] The first dielectric layer **112***a* may include a first intervention IN**1***a* and a first connector CO**1***a*. The first dielectric layer **112***a* may have a portion between one of the first conductive structures **120***a* and an adjacent one or a proximate one of the second conductive structures **130***a*, and the first connector CO**1***a* may be the portion of the first dielectric layer **112***a*.

[0062] The second dielectric layer **113***a* may include a second intervention IN**2***a* and a second connector CO**2***a*. The second dielectric layer **113***a* may have a portion between one of the first conductive structures **120***a* and the adjacent one or the proximate one of the second conductive structures **130***a*, and the second connector CO**2***a* may be the portion of the second dielectric layer **113***a*.

[0063] The first connector CO**1***a* and the second connector CO**2***a* may be provided between a first conductive structure **120***a* and a second conductive structure **130***a* that are adjacent to each other or proximate with each other. The first connector CO**1***a* and the second connector CO**2***a* may be in contact with each other. Each of the first connector CO**1***a* and the second connector CO**2***a* may have sidewalls that are inclined. In some embodiments, each of the first connector CO**1***a* and the second connector CO**2***a* may have sidewalls that are non-perpendicular with a bottom surface of the dielectric structure **110***a* (e.g., a bottom surface of the lower dielectric layer **111***a*). The first connector CO**1***a* may have a first sidewall CO**1***a*_S**1** that is in contact with the first conductive structure **120***a*, and the first connector CO**1***a* may also have a second sidewall CO**1***a*_S**2** that is opposite to the first sidewall CO**1***a*_S**1** and in contact with the second connector CO**2***a*. The second connector CO**2***a* may have a first sidewall CO**2***a*_S**1** that is in contact with the second conductive structure **130***a*, and the second connector CO**2***a* may also have a second sidewall CO**2***a*_S**2** that is opposite to the first sidewall CO**2***a*_S**1** and in contact with the second sidewall CO**1***a*_S**2** of the first connector CO**1***a*.

[0064] The first connector CO**1***a* may have a width that decreases with decreasing distance from the substrate **100***a* and the lower dielectric layer **111***a*. Stated differently, the first connector CO**1***a* may have a width that increases with increasing distance from the substrate **100***a* and the lower dielectric layer **111***a*. For example, a width W**5** in the first direction D**1** of the first connector CO**1***a* may decrease with decreasing distance from the substrate **100***a* and the lower dielectric layer **111***a*. The width of the first connector CO**1***a* may decrease in a direction from a top surface CO**1***a*_T toward a bottom surface CO**1***a*_B of the first connector CO**1***a*. The first connector CO**1***a* may have a width at the top surface CO**1***a*_T that is greater than a width at the bottom surface CO**1***a*_B.

[0065] The second connector CO**2***a* may have a width that decreases with increasing distance from the substrate **100***a* and the lower dielectric layer **111***a*. Stated differently, the second connector CO**2***a* may have a width that increases with decreasing distance from the substrate **100***a* and the lower dielectric layer **111***a*. For example, a width W**6** in the first direction D**1** of the second connector CO**2***a* may increase with decreasing distance from the substrate **100***a* and the lower dielectric layer **111***a*. The width of the second connector CO**2***a* may increase in a direction from a top surface CO**2***a*_T toward a bottom surface CO**2***a*_B of the second connector CO**2***a*. The second connector CO**2***a* may have a width at the top surface CO**2***a*_T that is less than a width at the bottom surface CO**2***a* B.

[0066] The first conductive structure **120***a* may be provided between the first connector CO**1***a* and the first intervention IN**1***a*. The second connective structure **130***a* may be provided between the second connector CO**2***a* and the second intervention IN**2***a*.

[0067] FIG. **5** illustrates a cross-sectional view showing a semiconductor device according to some embodiments.

[0068] Referring to FIG. **5**, a semiconductor device may include a substrate **100***b*. A dielectric structure **110***b* may be provided on the substrate **100***b*. The dielectric structure **110***b* may include a first lower dielectric layer **111***b* that is on (and in some embodiments, covers) the substrate **100***b*, a second lower dielectric layer **118***b* on the first lower dielectric layer **111***b*, and a first dielectric layer **112***b* and a second dielectric layer **113***b* that are on the second lower dielectric layer **118***b*.

[0069] A first transistor TR**1** and a second transistor TR**2** may be provided between the substrate **100***b* and a portion of the dielectric structure **110***b*. For example, the first and second transistors TR**1** and TR**2** may be cell transistors and/or peripheral transistors that constitute memory devices, logic devices, and/or image sensor devices. In some embodiments, the first and second transistors TR**1** and TR**2** may be covered with the first lower dielectric layer **111***b* of the dielectric structure **110***b*. The first and second transistors TR**1** and TR**2** may have different sizes and/or functions.

[0070] Each of the first and second transistors TR**1** and TR**2** may include impurity regions IR, and may also include a channel and a gate structure that are between the impurity regions IR. The gate structure may include gate spacers GS, and may also include a gate dielectric layer GI, a gate electrode GE, and a gate capping layer GP that are between the gate spacers GS. The impurity regions IR may be formed by implanting the substrate **100***b* with impurities. A dielectric material may be included in the gate spacers GS, the gate dielectric layer GI, and the gate capping layer GP. The gate electrode GE may include a conductive material. Other structures of the first and second transistors TR**1** and TR**2** are contemplated, and no limitation is imposed on the structures of the first and second transistors TR**1** and TR**2**. In some embodiments, the first and second transistors TR**1** and TR**2** may each include a buried gate electrode. In some embodiments, the first and second transistors TR**1** and TR**2**

may each include a vertical gate electrode. In some embodiments, the first and second transistors TR**1** and TR**2** may each include a gate-all-around structure.

[0071] The substrate **100***b* may be provided with device isolation layers STb therein. The first and second transistors TR**1** and TR**2** may be provided between the device isolation layers STb. The device isolation layers STb may include a dielectric material.

[0072] First contacts CT**1***b* and second contacts CT**2***b* may be provided in the first lower dielectric layer **111***b* of the dielectric structure **110***b*. The first contacts CT**1***b* may be connected to the first transistor TR**1**, and the second contacts CT**2***b* may be connected to the second transistor TR**2**. The first and second contacts CT**1***b* and CT**2***b* may include a conductive material.

[0073] First conductive lines CL**1***b* and second conductive lines CL**2***b* may be provided in the second lower dielectric layer **118***b* of the dielectric structure **110***b*. The first conductive line CL**1***b* may be connected to the first contact CT**1***b*, and the second conductive line CL**2***b* may be connected to the second contact CT**2***b*. The first and second conductive lines CL**1***b* and CL**2***b* may include a conductive material.

[0074] The first dielectric layer **112***b* may be provided with first conductive structures **120***b* therein. The first conductive structures **120***b* may have widths that increase with decreasing distance from the substrate **100***b* or from a top surface of the substrate **100***b*. The second dielectric layer **113***b* may be provided with second conductive structures **130***b* therein. The second conductive structures **130***b* may have widths that decrease with decreasing distance from the substrate **100***b* or from the top surface of the substrate **100***b*. The first dielectric layer **112***b* may include a first intervention IN**1***b* between the first conductive structures **120***b*. The second dielectric layer **113***b* may include a second intervention IN**2***b* between the second conductive structures **130***b*. The first dielectric layer **112***b* and the second dielectric layer **113***b* may include dielectric materials that are different from each other.

[0075] FIG. **6**A illustrates a plan view showing a semiconductor device according to some embodiments. FIG. **6**B illustrates a cross-sectional view taken along line A**3**-A**3**' of FIG. **6**A. FIG. **6**C illustrates a cross-sectional view taken along line B**3**-B**3**' of FIG. **6**A.

[0076] Referring to FIGS. **6**A, **6**B, and **6**C, a semiconductor device may include a substrate **100***c*.

[0077] The substrate **100***c* may include active patterns APc. Each of the active patterns APc may protrude or extend in height in the third direction D**3**. The active patterns APc may be portions of the substrate **100***c*. The active patterns APc may extend in length in the first direction D**1**.

[0078] A device isolation layer STc may be provided on the substrate **100***c*. The device isolation layer STc may include a dielectric material. For example, the device isolation layer STc may include oxide. The active patterns APc may extend between the device isolation layer STc. The device isolation layer STc may define the active patterns APc, for example in the second direction D**2**.

[0079] Source/drain patterns SDc may be provided on the active patterns APc. In some embodiments, the source/drain patterns SDc may include p-type impurity regions and n-type impurity regions. Channel CHc arranged in the third direction D**3** may be provided between the source/drain patterns SDc adjacent or proximate to each other in the first direction D**1**. The channels CHc may be portions of the active pattern APc. The active pattern APc may have a portion interposed between the source/drain patterns SDc adjacent to each other in the first direction D**1**, and the channel CHc may be or may include the interposed portion of the active pattern APc.

[0080] The source/drain patterns SDc may be epitaxial patterns formed by a selective epitaxial growth process. The source/drain patterns SDc may include a semiconductor material.

[0081] Gate structures GTc may be provided on the active patterns APc. The gate structures GTc may extend in the second direction D**2**. The gate structures GTc may be spaced apart from each other in the first direction D**1**. Each of the gate structures GTc may cover top and bottom surfaces of the channels CHc that are arranged in the third direction D**3**.

[0082] Each of the gate structures GTc may include a gate electrode GEc, a gate dielectric layer GIc, gate spacers GSc, and a gate capping layer GPc. The gate electrode GEc may include a conductive material. The gate electrode GEc may include a portion that is interposed between the channels CHc adjacent to each other in the third direction D**3**. The gate spacers GSc may be provided on opposite sides (in the first direction D**1**) of a portion of the gate electrode GEc. The gate spacers GSc may include a dielectric material. The gate dielectric layer GIc may include, for example, a portion interposed between the gate electrode GEc and the channel CHc and a portion interposed between the gate electrode GEc and the gate spacer GSc. The gate dielectric layer GIc may separate the gate electrode GEc from the channel CHc. In some embodiments, the gate dielectric layer GIc may be between the gate electrode GEc and the source/drain patterns SDc. The gate dielectric layer GIc may include a dielectric material. The gate capping layer GPc may cover a top surface of the gate electrode GEc. The gate capping layer GPc may include a dielectric material.

[0083] A dielectric structure **110***c* may be provided on the source/drain patterns SDc and the gate structures GTc. The dielectric structure **110***c* may include a lower dielectric layer **111***c*, a first dielectric layer **112***c*, and a second dielectric layer **113***c*. The lower dielectric layer **111***c* may be provided on the device isolation layer STc. The first dielectric layer **112***c* and the second dielectric layer **113***c* may be provided on the lower dielectric layer **111***c*. The first dielectric layer **112***c* and the second dielectric layer **113***c* may include dielectric materials that are different from each other. The first dielectric layer **112***c* may include a dielectric layer having an etch selectivity with respect to the second dielectric layer **113***c*.

[0084] First conductive structures **120***c* may be provided in the first dielectric layer **112***c* of the dielectric structure **110***c*. The first conductive structures **120***c* may be active contacts. The first conductive structures **120***c* may be connected to the source/drain patterns SDc. The first conductive structures **120***c* may have widths (in the second direction D**2**) that increase with decreasing distance from the substrate **100***c* or from a top surface of the substrate **100***c*. The first dielectric layer **112***c* may include a first intervention IN**1***c* between the first conductive structures **120***c* adjacent or proximate to each other. The first intervention IN**1***c* may have a width that decreases with decreasing distance from the substrate **100***c* or from the top surface of the substrate **100***c*. A portion of the first conductive structure **120***c* may be provided in the source/drain pattern SDc. Portions of the source/drain pattern SDc may be correspondingly on oppo-

site sides (in the first direction D**1**) of a portion of the first conductive structure **120***c*. A portion of the source/drain pattern SDc may be removed in or during forming the first conductive structure **120***c*. A portion of the first dielectric layer **112***c* may be provided between the first conductive structure **120***c* and the gate structure GTc.

[0085] Second conductive structures **130***c* may be provided in the second dielectric layer **113***c* of the dielectric structure **110***c*. The second conductive structures **130***c* may be active contacts. The second conductive structures **130***c* may be connected to the source/drain pattern SDc. The second conductive structure **130***c* may have a width (in the second direction D**2**) that decreases with decreasing distance from the substrate **100***c* or from the top surface of the substrate **100***c*. The second dielectric layer **113***c* may include a second intervention IN**2***c* between the second conductive structures **130***c* adjacent or proximate to each other. The second intervention IN**2***c* may have a width that increases with decreasing distance from the substrate **100***c* or from the top surface of the substrate **100***c*. As seen in FIG. **6**C, a portion of the second conductive structure **130***c* may be provided in the source/drain pattern SDc. Portions of the source/drain pattern SDc may be correspondingly on opposite sides (in the first direction D**1**) of a portion of the second conductive structure **130***c*. A portion of the source/drain pattern SDc may be removed in or during forming the second conductive structure **130***c*. A portion of the second dielectric layer **113***c* may be provided between the second conductive structure **130***c* and the gate structure GTc.

[0086] A first upper dielectric layer **150***c* may be provided on the dielectric structure **110***c*, the first conductive structures **120***c*, and the second conductive structures **130***c*, and in some embodiments the first upper dielectric layer **150***c* may at least partially cover the dielectric structure **110***c*, the first conductive structures **120***c*, and the second conductive structures **130***c*. The first upper dielectric layer **150***c* may include a dielectric material. The first upper dielectric layer **150***c* may be provided therein with first contacts CT**1***c* and first conductive lines CL**1***c*. Each first contact CT**1***c* may be connected to one of the first conductive structures **120***c* or one of the second conductive structures **130***c*. Each first conductive line CL**1***c* may be connected to at least one of the first contacts CT**1***c*. The first contacts CT and the first conductive lines CL may include a conductive material.

[0087] A second upper dielectric layer **160***c* may be provided on the first upper dielectric layer **150***c*, and in some embodiments the second upper dielectric layer **160***c* may at least partially cover the first upper dielectric layer **150***c*. The second upper dielectric layer **160***c* may include a dielectric material. The second upper dielectric layer **160***c* may be provided therein with second contacts CT**2***c* and second conductive lines CL**2***c*. The second contacts CT**2***c* may be connected to the first conductive lines CL**1***c*. The second conductive lines CL**2***c* may be connected to the second contacts CT**2***c*. The second contacts CT**2***c* and the second conductive lines CL**2***c* may include a conductive material.

[0088] FIG. **7** illustrates a cross-sectional view showing a semiconductor device according to some embodiments.

[0089] Referring to FIG. **7**, a semiconductor device may include a substrate **100***d* including active patterns APd, a device isolation layer STd, a dielectric structure **110***d*, source/drain patterns SDd, gate structures (not shown in FIG. **7**), first conductive structures **120***d*, second conductive structures **130***d*, a first upper dielectric layer **150***d*, a second upper dielectric layer **160***d*, first contacts CT**1***d*, first conductive lines CL**1***d*, second contacts CT**2***d*, and second conductive lines CL**2***d*.

[0090] The dielectric structure **110***d* may include a lower dielectric layer **111***d* on the device isolation layer STd, and may also include a first dielectric layer **112***d* and a second dielectric layer **113***d* on the lower dielectric layer **111***d*. The first dielectric layer **112***d* may include a first intervention IN**1***d* between first conductive structures **120***d* adjacent or proximate to each other. The second dielectric layer **113***d* may include a second intervention IN**2***d* between second conductive structures **130***d* adjacent or proximate to each other.

[0091] Portions of one of the first and second conductive structures **120***c* and **130***c* may be correspondingly on opposite sides (in the second direction D**2**) of the source/drain pattern SDd. The first conductive structure **120***c* and the second conductive structure **130***c* may be formed without removing a portion of the source/drain pattern SDd.

[0092] For semiconductor devices according to some embodiments of the present inventive concepts, as regions differing from each other may be provided thereon with conductive structures having different shapes and sizes, it may be possible to optimize electrical properties of the semiconductor device.

[0093] Although the present inventive concepts have been described in connection with the some embodiments thereof illustrated in the accompanying drawings, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the scope of the present inventive concepts as defined by the appended claims. The above disclosed embodiments should thus be considered illustrative and not restrictive.

What is claimed is:

1. A semiconductor device, comprising:

a dielectric structure; and

first conductive structures and second conductive structures in the dielectric structure,

wherein the dielectric structure includes a first dielectric layer that surrounds the first conductive structures and a second dielectric layer that surrounds the second conductive structures,

wherein the first dielectric layer includes a first intervention in contact with and between the first conductive structures,

wherein the second dielectric layer includes a second intervention in contact with and between the second conductive structures,

wherein a width in a first direction of the first intervention decreases in a second direction from a top surface of the first intervention toward a bottom surface of the first intervention,

wherein a width in the first direction of the second intervention increases in the second direction from a top surface of the second intervention toward a bottom surface of the second intervention, and

wherein the first dielectric layer and the second dielectric layer include different dielectric materials from each other.

2. The semiconductor device of claim **1**, wherein

the first dielectric layer includes a first dielectric material, and

the second dielectric layer includes a second dielectric material having an etch selectivity with respect to the first dielectric material.

3. The semiconductor device of claim **1**, wherein

a width of each of the first conductive structures increases in the second direction from a top surface of each of the first conductive structures toward a bottom surface of the each of the first conductive structures, and

a width of each of the second conductive structures decreases in the second direction from a top surface of each of the first conductive structures toward a bottom surface of the each of the second conductive structures.

4. The semiconductor device of claim **1**, wherein

the first conductive structures are spaced apart from the second conductive structures in the first direction, with one of the first conductive structures proximate to one of the second conductive structures,

the first dielectric layer further includes a first connector between the one of the first conductive structures and the proximate one of the second conductive structures, and

the second dielectric layer further includes a second connector between the one of the first conductive structures and the proximate one of the second conductive structures.

5. The semiconductor device of claim **4**, wherein a width in the first direction of the first connector decreases in the second direction from a top surface of the first connector toward a bottom surface of the first connector.

6. The semiconductor device of claim **4**, wherein a width in the first direction of the second connector increases in the second direction from a top surface of the first connector toward a bottom surface of the second connector.

7. The semiconductor device of claim **4**, wherein

a sidewall of the first connector is in contact with a sidewall of the second connector, and

the sidewall of each of the first and second connectors is non-perpendicular with a bottom surface of the dielectric structure.

8. The semiconductor device of claim **1**, wherein upper surfaces of each of the first dielectric layer, the second dielectric layer, the first conductive structures, and the second conductive structures are coplanar.

9. The semiconductor device of claim **1**, wherein

the first dielectric layer includes nitride or carbonitride, and

the second dielectric layer includes oxide.

10. A semiconductor device, comprising:

a substrate;

a dielectric structure on the substrate; and

first conductive structures and second conductive structures in the dielectric structure,

wherein the dielectric structure includes a first dielectric layer that surrounds the first conductive structures and a second dielectric layer that surrounds the second conductive structures,

wherein the first dielectric layer includes a first intervention between the first conductive structures,

wherein the second dielectric layer includes a second intervention between the second conductive structures,

wherein a width of the first intervention in a first direction decreases with decreasing distance from a top surface of the substrate,

wherein a width of the second intervention in the first direction increases with decreasing distance from the top surface of the substrate, and

wherein the first dielectric layer and the second dielectric layer include different dielectric materials from each other.

11. The semiconductor device of claim **10**, wherein bottom surfaces of the first dielectric layer, the second dielectric layer, the first conductive structures, and the second conductive structures are coplanar with each other.

12. The semiconductor device of claim **10**, wherein top surfaces of the first dielectric layer, the second dielectric layer, the first conductive structures, and the second conductive structures are coplanar with each other.

13. The semiconductor device of claim **10**, wherein the first conductive structures and the second conductive structures are in direct contact with the top surface of the substrate.

14. The semiconductor device of claim **10**, wherein

the first conductive structures are spaced apart from the second conductive structures in the first direction, with one of the first conductive structures proximate to one of the second conductive structures,

the first dielectric layer further includes a first connector between the one of the first conductive structures and the proximate one of the second conductive structures, and

the second dielectric layer further includes a second connector between the one of the first conductive structures and the proximate one of the second conductive structures.

15. The semiconductor device of claim **14**, wherein

a width of the first connector in the first direction decreases with decreasing distance from the substrate, and

a width of the second connector in the first direction increases with decreasing distance from the substrate.

16. The semiconductor device of claim **14**, wherein

a first sidewall of the first connector is in contact with the one of the first conductive structures,

a second sidewall of the first connector is in contact with the second connector, and

the first and second sidewalls of the first connector are non-perpendicular with a bottom surface of the dielectric structure.

17. The semiconductor device of claim **16**, wherein

a first sidewall of the second connector is in contact with the one of the second conductive structures,

a second sidewall of the second connector is in contact with the second sidewall of the first connector, and

the first and second sidewalls of the second connector are non-perpendicular with a bottom surface of the dielectric structure.

18. A semiconductor device, comprising:

a substrate that includes an active pattern;

a source/drain region on the active pattern;

a conductive structure connected to the source/drain region; and

a dielectric structure that surrounds the conductive structure,

wherein the dielectric structure includes a first dielectric layer and a second dielectric layer that include different dielectric materials from each other,

wherein the conductive structure includes first conductive structures in the first dielectric layer and second conductive structures in the second dielectric layer,

wherein the first dielectric layer includes a first separation structure between the first conductive structures,

wherein the second dielectric layer includes a second separation structure between the second conductive structures,

wherein a width in a first direction of each of the first conductive structures increases with decreasing distance from the substrate,

wherein a width in the first direction of each of the second conductive structures decreases with decreasing distance from the substrate,

wherein a width in the first direction of the first separation structure decreases with decreasing distance from the substrate, and

wherein a width in the first direction of the second separation structure increases with decreasing distance from the substrate.

19. The semiconductor device of claim **18**, wherein the first dielectric layer includes a dielectric material having an etch selectivity with respect to the second dielectric layer.

20. The semiconductor device of claim **19**, wherein lower surfaces of the first dielectric layer and the second dielectric layer are coplanar.

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