US 20230011215A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2023/0011215 A1**

(43) **Pub. Date: Jan. 12, 2023**

LEE et al.

(54) **NEUROMORPHIC CIRCUIT CAPABLE OF SETTING NEGATIVE WEIGHTS AND BACK PROPAGATION**

(71) Applicant: **Korea University Research and Business Foundation**, Seoul (KR)

(72) Inventors: **Hyung-Min LEE**, Seoul (KR); **Minil KANG**, Seoul (KR); **Min-Seong UM**, Seoul (KR)

(73) Assignee: **Korea University Research and Business Foundation**, Seoul (KR)

(21) Appl. No.: **17/825,574**

(22) Filed: **May 26, 2022**

(30) **Foreign Application Priority Data**

Jul. 6, 2021 (KR) 10-2021-0088327

Publication Classification

(51) **Int. Cl.**
G06N 3/063 (2006.01)

(52) **U.S. Cl.**
CPC ***G06N 3/063*** (2013.01)

(57) **ABSTRACT**

Provided is a neuromorphic circuit including an input module configured to generate an input voltage, an output module configured to measure a current transmitted from the input module and generate an output voltage, synapse modules configured to electrically connect the input module and the output module and determine a current to be transmitted to the output module and including a memory element to which a weight is assigned, and a crossing module configured to control a direction of current flowing through the synapse modules.

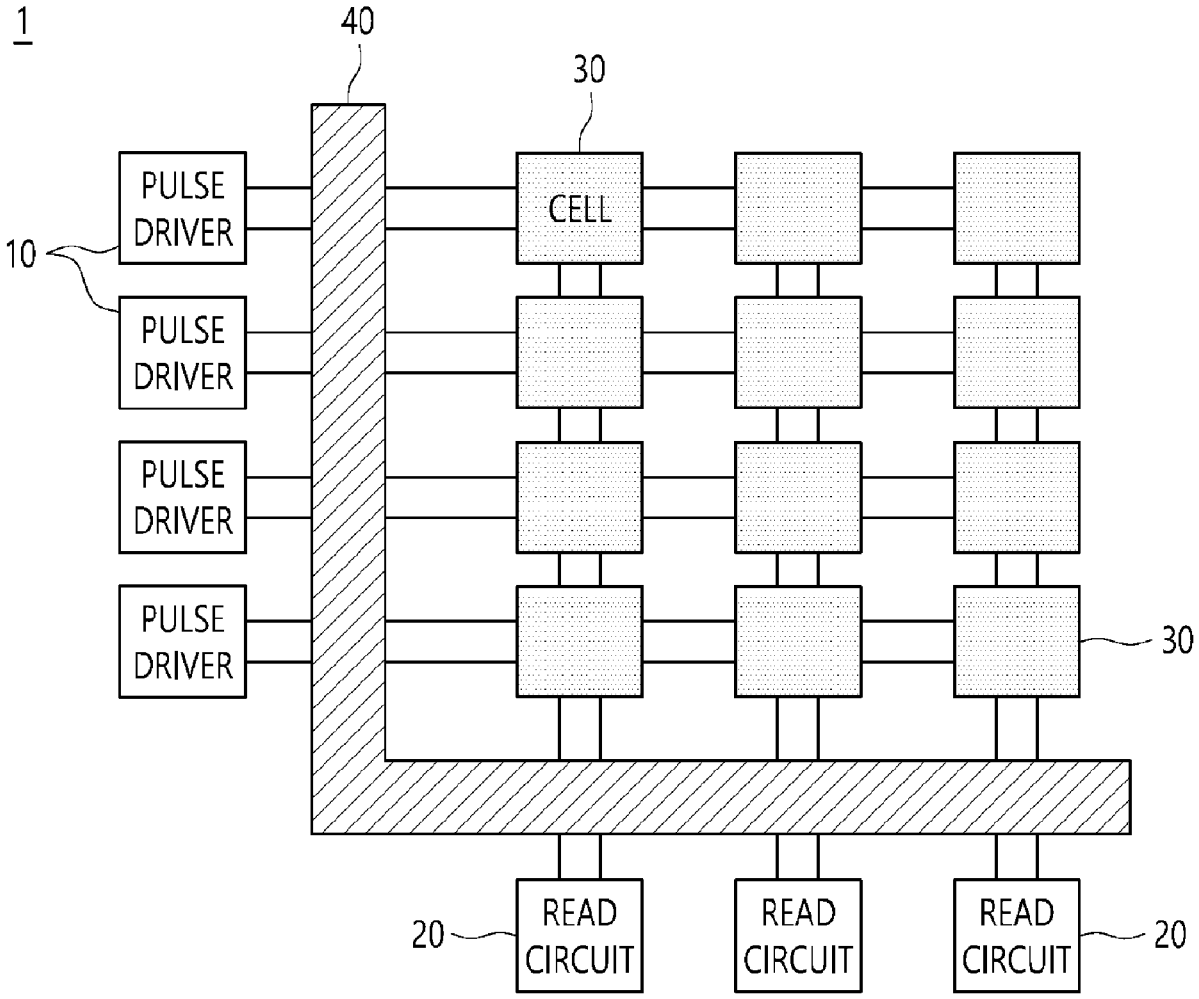


FIG. 1

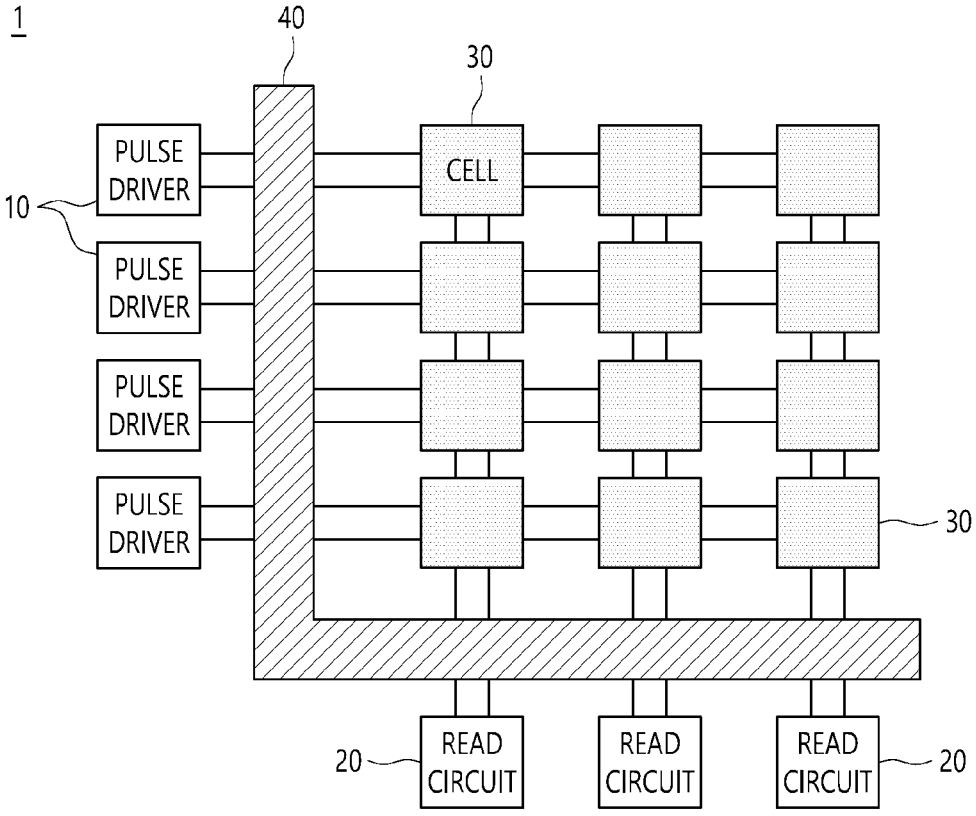

1
40
30
PULSE DRIVER
PULSE DRIVER
PULSE DRIVER
PULSE DRIVER
10
CELL
30
20
READ CIRCUIT
READ CIRCUIT
READ CIRCUIT
20

FIG. 2

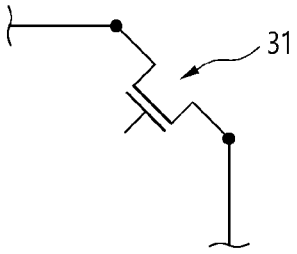


FIG. 3

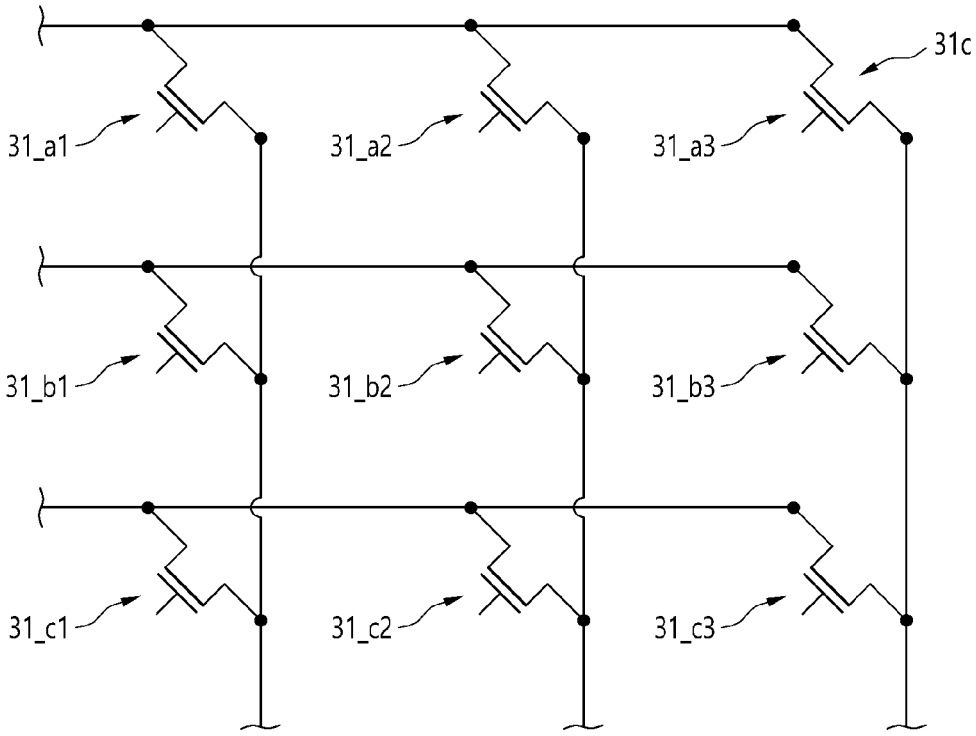


FIG. 4

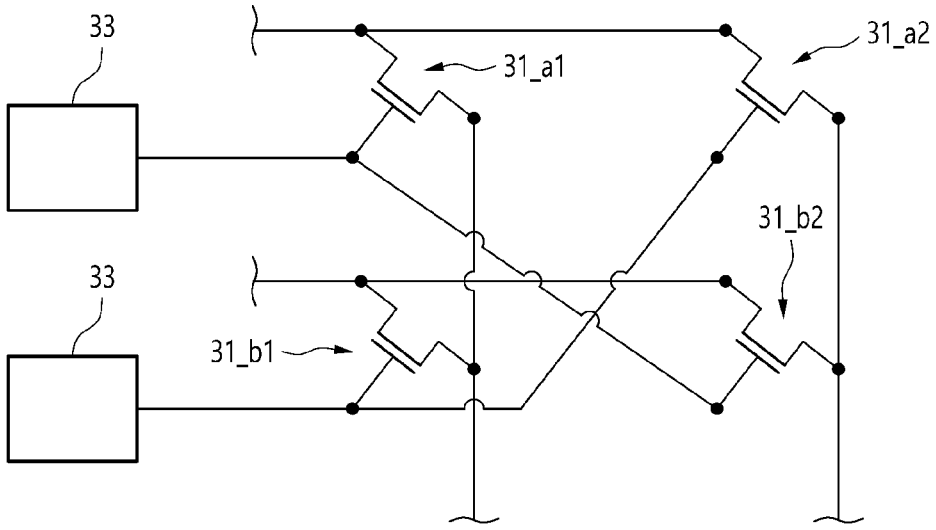


FIG. 5

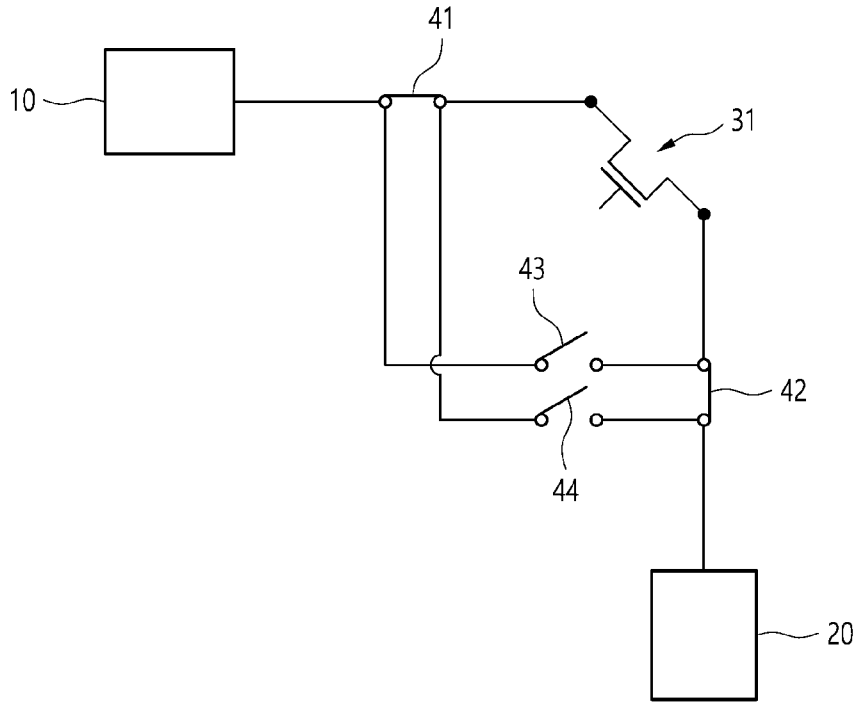


FIG. 6

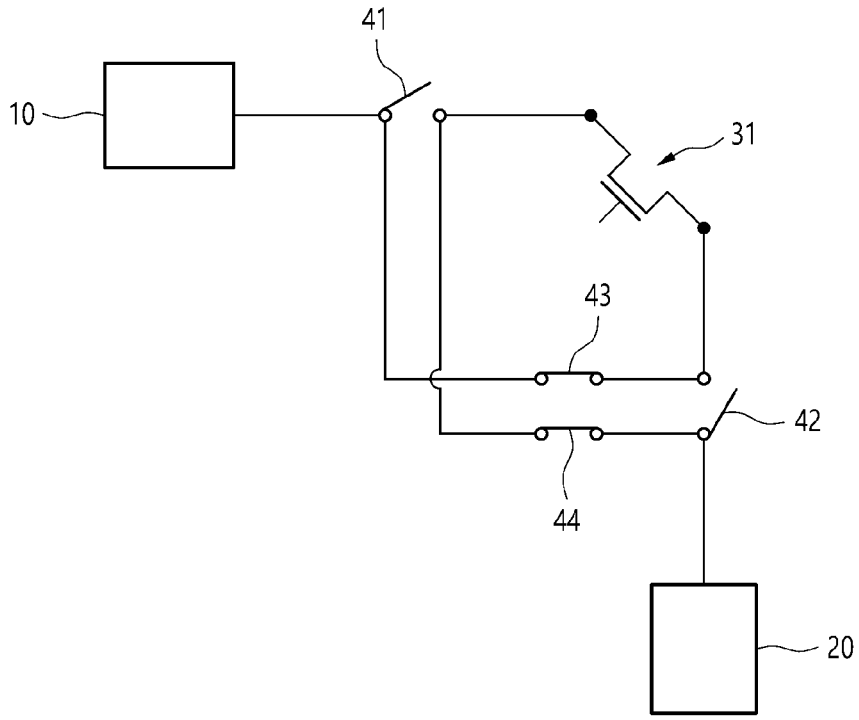


FIG. 7

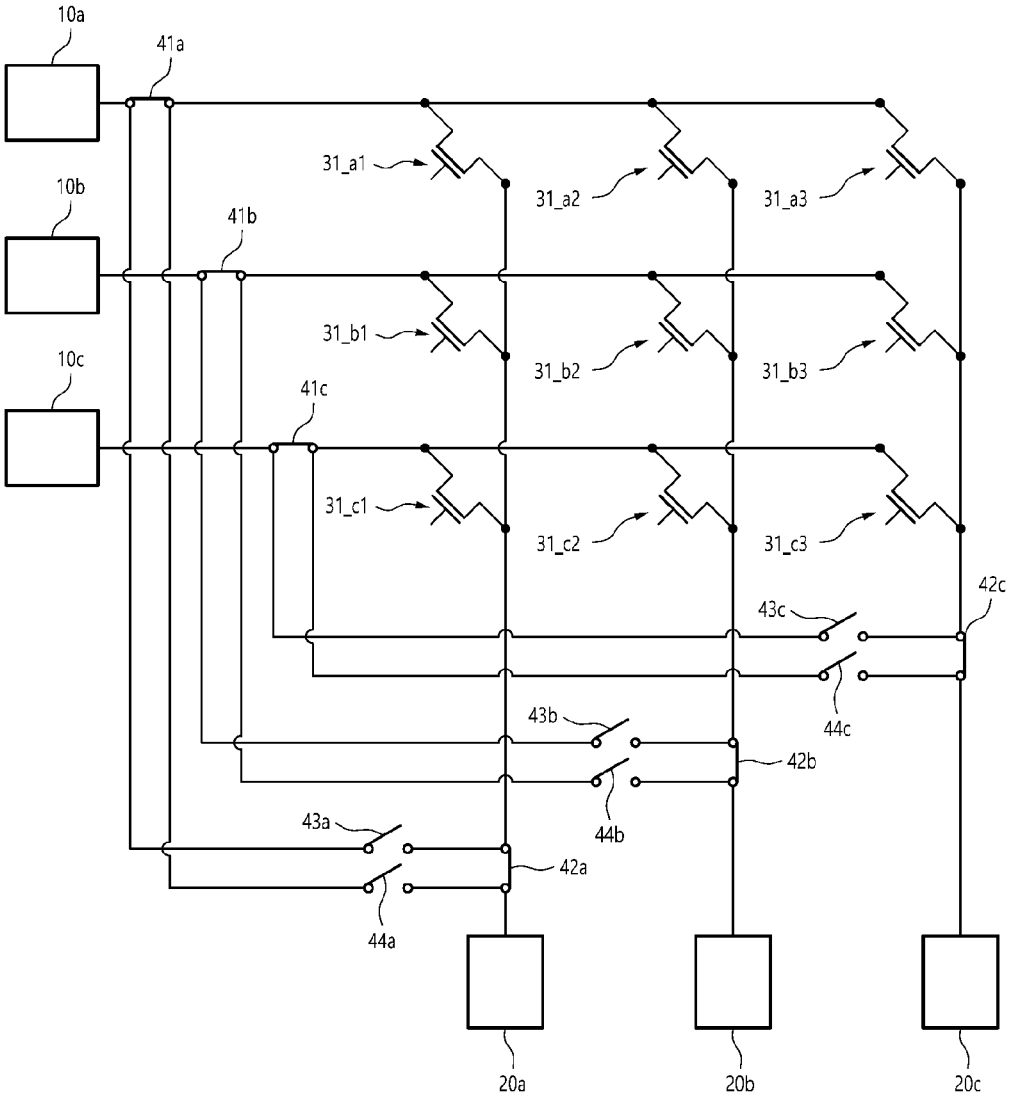
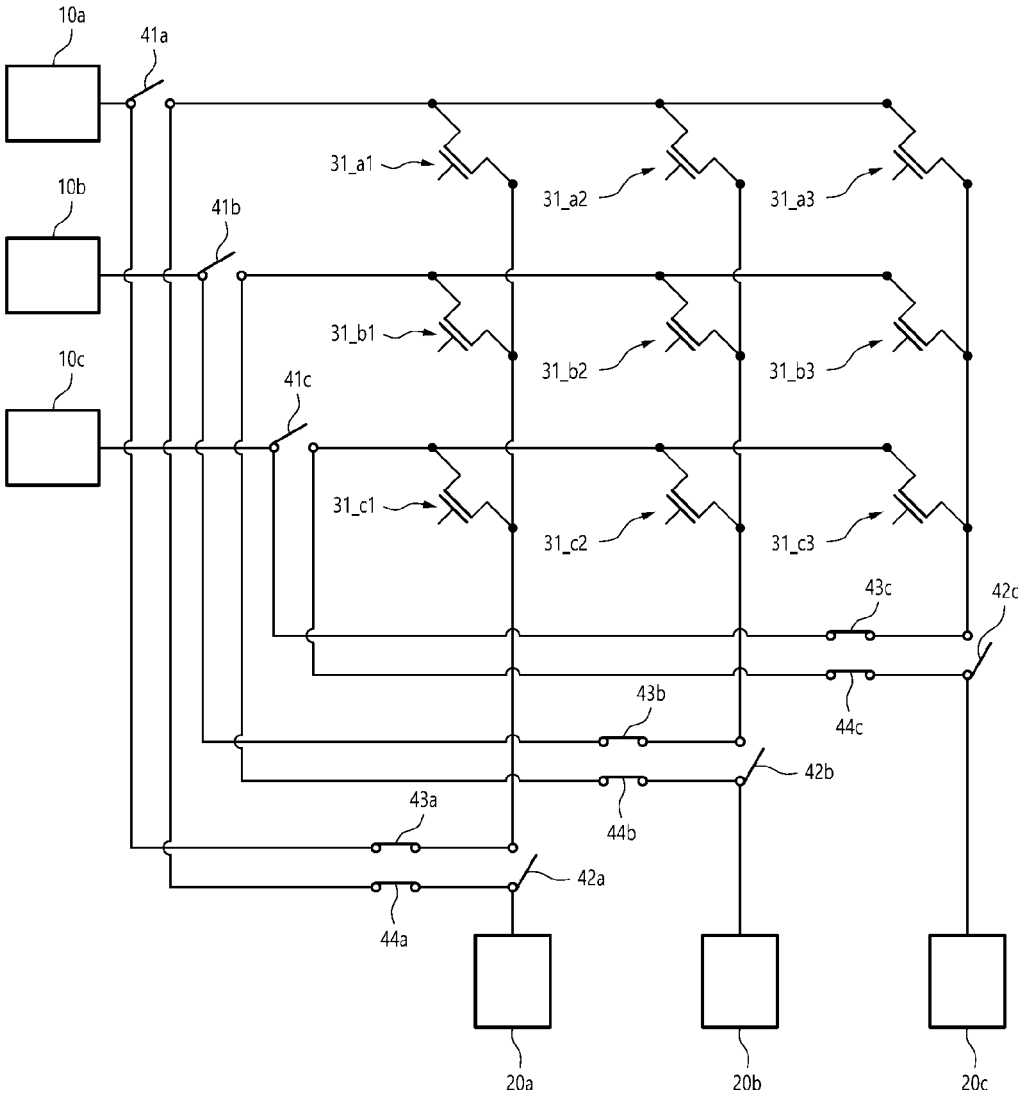

10a
41a
31_a1
31_a2
31_a3
10b
41b
31_b1
31_b2
31_b3
10c
41c
31_c1
31_c2
31_c3
42c
43c
44c
43b
42b
44b
43a
42a
44a
20a
20b
20c

FIG. 8


10a
41a
31_a1
31_a2
31_a3
10b
41b
31_b1
31_b2
31_b3
10c
41c
31_c1
31_c2
31_c3
43c
42c
44c
43b
42b
44b
43a
42a
44a
20a
20b
20c

NEUROMORPHIC CIRCUIT CAPABLE OF SETTING NEGATIVE WEIGHTS AND BACK PROPAGATION

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2021-0088327, filed on Jul. 6, 2021, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

1. Field of the Invention

[0002] The present disclosure relates to a neuromorphic circuit capable of setting back propagation and negative weights.

2. Discussion of Related Art

[0003] As the era of big data has opened, a variety of technologies have been introduced, and deep learning, machine learning, and artificial intelligence among the technologies have drawn attention. As such, with the advent of big data technologies, a large amount of data has been used for modeling and the accuracy and efficiency of artificial intelligence are increasing accordingly.

[0004] To this end, various techniques for effectively performing deep learning and artificial intelligence are being studied. In most technologies currently used, digital programming techniques using supercomputers are used and many studies are being conducted to apply the digital programming techniques in analog form.

[0005] In this regard, an integrated circuit has a variety of advantages in terms of a small size, high reliability, extension of functions, and costs and thus have been applied to various types of systems. At the present time, deep learning techniques implemented by supercomputers are disadvantageous in that high power consumption and large areas are necessary to run programs.

[0006] To remedy the disadvantage, a neuromorphic technology for emulating the neural structure of the brain to significantly reduce hardware size and power consumption is becoming an issue. A neuromorphic system implemented in an analog form can be highly integrated using a crossbar-array structure and thus has drawn a lot of attention as a neuromorphic hardware structure.

[0007] Operations of such a neuromorphic system are largely divided into two parts, i.e., training and inference. Inference is a process of deriving a result value from input data using a predetermined weight, and training is a process of inputting a large number of data sets and changing a weight by comparing a result output from the neuromorphic system with a predetermined answer.

SUMMARY OF THE INVENTION

[0008] The present disclosure is directed to providing a neuromorphic circuit capable of performing forward propagation or back propagation by controlling a direction of current flowing through a synapse module and setting negative weights by controlling a voltage to be applied to the synapse module.

[0009] An aspect of the present disclosure provides a neuromorphic circuit including an input module configured to generate an input voltage, an output module configured to measure a current transmitted from the input module and generate an output voltage, synapse modules configured to electrically connect the input module and the output module and determine a current to be transmitted to the output module, the synapse modules each including a memory element to which a weight is assigned, and a crossing module configured to control a direction of current flowing through the synapse modules.

[0010] The crossing module may include a first switch configured to connect the input module and one side of the synapse module, a second switch configured to connect the output module and the other side of the synapse module, a third switch configured to connect the input module and the other side of the synapse module, and a fourth switch configured to connect the output module and one side of each of the synapse modules.

[0011] The crossing module may be provided to operate in a forward propagation mode or a back propagation mode, wherein a current is set to flow through the synapse modules in a first direction in the forward propagation mode and to flow through the synapse modules in a second direction opposite to the first direction in the back propagation mode.

[0012] The crossing module may be provided to transmit a current to the output module according to a synapse module connected to a column line in the forward propagation mode and according to a synapse module connected to a row line in the back propagation mode.

[0013] When one or more input modules and a plurality of output modules are provided, the crossing module may be provided to select output modules, the number of which is equal to the number of the one or more input modules and to pair and connect the selected output modules and the one or more modules.

[0014] When one or more input modules and a plurality of output modules are provided, synapse modules may be arranged in row lines, the number of which is equal to the number of the one or more input modules, and arranged in column lines, the number of which is equal to the number of the plurality of output modules.

[0015] When the number of the column lines and the number of the row lines are equal to each other, weights assigned to one or more synapse modules arranged in one or more row lines of one of the column lines may be set to cross weights assigned to one or more synapse modules arranged in one or more row lines of another of the column lines.

[0016] When the number of the column lines is greater than the number of the row lines, the weights may be set to cross each other in column lines, the number of which is equal to the number of the row lines among the plurality of column lines.

[0017] An arbitrary weight may be assigned to the synapse modules in the column lines, the number of which is greater than the number of the row lines.

[0018] The number of the synapse modules arranged in the column lines may be less than or equal to the number of the synapse modules arranged in the row lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The above and other objects, features and advantages of the present disclosure will become more apparent to those of ordinary skill in the art by describing exemplary embodiments thereof in detail with reference to the accompanying drawings, in which:

[0020] FIG. **1** is a circuit diagram of a neuromorphic circuit according to an embodiment of the present disclosure;

[0021] FIGS. **2** to **4** are circuit diagrams of examples of a synapse module of FIG. **1**; and

[0022] FIGS. **5** to **8** are circuit diagrams of examples of a crossing module of FIG. **1**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0023] Hereinafter, the present disclosure will be described in detail with respect to embodiments thereof as examples with reference to the accompanying drawings. These embodiments will be described herein in sufficient detail to enable those of ordinary skill in the art to practice the present disclosure. It should be understood that various embodiments of the present disclosure are different from each other but need not be mutually exclusive. For example, specific shapes, structures and characteristics described herein may be implemented in different embodiments without departing from the spirit and scope of the present disclosure in connection with an embodiment. In addition, it should be understood that the position or arrangement of each element in each embodiment set forth herein may be changed without departing from the spirit and scope of the present disclosure. Therefore, the following detailed description is not intended to restrict the present disclosure, and the scope of the present disclosure should be limited only by the appended claims, including all ranges equivalent to that defined in the claims when appropriately described. In the drawings, like reference numerals represent the same or similar functions in various aspects.

[0024] Hereinafter, example embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

[0025] FIG. **1** is a circuit diagram of a neuromorphic circuit according to an embodiment of the present disclosure.

[0026] A neuromorphic circuit **1** may include an input module **10**, an output module **20**, a synapse module **30**, and a crossing module **40**.

[0027] The neuromorphic circuit **1** may include other components in addition to the components shown in FIG. **1** or may include only some of the components shown in FIG. **1**. Alternatively, at least two components in the neuromorphic circuit **1** may be integrated into one component that performs multiple functions. The above-described components will be described in detail below.

[0028] The input module **10** may generate an input voltage. Thus, the input module **10** may generate an input voltage to represent an input value to be used in a learning or inference process of the neuromorphic circuit **1**.

[0029] To this end, the input module **10** may be provided to generate different input voltages.

[0030] The output module **20** may measure a current transmitted from the input module **10** and generate an output voltage.

[0031] In this case, the output voltage of the output module **20** may be set to correspond to an input voltage during learning of the neuromorphic circuit **1**, so that the synapse module **30** may learn a weight.

[0032] The synapse module **30** may be provided with a memory element **31** and a weight may be assigned to the memory element **31**. The synapse module **30** may electrically connect the input module **10** and the output module **20** and determine a current to be supplied to the output module **20**.

[0033] Accordingly, the synapse module **30** may learn a weight so that output voltages corresponding to different input voltages may be generated by the output module **20**. Here, the learning of the weight by the synapse module **30** may be understood to mean that when different input voltages are input to the input module **10**, a weight is set so that output voltages corresponding to the different input voltages may be generated in the output module **20**.

[0034] For example, the synapse module **30** may set a weight by changing a resistance value of the memory element **31**. To this end, the synapse module **30** may set different levels of conductance and thus may be provided to memorize the set different levels of conductance. Examples of the synapse module **30** may include a phase change random access memory, a resistive random access memory, a ferroelectric random access memory (FRAM), a flash memory, etc.

[0035] Accordingly, the output module **20** may receive a current from the input module **10** according to a weight set in the synapse module **30** during the inferring process of the neuromorphic circuit **1** and generate an output voltage corresponding to the current.

[0036] In this case, the neuromorphic circuit **1** may include a plurality of synapse modules **30** to make more complicated calculations.

[0037] The crossing module **40** may control a direction of current flowing through the synapse module **30**. Thus, the neuromorphic circuit **1** may learn the weight of the synapse module **30** more accurately and quickly identify a synapse module **30** that malfunctions among a plurality of synapse modules **30** when an error occurs.

[0038] In this regard, the controlling of the direction of the current flowing through the synapse module **30** by the crossing module **40** may be understood to mean that the neuromorphic circuit **1** may be trained by forward propagation and back propagation.

[0039] In this case, the direction of the current flowing through the synapse module **30** described herein should be understood as being described based on a case in which an input voltage set for the input module **10** is higher than an output voltage set for the output module **20**.

[0040] However, such a criterion is merely provided to clearly describe forward propagation and back propagation, and therefore, it should be understood that an actual direction of current may be different from the direction of current set according to the criterion when an input voltage is lower than or equal to an output voltage during the training of the neuromorphic circuit **1** through forward propagation or back propagation according to an embodiment of the present disclosure.

[0041] FIGS. **2** to **4** are circuit diagrams of examples of the synapse module **30** of FIG. **1**.

[0042] Referring to FIG. **2**, one synapse module **30** is installed in the neuromorphic circuit **1**, and referring to FIG. **3**, a plurality of synapse modules **30** are installed in the neuromorphic circuit **1**.

[0043] In this regard, the synapse module **30** may be provided with one or more input modules **10** and a plurality of output modules **20**. In this case, synapse modules **30** may be arranged in row lines, the number of which is equal to the number of the one or more input modules **10** and in column

lines, the number of which is equal to the number of the plurality of output modules **20**.

[0044] Here, the row lines may be understood to mean rows of a matrix, and the column line may be understood to mean columns of the matrix.

[0045] In this case, the number of the synapse modules **30** arranged in the column lines may be less than or equal to the number of the synapse modules **30** arranged in the row lines.

[0046] In an example embodiment, the number of the synapse modules **30** arranged in the column lines may be equal to the number of the synapse modules **30** arranged in the row lines.

[0047] Referring to FIG. **4**, every two synapse modules **30** are paired and connected.

[0048] Here, the pairing and connection of every two synapse modules **30** may be understood to mean that a signal input to the synapse module **30** to determine a weight of the synapse module **30** is identically set for the other synapse modules **30**.

[0049] To this end, the synapse module **30** may include a signal generator to generate a signal to generate a weight and maintain the signal.

[0050] Accordingly, the pairing and connection of every two synapse modules **30** may be understood to mean that different synapse modules **30** are set to be assigned the same weight.

[0051] As described above, when the number of column lines and the number of row lines are equal to each other, weights of one or more synapse modules **30** arranged in one or more row lines of one of the column lines may be set to cross those of synapse modules arranged in one or more row lines of another of the column lines.

[0052] For example, as shown in FIG. **4**, when the neuromorphic circuit **1** is provided with two synapse modules **30** in a column line and two synapse modules **30** in a row line, i.e., a total of four synapse modules **30**, a first synapse module **31**_*a***1** and a fourth synapse module **31**_*b***2** may be paired and connected and a second synapse module **31**_*a***2** and a third synapse module **31**_*b***1** may be paired and connected.

[0053] As shown in FIG. **3**, when the neuromorphic circuit **1** is provided with three synapse modules **30** in a column line and three synapse modules **30** in a row line, i.e., a total of nine synapse modules **30**, a first synapse module **31**_*a***1**, a sixth synapse module **31**_*b***3**, and an eighth synapse module **31**_*c***2** may be paired and connected, a second synapse module **31**_*a***2**, a fourth synapse module **31**_*b***1**, and a ninth synapse module **31**_*c***3** may be paired and connected, and a third synapse module **31**_*a***3**, a fifth synapse module **31**_*b***2**, and a seventh synapse module **31**_*c***1** may be paired and connected.

[0054] When the number of column lines is greater than the number of row lines, weights may be set to be crossed for only column lines, the number of which is equal to the number of the row lines among the plurality of column lines.

[0055] When the number of column lines is greater than the number of row lines, the crossing module **40** may be provided to be connected only to the column lines, the number of which is equal to the number of the row lines among the plurality of column lines.

[0056] In this case, an arbitrary weight may be assigned to synapse modules **30** in column lines, the number of which is greater than the number of the row lines among the plurality of column lines.

[0057] FIGS. **5** to **8** are circuit diagrams of examples of the crossing module **40** of FIG. **1**.

[0058] The crossing module **40** may include a first switch **41**, a second switch **42**, a third switch **43**, and a fourth switch **44**.

[0059] The first switch **41** may be provided to connect the input module **10** and one side of the synapse module **30**, and the second switch **42** may be provided to connect the output module **20** and the other side of the synapse module **30**.

[0060] The third switch **43** may be provided to connect the input module **10** and the other side of the synapse module **30**, and the fourth switch **44** may be provided to connect the output module **20** and one side of the synapse module **30**.

[0061] Thus, the crossing module **40** may be provided to operate in a forward propagation mode in which a current is set to flow through the synapse modules **30** in a first direction and a back propagation mode in which a current is set to pass through the synapse modules **30** in a second direction opposite to the first direction.

[0062] For example, in FIG. **5**, the first direction may refer to a direction in which a current flows from an upper node of the memory element **31** to a lower node of the memory element **31**, and the second direction may refer to a direction in which a current flows from the lower node of the memory element **31** to the upper node of the memory element **31**.

[0063] However, it will be understood that the first direction and the second direction have been described herein based on a case in which the input voltage set for the input module **10** is higher than the output voltage set for the output module **20**, and thus, an actual direction of a current in the forward propagation mode may be different from the first direction when the input voltage is lower than or equal to the output voltage and an actual direction of a current in the back propagation mode may be different from the second direction when the input voltage is less than or equal to the output voltage.

[0064] When the crossing module **40** operates in the forward propagation mode, the first switch **41** and the second switch **42** may be turned on to be electrically connected and the third switch **43** and the fourth switch **44** may be turned off to be electrically disconnected.

[0065] When the crossing module **40** operates in the back propagation mode, the first switch **41** and the second switch **42** may be turned off to be electrically disconnected and the third switch **43** and the fourth switch **44** may be turned on to be electrically connected.

[0066] Accordingly, the crossing module **40** may be provided to supply a current to the output module **20** according to a synapse module **30** connected to a column line in the forward propagation mode, and supply a current to the output module **20** according to a synapse module **30** connected to a row line in the back propagation mode.

[0067] In this regard, FIG. **5** illustrates an example in which a neuromorphic circuit **1** with one synapse module **30** operates in the forward propagation mode, and FIG. **6** illustrates an example in which the neuromorphic circuit **1** with one synapse module **30** operates in the back propagation mode.

[0068] FIG. **7** illustrates an example in which a neuromorphic circuit **1** with nine synapse modules **30** operates in the forward propagation mode, and FIG. **8** illustrates an example in which the neuromorphic circuit **1** with nine synapse modules **30** operates in the back propagation mode.

[0069] In this case, a first output module **20***a* may be supplied with a current according to synapse modules **31**_*a***1**, **31**_*b***1**, and **31**_*c***1** connected to a first column line in the forward propagation mode, a second output module **20***b* may be supplied with a current according to synapse modules **31**_*a***2**, **31**_*b***2**, and **31**_*c***2** connected to a second column line in the forward propagation mode, and a third output module **20***c* may be supplied with a current according to synapse modules **31**_*a***3**, **31**_*b***3**, and **31**_*c***3** connected to a third column line in the forward propagation mode.

[0070] In addition, the first output module **20***a* may be supplied with a current according to synapse modules **31**_*a***3**, **31**_*a***2**, and **31**_*a***1** connected to a first row line in the back propagation mode, the second output module **20***b* may be supplied with a current according to synapse modules **31**_*b***3**, **31**_*b***2**, and **31**_*b***1** connected to a second row line in the back propagation mode, and the third output module **20***c* may be supplied with a current according to synapse modules **31**_*c***3**, **31**_*c***2**, and **31**_*c***1** connected to a third row line in the back propagation mode.

[0071] In this regard, a weight for the synapse module **30** may be set to be a negative weight when an input voltage set in an arbitrary input module **10** is lower than an output voltage set in an arbitrary output module **20**.

[0072] In this case, as described above, it may be understood that the synapse module **30** is paired and connected with a synapse module **30** arranged in a different column line and a different row line to set weights in a symmetrical structure, and therefore, a learning result of the synapse module **30** in the forward propagation mode and a learning result of the synapse module **30** in the back propagation mode may be the same when an input voltage and an output voltage are the same in the forward propagation mode and the back propagation mode.

[0073] As described above, an aspect of the present disclosure provides a neuromorphic circuit capable of setting back propagation and negative weights, and thus, a direction of a current flowing through a synapse module may be controlled to perform a forward propagation or back propagation operation and a voltage applied to the synapse module may be controlled to set negative weights.

[0074] While the present disclosure has been described above with respect to embodiments thereof, it will be understood by those of ordinary skill in the art that various changes and modifications may be made without departing from the spirit and scope of the present disclosure defined in the following claims.

What is claimed is:

1. A neuromorphic circuit comprising:

an input module configured to generate an input voltage;

an output module configured to measure a current transmitted from the input module and generate an output voltage;

synapse modules configured to electrically connect the input module and the output module and determine a current to be transmitted to the output module, the synapse modules each including a memory element to which a weight is assigned; and

a crossing module configured to control a direction of current flowing through the synapse modules.

2. The neuromorphic circuit of claim **1**, wherein the crossing module comprises:

a first switch configured to connect the input module and one side of the synapse module;

a second switch configured to connect the output module and the other side of the synapse module;

a third switch configured to connect the input module and the other side of the synapse module; and

a fourth switch configured to connect the output module and one side of the synapse module.

3. The neuromorphic circuit of claim **1**, wherein the crossing module is provided to operate in a forward propagation mode or a back propagation mode, wherein a current is set to flow through the synapse modules in a first direction in the forward propagation mode and to flow through the synapse modules in a second direction opposite to the first direction in the back propagation mode.

4. The neuromorphic circuit of claim **3**, wherein the crossing module is provided to transmit a current to the output module according to a synapse module connected to a column line in the forward propagation mode and according to a synapse module connected to a row line in the back propagation mode.

5. The neuromorphic circuit of claim **1**, wherein, when one or more input modules and a plurality of output modules are provided, the crossing module is provided to select output modules, the number of which is equal to the number of the one or more input modules and pair and connect the selected output modules and the one or more modules.

6. The neuromorphic circuit of claim **1**, wherein, when one or more input modules and a plurality of output modules are provided, synapse modules are arranged in row lines, the number of which is equal to the number of the one or more input modules, and arranged in column lines, the number of which is equal to the number of the plurality of output modules.

7. The neuromorphic circuit of claim **6**, wherein, when the number of the column lines and the number of the row lines are equal to each other, weights assigned to one or more synapse modules arranged in one or more row lines of one of the column lines are set to cross weights assigned to one or more synapse modules arranged in one or more row lines of another of the column lines.

8. The neuromorphic circuit of claim **6**, wherein, when the number of the column lines is greater than the number of the row lines, the weights are set to cross each other in column lines, the number of which is equal to the number of the row lines among the plurality of column lines.

9. The neuromorphic circuit of claim **8**, wherein an arbitrary weight is assigned to the synapse modules in the column lines, the number of which is greater than the number of the row lines.

10. The neuromorphic circuit of claim **6**, wherein the number of the synapse modules arranged in the column lines is less than or equal to the number of the synapse modules arranged in the row lines.

* * * * *