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(54) **Methods for enhancing the metal removal rate during the chemical-mechanical polishing process of a semiconductor**

Verbesserung der Metallentfernung bei einem chemisch-mechanischen Polierprozess eines Halbleiters

Procédé pour améliorer l'élimination d'un métal lors d'une étape de polissage méchano-chimique d'un semiconducteur

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## Description

BACKGROUND

1. Technical Field

**[0001]** Methods for enhancing the metal removal rate during chemical-mechanical polishing (CMP) of a semiconductor wafer are described herein. More particularly, the removal rate of a metal barrier layer on a semiconductor wafer is enhanced by employing a chelating agent in the chemical-mechanical polishing slurry during chemical-mechanical polishing of the semiconductor wafer.

2. Background of Related Art

**[0002]** Generally, semiconductor wafers include a plurality of circuits which form an integrated circuit. At some point when fabricating the integrated circuit on the semiconductor wafer, an oxide layer is formed on the wafer. Thereafter, the oxide layer is processed to pattern trenches or openings therein. Next, a metal barrier layer such as, for example, Ti/TiW, Ti/TiN or TaSiN is formed on the oxide layer by such techniques as physical vapor deposition (PVD) or chemical vapor deposition (CVD). Finally, a conductive layer, e.g., Al, W or Cu, will be deposited within the trenches or openings and over the top surface of the barrier layer. The semiconductor wafer is then polished to level its surface. During polishing, portions of the metal barrier layer and the conductive layer are removed from the top surface of the wafer.

**[0003]** One known polishing process is chemical-mechanical polishing (CMP) in which the semiconductor wafer is polished by employing a chemical-mechanical polishing apparatus. As seen in FIG. 1, a chemical mechanical polishing apparatus will ordinarily include a wafer carrier 15 for holding the semiconductor wafer 10. The wafer carrier 15 can be rotated during the polishing process by motor 17. CMP polishing platen 30, which carries the polishing pad 35, can be rotated by motor 37. The polishing slurry used during the process can be applied to polishing pad 35 via conduit 40.

**[0004]** Generally, the chemical-mechanical polishing process will involve holding the semiconductor wafer 10 against the rotating, wetted polishing surface of polishing pad 35. The polishing slurry is used to wet the polishing surface. The slurry may include a basic or acidic solution used as a chemical etch component in combination with an abrasive, such as alumina or silica particles. A rotating polishing head or the wafer carrier 15 is typically utilized to hold the wafer 10 against the rotating polishing platen 30 under controlled pressure. A backing film is optionally positioned between the wafer carrier 15 and the wafer. The polishing platen 30 is typically covered with a relatively soft wetted pad material such as blown polyurethane.

**[0005]** One drawback of the CMP process is that the different materials present at the surface of the wafer may polish at different rates. These different rates of removal can result simply from the different hardnesses of the materials or from different chemical interactions between the slurry and the materials. Thus, for example, the conductive layer may be easily removed by the abrasive action and an acidic slurry, while the metal barrier layer is not subject to such removal. This unwanted, excessive isotropic removal of the conductive metal layer can leave large metal areas "dished" toward the center. Thus, the goal of achieving a flat surface comprised of metal and insulator at various locations across the wafer surface is not achieved.

**[0006]** U.S. Patent No. 5,676,587 discloses a two step CMP process. The first step employs a standard alumina-based CMP slurry to remove the metal barrier layer and the conductive layer but stops before it reaches the oxide layer. The second step employs a neutral pH silica and water or silica-based CMP solution to remove the remainder of the metal barrier layer. WO 98/53488 A discloses a two step CMP process, wherein the second step uses the same slurry as in the first step to which $H_2O_2$ has been added.

**[0007]** It would be desirable to provide an easily implemented CMP method that substantially equalizes the removal rate of the metal barrier layer and the conductive layer from a semiconductor wafer during a chemical-mechanical polishing process to provide a flat surface comprised of metal and insulator regions across the surface of the wafer or alternately it would be desirable to provide a method of enhancing the removal rate of the metal barrier layer in the aforementioned two step CMP process.

SUMMARY OF THE INVENTION

**[0008]** A novel method for enhancing the removal rate of a metal barrier layer without affecting the removal rate of a conductive layer on a semiconductor wafer during CMP has been discovered which includes the steps of providing a semiconductor wafer and polishing the semiconductor wafer with a CMP slurry containing a metal removal-enhancing amount of a chelating agent.

**[0009]** The method involves providing a semiconductor wafer having an insulator layer, a metal barrier layer formed on at least a portion of the insulator layer and a conductive layer formed thereon and polishing the semiconductor wafer with a first CMP slurry and then polishing the semiconductor wafer with a second CMP slurry, wherein said first or said second slurry contains a metal removal-enhancing amount of a chelating agent.

**[0010]** The method is as exposed in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0011]**

FIG. 1 shows a schematic view of a CMP polishing apparatus in accordance with the prior art;

FIG. 2 is a cross-sectional view of an insulating layer with an opening formed therein on a semiconductor substrate with a metal barrier layer and conductive layer disposed thereover;

FIG. 3 shows a cross-sectional view of FIG. 2 after completion of the CMP process in accordance with this disclosure; and

FIG. 4 shows a cross-sectional view of FIG. 3 after completion of the touchup CMP process in accordance with this disclosure.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0012]** The novel methods described herein involve subjecting a semiconductor wafer having an insulator layer, a metal barrier layer formed on at least a portion of the insulator layer and a conductive layer formed thereon to a CMP process. These methods are based on the discovery that a CMP slurry containing a chelating agent will enhance the removal rate of the metal barrier layer without affecting the removal rate of the conductive layer during CMP.

**[0013]** Referring to FIG. 2, the method involves providing a semiconductor wafer 8 that is of the conventional type and may contain, for example, circuitry and other interconnection levels. Generally, the semiconductor wafer 8 will include a substrate 10 having an insulator layer 12 with an opening 25 formed therein. A metal barrier layer 14 is then formed on the surface of the insulator layer 12 and within opening 25 with a conductive layer 16 being deposited over the top surface of the metal barrier layer 14 and filling opening 25. Suitable materials for the three layers 12, 14 and 16 can include any conventional material known to one skilled in the art. Preferred materials include but are not limited to $SiO_2$, PSG or BPSG for insulator layer 12, Ti/TiN for metal barrier layer 14 and Al or Cu for conductive layer 16. Techniques and parameters for forming layers 12, 14 and 16 on substrate 10 (e.g., chemical vapor deposition, physical vapor deposition, time, temperature, thickness, etc.) are within the purview of one skilled in the art.

**[0014]** Opening 25 can be formed in insulator layer 12 by techniques known to those skilled in the art. For example, a resist layer (not shown) can be applied to the top surface of the insulator layer 12. The resist layer is patterned and developed using known photolithographic techniques. Then etching is conducted to form opening 25, such as, by employing a suitable anisotropic etching technique, e.g., reactive ion etching. A desired width of each opening 25 will normally vary according to the current-carrying requirements for a given conductor.

**[0015]** To carry out the novel methods described herein, the semiconductor wafer 8 is subjected to a standard CMP polishing process to advantageously remove the metal barrier layer 14 and the conductive layer 16 from the top surface of the insulator layer 12 to provide a substantially planar top surface of semiconductor wafer 8 as shown in FIG. 4. In general, a CMP slurry will be used during the polishing process to remove the metal barrier layer 14 and the conductive layer 16 from the wafer 8. The slurry can be any conventional CMP slurry known to one skilled in the art. A preferred slurry for use herein include any alumina or silica based slurry, which can be basic or acidic. Conditions such as the amount of pressure and rotation speeds of the polishing platen to be used during the CMP process are within the purview of one skilled in the art.

**[0016]** During the CMP polishing step, the metal barrier layer 14 polishes at a lower rate than the conductive layer 16. Thus, when the metal barrier layer 14 and conductive layer 16 are substantially removed, there can be residue of the metal barrier layer 14, e.g., Ti/TiN material, remaining on the top surface of insulator layer 12 (See FIG. 3). Accordingly, it may be necessary to conduct a second CMP processing step, generally referred to as a touchup CMP step, to remove any remaining residue from the top surface of the exposed insulator layer 12 and exposed conductive material in opening 25 to provide a substantially planar top surface of semiconductor wafer 8. (See FIG. 4).

**[0017]** When the CMP process is being utilized on wafer 8, a CMP slurry containing a metal removal-enhancing amount of a chelating agent is contacted with the top surface of the wafer 8, i.e., the conductive layer 16, either in the first CMP step or in the touchup CMP step. It is highly advantageous to employ a chelating agent since the chelator will not increase or decrease the pH of the slurry. The wafer 8 can be contacted with the chelator during the CMP process to substantially remove the metal barrier layer 14 and the conductive layer 16 as part of the CMP slurry or, alternatively, simultaneously with the CMP slurry during the touchup CMP step to remove any residue remaining on the top surface of wafer 8 as discussed hereinabove.

**[0018]** Chelating agents useful herein include aminocarboxylic acids such as ethylenediaminetetraacetic acid (EDTA), hydroxyethylethylenediaminetriacetic acid (HEDTA), nitrilotriacetic acid (NTA), N-dihydroxyethylglycine and ethylene bis(hydroxyphenylglycine) (EHPG); with ethylenediaminetetraacetic acid being more preferred.

**[0019]** The amount of chelators contacted with the wafer 8 should be a metal removal-enhancing amount. What constitutes a metal removal-enhancing amount of chelator will depend on a number of factors including, for example, the specific chelator used, the size of the wafer 8 and the composition and surface characteristics of the wafer 8. Typically, a metal removal-enhancing amount will ordinarily range from about 0.1 to about 30 weight percent, preferably from about 1 to about 20 weight percent, and more preferably from about 2 to about 10 weight percent. When employing the chelator in the CMP slurry to remove any remaining residue, the wafer 8 should be

contacted with the chelator slurry for a time period ranging from about 5 to about 300 seconds and preferably from about 20 to about 100 seconds. Though not critical, the wafer 8 should be contacted with the chelator slurry for a time ranging from about 5 to about 400 seconds, preferably from about 20 to about 300 seconds and more preferably from about 100 to about 200 seconds when removing the metal barrier layer 14 and conductive layer 16. The temperature during contact with the chelator slurry need not be precisely controlled, but normally can range from about 0°C to about 50°C and more preferably from about 10°C to about 20°C.

**Claims**

**1.** A method for enhancing the metal removal rate of a metal barrier layer during a chemical-mechanical polishing of a semiconductor wafer, comprising:

providing the semiconductor wafer having an insulator layer, a metal barrier layer formed on at least a portion of the insulator layer and a conductive layer formed thereon;
polishing the semiconductor wafer with a first chemical-mechanical polishing slurry; and
polishing the semiconductor wafer with a second chemical-mechanical polishing slurry,

wherein said first or said second chemical-mechanical polishing slurry contains a metal removal-enhancing amount of an aminocarboxylic acid in an amount from about 0.1 to about 30 weight percent.

**2.** The method of claim 1 wherein the insulator layer is $SiO_2$.

**3.** The method of claim 1 wherein the metal barrier layer is Ti/TiN.

**4.** The method of claim 1 wherein the conductive layer is selected from the group consisting of Al and Cu.

**5.** The method of one of claims 1 to 4, wherein the aminocarboxylic acid is selected from the group consisting of ethylenediaminetetraacetic acid, hydroxyethylenediaminetriacetic acid, nitrilotriacetic acid, N-dihydroxyethylglycine and ethylene bis (hydroxyphenylglycine).

**Patentansprüche**

**1.** Verfahren zum Verbessern der Metallabtragungsrate einer Metallbarrierenschicht beim chemisch-mechanischen Polieren eines Halbleiterwafers, das aufweist:

Bereitstellen des Halbleiterwafers mit einer Isolatorschicht, einer Metallbarrierenschicht, die auf mindestens einem Abschnitt der Isolatorschicht ausgebildet ist, und einer darauf ausgebildeten leitfähigen Schicht;
Polieren des Halbleiterwafers mit einer ersten chemisch-mechanischen Poliersuspension; und
Polieren des Halbleiterwafers mit einer zweiten chemisch-mechanischen Poliersuspension,
wobei die erste oder die zweite chemisch-mechanische Poliersuspension eine die Abtragung von Metall verbessernde Menge einer Aminocarboxylsäure in einer Menge von etwa 0,1 bis etwa 30 Gewichtsprozent enthält.

**2.** Verfahren nach Anspruch 1, wobei die Isolatorschicht $SiO_2$ ist.

**3.** Verfahren nach Anspruch 1, wobei die Metallbarrierenschicht Ti/TiN ist.

**4.** Verfahren nach Anspruch 1, wobei die leitfähige Schicht aus der Gruppe ausgewählt ist, die aus Al und Cu besteht.

**5.** Verfahren nach einem der Ansprüche 1 bis 4, wobei die Aminocarboxylsäure aus der Gruppe ausgewählt ist, die aus Ethylendiamintetraessigsäure, Hydroxyethylendiamiritriessigsäure, Nitrilotriessigsäure, N-Dihydroxyethylglycin und Ethylen-bis(hydroxyphenylglycin) besteht.

**Revendications**

**1.** Procédé pour améliorer le taux de dépose du métal d'une couche barrière en métal au cours d'un polissage mécano-chimique d'une tranche semi-conductrice, consistant à :

- fournir la tranche semi-conductrice ayant une couche d'isolant, une couche barrière en métal formée sur au moins une partie de la couche d'isolant et une couche conductrice formée sur celle-ci ;
- polir la tranche semi-conductrice avec une première pâte de polissage mécano-chimique ; et
- polir la tranche semi-conductrice avec une deuxième pâte de polissage mécano-chimique,

**caractérisé en ce que**
la première ou la deuxième pâte de polissage mécano-chimique contient une quantité d'acide aminocarboxylique améliorant la dépose du métal dans une quantité allant d'environ 0,1 à environ 30 % en poids.

**2.** Procédé selon la revendication 1, dans lequel la couche d'isolant est en $SiO_2$.

**3.** Procédé selon la revendication 1, dans lequel la couche barrière en métal est en Ti/TiN.

**4.** Procédé selon la revendication 1, dans lequel la couche conductrice est choisie dans le groupe constitué par l'A1 et le Cu.

**5.** Procédé selon l'une des revendications 1 à 4, dans lequel l'acide aminocarboxylique est choisi dans le groupe constitué par l'acide éthylènediaminetétraacétique, l'acide hydroxyéthylènediaminetriacétique, l'acide nitrilotriacétique, N-dihydroxyéthylglycine et éthylène bis-(hydroxyphénylglycine).

FIG. 1

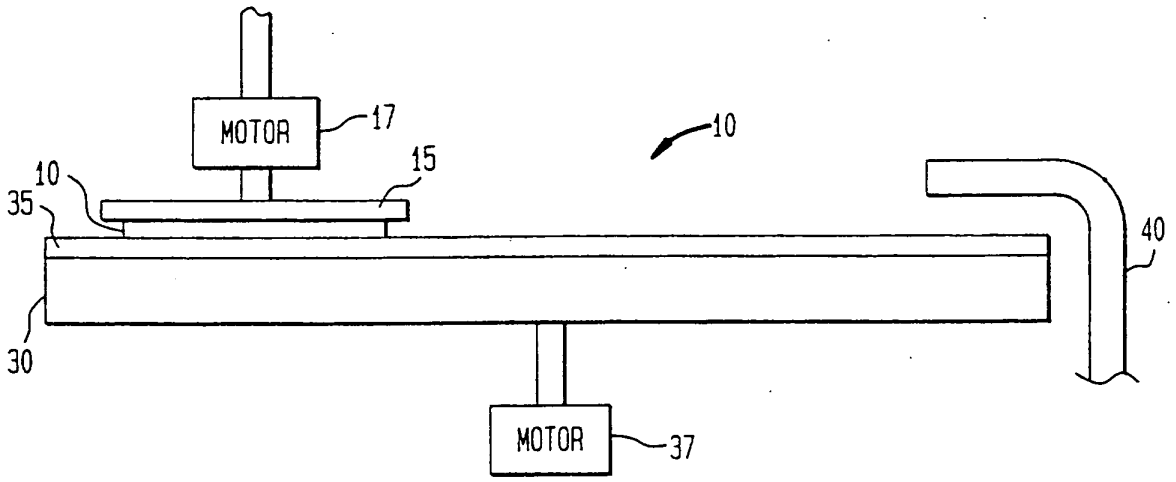


FIG. 2

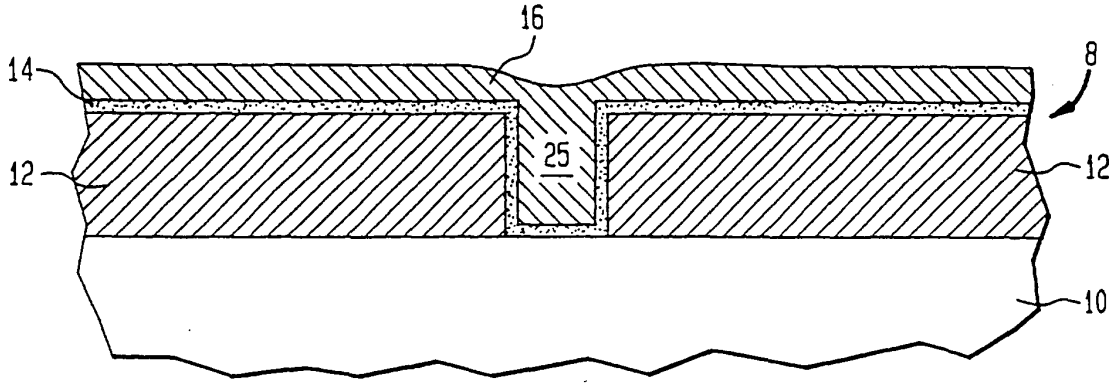



FIG. 3

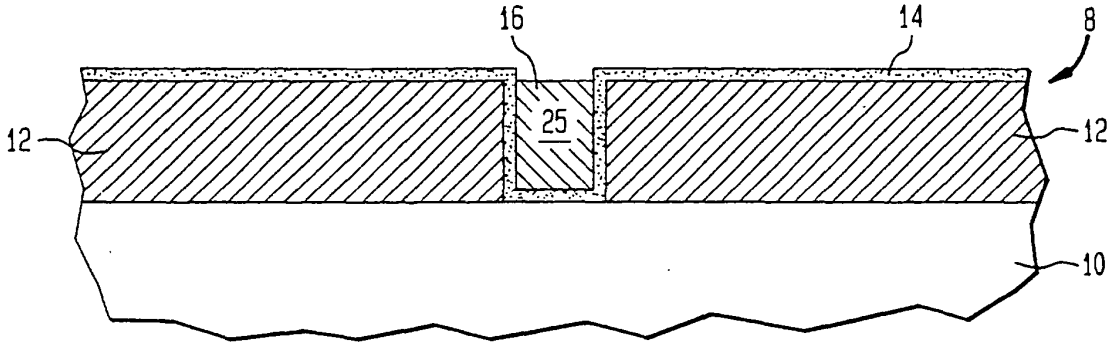
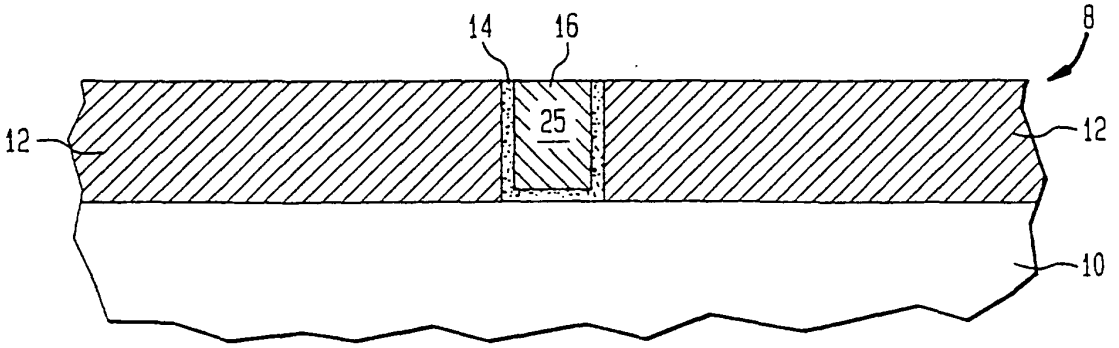



FIG. 4



## REFERENCES CITED IN THE DESCRIPTION

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