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(54) **SCALABLE ORTHOGONAL SPIN TRANSFER MAGNETIC RANDOM ACCESS MEMORY DEVICES WITH REDUCED WRITE ERROR RATES**

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CPC *H01L 43/02* (2013.01); *H01L 27/222* (2013.01)
USPC **365/158**

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USPC 365/171, 173; 257/421
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(57) **ABSTRACT**

A magnetic device includes a pinned polarizing magnetic layer having a magnetic vector parallel to a plane of the pinned polarizing magnetic layer. The magnetic device also includes a free layer, separated from the polarizing magnetic layer by a first non-magnetic layer, having a magnetization vector with a changeable magnetization direction. The changeable magnetization vector is configured to change to a first state upon application of a first current of a first polarity and to change to a second state upon application of a second current of a second, opposite polarity. The magnetic device also has a reference layer having a magnetic vector perpendicular to the plane of the reference layer and separated from the free layer by a second non-magnetic layer.

14 Claims, 7 Drawing Sheets

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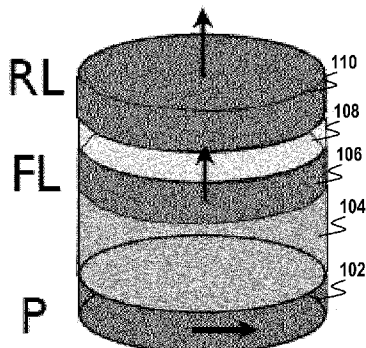
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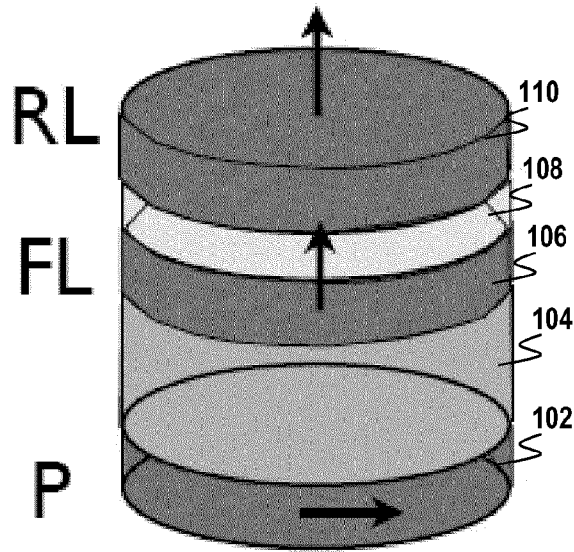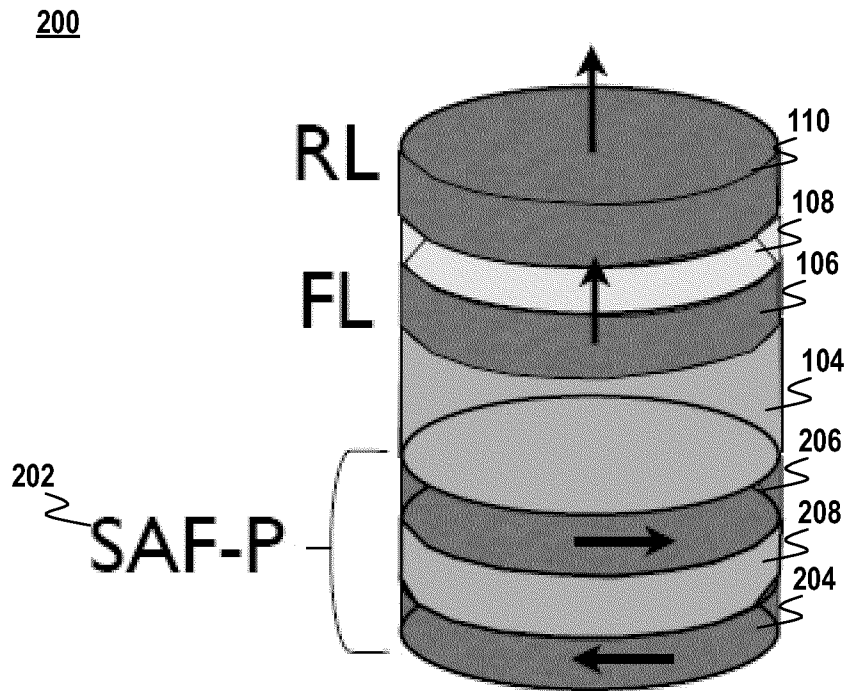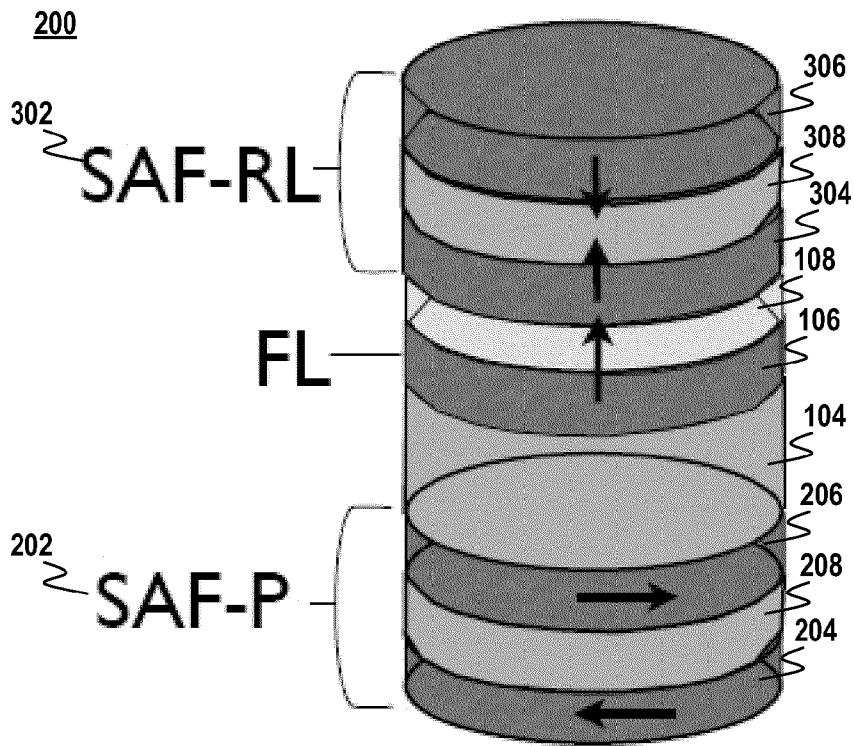
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100

RL

FL

P

110
108
106
104
102

Fig. 1

200

Fig. 2

200

302
SAF-RL

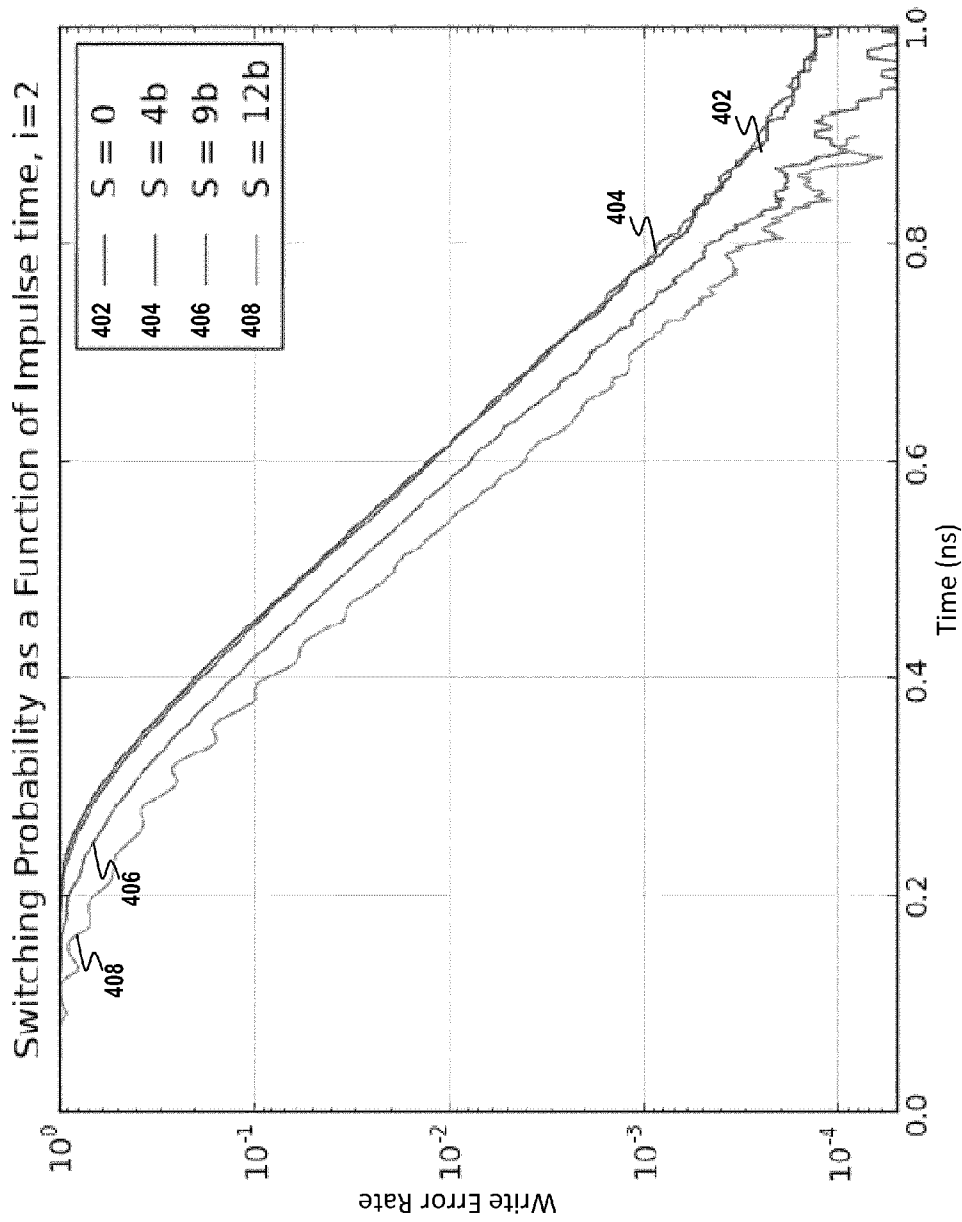FL

202
SAF-P

306
308
304
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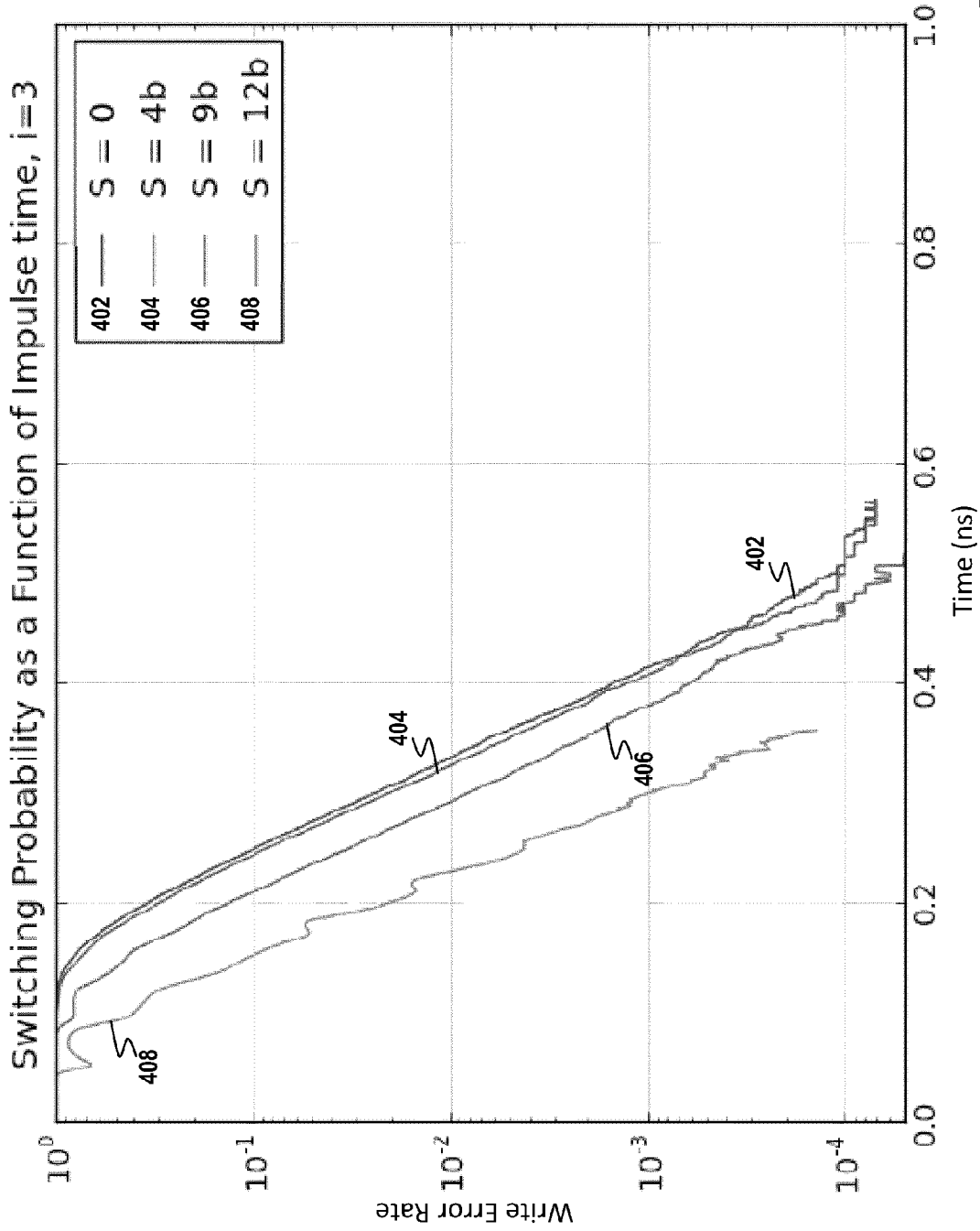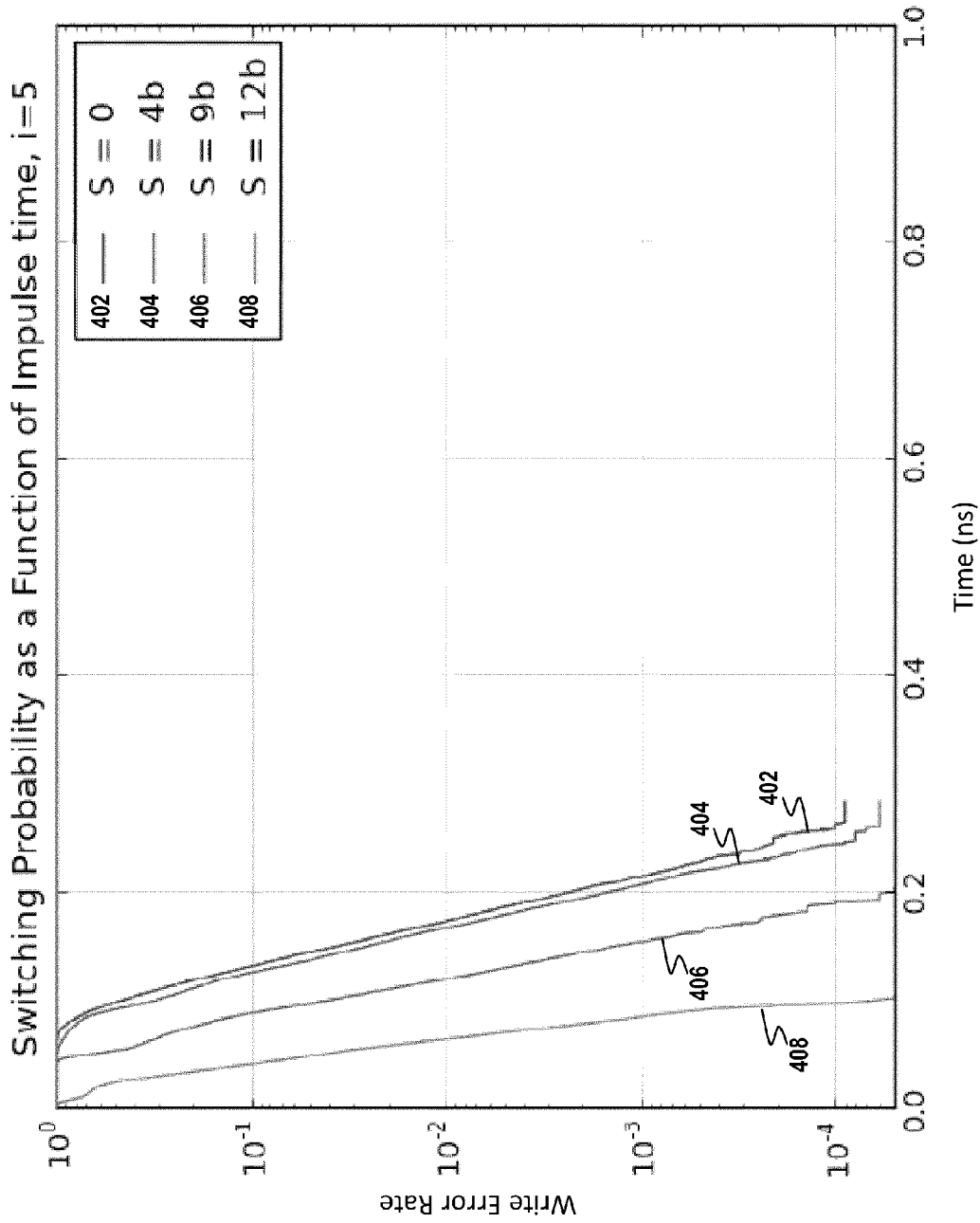106
104
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208
204

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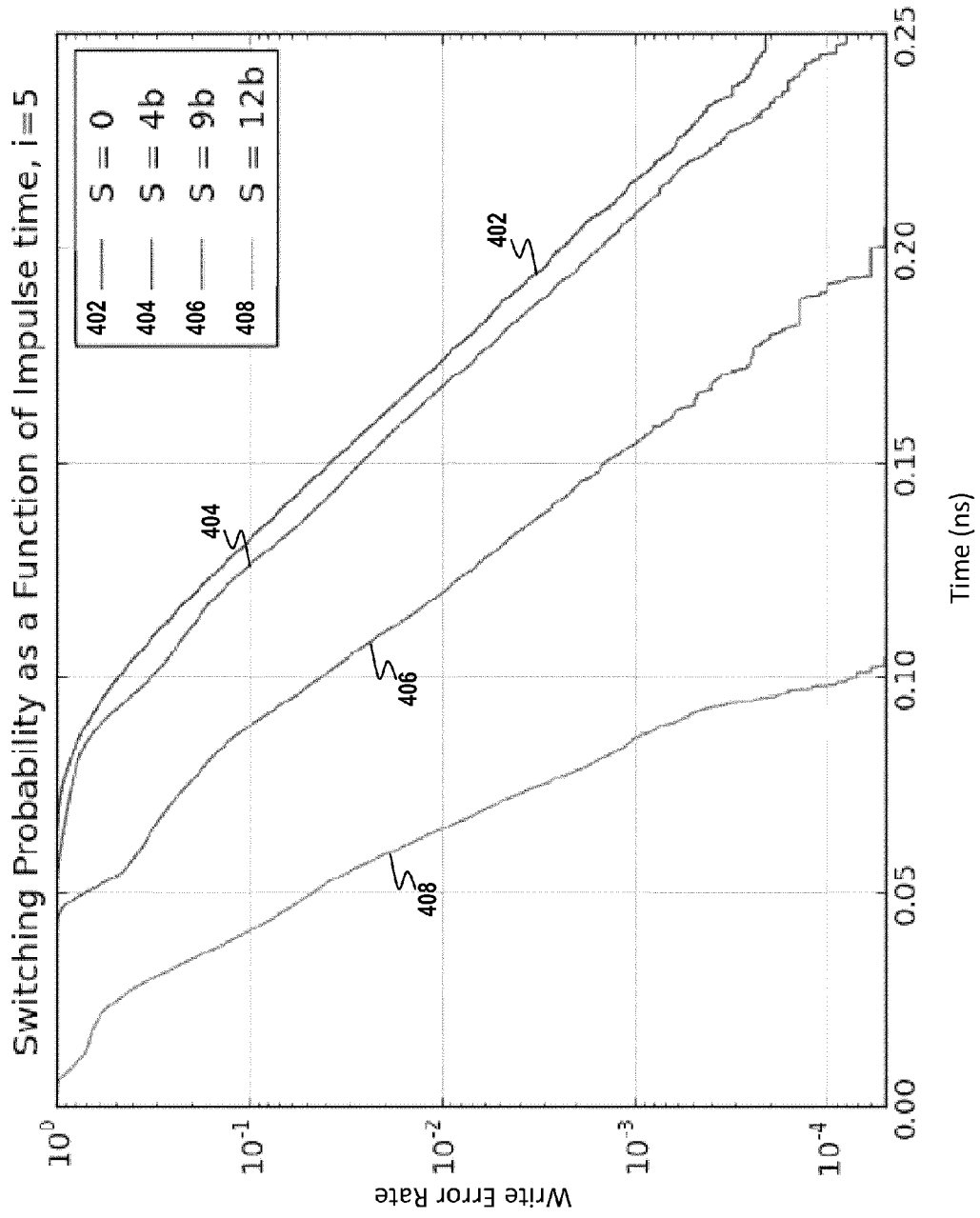
Fig. 4

Fig. 5

Fig. 6

Fig. 7

SCALABLE ORTHOGONAL SPIN TRANSFER MAGNETIC RANDOM ACCESS MEMORY DEVICES WITH REDUCED WRITE ERROR RATES

BACKGROUND

Orthogonal spin transfer magnetic random access memory devices offer fast (sub-nanosecond) initiations of the magnetization write process, combined with low energy operation. These devices employ at least two thin magnetic layers whose preferred magnetization directions are not oriented along the same axis (i.e. not collinear). This assures that a spin-transfer torque acts on a switchable magnetic layer (free layer) of the device when a write pulse (a voltage or current pulse) is applied to a device.

SUMMARY

In general, one aspect of the subject matter described in this specification can be embodied in a magnetic device includes a pinned polarizing magnetic layer having a magnetic vector parallel to a plane of the pinned polarizing magnetic layer. The magnetic device also includes a free layer, separated from the polarizing magnetic layer by a first non-magnetic layer, having a magnetization vector with a changeable magnetization direction. The changeable magnetization vector is configured to change to a first state upon application of a first current of a first polarity and to change to a second state upon application of a second current of a second, opposite polarity. The magnetic device also has a reference layer having a magnetic vector perpendicular to the plane of the reference layer and separated from the free layer by a second non-magnetic layer. Other implementations of this aspect include corresponding systems, memory arrays, and apparatuses.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, implementations, and features described above, further aspects, implementations, and features will become apparent by reference to the following drawings and the detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. Understanding that these drawings depict only several implementations in accordance with the disclosure and are, therefore, not to be considered limiting of its scope, the disclosure will be described with additional specificity and detail through use of the accompanying drawings.

FIG. 1 shows an orthogonal spin transfer magnetic random access memory device in accordance with an illustrative implementation.

FIG. 2 shows an orthogonal spin transfer magnetic random access memory device with a polarizing magnetic layer that includes a synthetic antiferromagnet layer in accordance with an illustrative implementation.

FIG. 3 shows an orthogonal spin transfer magnetic random access memory device with a reference layer that includes a synthetic antiferromagnet layer in accordance with an illustrative implementation.

FIG. 4 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i=I/I_{c0}=2$, a current amplitude of twice the threshold current in accordance with an illustrative implementation.

FIG. 5 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i=I/I_{c0}=3$ in accordance with an illustrative implementation.

FIG. 6 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i=I/I_{c0}=5$ in accordance with an illustrative implementation.

FIG. 7 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i=I/I_{c0}=5$ with an expanded×(time) axis, 0 to 0.25 ns in accordance with an illustrative implementation.

Reference is made to the accompanying drawings throughout the following detailed description. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. The illustrative implementations described in the detailed description, drawings, and claims are not meant to be limiting. Other implementations may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented here. It will be readily understood that the aspects of the present disclosure, as generally described herein, and illustrated in the figures, can be arranged, substituted, combined, and designed in a wide variety of different configurations, all of which are explicitly contemplated and made part of this disclosure.

DETAILED DESCRIPTION

An orthogonal spin transfer magnetic random access memory device generally consists of a polarizing magnetic layer oriented orthogonally to a free layer and includes a reference magnetic layer. These magnetic layers are separated by thin non-magnetic metallic or insulating layers. Described herein, are orthogonal spin transfer magnetic random access memory devices that can be reduced in lateral size to the nanometer scale, e.g., ~3 nanometers (nm), while maintaining the following characteristics for a memory devices: long term stability of the magnetic states used to represent data; reduced write error rates for short (sub nanosecond) write pulses; and reduced interaction between magnetic devices in a densely packed memory array. In some described implementations, an orthogonal spin transfer magnetic random access memory device uses balanced switching currents such that the switching currents for writing "1" and "0" states are of similar magnitude. Multiple stable states of the free layer can be envisioned that would enable one device to store more than one bit of information.

In some implementations, a memory device can be configured such that the write current polarity determines the bit state, e.g., a positive polarity pulse for a sub-nanosecond duration sets the "1" state and a negative polarity pulse for a sub-nanosecond duration sets the "0" state. In one implementation, the memory device shape can have a circular cross-section. In contrast, when the free layer is magnetized in-plane the free layer must have an asymmetric shape, because magnetic shape anisotropy is used to stabilize the magnetic states (i.e. to set energy barrier separating the "left" and "right" magnetized magnetic states of the free layer.) Each layer is thin enough that it can be referred to as a plane. Accordingly, a magnetization field that is "in-plane" means a magnetization field that is parallel to the layer. As an example, the perpendicular polarizer 102 in FIG. 1 is in-plane. An advantage of having a device with a circular shape is that circles are far easier to fabricate than asymmetric shapes.

The orthogonal spin transfer magnetic random access memory device disclosed herein can employ a free layer with a large perpendicular magnetic anisotropy (PMA). The polarizing layer is magnetized in-plane, and thus provides an initial spin-transfer torque perpendicular to the preferred magnetization direction of the free layer the instant the device is energized with a write pulse. The perpendicular anisotropy of

the free layer is sufficient that the free layer's lateral extend can be just 3 nm. That is, the free layer can be a thin film that is circular in cross-section and 3 nm in diameter and a few nanometers thick (0.8 to 3 nm), while still being substantially stable against random thermal fluctuations. The condition for stability is that the energy barrier to reverse the magnetization direction K be much greater than the thermal energy k_BT, $K/k_BT>60$, where T is the device operating temperature, typically less than 450 K and k_B is Boltzmann's constant.

FIG. 1 shows an orthogonal spin transfer magnetic random access memory device 100 in accordance with an illustrative implementation. From bottom to top: there is an in-plane magnetized polarizing layer (P) 102, a non-magnetic layer (NM1-metallic or thin insulator) 104, the free layer (FL) 106 which has stable (storage) magnetic states oriented perpendicular to the plane of the layer, either up or down, a thin insulating layer 108, also called a tunnel barrier (NM2), and a reference layer (RL) 110 that is magnetized perpendicular to the plane of the layer. The in-plane magnetized polarizing layer 102 has a magnetic state that is oriented parallel to the plane of the layer. This layer 102 can be pinned, such that the magnetic state remains parallel to the plane of the layer when current or voltage is applied to the device.

FIG. 2 shows a device 200 with a polarizing magnetic layer (P) that includes a synthetic antiferromagnet (SAF) layer 202. The SAF layer 202 has two magnetic layers 204 and 206 that are separated by a non-magnetic metallic later 208. The magnetic layers 204 and 206 interact antiferromagnetically and thus form magnetic states with their magnetizations oriented opposite to one-another. One of the magnetic layers 204 (the lower one in FIG. 2—but, in general, the one that is furthest from the FL 106) can be placed into contact with an antiferromagnetic to pin (i.e. set) the direction of this magnetic layer 204. The magnetic layers 204 and 206 can be coupled antiferromagnetically. Then the magnetization direction of the magnetic layer 206 will be antiparallel to the magnetization of magnetic layer 204. Note while the polarizer 202 is indicated as being on the bottom of the layer stack 200, the stack can in inverted without changing any essential aspect of this invention disclosure.

FIG. 3 shows a device 300 with a reference magnetic (RL) layer 302 that consists of a synthetic antiferromagnet (SAF) layer. The SAF layer 302 has two perpendicularly magnetized layers 304 and 306 that are separated by a non-magnetic metallic later 308. The magnetic layers interact antiferromagnetically and thus form states in which the layer magnetizations are oriented opposite to one-another. One of the magnetic layers 306 (the upper one in FIG. 3—but, in general, the one that is furthest from the FL) can be put in contact with an antiferromagnetic that can be used to pin (i.e. set) the direction of this magnetic layer 306. The antiferromagnetic layer, however, is not needed for a perpendicularly magnetized SAF. That is, the antiferromagnetic layer is not required to pin the direction of the magnetic layer 306, because the magnetic anisotropy of the layers 302 can be sufficient to fix the magnetization directions of these layers 302.

The layer structures shown in FIGS. 2 and 3 can be used to optimize device preference. First, the SAF layers 202 and/or 302 allow the magnetic interactions between these layers 202 and/or 302 and the free layer 106 to be configured for various performance needs. The SAF RL structure (the thicknesses of the magnetic and non-magnetic layers comprising the SAF) can be used to produce a magnetic field that acts on the free layer 106. This magnetic field can balance the switching currents for anti-parallel (AP) to parallel (P) and P to AP. For example, if the switching current is larger for the P to AP transition then the magnetic field from the RL SAF can be set to be parallel to FL magnetization in the AP state. This can be accomplished by making the magnetic layer 304 in proximity to the free layer 106 within the SAF RL 302 thinner or of a

lower magnetization density material than the other magnetic layer 306 in the SAF. In this implementation, the amplitude and the switching current can be significantly the same for switching the device from P to AP and also from AP to P. The currents are significantly the same when only the current polarity needs to be reversed between switching from P to AP and AP to P. The current magnitude can be the same. This enables use of the same driving circuits for switching from P to AP and from AP to P. In these implementations, the polarity of the current determines the device state.

As an example of balancing the switching currents, the SAF RL structure can have a preference for the P state of the device. Accordingly, less current is needed to switch to the P state compared to switching to the AP state. To balance the current, such that the same amount of current is needed to switch to either state, the SAF RL layer can be modified in various different wants. These modifications introduce some asymmetry in the SAF RL layer. In one implementation, the magnetic layer 306 can be made thicker. In other implementations, the magnetic layer 304 can be made thinner and/or can be made of a material with a lower magnetic moment density. Two or more of these changes can be made to a single device to balance the switching currents. An initial SAF-RL that would have a preference for the P state of the device consists of magnetic layers 304 and 306 with the same or significantly similar magnetization densities but with layer 304 being thicker than layer 306. Each layer, for example could be composed of [0.3 nm Co/0.9 nm Pt] units repeated N1 times for layer 304 and N2 times for layer 306 with N1 greater than N2. A modified SAF-RL would have layer 306 thicker than layer 304 or, as in the [0.3 nm Co/0.9 nm Pt] example given above, N2 would be greater than N1. In the modified SAF-RL the net magnetic field acting on layer FL 106 would be opposite the direction of the magnetization of layer 304 and thus favor the AP state. Another example would have layers with different magnetization densities but with similar thicknesses. Layer 304 could be composed of [0.3 nm Co/0.9 nm Pt]×N while layer 306 could be composed of [0.5 nm Co/0.8 nm Pt]×N (with "×N" meaning the that bilayer of Co/Pt is repeated N times). As the magnetization density [0.5 nm Co/0.8 nm Pt] is larger than that of [0.3 nm Co/0.9 nm Pt] this modified SAF-RL would lead to a net field on FL layer 106 that is opposite the magnetization of layer 304 thus favoring the AP state of the device. Having the switching currents balanced allows for reduced complexity in the driving circuitry.

The devices of various implementations are scalable because the free layer consists of a thin film material with a large perpendicular magnetic anisotropy (PMA). The energy barrier that determines the stability of the magnetic storage states is proportional the magnetic anisotropy and the volume of the element. The larger the magnetic anisotropy the smaller the volume of the element can be. For fixed element thickness (~2 nm) this means that the lateral size of the element can be reduced. Examples of materials with large perpendicular magnetic anisotropy are FeCoB in contact with MgO (due to an interface PMA at the FeCoB/MgO interface). Fe/Pt, Co/Ni, Fe/Pd, Fe/Pt, Co/Pt and CoPd multilayers. The hard-disk industry uses CoFeCr alloys as the media which have large PMA. FePt when formed in the L10 phase has among the highest PMA of any transition metal magnet. For example, with the PMA of FePt L10 multilayers, elements that are 2 nm in thickness and 3 nm in diameter are thermally stable, i.e. have energy barriers K to magnetization reversal greater than $60k_BT$ (K>60 times the thermal energy at room temperature (T=300 K)).

Multiple devices can be integrated into a memory array capable of storing multiple bits of data. For example, multiple devices can be grown together on a single chip that can be used as memory to store data.

Physical Model of Device

The magnetization dynamics of the device of one implementation can be modeled to a good approximation by considering the spin transfer torques associated with the perpendicular polarizer and the reference layer as follows:

$$\frac{d\hat{m}}{dt} = -\gamma\mu_0\hat{m} \times \vec{H}_{eff} + \alpha\hat{m} \times \frac{d\hat{m}}{dt} + \sin(S)\gamma a_J\hat{m} \times (\hat{m} \times \hat{m}_P) - \cos(S)\gamma a_J\hat{m} \times (\hat{m} \times \hat{m}_R)$$

(Eqn. 1)

(Eqn. 1), where m represents the magnetization direction of the free layer (it is a unit vector in the direction of the free layer magnetization), and α is the damping parameter of the free layer. The prefactor, a_J, depends on the current density J, the spin-polarization P of the current density J, and the cosine of the angle between the free and pinned magnetic layers, $\cos(\theta)$, such that $a_J = \hbar Jg(P,\cos(\theta))/(2eMt)$, where h is the reduced Planck's constant, g is a function of the spin-polarization P and $\cos(\theta)$, M is the magnetization density of the free layer, e is the electron charge, and t is the thickness of the free layer. The last two terms are the spin transfer from the in-plane polarizer (m_P) and the perpendicular magnetized reference layer (m_R). $\tan(S)$ represents the ratio of the magnitude of these two spin transfer torques.

The magnetic energy of the free layer is given by:

$$U(m) = -K[(\hat{n}_K \cdot m)^2 + 2h \cdot m]$$

(Eqn. 2)

where $h = H_{ext}/H_K$ is the reduced applied field and HK is the anisotropy field given by the relation: $K = (\frac{1}{2})M_S V H_K$. n_K is a unit vector in the direction of the magnetic easy axis of the FL, i.e. perpendicular to the layer plane.

And the effective field in Eqn. 1 is derived from Eqn. 2 as follows:

$$H_{eff} = -\frac{1}{M_S V}\nabla_m U(m) = H_k[(\hat{n}_k \cdot m)\hat{n}_k + h].$$

(Eqn. 3)

Analysis of Eqns. 1 to 3 shows that there is a threshold current for the switching of the magnetization direction from aligned parallel to the direction $\hat{n}_K$ to antiparallel to $\hat{n}_K$ and vice-versa. For currents larger than or equal to this threshold value, the initial magnetization state is unstable and will eventually decay into the complementary state. The larger the current above this threshold value the faster the magnetization decay rate. Fast device writing generally requires currents larger than the threshold value. The decay rate is increased in the presence of thermal noise, which can aid the write process.

Threshold values of the current are given by:

$$I_{c0} = \frac{2e}{\hbar}\frac{\alpha}{P}K,$$

(Eqn. 4)

for $g(P,\cos(\theta)) = P$, that is the function g is a constant equal to P, the spin polarization of the current. In general I_{co} will depend on the form of the function g. When g depends on the angle θ there can be different threshold currents for switching from P to AP and AP to P.

In order to describe the device writing process, thermal fluctuations of the magnetization must be included in the physical model of the device. This is included by adding a Langevin field to the effective field:

$$H_{eff} \rightarrow H_{eff} + H_{th}$$

(Eqn. 5),

where H^{th} is a Gaussian distributed random magnetic field that represents the thermal noise associated with the switchable layer being at a temperature T:

$$\langle H_{th}\rangle = 0$$

$$\langle H_{th,i}(t)H_{th,k}(t')\rangle = 2D\delta_{i,k}\delta(t-t')$$

(Eqn. 6a and 6b).

The quantity D is given by:

$$D = \frac{ak_B T}{2K(1+a^2)} = \frac{a}{2(1+a^2)\xi}.$$

(Eqn. 7)

The value ξ is introduced as $K/k_B T = \xi$, so that ξ is the ratio of the energy barrier to the reversal of the magnetization divided by the thermal energy. As noted above, ξ is typically larger that 60 for long term stability of the device memory states.

The write error rate of the device can be determined by solving the stochastic differential equations (Eqn. 1 to 7) numerically using parallel computational methods based in graphical processing units simulated in parallel on an NVidia Tesla C2050 graphics card. The large number of necessary random numbers were generated by employing a combination of the three-component combined Tausworthe "taus88" 16 and the 32-bit "Quick and Dirty" LCG17.

FIGS. 4-7 show the results of these calculations and methods to optimize device performance. FIG. 4 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i = 1/1_{c0} = 2$, a current amplitude of twice the threshold current. Results are shown for different ratios of the spin transfer torques from the polarizer and reference layer, the parameter S. Larger values of S give a reduced WER. For example, for a 1 ns pulse the WER can be reduced by a factor of 5 by increasing S from 0 to 9b, where b is $\pi/36$.

FIG. 5 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i = 1/1_{co} = 3$.

FIG. 6 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i = 1/1_{co} = 5$.

FIG. 7 shows the write error rate (WER) as a function of pulse duration for a pulse amplitude $i = 1/1_{co} = 5$ with an expanded×(time) axis, 0 to 0.25 ns.

These results show that increasing S can greatly reduce the WER for sub-1 ns pulses. The effect is very significant as the current pulse amplitude is increased. For example, for $i = 3$ the WER can be reduced by a factor of 30 for pulses between 0.1 and 1 ns when S is increased from 0 to 12b. For $i = 5$ the WER is reduced by a factor of 10,000 for the same time range when S is increased from 0 to 12b. These are very significant effects and reducing the WER at these time scales can reduce a memory array's complexity (for example, less error correction circuitry is needed in the memory array).

Having a free layer that is perpendicular to the plane of the device, as shown in FIGS. 1-3, eliminates or greatly reduces the precessional switching of device's state that can occur at high currents. In some orthogonal spin transfer magnetic random access memory devices, when a sufficiently large current or voltage is applied, the spin-transfer torque of the polarizer can lead to a torque that rotates the free layer magnetization out of the free layer's plane. This can then produce a demagnetization field perpendicular to the free layer's plane around which the free layer magnetization precesses. Precession can occur for both signs of the current, since in both cases the free layer magnetization is tilted out of the free layer's plane. The free layer magnetization rotation about its demagnetizing field will result in a switching probability of the free layer's magnetic state that is a nonmonotonic function of the pulse amplitude or duration, since if the pulse ends after the free layer magnetization finishes a full rotation (i.e., a 2π rotation), the probability of switching will be reduced. Eliminating or greatly reducing precessional switching means the magnetic state of the free layer will not precess. Accordingly,

the timing of the current pulse is not required to be as exact as compared to the timing requirements when precessional switching can occur, e.g., when the magnetization vector of the free layer is parallel to the plane of the free layer.

While this specification contains many specific implementation details, these should not be construed as limitations on the scope of any inventions or of what may be claimed, but rather as descriptions of features specific to particular implementations of particular inventions. Certain features described in this specification in the context of separate implementations can also be implemented in combination in a single implementation. Conversely, various features described in the context of a single implementation can also be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Thus, particular implementations of the subject matter have been described. Other implementations are within the scope of the following claims.

What is claimed is:

1. A magnetic device comprising:
a pinned polarizing magnetic layer having a magnetic vector parallel to a plane of the pinned polarizing magnetic layer;
a free layer, separated from the polarizing magnetic layer by a first non-magnetic layer, having a magnetization vector with a changeable magnetization direction, wherein the changeable magnetization vector has a state that changes to a first state upon application of a first current of a first polarity and that changes to a second state upon application of a second current of a second, opposite polarity; and
a reference layer having a magnetic vector perpendicular to the plane of the reference layer and separated from the free layer by a second non-magnetic layer, wherein the reference layer and the pinned polarizing magnetic layer balances is an amplitude of current required to change the changeable magnetization vector state such that the amplitude of the first current is significantly the same as the amplitude of the second current, and wherein the reference layer comprises:
a first magnetic layer that has a first magnetization vector oriented perpendicular to the first magnetic layer; and
a second magnetic layer, separated from the first magnetic layer by a reference layer non-magnetic layer, that has a second magnetization vector oriented perpendicular to the second magnetic layer and opposite of the first magnetization vector, wherein widths of the first magnetic layer and the second magnetic layer are different and balance the amplitude of current required to change the changeable magnetization vector state.

2. The magnetic device of claim 1, wherein the magnetic device is between 3 nanometers and 10 nanometers in height.

3. The magnetic device of claim 1, wherein the changeable magnetization vector changes to the first state based upon a pulse of the first current between 0.1 nanoseconds and 0.8 nanoseconds.

4. The magnetic device of claim 3, wherein the changeable magnetization vector changes to the second state based upon a pulse of the second current between 0.1 nanoseconds and 0.8 nanoseconds.

5. The magnetic device of claim 4, wherein the pinned polarizing magnetic layer has a first spin torque and the reference layer has a second spin torque, and wherein a ratio of the first spin torque and the second spin torque reduces write error rates.

6. The magnetic device of claim 5, wherein the ratio of the first spin torque and the second spin is between 0.36 and 1.8.

7. The magnetic device of claim 1, wherein the magnetic device has a circular cross section.

8. A memory array comprising:
a plurality of memory cells, wherein each memory cell comprises:
a pinned polarizing magnetic layer having a magnetic vector parallel to a plane of the pinned polarizing magnetic layer;
a free layer, separated from the polarizing magnetic layer by a first non-magnetic layer, having a magnetization vector with a changeable magnetization direction, wherein the changeable magnetization vector changes to a first state upon application of a first current of a first polarity and to change to a second state upon application of a second current of a second, opposite polarity; and
a reference layer having a magnetic vector perpendicular to the plane of the reference layer and separated from the free layer by a second non-magnetic layer, wherein the reference layer and the pinned polarizing magnetic layer balances an amplitude of current to change the changeable magnetization vector state such that the amplitude of the first current is the same as the amplitude of the second current, and wherein the reference layer comprises:
a first magnetic layer has a first magnetization vector oriented perpendicular to the first magnetic layer; and
a second magnetic layer, separated from the first magnetic layer by a reference layer non-magnetic layer, has a second magnetization vector oriented perpendicular to the second magnetic layer and opposite of the first magnetization vector, wherein widths of the first magnetic layer and the second magnetic layer are different and balance the amplitude of current required to change the changeable magnetization vector state.

9. The memory array of claim 8, wherein each of the memory cells is between 3 nanometers and 10 nanometers in height.

10. The memory array of claim 8, wherein the changeable magnetization vector of each of the memory cells changes to the first state based upon a pulse of the first current between 0.1 nanoseconds and 0.8 nanoseconds.

11. The memory array of claim 10, wherein the changeable magnetization vector of each of the memory cells changes to the second state based upon a pulse of the second current between 0.1 nanoseconds and 0.8 nanoseconds.

12. The memory array of claim 11, wherein the pinned polarizing magnetic layer of each of the memory cells has a first spin torque and the reference layer of each of the memory cells has a second spin torque, and wherein a ratio of the first spin torque and the second spin torque reduces write error rates.

13. The memory array of claim 12, wherein the ratio of the first spin torque and the second spin is between 0.36 and 1.8.

14. The memory array of claim 8, wherein each of the memory cells has a circular cross section.

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