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(54) **FORCING STUCK BITS, WATERFALL BITS, SHUNT BITS AND LOW TMR BITS TO SHORT DURING TESTING AND USING ON-THE-FLY BIT FAILURE DETECTION AND BIT REDUNDANCY REMAPPING TECHNIQUES TO CORRECT THEM**

(71) Applicant: **SPIN TRANSFER TECHNOLOGIES, INC.**, Fremont, CA (US)

(72) Inventors: **Neal Berger**, Cupertino, CA (US); **Benjamin Louie**, Fremont, CA (US); **Mourad El-Baraji**, Fremont, CA (US); **Lester Crudele**, Tomball, TX (US)

(73) Assignee: **Spin Memory, Inc.**, Fremont, CA (US)

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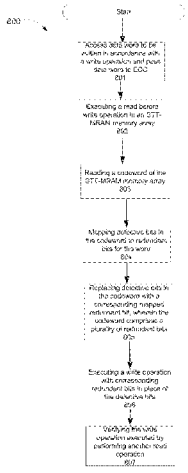
(57) **ABSTRACT**

A method for correcting bit defects in a memory array is disclosed. The method comprises determining, during a characterization stage, a resistance distribution for the memory array by classifying a state of each bit-cell in the memory array, wherein the memory array comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bits. Further, the method comprises determining bit-cells in the resistance distribution that are ambiguous, wherein ambiguous bit-cells have ambiguous resistances between being high or low bits. Subsequently, the method comprises forcing the ambiguous bit-cells to short circuits and replacing each short-circuited ambiguous bit-cell with a corresponding redundant bit from an associated codeword.

20 Claims, 12 Drawing Sheets



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JP	2014-039061		2/2014
JP	5635666		12/2014
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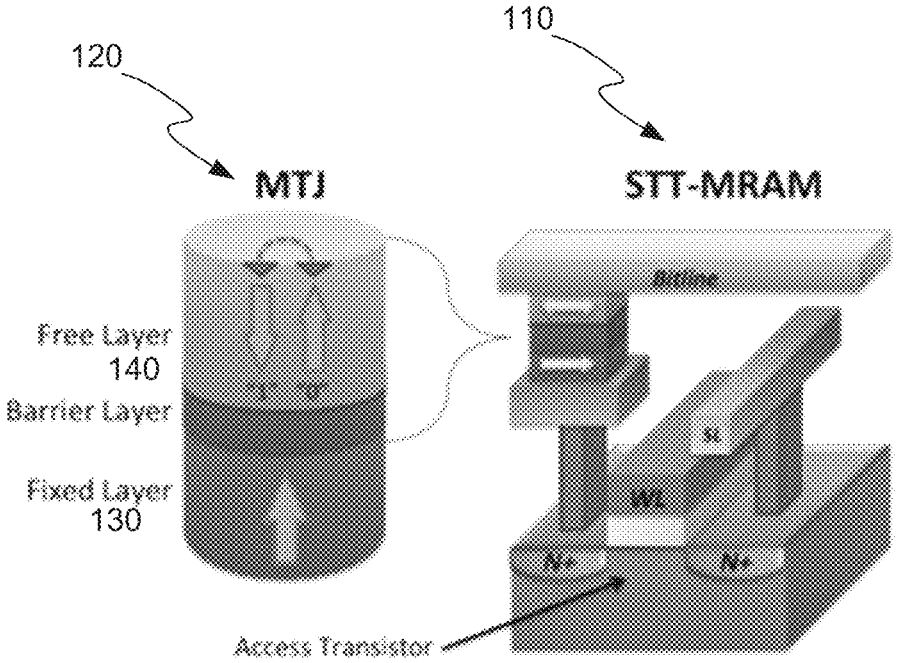
120
110
MTJ
STT-MRAM
Free Layer
140
Barrier Layer
Fixed Layer
130
Access Transistor

FIG. 1

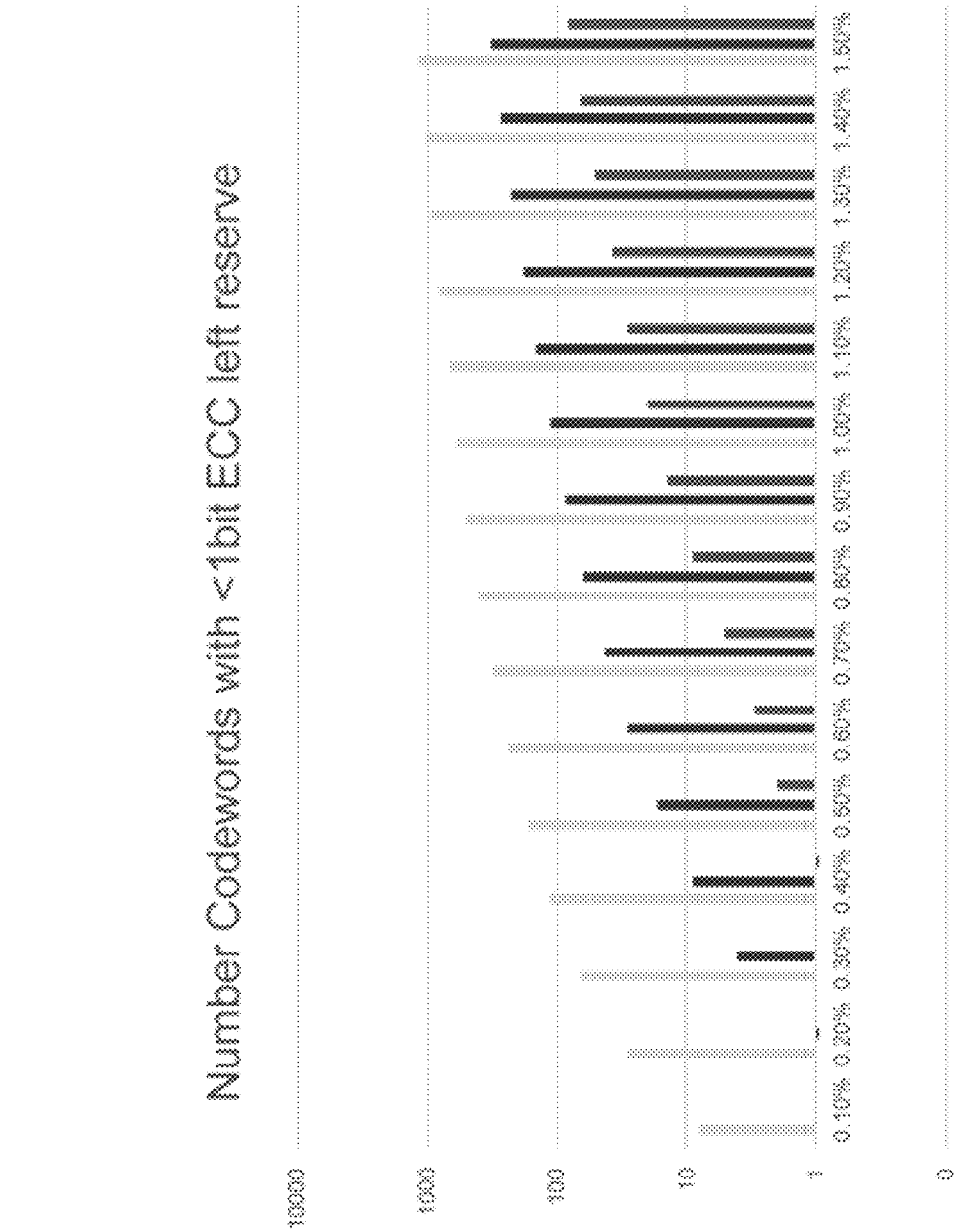
Number Codewords with <1bit ECC left reserve
10000
1000
100
10
1
0
0.10% 0.20% 0.30% 0.40% 0.50% 0.60% 0.70% 0.80% 0.90% 1.00% 1.10% 1.20% 1.30% 1.40% 1.50%
Defect rate
BCH 2 BCH 3 BCH 4

FIG. 2

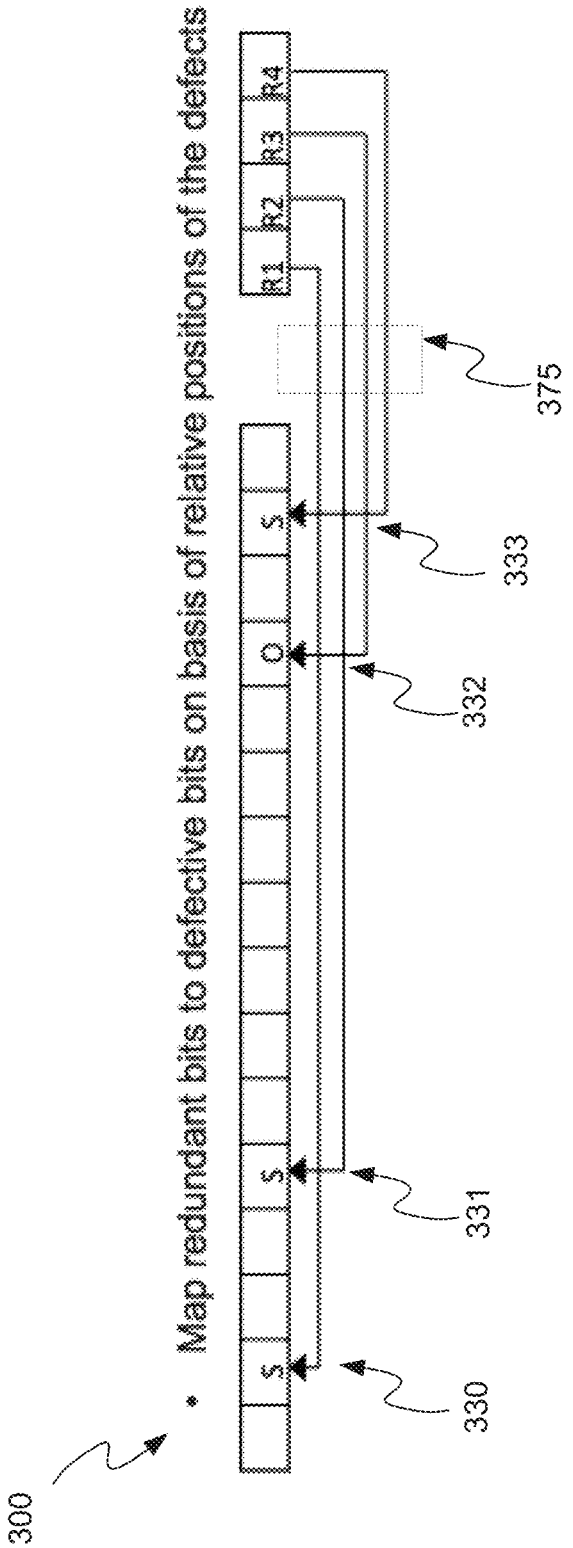
300
• Map redundant bits to defective bits on basis of relative positions of the defects
S
S
S
O
S
R1
R2
R3
R4
330
331
332
333
375

FIG. 3

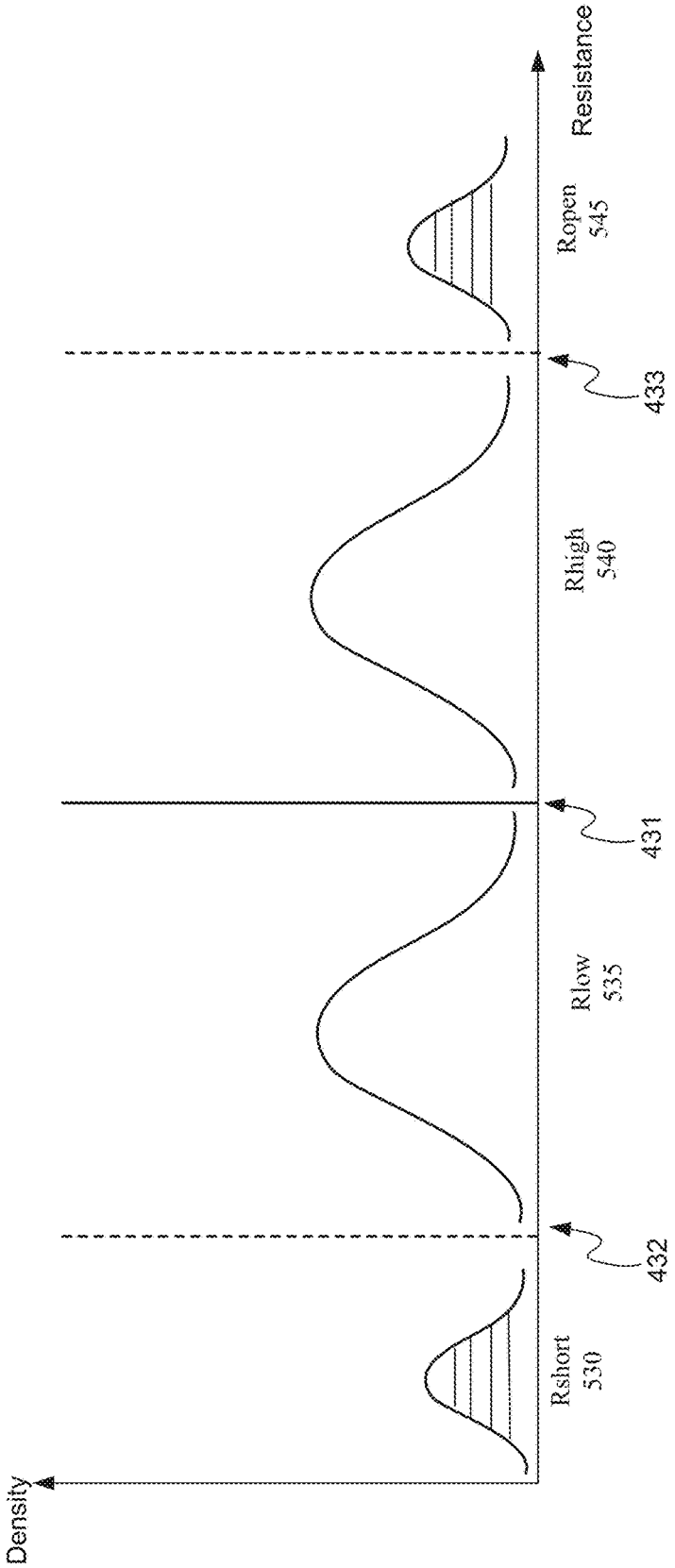
STT MRAM RESISTIVE MEMORY
Density
Resistance
Rshort
530
Rlow
535
Rhigh
540
Ropen
545
432
431
433

FIG. 4

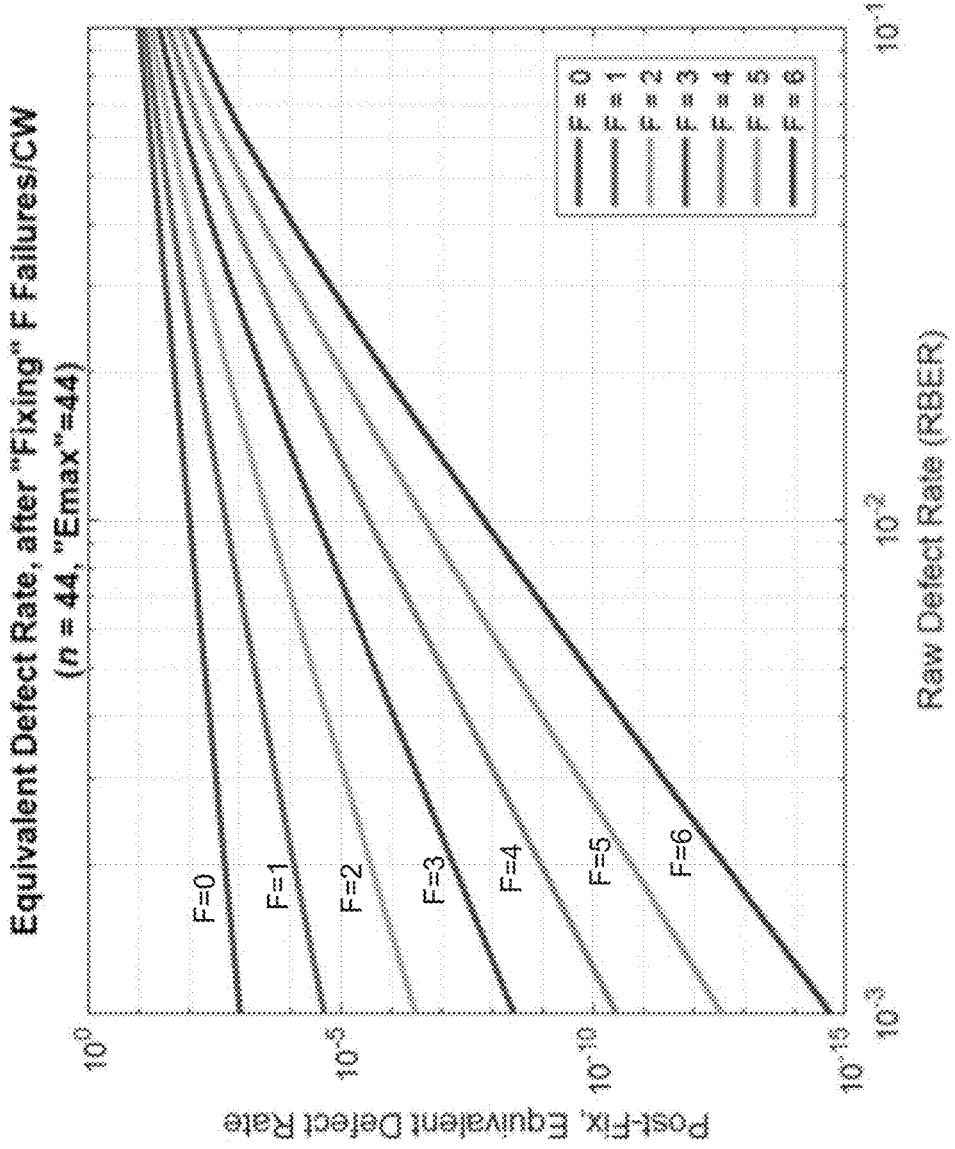
Equivalent Defect Rate, after "Fixing" F Failures/CW
(n = 44, "Emax"=44)
Post-Fix, Equivalent Defect Rate
Raw Defect Rate (RBER)
F=0
F=1
F=2
F=3
F=4
F=5
F=6
F = 0
F = 1
F = 2
F = 3
F = 4
F = 5
F = 6
10^{0}
10^{-5}
10^{-10}
10^{-15}
10^{-3}
10^{-2}
10^{-1}

FIG. 5

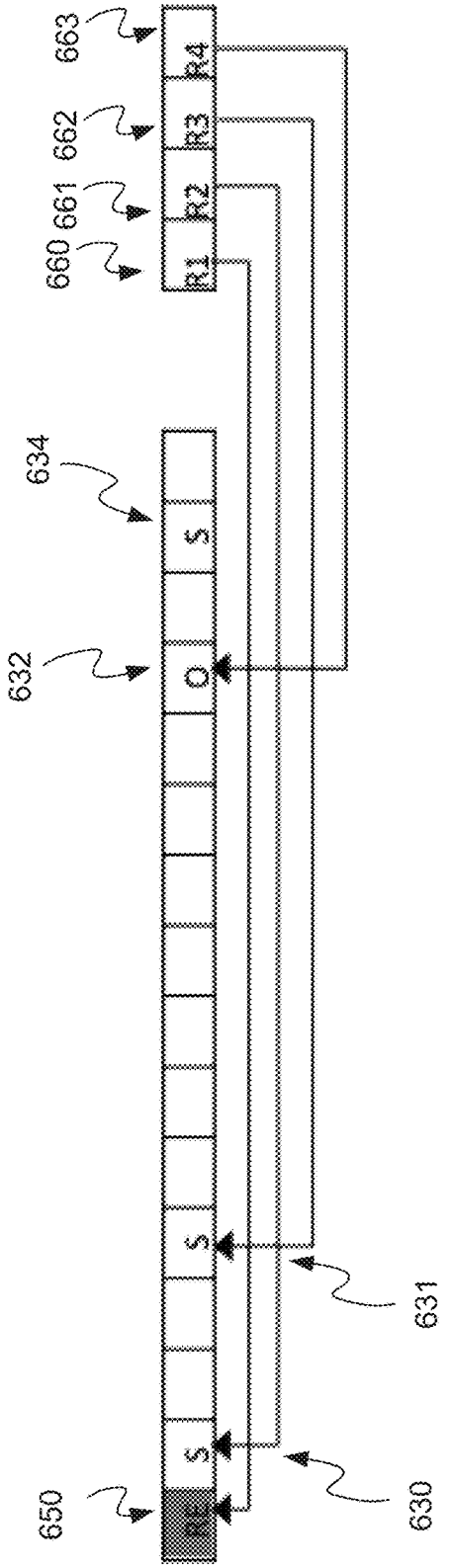

FIG. 6

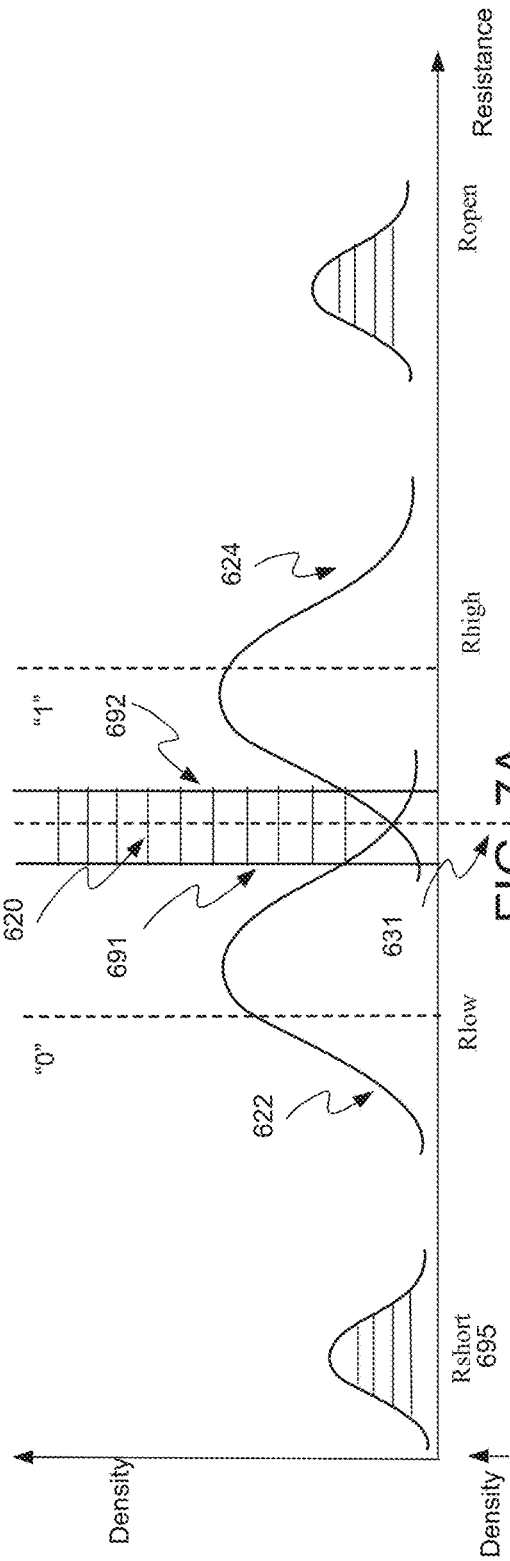
Density
Resistance
Rshort
695
Rlow
Rhigh
Ropen
"0"
"1"
620
691
692
631
622
624

FIG. 7A

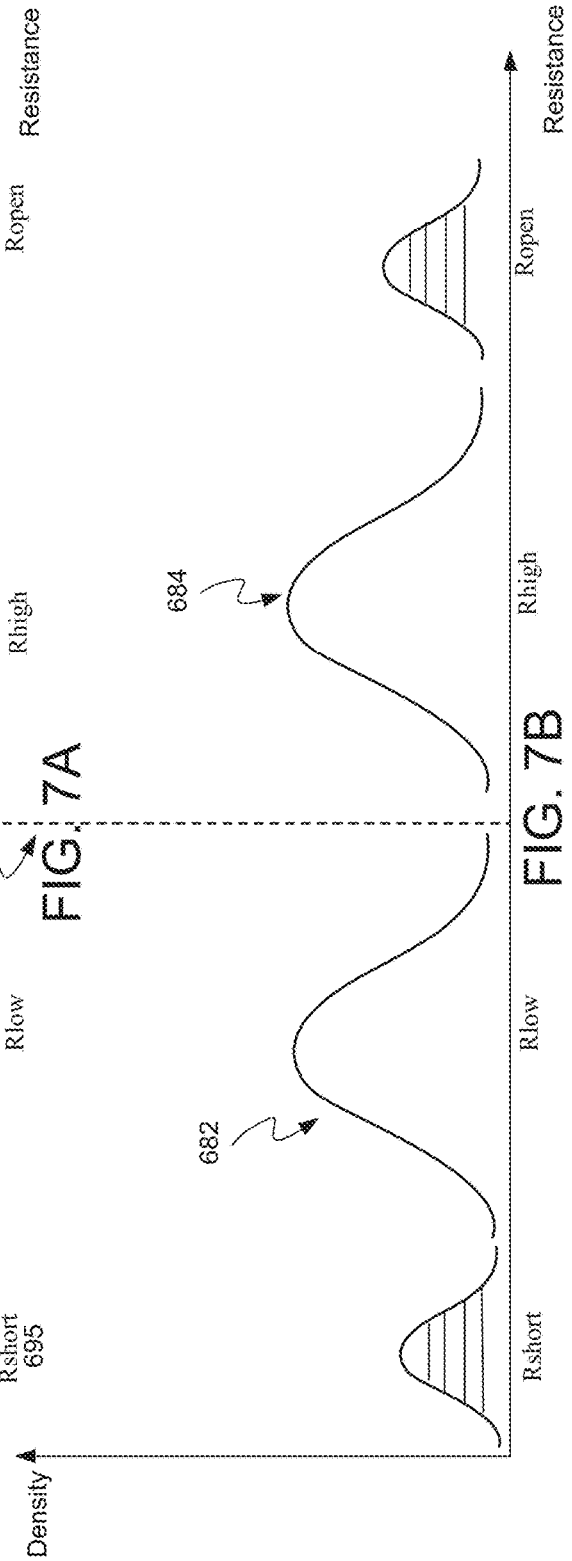
Density
Resistance
Rshort
Rlow
Rhigh
Ropen
682
684

FIG. 7B

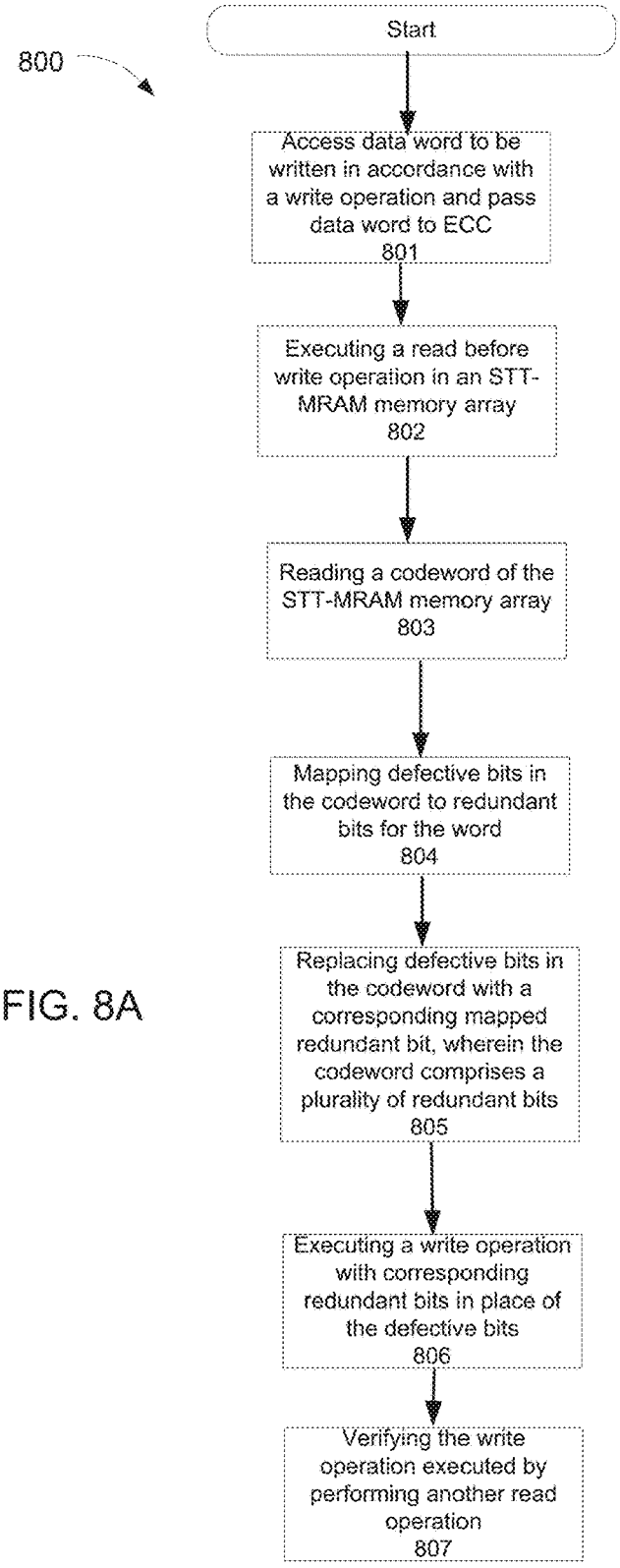
800
Start
Access data word to be written in accordance with a write operation and pass data word to ECC
801
Executing a read before write operation in an STT-MRAM memory array
802
Reading a codeword of the STT-MRAM memory array
803
Mapping defective bits in the codeword to redundant bits for the word
804
Replacing defective bits in the codeword with a corresponding mapped redundant bit, wherein the codeword comprises a plurality of redundant bits
805
Executing a write operation with corresponding redundant bits in place of the defective bits
806
Verifying the write operation executed by performing another read operation
807

FIG. 8A

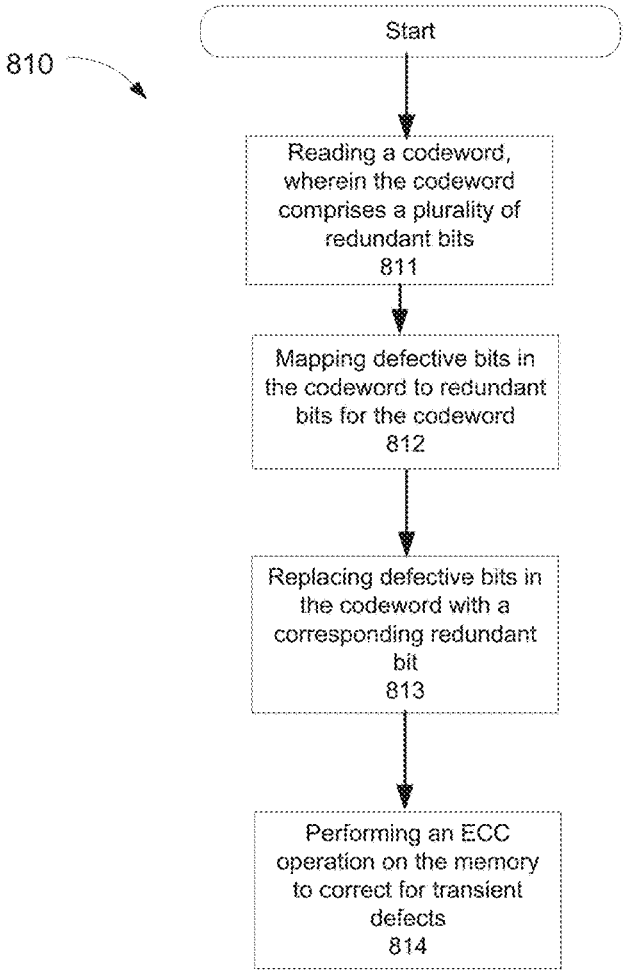
810
Start
Reading a codeword, wherein the codeword comprises a plurality of redundant bits
811
Mapping defective bits in the codeword to redundant bits for the codeword
812
Replacing defective bits in the codeword with a corresponding redundant bit
813
Performing an ECC operation on the memory to correct for transient defects
814

FIG. 8B

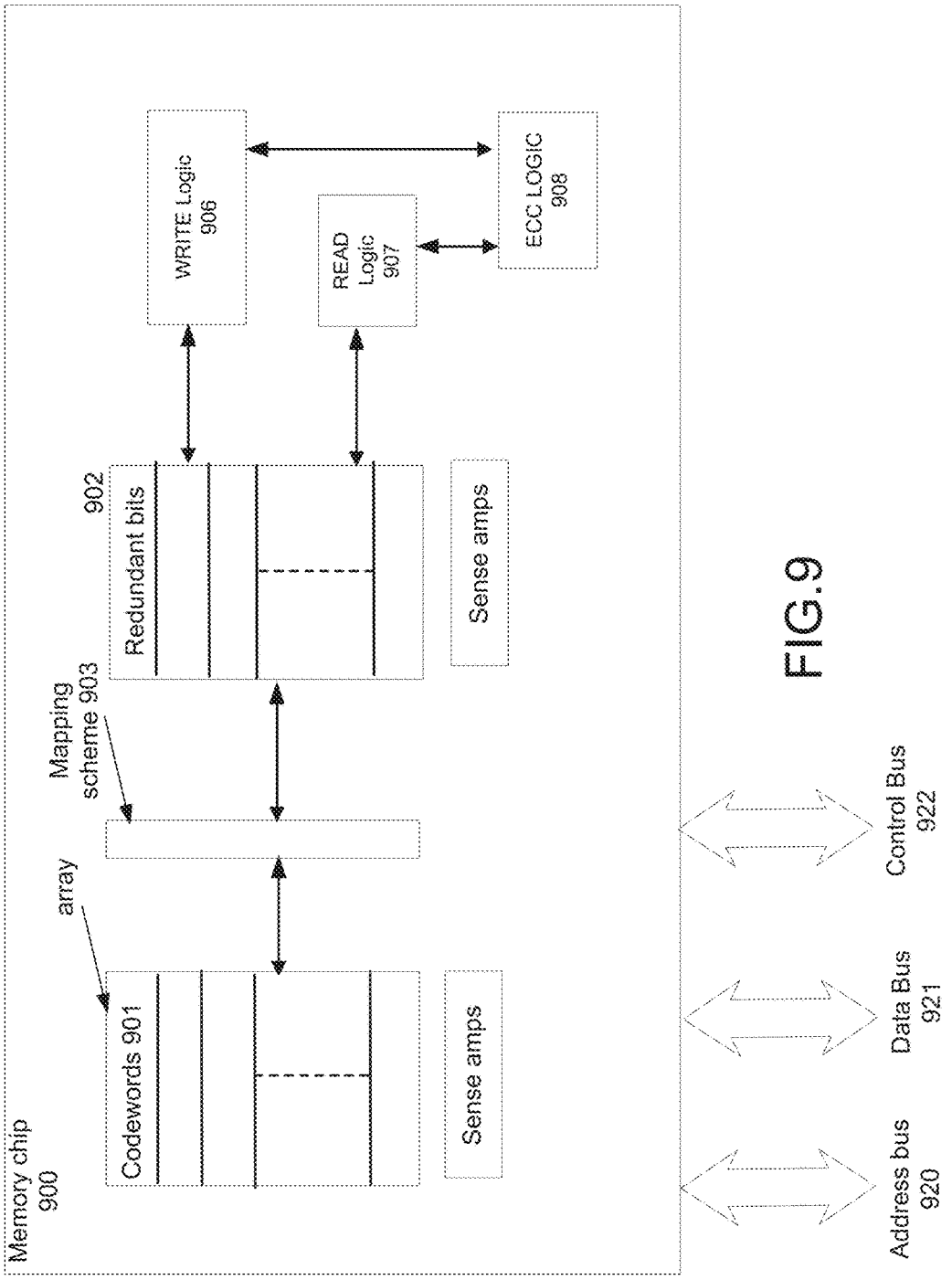
Memory chip
900
array
Codewords 901
Sense amps
Mapping
scheme 903
902
Redundant bits
Sense amps
WRITE Logic
906
READ
Logic
907
ECC LOGIC
908
Address bus
920
Data Bus
921
Control Bus
922

FIG.9

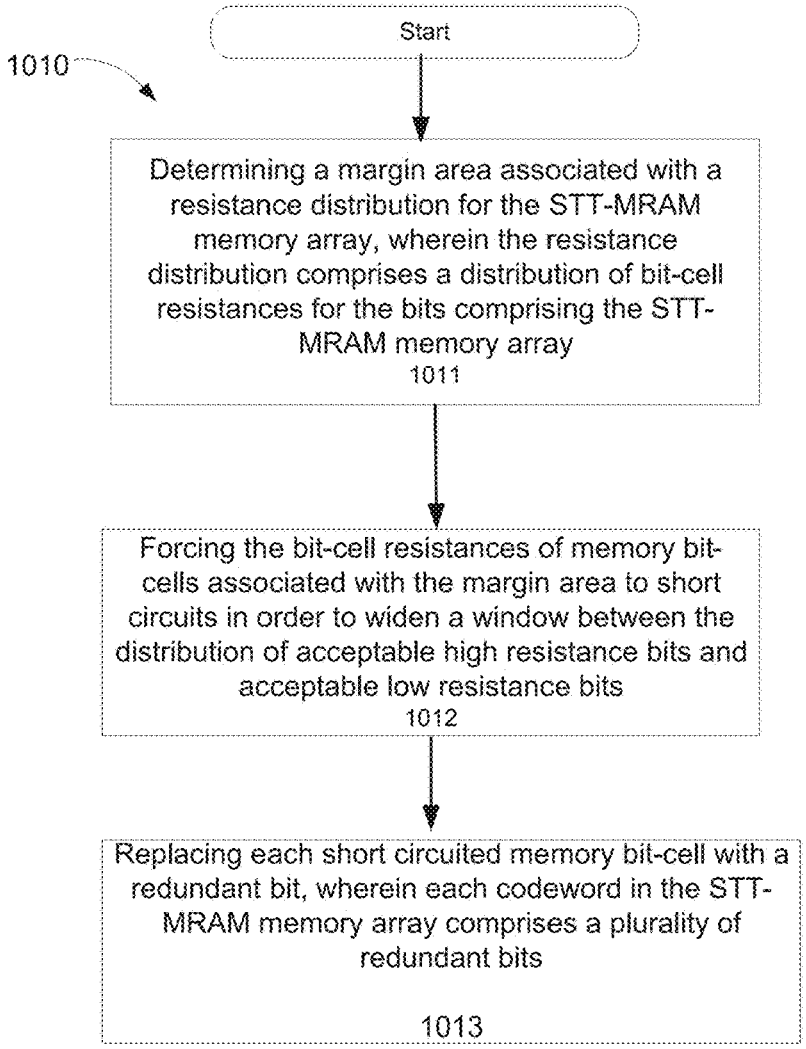
Start
1010
Determining a margin area associated with a resistance distribution for the STT-MRAM memory array, wherein the resistance distribution comprises a distribution of bit-cell resistances for the bits comprising the STT-MRAM memory array
1011
Forcing the bit-cell resistances of memory bit-cells associated with the margin area to short circuits in order to widen a window between the distribution of acceptable high resistance bits and acceptable low resistance bits
1012
Replacing each short circuited memory bit-cell with a redundant bit, wherein each codeword in the STT-MRAM memory array comprises a plurality of redundant bits
1013

FIG.10

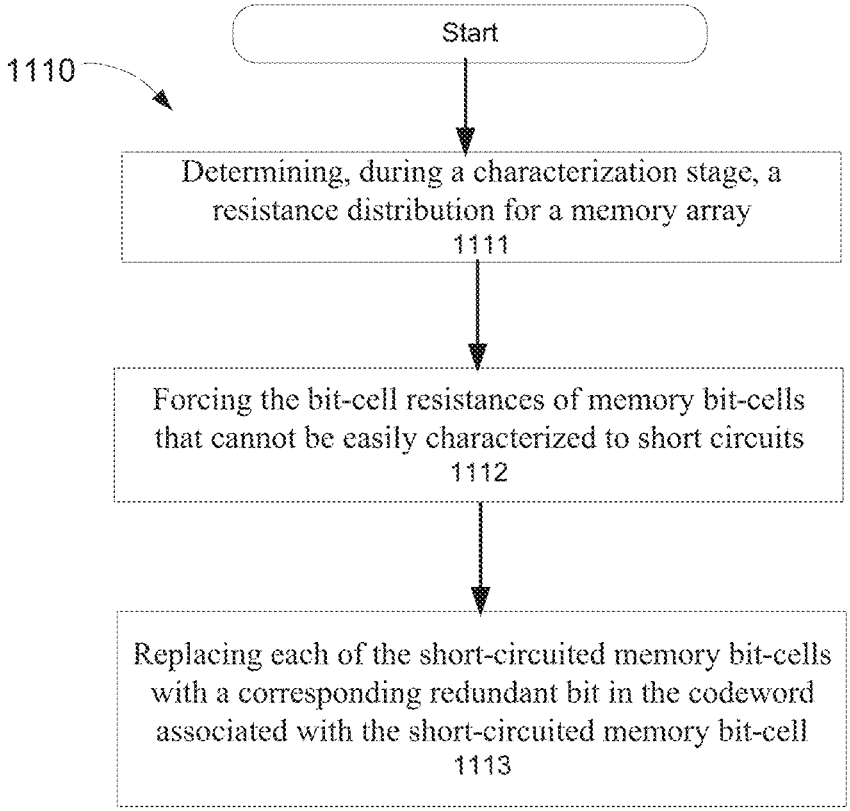
Start
1110
Determining, during a characterization stage, a resistance distribution for a memory array
1111
Forcing the bit-cell resistances of memory bit-cells that cannot be easily characterized to short circuits
1112
Replacing each of the short-circuited memory bit-cells with a corresponding redundant bit in the codeword associated with the short-circuited memory bit-cell
1113

FIG.11

FORCING STUCK BITS, WATERFALL BITS, SHUNT BITS AND LOW TMR BITS TO SHORT DURING TESTING AND USING ON-THE-FLY BIT FAILURE DETECTION AND BIT REDUNDANCY REMAPPING TECHNIQUES TO CORRECT THEM

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a Continuation-in-Part of, claims the benefit of and priority to U.S. application Ser. No. 15/792,672, filed Oct. 24, 2017, entitled "ON-THE-FLY BIT FAILURE DETECTION AND BIT REDUNDANCY REMAPPING TECHNIQUES TO CORRECT FOR FIXED BIT DEFECTS" and hereby incorporated by reference in its entirety.

FIELD

The present patent document relates generally to random access memory (RAM). More particularly, the present patent document relates to failure detection and correction operations in magnetoresistive random-access-memory ("MRAM"). The methods and devices described herein are particularly useful in spin-transfer torque magnetic memory (STT-MRAM) devices.

BACKGROUND

Magnetoresistive random-access memory ("MRAM") is a non-volatile memory technology that stores data through magnetic storage elements. These elements are two ferromagnetic plates or electrodes that can hold a magnetic field and are separated by a non-magnetic material, such as a non-magnetic metal or insulator. This structure is known as a magnetic tunnel junction ("MTJ"). FIG. **1** illustrates an exemplary MRAM cell **110** comprising a MTJ **120**. In general, one of the plates has its magnetization pinned (i.e., a "reference layer" or "fixed layer" **130**), meaning that this layer has a higher coercivity than the other layer and requires a larger magnetic field or spin-polarized current to change the orientation of its magnetization. The second plate is typically referred to as the free layer **140** and its magnetization direction can be changed by a smaller magnetic field or spin-polarized current relative to the reference layer.

MRAM devices can store information by changing the orientation of the magnetization of the free layer. In particular, based on whether the free layer is in a parallel or anti-parallel alignment relative to the reference layer, either a "1" or a "0" can be stored in each MRAM cell as shown in FIG. **1**. Due to the spin-polarized electron tunneling effect, the electrical resistance of the cell change due to the orientation of the magnetic fields of the two layers. The electrical resistance is typically referred to as tunnel magnetoresistance (TMR) which is a magnetoresistive effect that occurs in a MTJ. The cell's resistance will be different for the parallel and anti-parallel states and thus the cell's resistance can be used to distinguish between a "1" and a "0". One important feature of MRAM devices is that they are non-volatile memory devices, since they maintain the information even when the power is off. The two plates can be sub-micron in lateral size and the magnetization direction can still be stable with respect to thermal fluctuations.

MRAM devices are considered as the next generation structures for a wide range of memory applications. MRAM products based on spin torque transfer switching are already

making its way into large data storage devices. Spin transfer torque magnetic random access memory ("STT-MRAM"), such as the one illustrated in FIG. **1**, or spin transfer switching, uses spin-aligned ("polarized") electrons to change the magnetization orientation of the free layer in the magnetic tunnel junction. In general, electrons possess a spin, a quantized number of angular momentum intrinsic to the electron. An electrical current is generally unpolarized, e.g., it consists of 50% spin up and 50% spin down electrons. Passing a current though a magnetic layer polarizes electrons with the spin orientation corresponding to the magnetization direction of the magnetic layer (e.g., polarizer), thus produces a spin-polarized current. If a spin-polarized current is passed to the magnetic region of a free layer in the magnetic tunnel junction device, the electrons will transfer a portion of their spin-angular momentum to the magnetization layer to produce a torque on the magnetization of the free layer. Thus, this spin transfer torque can switch the magnetization of the free layer, which, in effect, writes either a "1" or a "0" based on whether the free layer is in the parallel or anti-parallel states relative to the reference layer.

Spin transfer torque magnetic random access memory ("STT-MRAM") has an inherently stochastic write mechanism, wherein bits have certain probability of write failure on any given write cycle. The write failures are most generally random, and have a characteristic failure rate. A high write error rate (WER) may make the memory unreliable. The error rate can typically increase with age and increased use of the memory. Bit-errors can result in system crashes, but even if a bit-error does not result in a system crash, it may cause severe problems because the error can linger in the system causing incorrect calculations and multiply itself into further data. This is problematic especially in certain applications, e.g., financial, medical, automotive, etc. and is generally commercially unacceptable. The corrupted data can also propagate to storage media and grow to an extent that is difficult to diagnose and recover.

Accordingly servers and other high reliability environments have conventionally integrated Error Correcting Code (ECC) into their memory subsystems to protect against the damage caused by such errors. ECC is typically used to enhance data integrity in error-prone or high-reliability systems. Workstations and computer server platforms have buoyed their data integrity for decades by adding additional ECC channels to their data buses.

Typically ECC adds a checksum stored with the data that enables detection and/or correction of bit failures. This error correction can be implemented, for example, by widening the data-bus of the processor from 64 bits to 72 bits to accommodate an 8-bit checksum with every 64-bit word. The memory controller will typically be equipped with logic to generate ECC checksums and to verify and correct data read from the memory by using these checksums. In conventional memories using STT-MRAM error correction an error correcting code (ECC), e.g., BCH (Bose-Chaudhuri-Hocquenghem) is used to correct errors.

While conventional error correction, e.g., ECC are effective, they have certain drawbacks. For example, the error correction using ECC is not performed in real-time. In other words, the ECC correction may be performed during a read operation, but the error is not corrected as the data is written into the STT-MRAM memory cell.

Further, other conventional error correction schemes may require considerable overhead because the addresses/locations of all the bad bits in the memory chip need to be stored prior to performing the correction. The Content Addressable Memories (CAMs) required to store such addresses and

locations occupy significant surface area and are expensive because of the high overhead involved in saving the bit addresses/locations for all the failing bits. Storing each address of a defective bit in a CAM also acts as a limit on the number of addresses that can potentially be stored. Further, storing addresses of bad bits and then replacing them with good bits is also not an optimal scheme for STT-MRAM memories because the defect rate is typically high and too much memory would be required to store the addresses of all the bad bits. Also, this error mitigation scheme does not work for defects that are discovered on-the-fly (e.g. replacing the bad bits with good bits may have only happened at the tester phase in manufacturing).

Further, typically, error schemes like ECC can detect and correct errors during a read operation, but it does not write the data back into the memory array. This behavior causes the error to stay resident inside the memory array across multiple accesses and may contribute to a memory failure at a later time when additional errors occur. For example, if the memory is used for longer periods of time, there is an increased probability of a second failure occurring in the same 'word' as a first failure. The first failure may lie silently for years as the internal ECC logic repairs the error every time the word is read. When a second (or third or fourth . . .) error hits the same word, the internal ECC circuitry is unable to repair the word and corrupted read data is provided to the system.

Additionally, ECC is not efficient for correcting high fixed defect rates. This is particularly problematic for memories comprising STT-MRAM that typically have higher failure rates as compared to other memories. FIG. **2** illustrates the number of codewords with less than 1 bit ECC left reserved as a function of the defect rate. As seen in FIG. **2**, for a 1% defect rate, using a BCH-3 ECC scheme, over a 100 words need repair. Conventionally, ECC is appropriate for applications where the defect rates are approximately 50 parts per million (ppm) or less. For memories with higher defect rates ECC and other error correction schemes become problematic. Accordingly, in memory applications comprising STT-MRAM where defect rates are higher, using only conventional error mitigation schemes like ECC results in inefficiencies.

BRIEF SUMMARY OF THE INVENTION

Accordingly, a need exists for a system and method that provides real-time detection and correction of STT-MRAM memory cells and that does not require storing any defective bit locations. In one embodiment, the present invention provides an effective method of replacing bit defects using redundant bits added to each codeword of the memory without incurring a large overhead to peripheral circuits. Rather than storing a map of the locations of the bad bits, embodiments utilize an algorithm to map bad bits of a particular codeword to the associated redundancy bits allocated to the codeword.

In one embodiment, the present invention comprises a memory wherein multiple redundant bits are added to each codeword of the memory. In other words, each codeword of the memory comprises multiple redundant bits, e.g., 4, 6, 8 or more redundant bits per word. Prior to performing a write operation during memory usage, a codeword is read and any shorted (short-circuited) or open (open-circuited) bits in the codeword are mapped out on-the-fly. Any shorted or open bits in the codeword that are defective are replaced with one of the redundant bits in accordance with a mapping algorithm. The write operation is then executed with the redundant bits used in place of the defective bits. In other words, instead of using the defective bits, the correct data is written into one of the redundant bits for that codeword. In this way, the defects are detected and corrected in real-time using embodiments of the present invention.

In one embodiment, the redundant bits are also used to correct defective bits when performing a read operation. During a read operation, a codeword is simultaneously read and any shorted or open bits in the word are on-the-fly mapped out. The defective bits in the word are replaced using the redundant bits using the same mapping scheme or algorithm that was used in the prior write operation. It is appreciated that once the defective bits are replaced in accordance with the above technique, ECC algorithms can still be applied to the resultant word to detect and correct for transient bit errors that may exist in the data word in accordance with embodiments of the present invention.

In one embodiment, a method for correcting bit defects in a STT-MRAM memory is disclosed. The method comprises executing a read before write operation in the STT-MRAM memory, wherein the STT-MRAM memory comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bits. The read before write operation comprises reading a codeword and on-the-fly mapping defective bits in the codeword. Further, the method comprises replacing the one or more defective bits in the codeword with a corresponding one or more redundant bits and executing a write operation with corresponding redundant bits in place of the defective bits. The selection of the redundant bits to use in place of the defective bits in the codeword is performed in accordance with a defect bit mapping scheme.

In another embodiment, a method for correcting bit defects in a STT-MRAM memory is discussed. The method comprises executing a read operation in the STT-MRAM memory, wherein the STT-MRAM memory comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bits, and wherein the read operation comprises: (a) reading a codeword; and (b) mapping defective bits in the codeword. Further, the method comprises replacing the one or more defective bits in the codeword with a corresponding one or more redundant bits, wherein the defective bits are replaced with the redundant bits based on relative positions of the defective bits in accordance with a mapping scheme.

In a different embodiment, an apparatus for correcting bit defects in a STT-MRAM memory is disclosed. The apparatus comprises a controller and an STT-MRAM memory comprising a plurality of codewords, wherein each codeword comprises a plurality of redundant bits, and wherein the controller is configured to perform a write operation, wherein the write operation comprises executing a read before write operation in the STT-MRAM memory. The read before write operation comprises: (a) reading a codeword; and (b) mapping on-the-fly defective bits in the codeword to redundant bits allocated to the codewords. Further, the write operation comprises replacing the one or more defective bits in the codeword with a corresponding one or more redundant bits and executing a write operation with corresponding redundant bits in place of the defective bits.

Embodiments of the present invention include any of the above described embodiments in combination with performing ECC error correction on the read data word to defect and correct for transient errors therein.

In one embodiment, a method for correcting bit defects in a memory array is disclosed. The method comprises determining, during a characterization stage, a resistance distri-

bution for the memory array by classifying a state of each bit-cell in the memory array, wherein the memory array comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bits. The method further comprises determining bit-cells of the resistance distribution that are ambiguous, wherein ambiguous bit-cells have ambiguous resistances. Further, the method comprises forcing the ambiguous bit-cells to short circuits and replacing each short-circuited ambiguous bit-cell with a corresponding redundant bit from an associated codeword.

In another embodiment, an apparatus for correcting bit defects is disclosed. The apparatus comprises a processor and a memory array comprising a plurality of codewords, wherein each codeword comprises a respective plurality of redundant bits. Further, the processor is configured to: (a) determine, during a characterization stage, a resistance distribution for the memory array by classifying a state of each bit-cell in the memory array; (b) determine bit-cells of the resistance distribution that are ambiguous, wherein ambiguous bit-cells have ambiguous resistances; (c) force the ambiguous bit-cells to short circuits; and (d) replace each short-circuited ambiguous bit-cell with a corresponding redundant bit from an associated codeword.

In a different embodiment, a method for correcting bit defects in a memory is disclosed. The method comprises determining, during a characterization stage, a resistance distribution for a memory array by classifying a state of each bit-cell in the memory array, wherein the memory array comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bit-cells. Further, the method comprises determining bit-cells of the resistance distribution that are defective. The method also comprises forcing defective bit-cells to short circuits and replacing each short-circuited defective bit-cell with a corresponding redundant bit-cell from an associated codeword.

The following detailed description together with the accompanying drawings will provide a better understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements.

FIG. **1** illustrates an exemplary MRAM cell comprising a magnetic-tunnel-junction.

FIG. **2** illustrates the number of codewords with less than 1 bit ECC left reserved as a function of the defect rate.

FIG. **3** illustrates the manner in which redundant bits are mapped to defective bits in accordance with an embodiment of the present invention.

FIG. **4** graphically illustrates the distribution of the resistance states across an STT-MRAM chip array.

FIG. **5** illustrates the behavior of the defect rate in a memory chip as more redundant bits per word are added in accordance with an embodiment of the present invention.

FIG. **6** illustrates the manner in which a malfunction can occur if a bit shorts during a read operation in accordance with an embodiment of the present invention.

FIG. **7**A graphically illustrates the manner in which the distribution of the resistance states across an STT-MRAM chip array wherein there is overlap between the high and low resistance states.

FIG. **7**B graphically illustrates the manner in which the distribution of the resistance states across an STT-MRAM chip array changes by shorting marginal TMR bits or by reducing TMR requirements for the sense amplifiers in accordance with embodiments of the present invention.

FIG. **8**A shows a flowchart of an exemplary method for correcting bit defects in a STT-MRAM memory array during a write operation in accordance with embodiments of the present invention.

FIG. **8**B shows a flowchart of an exemplary method for correcting bit defects in a STT-MRAM memory array during a read operation in accordance with embodiments of the present invention.

FIG. **9** illustrates an apparatus for correcting bit defects in a STT-MRAM memory array in accordance with embodiments of the present invention.

FIG. **10** shows a flowchart **1010** of an exemplary method for correcting bit defects in a STT-MRAM memory array in accordance with embodiments of the present invention.

FIG. **11** shows a flowchart **1110** of another exemplary method for correcting bit defects in a STT-MRAM memory array in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the various embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. While described in conjunction with these embodiments, it will be understood that they are not intended to limit the disclosure to these embodiments. On the contrary, the disclosure is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the disclosure as defined by the appended claims. Furthermore, in the following detailed description of the present disclosure, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. However, it will be understood that the present disclosure may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present disclosure.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. In the present application, a procedure, logic block, process, or the like, is conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those utilizing physical manipulations of physical quantities. Usually, although not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as transactions, bits, values, elements, symbols, characters, samples, pixels, or the like.

Forcing Stuck Bits, Waterfall Bits, Shunt Bits and Low TMR Bits to Short During Testing and Using On-The-Fly Bit Failure Detection And Bit Redundancy Remapping Techniques to Correct Them

Embodiments of the present invention provide real-time detection and correction of MRAM memory cells, and in

particular, STT-MRAM cells. In one embodiment, the present invention provides an effective method of replacing defects using redundant bits added to each codeword of the memory without incurring a large overhead to peripheral circuits.

As used herein, the term "data word" shall apply to the informational bits that are to be written to a memory cell or read from a memory cell. The term "codeword" shall apply to the memory storage elements that store the data word. The term "redundant bits" shall apply to additional memory storage elements that each codeword is supplemented with to store the correct state for defective bits within the associated codeword.

As explained above, conventional methods of error correction have shortcomings that make them less efficient especially when addressing higher error rates for STT-MRAM. For example, the error correction may not be performed in real time. Further, the error correction scheme may be able to detect and correct errors during a read operation, but it does not write the correct data back into the memory array. This behavior causes the error to stay resident inside the memory array across multiple accesses and may contribute to a memory failure at a later time when additional errors occur.

Additionally, conventional error correction schemes are not efficient for correcting high fixed defect rates. This is particularly problematic for memories comprising STT-MRAM that typically have higher failure rates as compared to other memories. One reason conventional schemes are inefficient for correcting high defect rates is because of the high overhead required to store addresses of all the defective bit locations. Accordingly, as described above, conventional defective bit mapping and replacement schemes consume a significant amount of space, power and speed. With the defect rates of STT-MRAM, the overhead associated with storing addresses for all the defective bit locations would be prohibitively high.

In order to address the shortcomings of conventional error correction schemes, embodiments of the present invention comprise a memory wherein multiple redundant bits are added to each codeword of the memory. In other words, each codeword of the memory comprises multiple redundant bits, e.g., 4, 6, 8 or more redundant bits per word.

FIG. **3** illustrates the manner in which redundant bits are mapped to defective bits in accordance with an embodiment of the present invention. FIG. **3** illustrates an exemplary word **300** that comprises 4 defective bits, namely, bit **330** (short circuit), bit **331** (short circuit), bit **332** (open circuit) and bit **333** (short circuit). Note that embodiments of the present invention are particularly suited for correcting defects related to open circuits ("opens") and short circuits ("shorts"), e.g., defective bits. For example, short circuited bits are a common occurrence in MRAMs and, accordingly, embodiments of the present invention provide an effective way for curing bit defects related to short circuits. Codeword **300** also comprises 4 redundant bits, R**1**, R**2**, R**3** and R**4** associated with codeword **300**. Typically, each codeword in the memory will comprise the same number of additional redundant bits.

Prior to performing a write operation to a codeword, embodiments of the present invention would first read the codeword on which the write operation is to be performed. For example, the reading may be in accordance with a read-before-write (RBW) operation. Accordingly, codeword **300** is read and the shorted (short-circuited) or open (open-circuited) bits in the codeword are mapped out. In other words, the read operation maps out the locations of the defective bits **330**, **331**, **332** and **333** on-the-fly. Note that the mapping of the defective bits is conducted simultaneously with the read operation. In one embodiment, the mapping may be performed substantially simultaneously with the read operation, e.g., in the same cycle with a slight delay or in a subsequent cycle.

The defective bits can be identified by their resistance which is detected by sense amplifiers used during the read. The codeword is read and the mapping of the defective bits is done simultaneously to avoid paying a time penalty. Further, note that performing a read before the write is advantageous because the read cycle can be used to determine which bits need to change when performing the write. Accordingly, a power savings can also result from only writing the bits in a codeword that need to change. In other words, during the write cycle, only the bits that need to change will be flipped.

Note that in rare instances it may not be efficient to perform a read prior to a write. In such cases, the mapping scheme that was determined in a prior read cycle may, in one embodiment, be used to perform the write operation (without conducting an immediately preceding read), e.g., where the last read was performed for the same location prior to attempting a write operation.

In one embodiment, a verify operation is performed after the write to ensure that no endurance fails happened during the write. If an endurance failure, e.g., a bit shorting during the write operation, etc. occurs during the write operation, it will trigger a failure during the verify operation. In other words, it will signal that the write operation failed.

The shorted or open bits in the codeword, namely bits **330**-**333**, are subsequently replaced with one of the redundant bits in accordance with a mapping scheme **375**. In other words, the defective bits are swapped out with the redundant bits. In one embodiment, a multiplexer network is used to perform this swapping operation. In one embodiment, one multiplexer network per bank of sense amplifiers would be required to implement this scheme.

In one embodiment, in the mapping scheme **375**, the redundant bits are mapped to the defective bits on the basis of relative positions of the defect. In other words, the first redundant bit (the left-most bit R**1** in FIG. **3**) gets mapped to the earliest defective bit in codeword **300** (bit **330** in FIG. **3**). The second redundant bit R**2** will get mapped to the second defective bit in codeword **300** (bit **331**). Similarly, redundant bit R**3** gets mapped to bit **332** while redundant bit R**4** gets mapped to bit **333**. Another relatively simple mapping scheme would map the redundant bits to the defective bit in a right to left orientation. For example, bit R**4** would be mapped to shorted bit **330**, bit R**3** would be mapped to shorted bit **331**, bit R**2** would be mapped to open bit **332** and bit R**1** will be mapped to shorted bit **333**. Because of the relative simplicity of these mapping schemes, they do not require storing any complex algorithms within the memory chip. Note, however, that some logic in the memory chip may need to be dedicated to implement even a simple mapping scheme.

In other embodiments, other replacement schemes or algorithms for mapping redundant bits to the defective bits can also be used to improve efficiency. Such schemes would be more complex than simply mapping bits on the basis of relative positions of the defects and may require programming and storing a corresponding algorithm into the memory chip. In some embodiments, however, the replacement scheme may be simpler schemes that can be implemented with additional logic.

Subsequently, the write operation is then executed with the redundant bits used in place of the defective bits to receive the write data. In other words, instead of using the defective bits, the correct data is written into one of the redundant bits for that codeword. Further, in order to save power, the write is disabled for the defective bits. In other words, the write operation does not attempt to write to the defective bits. In this way, the defects are advantageously detected and corrected in real-time using embodiments of the present invention. The local bit redundancy scheme advantageously replaces defects at the bit level in real-time without incurring a large overhead in peripheral circuits. Unlike prior error correction schemes that incurred a significant overhead as a result of needing to store defective bit addresses to correct at a later time, embodiments of the present invention advantageously correct bit defects in memory without the need for storing any defective bit addressees. Further, unlike prior error mitigation schemes that would perform detection and correction procedures during the testing process prior to shipping, embodiments of the present invention perform detection and correction of errors in real-time (or in situ).

In one embodiment, the RBW operation is performed simultaneously or partially simultaneously with the write operation in order to decrease the overall length of the write operation.

Embodiments of the present invention also advantageously mitigate errors in the memory chip over the lifetime of the chip. In other words, the error correction scheme is not merely limited to a particular duration of time, e.g., during testing of the chip. If a bit in the memory fails after the chip has already shipped and is in use by an end user, the error mitigation scheme will detect the defective bit during a pre-read for a write operation (or a verify operation) and replace the defective bit in the word with a redundant bit. In other words, the error correction scheme of the present invention can detect defective bits on-the-fly over the lifetime of the chip and replace the defective bits with redundant bits (provided there are redundant bits remaining). Note, that it is not uncommon for bits to be shorted out over the lifetime of an MRAM chip. Accordingly, it is advantageous to have an error correction scheme that accommodates defects that develop over time in a chip. If a newly discovered defective bit is present, then the mapping scheme will remap the redundant bits to the defective bits in accordance with the mapping scheme.

By comparison, conventional redundancy schemes store information regarding the locations of the defective bits in CAMs and find and replace the defective portions of the memory only during the testing process. Embodiments of the present invention perform correction over the lifetime of the chip without storing any such locations/addresses of the defective bits. Further, the correction of the present embodiment is performed on-the-fly at read and write speeds. Replacing defective bits over the lifetime of the chip with functional redundant bits also increases the lifetime of the chip. For example, if a bit is shorted after the memory chip has already been shipped, it will simply be replaced by a heretofore unused redundant bit. Accordingly, the lifetime of the chip is increased because a new redundant bit replaces an older bit which became defective during use.

In one embodiment, the redundant bits are also used to correct defective bits when performing a read operation in accordance with a mapping scheme. During a read operation, a codeword is simultaneously read and any shorted or open bits in the word are mapped out based on their resistance. The defective bits in the word are replaced using the redundant bits using the same mapping scheme that was used in the prior write operation in order to determine the data word to be read out. Note that in order to speed up the read operation, both the codeword is simultaneously read and any mapping of shorted and open bits is performed at the same time. If speed is not a consideration, then, in one embodiment, the reading of the codewords and the mapping of the defective bits can be separate operations.

In one embodiment, if a codeword uses up its allocation of redundant bits, it may borrow redundant bits from neighboring words. For example, if 4 redundant bits are allocated per codeword and if a word has more than 4 defective bits, in one embodiment, it may be possible for the codeword to borrow vacant redundant bits from neighboring codewords. This may be possible, for example, if multiple words can be read simultaneously (or in the same cycle). In such cases, redundant bits may be borrowed from other words that are read in the same cycle.

FIG. **4** graphically illustrates the distribution of the resistance states across an STT-MRAM chip array. This is a resistance distribution. As discussed above, MRAM devices store information by changing the orientation of the magnetization of the free layer. In particular, based on whether the free layer is in a parallel or anti-parallel alignment relative to the reference layer, either a "1" or a "0" can be stored in each MRAM cell as shown in FIG. **1**. Due to the spin-polarized electron tunneling effect, the electrical resistance of the cell change due to the orientation of the magnetic fields of the two layers. The cell's resistance will be different for the parallel and anti-parallel states and thus the cell's resistance can be used to distinguish between a "1" and a "0". Typically, if the free layer is in parallel alignment relative to the reference layer (low resistance state, Rlow **535**), this is considered to mean "1" while if alignment is anti-parallel the resistance will be higher (high resistance state, R-high **540**) and this means "0."

As seen in FIG. **4**, memory cells in the STT-MRAM chip array be distributed so that the cells can typically have one of four resistance states: R-high **540**, R-low **535**, R-open **545** or R-short **530**. Defective bits that are short-circuited (and correspond to R-short **530**) or open-circuited (and correspond to R-open **545**) can be identified because their resistance will either be significantly lower (in the case of R-short) or higher (in the case of R-open) than the typical resistances of the R-low and R-high states respectively.

In one embodiment, in order for the additional states R-open and R-short to be identified during a typical STT-MRAM read operation, additional sense amplifiers are incorporated into the memory chip to perform the resistance measurements. A sense amplifier is one of the elements which make up the circuitry on a memory chip and are well known. A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bit-line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

Conventionally, there is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. However, in conventional memories, the sense amplifiers may only have a single sense reference. In other words, the sense amplifiers in conventional memories may only be able to distinguish between a "1" and a "0".

Embodiments of the present invention, however, require sensing of additional states (namely R-open and R-short) and, therefore, may require additional sense amplifiers for

each column of memory cells so that during a read operation, all four states can be distinguished from each other. As discussed in connection with FIG. **3**, a read operation needs to read the bits in the codeword and map out all the defective bits within the codeword. In order for the read operation to distinguish between the four potential states (namely, a "1", a "0", a short circuit and an open circuit), additional sense amplifiers are incorporated in the circuitry for the memory chip. Accordingly, with the additional sense amplifiers, multiple sense points, e.g., sense points **432**, **431** and **433** may be detected. To detect the additional sense points, embodiments of the present invention may, for example, require two different extra sense amplifiers per bit (or per column, depending on the structure of the memory). Note that sense point or sense reference **431** can be determined using a simple calculation: ((R-high+R-low)/2).

The various reference points (e.g., **431**, **432** and **433**) can be set simultaneously so that during a read cycle, the different states can be mapped out at the same time. Alternatively, if time is not a constraint, the different reference points can be set serially so that the detection of the various states is done serially.

FIG. **5** illustrates the behavior of the defect rate in a memory chip as more redundant bits per word are added in accordance with an embodiment of the present invention. In FIG. **5**, "F" represents the number of redundant bits added per code word. As seen in FIG. **5**, when F=4 (each code word has 4 redundant bits), the defect rate falls lower than 10^{-10}. With additional redundant bits, e.g., 6 bits, the defect rate falls lower than 10^{-15} but there will be a trade-off between a low defect rate and efficiency with increasing number of redundant bits because processing a higher number of redundant bits takes longer.

In one embodiment, the redundant bits of the present invention can be combined with other error mitigation schemes to further reduce defect rates. For example, a hybrid scheme may utilize both redundant bits and BCH**2** or BCH**3** error correction. For example BCH**2** can be combined with redundant bits so that each word in the memory comprises 32 data-bits, 12 parity bits for BCH**2** and 6 redundant bits. Bit redundancy is used to correct any word that has a defect in it. BCH**2** error correction is then used to correct data words which are not completely cleaned up by bit redundancy. The hybrid schemes are also effective because using an ECC scheme, e.g., BCH**2**, BCH**3**, Reed Solomon, Hamming code and Low Density Parity Check (LDPC), etc. in conjunction with redundant bits may be able to correct for errors, e.g., write errors, data retention failures, transient errors, etc. that cannot be cleaned up using only redundant bits. Accordingly, while redundant bits may be effective at correcting for hard defects within a codeword, the error correction process can be supplemented with an ECC scheme to correct for other types of errors, e.g., transient errors that are not caused by hard defects. The ECC scheme will typically be applied to a data word after the redundant bit replacement scheme has already been implemented to replace bit defects in the corresponding codeword with corresponding redundant bits. Further, instead of using an expensive type of ECC, e.g., a 4-bit ECC exclusively to correct for errors, embodiments of the present invention supplement the redundant bit scheme with a less expensive type of ECC, e.g., a 2-bit to achieve the same or better results than a prohibitively expensive ECC. In other words, combining the inclusion of redundant bits with other redundancy schemes (e.g., ECC) results in power, time and space savings because less complex redundancy schemes need to be employed.

A typical STT-MRAM may contain certain memory cells that may not clearly fall within any of the states illustrated in FIG. **4**. In other words, the resistance of certain STT-MRAM cells may be ambiguous preventing them from being easily classified as either a high, low, short or open. For example, if the resistance of a cell is in close proximity to any of the sense points, e.g., points **432**, **432** or **433**, it may be difficult to classify the state of that cell. Such defects, which are neither shorts nor open circuits, are not detectable during user read or verify operations. Examples of such defects include stuck bits, waterfalls, shunts and low tunnel magnetoresistance (TMR) bits.

In one embodiment of the present invention, all cells with resistances that cannot be easily classified are converted or forced into short circuited cells during the testing or characterization stage. Shorting such problematic bits allows them to be replaced by redundant bits, thereby, precluding them from being corrected using a more expensive ECC process. In one embodiment, during the testing phase, a test algorithm is executed that determines the number of such bits and converts them into shorts.

For example, there may be certain shunted bits in the region between Rlow **535** and Rshort **530**. These bits are not short circuits, however, they are also not completely functional bits. As a result of certain process anomalies, these bits may not be capable of a full swing between Rhigh and Rlow. In other words, while the bits may exhibit some switching behavior, they are not capable of exhibiting a full TMR swing in a way that the sense amplifier can clearly distinguish between the two states of the bit and classify them as either Rhigh or Rlow. In one embodiment, the shunted bits are shorted out so that they can be replaced by a corresponding redundant bit.

In certain cases, there may be defective bits that skew the WER of the MRAM device. For example, in the case of magnetic defects, there may be cases where certain bits have a defect rate that are much higher than the other bits in the MRAM device. One bit in the memory may, for example, have a high defect rate of 10^{-5} while other bits in the same device have an average defect rate of 10^{-6}. In order to prevent the bits with the high defect rate from skewing the WER, in one embodiment, these bits can be shorted out and replaced with redundant bits, e.g., during memory operation.

By way of further example, certain bits may be classified as waterfall bits. These bits are typically stuck bits that do not switch at all either because of a process or magnetic defect. They may be either stuck high or stuck low. These bits may be found in the middle of the distribution, e.g., either in the middle of the Rlow distribution **535** or the middle of the Rhigh distribution **540**. Low TMR bits may exhibit the same behavior as waterfall bits. In other words, low TMR bits may also be either stuck high or stuck low. Low TMR bits can also be caused by either a magnetic or process defect. In one embodiment, the waterfall or low TMR bits are shorted out so that they can be replaced by a corresponding redundant bit.

One of the metrics monitored for the bits in an MRAM device is retention. The retention of the bit is related to the stability of the bit. Retention relates to the amount of time that a bit will retain its data. The bits in a memory device may have a retention distribution. Some bits, for example, may retain their data for several hours while some may only retain their information for under an hour. A given application for an MRAM device may, however, require a minimum retention period. For example, a given application may require a minimum retention period of an hour. In one embodiment, all bits that have retention rates below an hour

can then be shorted out and replaced by redundant bits. In other words, bits that do not meet the requirements of a particular application can be blown out of the distribution and replaced by the redundant bits.

Typically, bits in a STT-MRAM memory chip will short during a write operation because of the higher voltage employed during a write operation (as compared to a read operation). In certain unlikely instances if a bit shorts during a read operation while the mapping of the defective bits is being performed, it can cause the replacement scheme to malfunction.

FIG. **6** illustrates the manner in which a malfunction can occur if a bit shorts during a read operation in accordance with an embodiment of the present invention. If a defect, e.g., a short **650** appears during a read operation that was not present during an earlier write operation, then all the redundant bits **660-663** can get incorrectly assigned especially if a simple replacement scheme is being followed, e.g., a left to right or right to left replacement scheme based on the relative positions of the defects. For example, if a simple left to right replacement scheme is being followed, then a short **650** that appears during a read operation (but was not present when the data was written) may incorrectly be mapped to redundant bit R**1 660**. This would result in all the following redundant bits also being incorrectly assigned, e.g., R**2 661** would be incorrectly assigned to bit **630** (instead of **631**), R**3 662** would be incorrectly assigned to bit **631** (instead of **632**) and so forth.

To reduce the impact of this issue, a more complex replacement scheme, e.g., replacement scheme **375** can be programmed into the memory chip. As mentioned above, in some embodiments, other replacement schemes or algorithms for mapping redundant bits to the defective bits can also be used to improve efficiency. Such schemes would be more complex than simply mapping bits on the basis of relative positions of the defects and would likely require programming and storing a corresponding algorithm into the memory chip. However, more complex schemes would prevent against problems created as a result of the rare circumstance of a bit shorting during a read operation.

In one embodiment, the replacement scheme may alternate between a left-to-right scheme and a right-to-left scheme. Such a scheme would prevent against all the redundant bits getting misassigned in the case of a bit failure during a read operation. For example, if bit **650** shorts during a read operation, in a scheme that alternates, redundant bit R**1 660** would be misassigned to bit **650**. However, if the scheme alternates, then redundant bit R**4 663** would be swapped with the right-most bit in the codeword, which in this case is, bit **634**. Accordingly, instead of all 4 redundant bits being misassigned, only 2 end up being misassigned in a scheme that alternates between the two replacement schemes.

In another embodiment, the replacement scheme may restrict the allocation of redundant bits to designated portions of the code word. For example, for a 32 bit codeword, redundant bit R**1 660** may be restricted to defects appearing in the first 8 bits of the codeword, R**2 661** may be restricted to defects appearing in the next 8 bits of the codeword, and so forth. While this scheme is effective in restricting the number of redundant bits that may potentially be misaligned if a bit shorts during the read operation, it may be problematic if all the defective bits are lumped together in one of the 8 bit sections.

Similar to a bit shorting during a read operation, it is possible that a bit may short during a write operation after the redundant bits have already been mapped out during the pre-write read operation. To mitigate against this, typically embodiments of the present invention will perform a verify operation following the write. In other words, a write-verify (which effectively is the same as a 'read' operation) can be performed to make sure no bits shorted or otherwise malfunctioned during the write operation. If a malfunction is detected during the verify operation, the entire write operation is performed again (which may include the pre-write read operation for mapping out the redundant bits).

In one embodiment, a verify operation occurs after the re-write also. In another embodiment, if the verify operation fails, the data word is entered into an error cache (or dynamic redundancy register) where it is stored for correcting at a later time. Examples of functionality that enables monitoring performance of a client device are described in U.S. patent application Ser. No. 15/277,799, entitled "DEVICE WITH DYNAMIC REDUNDANCY REGISTERS", filed on 27 Sep. 2016, and which is hereby incorporated by reference in its entirety for all purposes.

If the data word needs to be accessed prior to fixing the malfunction, it is read directly from the cache. In one embodiment, a verify operation occurs after the write to error buffer to ensure that the proper information was written to the error buffer.

In one embodiment, in order to improve read speed, the bit-cell resistance distribution can be cleaned up by shorting marginal TMR bits or by reducing TMR requirements for the sense amplifiers. FIG. **7**A graphically illustrates the manner in which the distribution of the resistance states across an STT-MRAM chip array wherein there is overlap between the high and low resistance states. As shown in FIG. **7**A, the bit-cell resistance distribution comprises region **620**, wherein certain bit-cells in the array have resistances that fall in the region **620**. This region is also known as the "margin area." The margin area is typically a bandwidth of resistances centered around reference point **631**, wherein a sense amplifier will not be able to accurately distinguish a resistance within the margin area as either Rhigh or Rlow. In other words, typically, bit-cells with resistances that fall within margin area **620** (either directly in the region overlapping the R-low **622** and R-high curves **624** or in close proximity to the overlap region) will likely not be read accurately by a sense amplifier at high speeds. The width of margin area **620** depends on the speed of the sense amplifier. A sense amplifier will typically be unable to discern between a "1" or a "0" for STT-MRAM cells when the bit-cell resistances are within region **620**. Such bits are unreliable because they may be detected as either a "0" or "1". In order to avoid the overhead of having an ECC process clean up such ambiguous bits, in one embodiment, all bit-cells with resistances that fall in the overlap region **620** are shorted out.

In one embodiment, the margin area **620** is determined by characterizing the sense amplifier. The width of the margin area is dependent on the speed of the sense amplifier. Characterizing the sense amplifier comprises moving the sense amplifier reference point to the left to determine the Margin High reference point **691**. After establishing the Margin High reference point **691**, the bits with resistance values higher than the reference point **691** are determined. Subsequently, the sense amplifier reference point is moved to the right to determine the Margin Low reference point **692**. After establishing the Margin Low reference point **692**, the bits with resistance values lower than the reference point **692** are determined. Thereafter, an XOR is performed between the two sets of results to establish the bits with resistance values that lie between the Margin High reference point **691** and Margin Low reference point **692**. The margin

bits in between the two reference points can then be shorted out and pushed towards the R-short distribution **695**.

FIG. **7**B graphically illustrates the manner in which the distribution of the resistance states across an STT-MRAM chip array changes by shorting marginal TMR bits or by reducing TMR requirements for the sense amplifiers in accordance with embodiments of the present invention. When unreliable bits in region **620** are shorted out, the R-low **682** and R-high **684** curves move further apart to where there is no overlapping region anymore. In other words, the sense amplifier window is opened up so a stringent sense amplifier is no longer required to distinguish between a "1" or "0" for ambiguous bits. More stringent sense amplifiers typically require more power and longer evaluation times, so by shorting out the ambiguous bits, the chip conserves power. Further, all the shorted bits can now be corrected by using the redundant bit replacement scheme rather than using costly ECC procedures. And because each codeword in the memory comprises at least 4 redundant bits, it is unlikely that any single codeword will have more than 4 bits shorted out during the process of cleaning up the sense amplifier window.

In one embodiment, the redundant bit replacement scheme of the present invention also results in higher tolerance for write endurance failures. Typically with MRAM, driving the cells at higher voltages at higher speeds results in lower endurance levels. With the bit replacement scheme of the present invention, lower endurance levels can be tolerated because each code word has multiple redundant bits to replace any defective bits. Accordingly, the chip can be allowed to operate at a higher voltage because statistically the error rates do not surpass a critical threshold as a result of the multiple redundant bits being used to replace any defects occurring on the fly. Further, because embodiments of the present invention can be used to correct bit defects over the lifetime of the chip, there is no time limit on the efficacy of the scheme.

FIG. **8**A shows a flowchart **800** of an exemplary method for correcting bit defects in a STT-MRAM memory array during a write operation in accordance with embodiments of the present invention.

At step **801**, a data word to be written into memory is accessed in accordance with a write operation command. The data word is passed to an ECC hash function, e.g., to determine a checksum.

At step **802**, a read-before-write operation is executed on the STT-MRAM memory array, wherein the STT-MRAM memory comprises a plurality of codewords. Further, each codeword comprises a plurality of redundant bits.

At step **803**, the read-before-write operation executes by reading a codeword. Subsequently, at step **804**, the read-before-write operation maps defective bits in the codeword to redundant bits for the word based on a mapping scheme.

At step **805**, the defective bits in the codeword are replaced with a corresponding mapped redundant bit.

At step **806**, a write operation is executed with corresponding redundant bits in place of the defective bits. Accordingly, the data word can be saved into the memory using both the codeword and corresponding redundant bits.

At step **807**, verification is performed that the write operation executed correctly by performing another read operation to read out the data word stored in the codeword and corresponding redundant bits.

FIG. **8**B shows a flowchart **810** of an exemplary method for correcting bit defects in a STT-MRAM memory array during a read operation in accordance with embodiments of the present invention.

At step **811**, a read operation comprises reading a codeword in an STT-MRAM memory, wherein the STT-MRAM memory comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bits.

At step **812**, the read operation maps defective bits in the codeword to redundant bits for the word based on a mapping scheme.

At step **813**, the defective bits in the codeword are replaced with a corresponding redundant bit in accordance with the mapping scheme.

At step **814**, an ECC operation is performed on the data word read out to correct for transient defects not corrected using the plurality of redundant bits.

FIG. **9** illustrates an apparatus for correcting bit defects in a STT-MRAM memory array **900** in accordance with embodiments of the present invention.

Shown in FIG. **9**, is the memory array **900** comprising a codewords array **901** with the corresponding redundant bits **902** allocated for each codeword. FIG. **9** also illustrates the logic **903** that implements the mapping scheme between the codewords and the redundant bits.

Write logic **906** implements a method for correcting bit defects in a STT-MRAM memory array during a write operation (as discussed in conjunction with FIG. **8**A). Read logic **907** implements a method for correcting bit defects in a STT-MRAM memory array during a read operation (as discussed in conjunction with FIG. **8**B).

Further, FIG. **9** illustrates ECC logic **908** that operates in conjunction with the read and write logic. Also, the memory comprises address **920** and data bus lines **921** that communicate with the processor. Further, control bus **922** is illustrates, wherein the control bus would receive commands regarding a read/write operation, etc.

FIG. **10** shows a flowchart **1010** of an exemplary method for correcting bit defects in a STT-MRAM memory array in accordance with embodiments of the present invention.

At step **1011**, a margin area is determined associated with a resistance distribution for a memory array, e.g., STT-MRAM memory array. A read operation is performed on the memory array to characterize the resistance distribution. The resistance distribution comprises a distribution of bit-cell resistances for all bits comprising the STT-MRAM memory array, wherein the distribution of bit-cell resistances comprises a distribution of acceptable high resistance bits and a distribution of acceptable low resistance bits, e.g., regions Rlow and Rhigh shown in FIG. **7**A. As discussed in connection with FIGS. **7**A and **7**B, the bit-cell resistance distribution comprises region **620**, wherein certain bit-cells in the array have resistances that fall in the region **620**. This region is also known as the "margin area." The margin area is typically a bandwidth of resistances centered around reference point **631**, wherein a sense amplifier will not be able to accurately distinguish a resistance within the margin area as either Rhigh or Rlow. In other words, typically, bit-cells with resistances that fall within margin area **620** (either directly in the region overlapping the R-low **622** and R-high curves **624** or in close proximity to the overlap region) will likely not be read accurately by a sense amplifier at high speeds

Once the margin area is determined, at step **1012**, the method comprises forcing the bit-cell resistances of memory bit-cells associated with the margin area to short circuits in order to widen a window between the distribution of acceptable high resistance bits and acceptable low resistance bits. Note that steps **1011** to **1012** can occur during product testing or characterization.

Finally, at step **1013**, the method comprises replacing each of the short-circuited memory bit-cells with a corresponding redundant bit in the codeword associated with the short-circuited memory bit-cell. For example, during memory operation, the replacing can occur in accordance with a mapping scheme. In other words, for example, a redundant bit is mapped to the short-circuited bit in the codeword in accordance with the position of the short-circuited memory bit-cell. During memory operation then, a redundant bit is stored in the associated codeword in lieu of the short-circuited bit in accordance with the mapping. As discussed above, a mapping scheme will dictate the manner in which the redundant bits get mapped to the short-circuited bit-cells.

FIG. **11** shows a flowchart **1110** of another exemplary method for correcting bit defects in a STT-MRAM memory array in accordance with embodiments of the present invention.

At step **1111**, the resistance distribution of a memory array, e.g., STT-MRAM is characterized. In other words, a read operation is performed on the memory array to characterize the resistance distribution.

At step **1112**, all bit-cells in the memory array that cannot be easily characterized are short-circuited. As noted above, such defects, which are neither shorts nor open circuits, are not detectable during user read or verify operations. Examples of such defects include stuck bits, waterfalls, shunts and low tunnel magnetoresistance (TMR) bits. Note that steps **1111** to **1112** can occur during product testing or characterization.

At step **1113**, the method comprises replacing each of the short-circuited memory bit-cells with a corresponding redundant bit in the codeword associated with the short-circuited memory bit-cell. For example, during memory operation, the replacing can occur in accordance with a mapping scheme. In other words, for example, a redundant bit is mapped to the short-circuited bit in the codeword in accordance with the position of the short-circuited memory bit-cell. During memory operation then, a redundant bit is stored in the associated codeword in lieu of the short-circuited bit in accordance with the mapping. As discussed above, a mapping scheme will dictate the manner in which the redundant bits get mapped to the short-circuited bit-cells.

The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments in this patent document are not considered as being limited by the foregoing description and drawings.

We claim:

1. A method for correcting bit defects in a memory array, the method comprising:

determining, during a characterization stage, a resistance distribution for the memory array by classifying a state of each bit-cell in the memory array, wherein the memory array comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bits;

determining bit-cells of the resistance distribution that are ambiguous, wherein ambiguous bit-cells have ambiguous resistances;

forcing the ambiguous bit-cells to short circuits; and

replacing each short-circuited ambiguous bit-cell with a corresponding redundant bit from an associated codeword.

2. The method of claim **1**, wherein the memory array is an STT-MRAM memory array.

3. The method of claim **1**, wherein the replacing comprises:

determining a position of a short-circuited bit-cell in an associated codeword; and

mapping a corresponding redundant bit of an associated plurality of redundant bits in the associated codeword to the short-circuited bit-cell in accordance with a bit position of the short-circuited bit-cell in the associated codeword.

4. The method of claim **3**, wherein the mapping is performed in accordance with a mapping scheme.

5. The method of claim **4**, wherein in the mapping scheme a short-circuited bit-cell is replaced with a corresponding redundant bit having a position that is based on the bit position of the short-circuited bit-cell.

6. The method of claim **1**, wherein said state is chosen from a group consisting of: high, low, short or open.

7. The method of claim **1**, wherein the ambiguous bit-cells are selected from a group consisting of: stuck bits; waterfall bits; shunted bits; and low tunnel magnetoresistance (TMR) bits.

8. An apparatus for correcting bit defects, the apparatus comprising:

a processor; and

a memory array comprising a plurality of codewords, wherein each codeword comprises a respective plurality of redundant bits, and wherein the processor is configured to:

determine, during a characterization stage, a resistance distribution for the memory array by classifying a state of each bit-cell in the memory array;

determine bit-cells of the resistance distribution that are ambiguous, wherein ambiguous bit-cells have ambiguous resistances;

force the ambiguous bit-cells to short circuits; and

replace each short-circuited ambiguous bit-cell with a corresponding redundant bit from an associated codeword.

9. The apparatus of claim **8**, wherein the memory array is an STT-MRAM memory array.

10. The apparatus of claim **8**, wherein to replace each short-circuited ambiguous bit-cell, the processor is configured to:

determine a position of a short-circuited bit-cell in an associated codeword; and

map the corresponding redundant bit of an associated plurality of redundant bits of the associated codeword to the short-circuited bit-cell in accordance with the position of the short-circuited bit-cell.

11. The apparatus of claim **10**, wherein the processor is further configured to map the corresponding redundant bit in accordance with a mapping scheme.

12. The apparatus of claim **11**, wherein in the mapping scheme the short-circuited bit-cell is replaced with the corresponding redundant bit based on the position of the short-circuited bit-cell.

13. The apparatus of claim **8**, wherein said state is chosen from a group consisting of:

high, low, short or open.

14. The apparatus of claim **8**, wherein the ambiguous bit-cells are selected from a group consisting of: stuck bits; waterfall bits; shunted bits; and low tunnel magnetoresistance (TMR) bits.

15. A method for correcting bit defects in a memory, the method comprising:

determining, during a characterization stage, a resistance distribution for a memory array by classifying a state of each bit-cell in the memory array, wherein the memory array comprises a plurality of codewords, wherein each codeword comprises a plurality of redundant bit-cells;

determining bit-cells of the resistance distribution that are defective;

forcing defective bit-cells to short circuits; and

replacing each short-circuited defective bit-cell with a corresponding redundant bit-cell from an associated codeword.

16. The method of claim **15**, wherein the memory array is a STT-MRAM memory array.

17. The method of claim **15**, wherein the defective bit-cells are ambiguous bit-cells having ambiguous resistances between being high or low bits.

18. The method of claim **17**, wherein the ambiguous bit-cells are selected from a group consisting of: stuck bits; waterfall bits; shunted bits; and low tunnel magnetoresistance (TMR) bits.

19. The method of claim **15**, wherein the defective bit-cells have a substantially higher WER compared to other bit-cells in the memory array.

20. The method of claim **15**, wherein the defective bit-cells retain their data for lower than a minimum retention period.

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