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(54) **METHODS FOR FORMING A SEMICONDUCTOR STRUCTURE AND RELATED SEMICONDUCTOR STRUCTURES**

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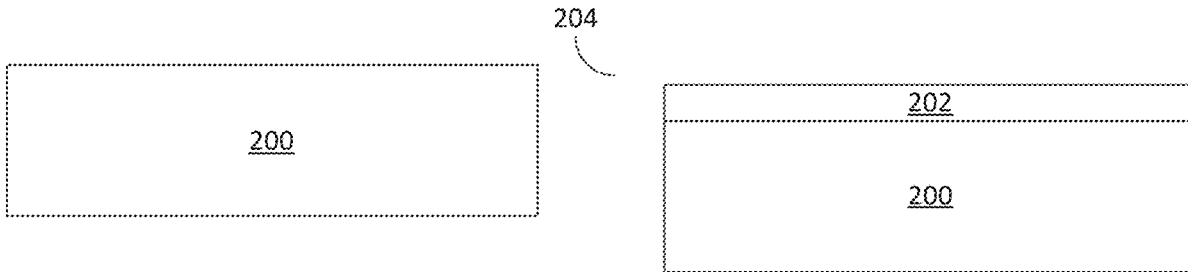
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(57) **ABSTRACT**

A method for forming a forming a semiconductor structure is disclosed. The method may include: forming a silicon oxide layer on a surface of a substrate, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer directly on the silicon oxide layer, and depositing a germanium (Ge) layer directly on the silicon germanium (Si_{1-x}Ge_x) seed layer. Semiconductor structures including a germanium (Ge) layer deposited on silicon oxide utilizing an intermediate silicon germanium (Si_{1-x}Ge_x) seed layer are also disclosed.

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17 Claims, 4 Drawing Sheets



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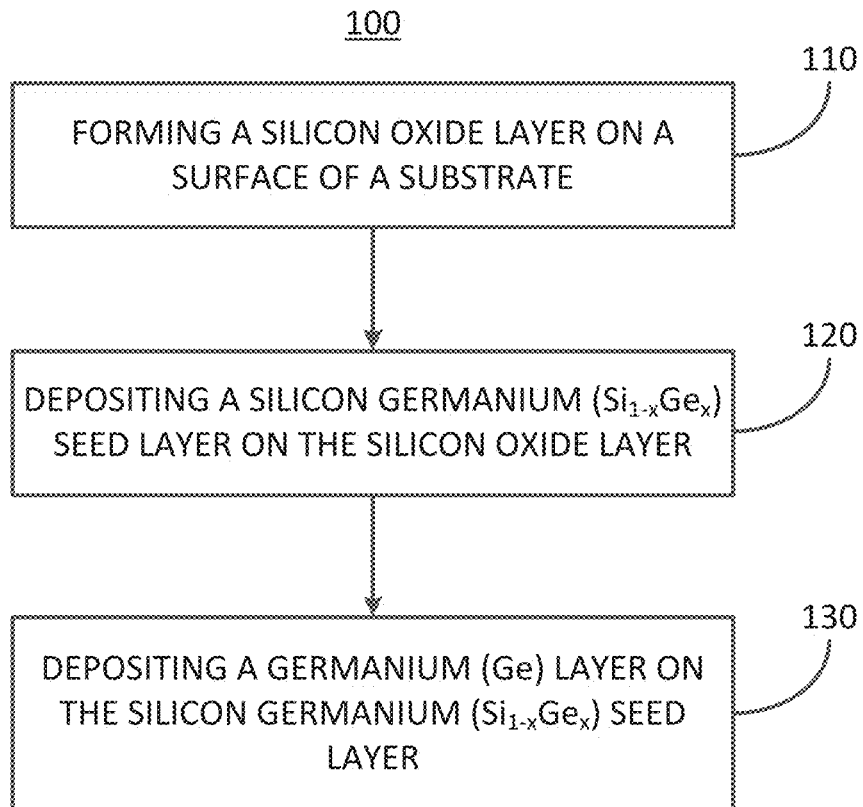


FIG. 1



FIG. 2A

204

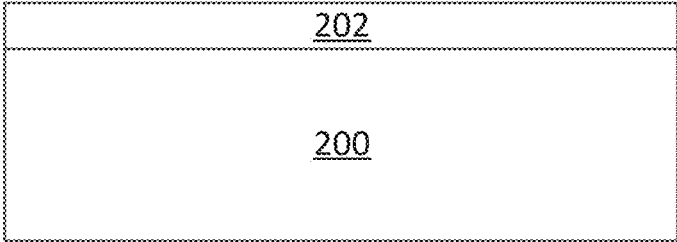


FIG. 2B

208

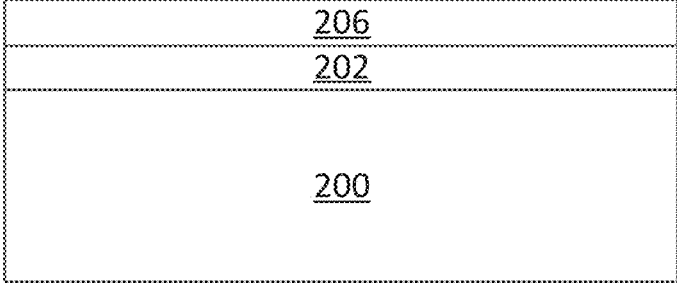


FIG. 2C

210

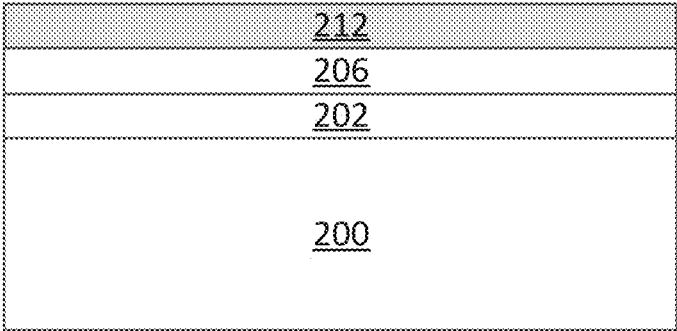


FIG. 2D

214

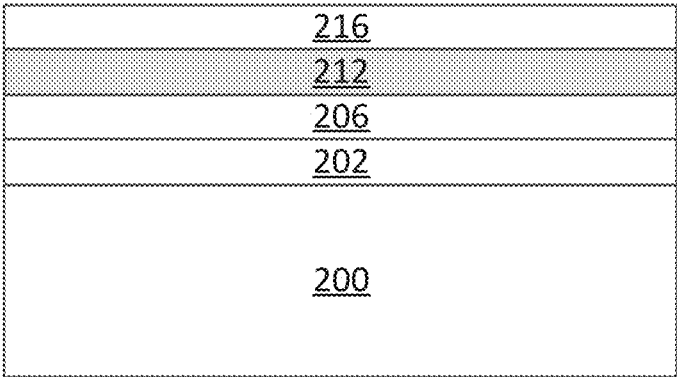


FIG. 2E

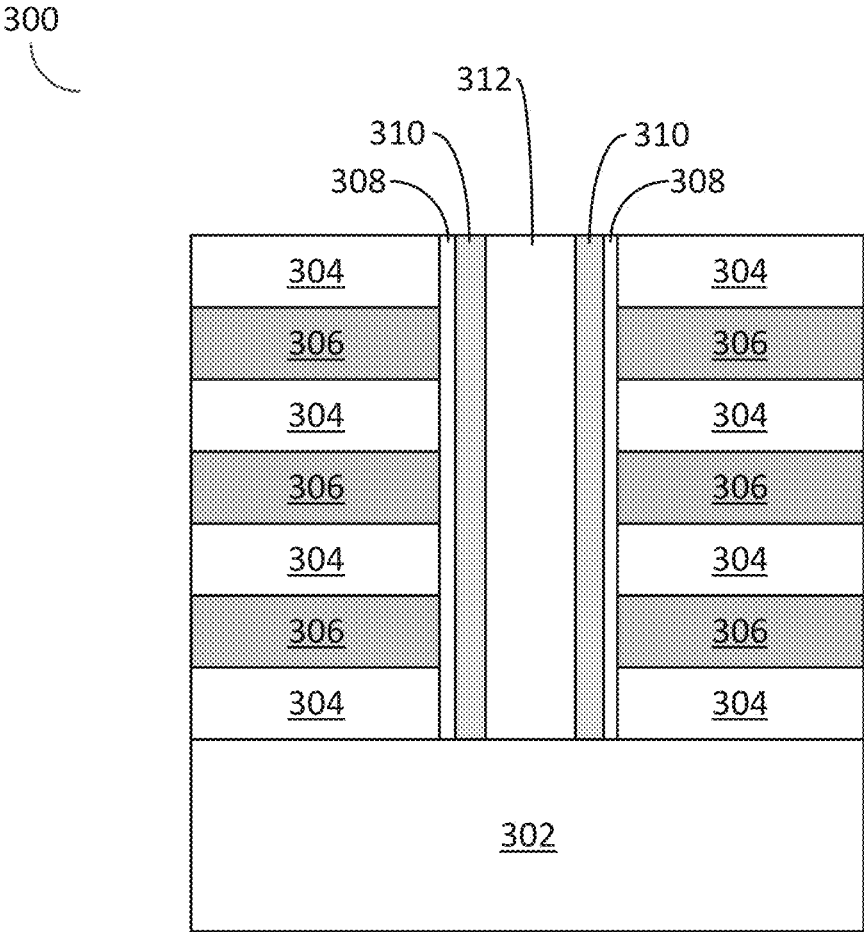


FIG. 3

1

METHODS FOR FORMING A SEMICONDUCTOR STRUCTURE AND RELATED SEMICONDUCTOR STRUCTURES

FIELD OF INVENTION

The present disclosure generally relates to methods for forming a semiconductor structure and particular to methods for depositing a germanium layer over a silicon oxide layer utilizing an intermediate silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) seed layer. The present disclosure also generally relates to semiconductor structures and particularly semiconductor structures including a germanium layer deposited over a silicon oxide layer utilizing an intermediate silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) seed layer.

BACKGROUND OF THE DISCLOSURE

As semiconductor devices continue to decrease in size in advanced technology nodes, a number of challenges arise in developing higher performance devices. One approach to increase the performance of semiconductor devices is to increase the carrier mobility, i.e., electrons and/or holes, in the channel region of the device. Although it is possible to obtain higher carrier mobilities with strained silicon, much higher mobilities may be achieved by using a different semiconductor material in the channel region other than silicon. For example, hole mobility in germanium (Ge) is known to be much higher than in silicon. However, using a bulk material other than silicon presents a huge integration and device design challenge. For example, diffusion enhancement of n-type dopants in germanium (Ge) makes it very challenging to obtain advantageous ultra-shallow junctions. Moreover, the majority of process steps commonly utilized in silicon device fabrication, such as silicidation and surface cleaning, are currently unsatisfactory for high mobility materials. As a result, it continues to be easier and more cost effective to use silicon as a bulk material and use the high mobility materials only in the channel regions.

In order to achieve a germanium (Ge) channel in a semiconductor device structure, such as, for example, a field effect transistor, or memory element, deposition methods may be utilized to deposit the germanium (Ge) high mobility channel over a suitable substrate. In some semiconductor device applications it may be necessary to deposit a germanium layer over the surface of a silicon oxide (e.g., SiO_2). However, germanium (Ge) deposition directly on a silicon oxide surface may be problematic because the common germanium deposition processes, utilizing germane (GeH_4) as the germanium precursor, do not deposit germanium directly on silicon oxide surfaces. It has been theorized, that the tendency of germanium to refrain from depositing on a silicon oxide surface may be due to a low density of germanium absorption sites available on a silicon oxide surface, such as, silicon dioxide (SiO_2).

Accordingly, methods for forming a germanium layer over a silicon oxide surface are desirable for fabricating semiconductor structures including a high mobility germanium (Ge) channel region.

SUMMARY OF THE DISCLOSURE

In accordance with at least one embodiment of the disclosure, a method for forming a semiconductor structure is disclosed. The method may comprise: forming a silicon oxide layer on a surface of a substrate; depositing a silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) seed layer directly on the silicon

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oxide layer; and depositing a germanium layer directly on the silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) seed layer.

The embodiments of the disclosure may also provide semiconductor structures comprising: a silicon oxide layer disposed directly on the surface of a substrate; a silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) seed layer disposed directly on the silicon oxide layer; and a germanium (Ge) layer disposed directly on the silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) seed layer.

For the purpose of summarizing the invention and the advantages achieved over the prior art, certain objects and advantages of the invention have been described herein above. Of course, it is to be understood that not necessarily all such objects or advantages may be achieved in accordance with any particular embodiment of the invention. Thus, for example, those skilled in the art will recognize that the invention may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught or suggested herein without necessarily achieving other objects or advantages as may be taught or suggested herein.

All of these embodiments are intended to be within the scope of the invention herein disclosed. These and other embodiments will become readily apparent to those skilled in the art from the following detailed description of certain embodiments having reference to the attached figures, the invention not being limited to any particular embodiment(s) disclosed.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

While the specification concludes with claims particularly pointing out and distinctly claiming what are regarded as embodiments of the invention, the advantages of embodiments of the disclosure may be more readily ascertained from the description of certain examples of the embodiments of the disclosure when read in conjunction with the accompanying drawing, in which:

FIG. 1 illustrates a process flow diagram illustrating an exemplary method in accordance with the embodiments of the disclosure;

FIGS. 2A, 2B, 2C, 2D and 2E illustrate cross sectional schematic diagrams of an exemplary process flow in accordance with the embodiments of the disclosure;

FIG. 3 illustrates a semiconductor device structure including a germanium (Ge) layer formed by the embodiments of the disclosure.

It will be appreciated that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve understanding of illustrated embodiments of the present disclosure.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Although certain embodiments and examples are disclosed below, it will be understood by those in the art that the invention extends beyond the specifically disclosed embodiments and/or uses of the invention and obvious modifications and equivalents thereof. Thus, it is intended that the scope of the invention disclosed should not be limited by the particular disclosed embodiments described below.

As used herein, the term “substrate” may refer to any underlying material or materials that may be used, or upon which, a device, a circuit or a film may be formed.

As used herein, the term “silicon germanium” and “Si_{1-x}Ge_x” may refer to an alloy of silicon and germanium, wherein the ratio of germanium to silicon may range as $1 \geq x \geq 0$.

As used herein, the term “chemical vapor deposition” may refer to any process wherein a substrate is exposed to one or more volatile precursors, which react and/or decompose on a substrate surface to produce a desired deposition.

In the specification, it will be understood that the term “on” or “over” may be used to describe a relative location relationship, another element or layer may be directly on the mentioned layer, or another layer (an intermediate layer) or element may be intervened therebetween, or a layer may be disposed on a mentioned layer but not completely cover a surface of the mentioned layer. Therefore, unless the term “directly” is separately used, the term “on” or “over” will be construed to be a relative concept. Similarly to this, it will be understood the term “under,” “underlying,” or “below” will be construed to be relative concepts.

The embodiments of the disclosure may include methods for forming a semiconductor structure and particularly methods for depositing a germanium (Ge) layer on a silicon oxide layer utilizing an intermediate silicon germanium (Si_{1-x}Ge_x) seed layer. For example, the silicon germanium (Si_{1-x}Ge_x) seed layer may be deposited directly on the surface of a silicon oxide layer and the germanium (Ge) layer may be deposited directly on the silicon germanium (Si_{1-x}Ge_x) seed layer, thereby enabling the deposition of a germanium layer on a silicon oxide layer.

Prior art solutions for depositing a germanium (Ge) layer on a silicon oxide may have a number disadvantages which are overcome by the methods and structures disclosed herein. A prior method for depositing a germanium (Ge) layer on a silicon oxide surface may employ an intermediate silicon (Si) seed layer disposed directly on the surface of the silicon oxide layer, between the silicon oxide layer and the germanium layer. However, the use of a silicon (Si) seed layer may require a substantial thickness of the silicon seed layer, such as, for example, a silicon seed layer thickness of between 1 nanometers and 5 nanometers. Such a thickness of a silicon seed layer directly on the silicon oxide surface may be disadvantageous in certain semiconductor device structures. An additional prior method for depositing a germanium (Ge) layer on a silicon oxide surface may utilize digermane (Ge₂H₆) as the germanium precursor for the deposition of the germanium layer. Utilizing digermane (Ge₂H₆) as the germanium precursor for the deposition of the germanium layer may allow for the direct deposition of a germanium layer on the surface of the silicon oxide layer. However, the digermane (Ge₂H₆) precursor may be prohibitively expensive and therefore may not be a cost effective solution to the problem of depositing a germanium (Ge) layer over a silicon oxide (e.g., SiO₂) layer.

The embodiments of the disclosure may include methods for forming a semiconductor structure, the methods may comprise: forming a silicon oxide layer on a surface of a substrate, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer directly on the silicon oxide layer, and depositing a germanium (Ge) layer directly on the silicon germanium (Si_{1-x}Ge_x) seed layer.

The methods of the disclosure are described in greater detail with reference to FIG. 1 which comprises a process flow diagram illustrating an exemplary method 100 and with

reference to FIG. 2A-2E which illustrate cross sectional schematic diagrams of the process flow of exemplary method 100.

The method 100 may commence with a process block 110 comprising, forming a silicon oxide layer on a surface of a substrate. In some embodiments, forming a silicon oxide layer on a surface of a substrate may comprise providing a substrate, such as, substrate 200 of FIG. 2A. In some embodiments of the disclosure, the substrate 200 may comprise a planar substrate or a patterned substrate. Patterned substrates may comprise substrates that may include semiconductor device structures formed into or onto a surface of the substrate, for example, the patterned substrates may comprise partially fabricated semiconductor device structures, such as, for example, transistors and/or memory elements. In some embodiments, the substrate may contain monocrystalline surfaces and/or one or more secondary surfaces that may comprise a non-monocrystalline surface, such as a polycrystalline surface and an amorphous surface. Monocrystalline surfaces may comprise, for example, one or more of silicon (Si), silicon germanium (SiGe), germanium tin (GeSn), or germanium (Ge). Polycrystalline or amorphous surfaces may include dielectric materials, such as oxides, oxynitrides or nitrides, such as, for example, silicon oxides and silicon nitrides.

In some embodiment of the disclosure, forming a silicon oxide on a surface of the substrate may comprise forming a silicon dioxide (SiO₂) 202 on the surface of the substrate 200 utilizing either a deposition process or a growth process, see semiconductor structure 204 of FIG. 2B. In some embodiment, a silicon dioxide (SiO₂) 202 may be formed on the surface of the substrate 200 by a thermal oxidation growth process comprising, heating the substrate 200 to temperature of between 800° C. and 1200° C. and further exposing the substrate 200 to water vapor or molecular oxygen (O₂). In some embodiments, the silicon dioxide 202 may be deposited over the surface of the substrate 200. For example, the substrate 200 may be heated to a temperature greater than approximately 400° C. and exposed to tetraethyl orthosilicate (TEOS) vapor to deposit a layer of silicon dioxide 202 over the surface of the substrate 200.

The method 100 may continue with process block 120 comprising, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer on the silicon oxide layer. In some embodiments of the disclosure, and as illustrated by semiconductor structure 208 of FIG. 2C, the silicon germanium (Si_{1-x}Ge_x) seed layer 206 may be deposited directly on the silicon oxide layer 202, such that the silicon oxide layer 202 is disposed directly between the substrate 200 and the silicon germanium (Si_{1-x}Ge_x) seed layer 206.

In some embodiments of the disclosure, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer may comprise, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer by chemical vapor deposition process. For example, the semiconductor structure 204 of FIG. 2B comprising the substrate 200, with the silicon oxide 202 thereon, may be provided into a reaction chamber and the substrate may be heated to a process temperature within the reaction chamber. As a non-limiting example, the reaction chamber may comprise a reaction chamber of a chemical vapor deposition system. Embodiments of the present disclosure may include deposition processes that may be performed in a chemical vapor deposition system available from ASM International N.V. under the name Intrepid™ XP or Epsilon®. However, it is also contemplated that other reaction chambers and alterna-

tive chemical vapor deposition systems from other manufacturers may also be utilized to perform the embodiments of the present disclosure.

In some embodiments of the disclosure, the semiconductor structure **204** comprising, the substrate **200** with the silicon oxide **202** (e.g., SiO₂) disposed thereon, may be heated to a desired substrate temperature within the reaction chamber of the chemical vapor deposition system. In some embodiments, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer **206** may comprise depositing the silicon germanium (Si_{1-x}Ge_x) seed layer **206** at a substrate temperature of less than approximately 600° C., or less than approximately 500° C., or less than approximately 400° C., or less than approximately 300° C., or even less than approximately 200° C. In some embodiments, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer **206** may comprise depositing the silicon germanium (Si_{1-x}Ge_x) seed layer at a substrate temperature of between approximately 250° C. and approximately 500° C.

In some embodiments, the pressure within the reaction chamber of the chemical vapor deposition system may be regulated to a desired set point during the deposition of the silicon germanium (Si_{1-x}Ge_x) seed layer **206**. For example, in some embodiments, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer comprises, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer at a reaction chamber pressure of between approximately 10 Torr and approximately 760 Torr.

Once the substrate is at a desired process temperature and the reaction chamber pressure is set to a desired set point, one or more precursor gases may be flowed into the reaction chamber of the chemical vapor deposition system to initiate the deposition of the silicon germanium (Si_{1-x}Ge_x) seed layer **206**.

In some embodiments, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer may comprise, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer utilizing germane (GeH₄) as the germanium precursor. For example, the germane (GeH₄) may be flowed into the reaction chamber at a flow rate greater than 10 sccm, or greater than 50 sccm, or greater than 100 sccm, or even greater than 200 sccm. In some embodiments of the disclosure, alternative germanium sources may be utilized as the germanium precursor, such as, for example, digermane (Ge₂H₆), trigermane (Ge₃H₈), or germylsilane (GeH₆Si). In some embodiments, the germanium precursor may comprise a Si—Ge-hydride precursor, such as, (H₃Ge)_xSiH_{4-x}, wherein x=1-4, or (H₃Si)_xGeH_{4-x}, where x=1-4.

In some embodiments, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer may comprise depositing the silicon germanium (Si_{1-x}Ge_x) seed layer utilizing trisilane (Si₃H₈) as the silicon precursor. For example, the trisilane (Si₃H₈) may be flowed into the reaction chamber at a flow rate greater than 10 sccm, or greater than 50 sccm, or greater than 100 sccm, or even greater than 200 sccm. In some embodiments of the disclosure, alternative silicon sources may be utilized as the silicon precursor, such as, for example, silane (SiH₄), disilane (Si₂H₆), tetrasilane (Si₄H₁₀), isopentasilane (Si₅H₁₂), neopentasilane (Si₅H₁₂), or dichlorosilane (DCS). In some embodiments, the silicon source may comprise a higher order silane precursor with the general empirical formula Si_xH_(2x+2).

In some embodiments of the disclosure, the germanium precursor (e.g., germane) and the silicon precursor (e.g., trisilane) are co-flowed into the reaction chamber, i.e., the silicon precursor and the germanium precursor flow into the reaction chamber simultaneously.

In some embodiments of the disclosure, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer may further comprise, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer with a germanium composition (x) less than 0.30, or less than 0.20, or less than 0.10, or less than 0.05, or even less than 0.01. In some embodiments, the germanium composition of the silicon germanium (Si_{1-x}Ge_x) seed layer may be between 0.01 and 0.30. In some embodiments, the germanium composition of the silicon germanium (Si_{1-x}Ge_x) seed layer may be between 0.10 and 0.30.

In some embodiments of the disclosure, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer may further comprise, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer to a thickness of less than 50 nanometers, or less than 40 nanometers, or less than 30 nanometers, or less than 20 nanometers, or less than 10 nanometers, or less than 5 nanometers, or even less than 3 nanometers. In some embodiments, the silicon germanium (Si_{1-x}Ge_x) seed layer may have thickness between approximately 3 nanometers and approximately 10 nanometers.

In some embodiments of the disclosure, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer may further comprise, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer with an amorphous crystalline structure. For example, a silicon germanium (Si_{1-x}Ge_x) seed layer which comprises an amorphous crystalline structure may comprise a material which displays no ordering, or substantially no ordering, of the crystalline structure. In some embodiments, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer may further comprise, depositing the silicon germanium (Si_{1-x}Ge_x) seed layer with a polycrystalline crystalline structure. For example, a silicon germanium (Si_{1-x}Ge_x) seed layer which comprises a polycrystalline crystalline structure may comprise a material which displays short range ordering of the crystalline structure.

The method **100** may continue with process block **130** comprising, depositing a germanium (Ge) layer on the silicon germanium (Si_{1-x}Ge_x) seed layer, as illustrated by the semiconductor structure **210** in FIG. 2D which comprises, the substrate **200**, the silicon oxide layer **202**, the silicon germanium (Si_{1-x}Ge_x) seed layer **206**, and germanium (Ge) layer **212**. For example, and as illustrated in FIG. 2D, depositing the germanium layer may comprise depositing the germanium (Ge) layer **212** directly on the silicon germanium (Si_{1-x}Ge_x) seed layer **206**. Not to be bound by any particular theory, but it is believed that depositing the germanium (Ge) layer **212** directly on a silicon germanium (Si_{1-x}Ge_x) seed layer **206** may result in a germanium (Ge) layer **212** with higher carrier mobility, which may consequently result in a semiconductor device structure with improved performance. For example, the germanium (Ge) layer **212** may have a carrier mobility greater than 10 cm²/(Vs), or greater than 20 cm²/(Vs), or greater than 30 cm²/(Vs), or greater than 40 cm²/(Vs), or even greater than 50 cm²/(Vs). In some embodiments of the disclosure, the germanium (Ge) layer may comprise a channel region of a device structure, consequently increasing the mobility in the germanium (Ge) layer **212** may result in a semiconductor device structure with improved performance.

In some embodiments of the disclosure, the germanium (Ge) layer **212** may be deposited in the same reaction chamber, of a chemical vapor deposition system, as utilized to deposit the silicon germanium (Si_{1-x}Ge_x) seed layer. For example, the semiconductor structure **208** of FIG. 2C may be disposed in a reaction chamber and heated to a desired process temperature. Therefore, in some embodiments, depositing the germanium layer **212** comprises,

depositing the germanium layer **212** at a substrate temperature of less than approximately 500° C., or less than approximately 400° C., or less than approximately 300° C., or less than approximately 200° C. In some embodiments, depositing the germanium layer **212** may comprise, depositing the germanium layer **212** at a substrate temperature between approximately 300° C. and approximately 350° C. In addition to heating the substrate to a desired process temperature, the reaction chamber may be set to a desired process pressure, such as, for example, a process pressure between approximately 10 Torr and approximately 760 Torr.

In some embodiments, depositing the germanium (Ge) layer **212** may comprise, depositing the germanium (Ge) layer utilizing germane (GeH₄) as the germanium precursor. For example, the germane (GeH₄) may be flowed into the reaction chamber at a flow rate greater than 10 sccm, or greater than 50 sccm, or greater than 100 sccm, or even greater than 200 sccm. In some embodiments of the disclosure, alternative germanium sources may be utilized as the germanium precursor, such as, for example, digermane (Ge₂H₆), trigermane (Ge₃H₈), or germylsilane (GeH₆Si).

In some embodiments of the disclosure, depositing the germanium (Ge) layer may further comprise, depositing the germanium (Ge) layer with an amorphous crystalline structure. For example, a germanium (Ge) layer which comprises an amorphous crystalline structure may comprise a material which displays no ordering, or substantially no ordering, of the crystalline structure. In some embodiments, depositing the germanium (Ge) layer may further comprise, depositing the germanium (Ge) layer with a polycrystalline crystalline structure. For example, a germanium (Ge) layer which comprises a polycrystalline crystalline structure may comprise a material which displays short range ordering of the crystalline structure. In some embodiments, depositing the germanium (Ge) layer may further comprise, depositing the germanium (Ge) layer with a substantially monocrystalline crystalline structure. For example, a germanium (Ge) layer which comprises a substantially monocrystalline crystalline structure may comprise a material which displays long range ordering of the crystalline structure.

In some embodiments of the disclosure, the germanium (Ge) layer may be deposited in an amorphous or polycrystalline state and subsequently converted to a substantially monocrystalline crystalline structure. For example, the germanium (Ge) layer may be deposited as an amorphous or polycrystalline material and subsequent subjected to a recrystallization process to convert the germanium (Ge) layer to a substantially monocrystalline material. Therefore, the embodiments of the disclosure may further comprise, heating the as-deposited germanium (Ge) layer to a recrystallization temperature greater than approximately 500° C., or greater than approximately 600° C., or even greater than approximately 700° C.

In some embodiments of the disclosure, depositing the germanium (Ge) layer may further comprise, depositing the germanium (Ge) layer to a thickness of less than 50 nanometers, or less than 40 nanometers, or less than 30 nanometers, or less than 20 nanometers, or less than 10 nanometers, or less than 5 nanometers, or even less than 3 nanometers. In some embodiments, the germanium (Ge) layer may have thickness between approximately 5 nanometers and approximately 15 nanometers.

The embodiments of the disclosure may include an additional process step, as illustrated by the semiconductor device structure **214** of FIG. 2E, wherein the method of forming a semiconductor structure further comprises, depositing an additional silicon dioxide (SiO₂) layer **216** on the

germanium (Ge) layer **212**. For example, in some embodiments the silicon dioxide (SiO₂) layer **216** may be deposited directly on the germanium (Ge) layer **212**, such that the germanium (Ge) layer **212** is disposed directly between the silicon dioxide (SiO₂) layer **216** and the silicon germanium (Si_{1-x}Ge_x) seed layer **206**. In some embodiments, the silicon dioxide layer **216** may have a thickness greater than 1 nanometer, or greater than 5 nanometers, or even greater than 10 nanometers.

The embodiments of the disclosure may also provide semiconductor structures, such as, for example, the semiconductor structure **214** of FIG. 2E. In more detail, the semiconductor structure **214** may comprise, a silicon dioxide (SiO₂) layer **202** disposed directly on the surface of a substrate **200**, a silicon germanium (Si_{1-x}Ge_x) seed layer **206** disposed directly on the silicon dioxide layer **202**, and a germanium (Ge) layer **212** disposed directly on the silicon germanium (Si_{1-x}Ge_x) seed layer **206**.

In some embodiments of the disclosure the silicon germanium (Si_{1-x}Ge_x) seed layer **206** may have a germanium composition (x) between approximately 0.01 and approximately 0.30. In some embodiments, the silicon germanium (Si_{1-x}Ge_x) seed layer **206** may have a thickness between approximately 3 nanometers and approximately 10 nanometers.

In some embodiments of the disclosure, the germanium (Ge) layer **200** may have a thickness between approximately 5 nanometers and approximately 15 nanometers. In some embodiments, the germanium (Ge) layer **212** may comprise a channel region of semiconductor device structure, wherein the term “channel region” may refer to a region of semiconductor device in which carrier flow may be controlled, e.g., by biasing of a gate electrode. In some embodiment, the germanium (Ge) layer may have a carrier mobility of greater than 30 cm²(Vs).

In some embodiments of the disclosure, the semiconductor structure **214** may further comprise an additional silicon dioxide (SiO₂) layer **216** disposed directly on the germanium (Ge) layer **212**.

It is should be noted that the semiconductor structure **214** and particularly the silicon germanium (Si_{1-x}Ge_x) seed layer **206** as well as the germanium (Ge) are formed by a deposition process. Therefore the semiconductor structure **214** does not comprise a bonded semiconductor structure whereby the silicon germanium (Si_{1-x}Ge_x) seed layer **206** as well as the germanium (Ge) layer **212** are formed over a silicon oxide layer **202** via a bonding process utilizing a bonding interface disposed between the substrate **200** and the germanium (Ge) layer **212**.

The methods and semiconductor structures disclosed herein may be utilized in a number of semiconductor device applications. As a non-limiting example embodiment of the current disclosure, FIG. 3 illustrates a partially fabricated semiconductor device structure **300** which may comprise, a partially fabricated memory element, such as, a vertical NAND memory element. In more detail, partially fabricated semiconductor device structure **300** may comprise a substrate **302** (e.g., bulk silicon) and disposed over the substrate **302** may be alternating layers of silicon oxide **304** and silicon nitride **306**. Disposed directly on a surface of the silicon nitride layers **306** and the silicon oxide layers **304** is one or more silicon germanium (Si_{1-x}Ge_x) seed layers **308** deposited utilizing the embodiments disclosed herein. In addition, disposed directly on a surface of the one or more silicon germanium (Si_{1-x}Ge_x) seed layers **208** is one or more germanium (Ge) layers **310**, deposited utilizing the embodiments disclosed herein. Finally, the partially fabricate semi-

conductor device structure **300** may comprise a silicon dioxide (SiO₂) layer disposed on the one or more germanium (Ge) layers **312**.

The example embodiments of the disclosure described above do not limit the scope of the invention, since these embodiments are merely examples of the embodiments of the invention, which is defined by the appended claims and their legal equivalents. Any equivalent embodiments are intended to be within the scope of this invention. Indeed, various modifications of the disclosure, in addition to those shown and described herein, such as alternative useful combination of the elements described, may become apparent to those skilled in the art from the description. Such modifications and embodiments are also intended to fall within the scope of the appended claims.

What is claimed is:

1. A method for forming a semiconductor structure, the method comprising:

forming a silicon oxide layer on a surface of a substrate; using a chemical vapor deposition process, depositing a silicon germanium (Si_{1-x}Ge_x) seed layer, where x is between 0.01 and 0.3, at a temperature between about 250° C. and about 500° C. directly on the silicon oxide layer; and depositing a germanium (Ge) layer directly on the silicon germanium (Si_{1-x}Ge_x) seed layer, wherein the germanium layer has a thickness of between 5 nanometers to 15 nanometers, wherein the silicon germanium (Si_{1-x}Ge_x) seed layer has a thickness of less than 30 nm, wherein depositing the silicon germanium (Si_{1-x}Ge_x) seed layer comprises flowing trisilane (Si₃H₈), tetrasilane (Si₄H₈), isopentasilane (Si₅H₁₂), or neopentasilane (Si₅H₁₂) as a silicon precursor, and wherein the silicon germanium (Si_{1-x}Ge_x) seed layer is amorphous, and wherein depositing the silicon germanium (Si_{1-x}Ge_x) seed layer further comprises, depositing the silicon germanium (Si_{1-x}Ge_x) seed at a reaction chamber pressure of between approximately 10 Torr and approximately 760 Torr.

2. The method of claim **1**, wherein x is less than 0.2.

3. The method of claim **1**, wherein depositing the silicon germanium (Si_{1-x}Ge_x) seed layer further comprises flowing germane (GeH₄) as a germanium precursor.

4. The method of claim **1**, wherein depositing the silicon germanium (Si_{1-x}Ge_x) seed layer further comprises flowing trisilane (Si₃H₈) as a silicon precursor.

5. The method of claim **1**, wherein the silicon germanium (Si_{1-x}Ge_x) seed layer has a thickness of between 1 nanometer to 10 nanometers.

6. The method of claim **1**, wherein the germanium (Ge) layer has an amorphous crystalline structure.

7. The method of claim **1**, wherein depositing the germanium layer occurs at a substrate temperature of between approximately 300° C. and approximately 350° C.

8. The method of claim **1**, wherein depositing the germanium layer further comprises flowing germane (GeH₄) as a germanium precursor.

9. The method of claim **1**, wherein the germanium layer has a polycrystalline crystalline structure.

10. The method of claim **1**, wherein the germanium layer has a substantially monocrystalline crystalline structure.

11. The method of claim **1**, wherein the germanium layer has a carrier mobility of greater than 30 cm²/(Vs).

12. The method of claim **1**, further comprising heating the germanium layer to a temperature greater than 400° C. to recrystallize the germanium layer.

13. The method of claim **1**, wherein the germanium layer comprises a channel region of a semiconductor device structure.

14. The method of claim **1**, further comprising depositing an additional silicon dioxide layer directly on the germanium layer.

15. The method of claim **1**, wherein depositing the silicon germanium (Si_{1-x}Ge_x) seed layer further comprises flowing germane (GeH₄), digermane (Ge₂H₆), or germylsilane (GeH₆Si) as a germanium precursor.

16. The method of claim **1**, wherein the germanium precursor comprise a Si—Ge-hydride precursor.

17. The method of claim **16**, wherein the Si—Ge-hydride precursor comprises (H₃Ge)_xSiH_{4-x}, wherein x=1 to 4 or (H₂Si)_xGe_{4-x}, wherein x=1 to 4.

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