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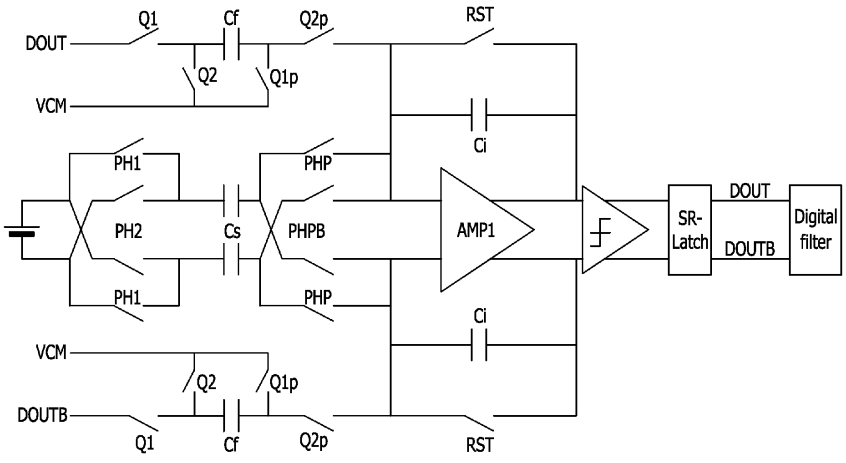
(54) **APPARATUS FOR MEASURING VOLTAGE**

(57) Disclosed herein is an apparatus for measuring a voltage including a primary integrator circuit configured to operate as a first integral stage of a sigma-delta analog-to-digital converter (ADC) circuit by a switching according to a control signal of a controller, a secondary integrator circuit configured to operate as a second integral stage by a switching of the controller, a comparator configured to compare final voltages modulated through the primary integrator circuit and the secondary integrator circuit, and a digital filter configured to delay an output of the comparator by a specified number of clocks according to a switching of the controller, pass the delayed output through a digital-to-analog converter (DAC) to feed the delayed output back to the primary and secondary integrator circuits, and receive the delayed output signal of the comparator as an input, wherein an output of the digital filter becomes a final measured value.

FIG.1



EP 4 372 993 A1

Description

BACKGROUND

FIELD

[0001] Exemplary embodiments of the present disclosure relate to an apparatus for measuring a voltage, and more particularly, to an apparatus for measuring a voltage, which can improve accuracy and reduce a measurement time with a small area, when measuring a voltage of a battery cell or the like, by increasing an order of an analog-to-digital converter (ADC) without increasing the number of amplifiers of the ADC.

DISCUSSION OF THE BACKGROUND

[0002] Generally, in electric vehicles (EVs) and hybrid EVs (HEVs), electric motors are driven by using batteries (or fuel cells).

[0003] Therefore, voltage measurement (or voltage monitoring) of each cell of a battery (or fuel cell) is required for voltage control (e.g., voltage balancing control for minimizing a voltage difference between cells).

[0004] A voltage measurement circuit used in this case generally employs a method of selecting one of a number of battery cells using a multiplexer (MUX), converting a high voltage into a low voltage, and then detecting the low voltage as a digital value using an analog-to-digital converter (ADC). In this case, as described above, since a high voltage element is generally used in order to convert the high voltage into the low voltage, the size of the voltage measurement circuit increases. Therefore, the MUX is used, but a switching element constituting the MUX should also be formed as the high voltage element. Accordingly, there are problems in that the overall size and costs of the apparatus for measuring a voltage increase and a cell voltage sensing speed is limited.

[0005] Accordingly, as shown in FIG. 1, the inventor of the present disclosure has developed a voltage measurement circuit using a primary ADC enabling the use of a low voltage element instead of a high voltage element by integrating a high voltage processing function with an ADC function. However, as shown in FIG. 2, when an order of the ADC is increased so as to improve voltage measurement accuracy and reduce a measurement time, the number of amplifiers AMPs required for a configuration of a circuit is increased so that there is a problem in that an area (size) of the circuit is increased.

[0006] Therefore, there is a need for an apparatus for measuring a voltage, which has an effect of increasing the order of the ADC without increasing the number of amplifier AMPs and thus can relatively reduce the size of the circuit compared to the case of increasing the number of amplifier AMPs, increase an operating speed of the circuit to increase a voltage measurement speed, and improve voltage measurement accuracy.

[0007] The background art of the present disclosure is disclosed in Korean Patent Registration No. 10-1527136 (registered on June 2, 2015 and entitled "Apparatus for Diagnosing Battery of Electric Vehicle and Method Thereof").

SUMMARY

[0008] Various embodiments are directed to an apparatus for measuring a voltage, which can improve accuracy and reduce a measurement time with a small area, when measuring a voltage of a battery cell or the like, by increasing an order of an analog-to-digital converter (ADC) without increasing the number of amplifiers of the ADC.

[0009] In an embodiment, an apparatus for measuring a voltage includes a primary integrator circuit configured to operate as a first integral stage of a sigma-delta analog-to-digital converter (ADC) circuit by a switching according to a control signal of a controller, a secondary integrator circuit configured to operate as a second integral stage by a switching of the controller, a comparator configured to compare final voltages modulated through the primary integrator circuit and the secondary integrator circuit, and a digital filter configured to delay an output of the comparator by a specified number of clocks according to a switching of the controller, pass the delayed output through a digital-to-analog converter (DAC) to feed the delayed output back to the primary and secondary integrator circuits, and receive the delayed output signal of the comparator as an input, wherein an output of the digital filter becomes a final measured value.

[0010] In the present disclosure, the sigma-delta ADC may include an amplifier (AMP) for an integrator, the amplifier (AMP) may be used as an amplifier (AMP) for an integrator of the primary integrator circuit when the primary integrator circuit operates, and the amplifier (AMP) may be used as an amplifier (AMP) for an integrator of the secondary integrator circuit when the secondary integrator circuit operates.

[0011] In the present disclosure, the controller may output an ST signal to operate the primary integrator circuit and output an ND signal to operate the secondary integrator circuit, the primary integrator circuit may operate when the ST signal is in a high section, and the secondary integrator circuit may operate when the ND signal, which is an inverted signal of the ST signal, is in a high section so that the controller may sequentially operate the primary integrator circuit and the secondary integrator circuit.

[0012] In the present disclosure, the primary integrator circuit may include an integrating circuit formed of a first switching capacitor part and the amplifier (AMP); the first switching capacitor part may include first, second, and third switching parts; the first switching part may include first and second switches (SW1, SW2) having first contact points commonly connected to a positive (+) terminal of a battery cell (CELL), and third and fourth switches (SW3, SW4) having first contact points commonly con-

nected to a negative (-) terminal of the battery cell (CELL); and second contact points of the first and third switches (SW1, SW3) may be commonly connected; second contact points of the second and fourth switches (SW2, SW4) may be commonly connected; one ends of insulating capacitors (C1-1, C1-2) having the same value may be connected in series to the second contact points of the first and third switches (SW1, SW3) and to the second contact points of the second and fourth switches (SW2, SW4); and a fifth switch (SW5) and a sixth switch (SW6) may be connected in series to the other ends of the insulating capacitors (C1-1, C1-2) to be connected to one input terminal and the other input terminal of the amplifier (AMP).

[0013] In the present disclosure, the first and fourth switches (SW1, SW4) may be simultaneously switched on/off by an STX1 signal, the second and third switches (SW2, SW3) may be simultaneously switched on/off by an STX2 signal which is an inverted signal of the STX1 signal, and the fifth and sixth switches (SW5, SW6) may be simultaneously switched on/off by the ST signal.

[0014] In the present disclosure, the second switching part may include a seventh switch (SW7) having a first contact point which receives a second positive measured voltage (DAC2P), an eighth switch (SW8) having a first contact point which receives a reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the seventh switch (SW7), an insulating capacitor (C3-1) having one end connected to the second contact point at which the seventh and eighth switches (SW7, SW8) are commonly connected, a ninth switch (SW9) having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor (C3-1), and a tenth switch (SW10) having a first contact point commonly connected to the second contact point of the ninth switch (SW9) and the other end of the insulating capacitor (C3-1) and having a second contact point connected to the one input terminal of the amplifier (AMP), wherein the second positive measured voltage (DAC2P) may be a voltage that is feedback of a positive voltage output from a second DAC (DAC2) after the ST signal is delayed by two clocks through a second D flip-flop of a voltage output circuit.

[0015] In the present disclosure, the seventh and ninth switches (SW7, SW9) may be simultaneously switched on/off by an STQ1 signal, and the eighth and tenth switches (SW8, SW10) may be simultaneously switched on/off by an STQ2 signal.

[0016] In the present disclosure, the third switching part may include an eleventh switch (SW11) having a first contact point which receives a second negative measured voltage DAC2N, a twelfth switch (SW12) having a first contact point which receives the reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the eleventh switch (SW11), an insulating capacitor (C3-2) having one end connected to the second contact point at which the eleventh and twelfth switches (SW11, SW12) are commonly connected, a thirteenth switch (SW13) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C3-2), and a fourteenth switch (SW14) having a first contact point commonly connected to the second contact point of the thirteenth switch (SW13) and the other end of the insulating capacitor (C3-2) and having a second contact point connected to the other input terminal of the amplifier (AMP), wherein the second negative measured voltage (DAC2N) may be a voltage that is feedback of a negative voltage output from the second DAC (DAC2) after the ST signal is delayed by two clocks through the second D flip-flop of the voltage output circuit.

[0017] In the present disclosure, the eleventh and thirteenth switches (SW11, SW13) may be simultaneously switched on/off by the STQ1 signal, the twelfth and fourteenth switches (SW12, SW14) may be simultaneously switched on/off by the STQ2 signal, and the STQ1 signal and the STQ2 signal may be output when the ST signal is in a high section while the primary integrator circuit operates.

[0018] In the present disclosure, the secondary integrator circuit may include an integrating circuit formed of a second switching capacitor part and the amplifier (AMP); the second switching capacitor part may include fourth, fifth, sixth, and seventh switching parts; the fourth switching part may include a seventeenth switch (SW17) having a first contact point which receives an amplifier positive output voltage (VOUTP), an eighteenth switch (SW18) having a first contact point which receives the reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the seventeenth switch (SW17), an insulating capacitor (C5-1) having one end connected to the second contact point at which the seventeenth and eighteenth switches (SW17, SW18) are commonly connected, a nineteenth switch (SW19) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C5-1), and a twentieth switch (SW20) having a first contact point commonly connected to the second contact point of the nineteenth switch (SW19) and the other end of the insulating capacitor (C5-1) and having a second contact point connected to the one input terminal of the amplifier (AMP), and the amplifier positive output voltage (VOUTP) may be a voltage that is feedback of a positive voltage output from the amplifier (AMP).

[0019] In the present disclosure, the seventeenth and nineteenth switches (SW17, SW19) may be simultaneously switched on/off by an NDQ1 signal, and the eighteenth and twentieth switches (SW18, SW20) may be simultaneously switched on/off by an NDQ2 signal.

[0020] In the present disclosure, the fifth switching part may include a twenty-first switch (SW21) having a first contact point which receives a first positive measured voltage DAC1P, a twenty-second switch (SW22) having a first contact point which receives the reference voltage

(VCM) and having a second contact point commonly connected to a second contact point of the twenty-first switch (SW21), an insulating capacitor (C6-1) having one end connected to the second contact point at which the twenty-first and twenty-second switches (SW21, SW22) are commonly connected, a twenty-third switch (SW23) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C6-1), and a twenty-fourth switch (SW24) having a first contact point commonly connected to the second contact point of the twenty-third switch (SW23) and the other end of the insulating capacitor (C6-1) and having a second contact point connected to the one input terminal of the amplifier (AMP), wherein the first positive measured voltage (DAC1P) may be a voltage that is feedback of a positive voltage output from a first DAC (DAC1) after the ST signal is delayed by one clock through a first D flip-flop of the voltage output circuit.

[0021] In the present disclosure, the twenty-first and twenty-third switches (SW21, SW23) may be simultaneously switched on/off by the NDQ1 signal, and the twenty-second and twenty-fourth switches (SW22, SW24) may be simultaneously switched on/off by the NDQ2 signal.

[0022] In the present disclosure, the sixth switching part may include a twenty-sixth switch (SW26) having a first contact point which receives an amplifier negative output voltage (VOUTN), a twenty-seventh switch (SW27) having a first contact point which receives the reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the twenty-sixth switch (SW26), an insulating capacitor (C5-2) having one end connected to the second contact point at which the twenty-sixth and twenty-seventh switches (SW26, SW27) are commonly connected, a twenty-eighth switch (SW28) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C5-2), and a twenty-ninth switch (SW29) having a first contact point commonly connected to the second contact point of the twenty-eighth switch (SW28) and the other end of the insulating capacitor (C5-2) and having a second contact point connected to the other input terminal of the amplifier (AMP), wherein the amplifier negative output voltage (VOUTN) may be a voltage that is feedback of a negative voltage output from the amplifier (AMP).

[0023] In the present disclosure, the twenty-sixth and twenty-eighth switches (SW26, SW28) may be simultaneously switched on/off by the NDQ1 signal, and the twenty-seventh and twenty-ninth switches (SW27, SW29) may be simultaneously switched on/off by the NDQ2 signal.

[0024] In the present disclosure, the seventh switching part may include a thirtieth switch (SW30) having a first contact point which receives a first negative measured voltage (DAC1N), a thirty-first switch (SW31) having a first contact point which receives the reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the thirtieth switch (SW30), an insulating capacitor (C6-2) having one end connected to the second contact point at which the thirtieth and thirty-first switches (SW30, SW31) are commonly connected, a thirty-second switch (SW32) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C6-2), and a thirty-third switch (SW33) having a first contact point commonly connected to the second contact point of the thirty-second switch (SW32) and the other end of the insulating capacitor (C6-2) and having a second contact point connected to the other input terminal of the amplifier (AMP), wherein the first negative measured voltage (DAC1N) may be a voltage that is feedback of a negative voltage output from the first DAC (DAC1) after the ST signal is delayed by one clock through the first D flip-flop of the voltage output circuit.

[0025] In the present disclosure, the thirtieth and thirty-second switches (SW30, SW32) may be simultaneously switched on/off by the NDQ1 signal, the thirty-first and thirty-third switches (SW31, SW33) may be simultaneously switched on/off by the NDQ2 signal, and the NDQ1 signal and the NDQ2 signal may be output when the ND signal is in a high section while the secondary integrator circuit operates.

[0026] In the present disclosure, a capacitor (C2-1) and a fifteenth switch (SW15), which are connected in series, may be connected between one input terminal and one output terminal of the amplifier (AMP); a capacitor (C4-1) and a twenty-fifth switch (SW25), which are connected in series, may be connected between the one input terminal and the one output terminal; a reset switch may be connected between the one input terminal and the one output terminal; a capacitor (C2-2) and a sixteenth switch (SW16), which are connected in series, may be connected between the other input terminal and the other output terminal of the amplifier (AMP); a capacitor (C4-2) and a thirty-fourth (SW34), which are connected in series, may be connected between the other input terminal and the other output terminal; and a reset switch (RST) may be connected between the other input terminal and the other output terminal.

[0027] In the present disclosure, the apparatus for measuring a voltage includes a voltage output circuit, wherein the voltage output circuit includes a first D flip-flop configured to receive one output and the other output of the comparator, a second D flip-flop connected to one output terminal and the other output terminal of the first D flip-flop, and a digital filter configured to filter and output voltages output from one output terminal and the other output terminal of the second D flip-flop, a first DAC (DAC1) is connected parallel to the one output terminal and the other output terminal of the first D flip-flop to feed a first positive measured voltage (DAC1P) and a first negative measured voltage (DAC1N) back to the secondary integrator circuit, and a second DAC (DAC2) is connect-

ed parallel to the one output terminal and the other output terminal of the second D flip-flop to feed a second positive measured voltage (DAC2P) and a second negative measured voltage (DAC2N) back to the primary integrator circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028]

FIG. 1 is an exemplary diagram illustrating a schematic configuration of an apparatus for measuring a voltage, which is configured using a conventional primary analog-to-digital converter (ADC).

FIG. 2 is an exemplary diagram for describing a problem of a case in which the apparatus for measuring a voltage is configured by increasing the number of amplifiers in FIG. 1.

FIG. 3 is an exemplary diagram illustrating a circuit configuration of an apparatus for measuring a voltage according to one embodiment of the present disclosure.

FIG. 4 is an exemplary diagram illustrating a timing chart of control signals output from a controller to switches of the apparatus for measuring a voltage shown in FIG. 3.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0029] The components described in the example embodiments may be implemented by hardware components including, for example, at least one digital signal processor (DSP), a processor, a controller, an application-specific integrated circuit (ASIC), a programmable logic element, such as an FPGA, other electronic devices, or combinations thereof. At least some of the functions or the processes described in the example embodiments may be implemented by software, and the software may be recorded on a recording medium. The components, the functions, and the processes described in the example embodiments may be implemented by a combination of hardware and software.

[0030] The method according to example embodiments may be embodied as a program that is executable by a computer, and may be implemented as various recording media such as a magnetic storage medium, an optical reading medium, and a digital storage medium.

[0031] Various techniques described herein may be implemented as digital electronic circuitry, or as computer hardware, firmware, software, or combinations thereof. The techniques may be implemented as a computer program product, i.e., a computer program tangibly embodied in an information carrier, e.g., in a machine-readable storage device (for example, a computer-readable medium) or in a propagated signal for processing by, or to control an operation of a data processing apparatus, e.g., a programmable processor, a computer, or multiple computers. A computer program(s) may be written in any form of a programming language, including compiled or interpreted languages and may be deployed in any form including a stand-alone program or a module, a component, a subroutine, or other units suitable for use in a computing environment. A computer program may be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a communication network.

[0032] Processors suitable for execution of a computer program include, by way of example, both general and special purpose microprocessors, and any one or more processors of any kind of digital computer. Generally, a processor will receive instructions and data from a read-only memory or a random access memory or both. Elements of a computer may include at least one processor to execute instructions and one or more memory devices to store instructions and data. Generally, a computer will also include or be coupled to receive data from, transfer data to, or perform both on one or more mass storage devices to store data, e.g., magnetic, magneto-optical disks, or optical disks. Examples of information carriers suitable for embodying computer program instructions and data include semiconductor memory devices, for example, magnetic media such as a hard disk, a floppy disk, and a magnetic tape, optical media such as a compact disk read only memory (CD-ROM), a digital video disk (DVD), etc. and magneto-optical media such as a floptical disk, and a read only memory (ROM), a random access memory (RAM), a flash memory, an erasable programmable ROM (EPROM), and an electrically erasable programmable ROM (EEPROM) and any other known computer readable medium. A processor and a memory may be supplemented by, or integrated into, a special purpose logic circuit.

[0033] The processor may run an operating system (OS) and one or more software applications that run on the OS. The processor device also may access, store, manipulate, process, and create data in response to execution of the software. For purpose of simplicity, the description of a processor device is used as singular; however, one skilled in the art will be appreciated that a processor device may include multiple processing elements and/or multiple types of processing elements. For example, a processor device may include multiple processors or a processor and a controller. In addition, different processing configurations are possible, such as parallel processors.

[0034] Also, non-transitory computer-readable media may be any available media that may be accessed by a computer, and may include both computer storage media and transmission media.

[0035] The present specification includes details of a number of specific implements, but it should be understood that the details do not limit any invention or what is claimable in the specification but rather describe features of the specific example embodiment. Features described in the specification in the context of individual

example embodiments may be implemented as a combination in a single example embodiment. In contrast, various features described in the specification in the context of a single example embodiment may be implemented in multiple example embodiments individually or in an appropriate sub-combination. Furthermore, the features may operate in a specific combination and may be initially described as claimed in the combination, but one or more features may be excluded from the claimed combination in some cases, and the claimed combination may be changed into a sub-combination or a modification of a sub-combination.

[0036] Similarly, even though operations are described in a specific order on the drawings, it should not be understood as the operations needing to be performed in the specific order or in sequence to obtain desired results or as all the operations needing to be performed. In a specific case, multitasking and parallel processing may be advantageous. In addition, it should not be understood as requiring a separation of various apparatus components in the above described example embodiments in all example embodiments, and it should be understood that the above-described program components and apparatuses may be incorporated into a single software product or may be packaged in multiple software products.

[0037] It should be understood that the example embodiments disclosed herein are merely illustrative and are not intended to limit the scope of the invention. It will be apparent to one of ordinary skill in the art that various modifications of the example embodiments may be made without departing from the spirit and scope of the claims and their equivalents.

[0038] Hereinafter, with reference to the accompanying drawings, embodiments of the present disclosure will be described in detail so that a person skilled in the art can readily carry out the present disclosure. However, the present disclosure may be embodied in many different forms and is not limited to the embodiments described herein.

[0039] In the following description of the embodiments of the present disclosure, a detailed description of known functions and configurations incorporated herein will be omitted when it may make the subject matter of the present disclosure rather unclear. Parts not related to the description of the present disclosure in the drawings are omitted, and like parts are denoted by similar reference numerals.

[0040] In the present disclosure, components that are distinguished from each other are intended to clearly illustrate each feature. However, it does not necessarily mean that the components are separate. That is, a plurality of components may be integrated into one hardware or software unit, or a single component may be distributed into a plurality of hardware or software units. Thus, unless otherwise noted, such integrated or distributed embodiments are also included within the scope of the present disclosure.

[0041] In the present disclosure, components described in the various embodiments are not necessarily essential components, and some may be optional components. Accordingly, embodiments consisting of a subset of the components described in one embodiment are also included within the scope of the present disclosure. In addition, embodiments that include other components in addition to the components described in the various embodiments are also included in the scope of the present disclosure.

[0042] Hereinafter, with reference to the accompanying drawings, embodiments of the present disclosure will be described in detail so that a person skilled in the art can readily carry out the present disclosure. However, the present disclosure may be embodied in many different forms and is not limited to the embodiments described herein.

[0043] In the following description of the embodiments of the present disclosure, a detailed description of known functions and configurations incorporated herein will be omitted when it may make the subject matter of the present disclosure rather unclear. Parts not related to the description of the present disclosure in the drawings are omitted, and like parts are denoted by similar reference numerals.

[0044] In the present disclosure, when a component is referred to as being "linked," "coupled," or "connected" to another component, it is understood that not only a direct connection relationship but also an indirect connection relationship through an intermediate component may also be included. In addition, when a component is referred to as "comprising" or "having" another component, it may mean further inclusion of another component not the exclusion thereof, unless explicitly described to the contrary.

[0045] In the present disclosure, the terms first, second, etc. are used only for the purpose of distinguishing one component from another, and do not limit the order or importance of components, etc., unless specifically stated otherwise. Thus, within the scope of this disclosure, a first component in one exemplary embodiment may be referred to as a second component in another embodiment, and similarly a second component in one exemplary embodiment may be referred to as a first component.

[0046] In the present disclosure, components that are distinguished from each other are intended to clearly illustrate each feature. However, it does not necessarily mean that the components are separate. That is, a plurality of components may be integrated into one hardware or software unit, or a single component may be distributed into a plurality of hardware or software units. Thus, unless otherwise noted, such integrated or distributed embodiments are also included within the scope of the present disclosure.

[0047] In the present disclosure, components described in the various embodiments are not necessarily essential components, and some may be optional com-

ponents. Accordingly, embodiments consisting of a subset of the components described in one embodiment are also included within the scope of the present disclosure. In addition, exemplary embodiments that include other components in addition to the components described in the various embodiments are also included in the scope of the present disclosure.

[0048] Hereinafter, an apparatus for measuring a voltage will be described below with reference to the accompanying drawings through various exemplary embodiments.

[0049] In the following description, thicknesses of lines and sizes of components shown in the drawings may be exaggerated for clarity and convenience of description. In addition, the terms described below are defined in consideration of the functions of the present invention, and these terms may be varied according to the intent of a user or an operator or practice. Therefore, these terms should be defined on the basis of the contents throughout the present application.

[0050] FIG. 3 is an exemplary diagram illustrating a circuit configuration of an apparatus for measuring a voltage according to one embodiment of the present disclosure, and FIG. 4 is an exemplary diagram illustrating a timing chart of control signals output from a controller to switches of the apparatus for measuring a voltage shown in FIG. 3.

[0051] Referring to FIG. 3, the apparatus for measuring a voltage according to the present embodiment includes a primary integrator circuit 110 configured to operate as a first integral stage of a sigma-delta analog-to-digital converter (ADC) circuit by a switching according to a control signal of a controller 150, secondary integrator circuits 120 and 130 configured to operate as a second integrator stage by the switching of the controller 150, and a voltage output circuit 140 configured to delay an output of the primary integrator circuit 110 by a specified number of clocks according to the switching of the controller 150 to feed the delayed output back to the secondary integrator circuits 120 and 130, delay outputs of the secondary integrator circuits 120 and 130 by a specified number of clocks to feed the delayed outputs back to the primary integrator circuit 110, and output a finally measured voltage value through the primary integrator circuit 110 and the secondary integrator circuits 120 and 130.

[0052] In this case, in the present embodiment, it is noted that when the primary integrator circuit 110 operates by the switching of the controller 150, an amplifier AMP is used as an amplifier AMP for an integrator of the primary integrator circuit 110 and, when the secondary integrator circuit 120 operates, the AMP is used as an amplifier AMP for an integrator of the secondary integrator circuit 120.

[0053] Referring to FIG. 4, when an ST signal is in a high section, the primary integrator circuit 110 operates (for convenience, it is indicated by a thick line), and when an ND signal is in a high section, the secondary integrator circuit 120 operates. In this case, since the ST signal and the ND signal are inverted pulse signals, the primary integrator circuit 110 and the secondary integrator circuit 120 operate sequentially.

[0054] As described above, the present embodiment is characterized in that a circuit in which the primary integrator circuit 110 and the secondary integrator circuit 120 operate sequentially is configured so that a single amplifier AMP is actually used to achieve the same effect as a circuit in which two amplifiers AMP are used as shown in FIG. 2 to increase an order of ADC (e.g., a sigma-delta ADC circuit).

[0055] For reference, in the timing chart shown in FIG. 4, a rising edge and a falling edge of each signal actually have a slight time difference, but in an ideal circuit, a time difference between signals is virtually meaningless. Hereinafter, even in the present embodiment, a description will be made on the assumption that there is no time difference between respective signals.

[0056] The primary integrator circuit 110 includes an integrating circuit formed of a first switching capacitor part (i.e., first to third switching parts 111 to 113 and capacitors C2-1 and C2-2) and the amplifier AMP, and the secondary integrator circuits 120 and 130 include an integrating circuit formed of a second switching capacitor part (i.e., fourth to seventh switching parts 121, 122, 131, and 132, capacitors C4-1 and C4-2), and the amplifier AMP.

[0057] The first switching part 111 includes first and second switches SW1 and SW2 each having a first contact point commonly connected to a positive (+) terminal of a battery cell CELL, and third and fourth switches SW3 and SW4 each having a first contact point commonly connected to a negative (-) terminal of the battery cell CELL. Second contact points of the first and third switches SW1 and SW3 are commonly connected, and second contact points of the second and fourth switches SW2 and SW4 are commonly connected. In addition, one ends of insulating capacitors C1-1 and C1-2 having the same value are connected in series to the second contact points of the first and third switches SW1 and SW3 and the second contact points of the second and fourth switches SW2 and SW4. A fifth switch SW5 and a sixth switch SW6 are connected in series to the other ends of the insulating capacitors C1-1 and C1-2 to be connected to one input terminal (e.g., a non-inverting input terminal) and the other input terminal (e.g., an inverting input terminal) of the amplifier AMP.

[0058] In this case, the first and fourth switches SW1 and SW4 are simultaneously switched on/off by an STX1 signal (that is, switched on in a high section and switched off in a low section), the second and third switches SW2 and SW3 are simultaneously switched on/off by an STX2 signal, and the fifth and sixth switches SW5 and SW6 are simultaneously switched on/off by the ST signal.

[0059] The second switching part 112 includes a seventh switch SW7 having a first contact point which receives a second positive measured voltage DAC2P (i.e.,

a voltage which is feedback of a positive voltage output from a second DAC DAC2 146 after the ST signal is delayed by two clocks through a second D flip-flop 145), an eighth switch SW8 having a first contact point which receives a reference voltage VCM and having a second contact point commonly connected to a second contact point of the seventh switch SW7, an insulating capacitor C3-1 having one end connected to the second contact point at which the seventh and eighth switches SW7 and SW8 are commonly connected, a ninth switch SW9 having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor C3-1, and a tenth switch SW10 having a first contact point commonly connected to the second contact point of the ninth switch SW9 and the other end of the insulating capacitor C3-1 and having a second contact point connected to the one input terminal (e.g., the non-inverting input terminal) of the amplifier AMP.

[0060] In this case, the seventh and ninth switches SW7 and SW9 are simultaneously switched on/off by an STQ1 signal (i.e., switched on in a high section and switched off in a low section), and the eighth and tenth switches SW8 and SW10 are simultaneously switched on/off by an STQ2 signal.

[0061] The third switching part 113 includes an eleventh switch SW11 having a first contact point which receives a second negative measured voltage DAC2N (i.e., a voltage which is feedback of a negative voltage output from the second DAC DAC2 146 after the ST signal is delayed by two clocks through the second D flip-flop 145), a twelfth switch SW12 having a first contact point which receives the reference voltage VCM and having a second contact point commonly connected to a second contact point of the eleventh switch SW11, an insulating capacitor C3-2 having one end connected to the second contact point at which the eleventh and twelfth switches SW11 and SW12 are commonly connected, a thirteenth switch SW13 having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor C3-2, and a fourteenth switch SW14 having a first contact point commonly connected to the second contact point of the thirteenth switch SW13 and the other end of the insulating capacitor C3-2 and having a second contact point connected to the other input terminal (e.g., the inverting input terminal) of the amplifier AMP.

[0062] In this case, the eleventh and thirteenth switches SW11 and SW13 are simultaneously switched on/off by the STQ1 signal (i.e., switched on in a high section and switched off in a low section), and the twelfth and fourteenth switches SW12 and SW14 are simultaneously switched on/off by the STQ2 signal.

[0063] For reference, the STQ1 signal and the STQ2 signal are output when the primary integrator circuit 110 operates (i.e., when the ST signal is in the high section).

[0064] The fourth switching part 121 includes a seventeenth switch SW17 having a first contact point which receives an amplifier positive output voltage VOUTP (i.e., a voltage which is feedback of a positive voltage output from the amplifier AMP), an eighteenth switch SW18 having a first contact point which receives the reference voltage VCM and having a second contact point commonly connected to a second contact point of the seventeenth switch SW17, an insulating capacitor C5-1 having one end connected to the second contact point at which the seventeenth and eighteenth switches SW17 and SW18 are commonly connected, a nineteenth switch SW19 having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor C5-1, and a twentieth switch SW20 having a first contact point commonly connected to the second contact point of the nineteenth switch SW19 and the other end of the insulating capacitor C5-1 and having a second contact point connected to the one input terminal (e.g., the non-inverting input terminal) of the amplifier AMP.

[0065] In this case, the seventeenth and nineteenth switches SW17 and SW19 are simultaneously switched on/off by an NDQ1 signal (i.e., switched on in a high section and switched off in a low section), and the eighteenth and twentieth switches SW18 and SW20 are simultaneously switched on/off by an NDQ2 signal.

[0066] The fifth switching part 122 includes a twenty-first switch SW21 having a first contact point which receives a first positive measured voltage DAC1P (i.e., a voltage which is feedback of a positive voltage output from a first DAC DAC1 144 after the ST signal is delayed by one clock through a first D flip-flop 143, a twenty-second switch SW22 having a first contact point which receives the reference voltage VCM and having a second contact point commonly connected to a second contact point of the twenty-first switch SW21, an insulating capacitor C6-1 having one end connected to the second contact point at which the twenty-first and twenty-second switches SW21 and SW22 are commonly connected, a twenty-third switch SW23 having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor C6-1, and a twenty-fourth switch SW24 having a first contact point commonly connected to the second contact point of the twenty-third switch SW23 and the other end of the insulating capacitor C6-1 and having a second contact point connected to the one input terminal (e.g., the non-inverting input terminal) of the amplifier AMP.

[0067] In this case, the twenty-first and twenty-third switches SW21 and SW23 are simultaneously switched on/off by the NDQ1 signal (i.e., switched on in the high section and switched off in the low section), and the twenty-second and twenty-fourth switches SW22 and SW24 are simultaneously switched on/off by the NDQ2 signal.

[0068] The sixth switching part 131 includes a twenty-sixth switch SW26 having a first contact point which receives an amplifier negative output voltage VOUTN (i.e., a voltage which is feedback of a negative voltage output

from the amplifier AMP), a twenty-seventh switch SW27 having a first contact point which receives the reference voltage VCM and having a second contact point commonly connected to a second contact point of the twenty-sixth switch SW26, an insulating capacitor C5-2 having one end connected to the second contact point at which the twenty-sixth and twenty-seventh switches SW26 and SW27 are commonly connected, a twenty-eighth switch SW28 having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor C5-2, and a twenty-ninth switch SW29 having a first contact point commonly connected to the second contact point of the twenty-eighth switch SW28 and the other end of the insulating capacitor C5-2 and having a second contact point connected to the other input terminal (e.g., the inverting input terminal) of the amplifier AMP.

[0069] In this case, the twenty-sixth and twenty-eighth switches SW26 and SW28 are simultaneously switched on/off by the NDQ1 signal (i.e., switched on in the high section and switched off in the low section), and the twenty-seventh and twenty-ninth switches SW27 and SW29 are simultaneously switched on/off by the NDQ2 signal.

[0070] The seventh switching part 132 includes a thirtieth switch SW30 having a first contact point which receives a first negative measured voltage DAC1N (i.e., a voltage which is feedback of a negative voltage output from the first DAC DAC1 144 after the ST signal is delayed by one clock through the first D flip-flop 143, a thirty-first switch SW31 having a first contact point which receives the reference voltage VCM and having a second contact point commonly connected to a second contact point of the thirtieth switch SW30, an insulating capacitor C6-2 having one end connected to the second contact point at which the thirtieth and thirty-first switches SW30 and SW31 are commonly connected, a thirty-second switch SW32 having a first contact point which receives the reference voltage VCM and having a second contact point connected to the other end of the insulating capacitor C6-2, and a thirty-third switch SW33 having a first contact point commonly connected to the second contact point of the thirty-second switch SW32 and the other end of the insulating capacitor C6-2 and having a second contact point connected to the other input terminal (e.g., the inverting input terminal) of the amplifier AMP.

[0071] In this case, the thirtieth and thirty-second switches SW30 and SW32 are simultaneously switched on/off by the NDQ1 signal (i.e., switched on in the high section and switched off in the low section), and the thirty-first and thirty-third switches SW31 and SW33 are simultaneously switched on/off by the NDQ2 signal.

[0072] For reference, the NDQ1 signal and the NDQ2 signal are output when the secondary integrator circuits 120 and 130 operate (i.e., when the ND signal is in the high section).

[0073] Meanwhile, the capacitor C2-1 and a fifteenth switch SW15, which are connected in series, are connected between the one input terminal (e.g., the non-inverting input terminal) and one output terminal (e.g., a VOUTP output terminal) of the amplifier AMP, the capacitor C4-1 and a fifteenth switch SW25, which are connected in series, are also connected between the one input terminal (e.g., the non-inverting input terminal) and the one output terminal (e.g., the VOUTP output terminal) of the amplifier AMP, and a reset switch RST is additionally connected between the one input terminal (e.g., the non-inverting input terminal) and the one output terminal (e.g., the VOUTP output terminal) of the amplifier AMP.

[0074] In addition, the capacitor C2-2 and a sixteenth switch SW16, which are connected in series, are connected between the other input terminal (e.g., the inverting input terminal) and the other output terminal (e.g., the VOUTN output terminal) of the amplifier AMP, the capacitor C4-2 and a thirty-fourth switch SW34, which are connected in series, are also connected between the other input terminal (e.g., the inverting input terminal) and the other output terminal (e.g., the VOUTN output terminal) of the amplifier AMP, and a reset switch RST is additionally connected between the other input terminal (e.g., the inverting input terminal) and the other output terminal (e.g., the VOUTN output terminal) of the amplifier AMP.

[0075] Here, when the ST signal is in the high section, the primary integrator circuit 110 operates, and thus the fifteenth and sixteenth switches SW15 and SW16 are switched on so that the amplifier AMP and the two capacitors C2-1 and C2-2 operate as an integrator. In addition, when the ND signal is in the high section, the secondary integrator circuits 120 and 130 operate, and thus the twenty-fifth and thirty-fourth switches SW25 and SW34 are switched on so that the amplifier AMP and the two capacitors C4-1 and C4-2 operate as an integrator.

[0076] Hereinafter, a configuration of the voltage output circuit 140 will be described.

[0077] The voltage output circuit 140 includes a comparator 141 connected to the one output terminal and the other output terminal of the amplifier AMP and configured to compare magnitudes of outputs (i.e., a finally modulated voltage through the primary integrator circuit and the secondary integrator circuits), an SR-latch 142 connected to one output terminal and the other output terminal of the comparator 141, the first D flip-flop 143 connected to one output terminal and the other output terminal of the SR-latch 142, the second D flip-flop 145 connected to one output terminal and the other output terminal of the first D flip-flop 143, and a digital filter 147 configured to filter and output voltages DOUT and DOUTB output from one output terminal and the other output terminal of the second D flip-flop 145.

[0078] That is, the digital filter 147 delays the output of the comparator 141 by a specified number of clocks according to the switching of the controller 150, passes the delayed output through the DAC to feed the delayed output back to the primary integrator circuit 110 and the secondary integrator circuits 120 and 130, and receives the delayed output signal of the comparator 141.

[0079] In addition, the first DAC DAC1 144 is connect-

ed parallel to the one output terminal and the other output terminal of the first D flip-flop 143 to feed the first positive measured voltage DAC1P and the first negative measured voltage DAC1N back to the secondary integrator circuits 120 and 130, and the second DAC DAC2 146 is connected parallel to the one output terminal and the other output terminal of the second D flip-flop 145 to feed the second positive measured voltage DAC2P and the second negative measured voltage DAC2N back to the primary integrator circuit 110.

[0080] In this case, the first D flip-flop 143 and the second D flip-flop 145 each receive the ST signal as a clock. That is, the first D flip-flop 143 feeds a value, which is output from the amplifier AMP and delayed by one clock by the ST signal, back to the secondary integrator circuits 120 and 130, and the second D flip-flop 145 feeds a value, which is output from the amplifier AMP and delayed by two clocks by the ST signal, back to the primary integrator circuit 110.

[0081] For reference, when the primary integrator circuit 110 operates, the value fed back from the second DAC DAC2 146 is a value of previous two clocks based on the ST (or ND) signal, and when the secondary integrator circuits 120 and 130 operate, the value fed back from the first DAC DAC1 144 is a value of a previous one clock based on the ST (or ND) signal. Therefore, the apparatus for measuring a voltage is configured such that the values obtained by delaying two clocks and one clock using the first and second D flip-flops 143 and 145 undergo DA conversion through the first DAC DAC1 144 and the second DAC DAC2 146 and are then fed back.

[0082] Thus, in the present embodiment, while the primary integrator circuit 110 and the secondary integrator circuits 120 and 130 actually use a single amplifier AMP, they operate, as shown in FIG. 2, in the same way as a circuit (e.g., a sigma-delta ADC circuit) in which the order of the ADC is increased using two amplifiers AMP. Rather, according to the present embodiment, while relatively further reducing the size of the circuit, there is an effect of increasing the voltage measurement speed to reduce the voltage measurement time and also to improve the voltage measurement accuracy.

[0083] FIG. 4 is an exemplary diagram illustrating a timing chart of control signals output from a controller to switches of the apparatus for measuring a voltage shown in FIG. 3.

[0084] Referring to FIG. 4, while the controller 150 outputs the ST signal in a high state, the fifth, sixth, fifteenth, and sixteenth switches SW5, SW6, SW15, and SW16 of the primary integrator circuit 110 are switched on, the primary integrator circuit 110 performs sampling in the high sections of the STX1 signal and the STQ1 signal (e.g., a former half high section of the ST signal), and the primary integrator circuit 110 performs an integral calculation (i.e., an integral calculation on a value fed back through the second D flip-flop 145 and the second DAC DAC2 146) in the high sections of the STX2 signal and the STQ2 signal (e.g., a latter half high section of the ST signal).

[0085] A value (that is, a measured voltage value) output after the integral calculation is completed by the primary integrator circuit 110 is fed back to the secondary integrator circuits 120 and 130 through the first D flip-flop 143 and the first DAC DAC1 144.

[0086] In addition, while the controller 150 outputs the ND signal in a high state, the twenty-fifth and thirty-fourth switches SW25 and SW34 of the secondary integrator circuits 120 and 130 are switched on, the secondary integrator circuits 120 and 130 perform sampling in the high section of the NDQ1 signal (e.g., a former half high period of the ND signal), and the secondary integrator circuits 120 and 130 perform an integral calculation (i.e., an integral calculation on a difference between a value fed back through the first D flip-flop 143 and the first DAC DAC1 144 and the value output from the amplifier) in the high section of the NDQ2 signal (e.g., a latter half high section of the ND signal).

[0087] That is, the controller 150 sequentially operates the primary integrator circuit 110 and the secondary integrator circuits 120 and 130 according to a switch control signal in the form of a pulse that is periodically output, so that, while the primary integrator circuit 110 and the secondary integrator circuits 120 and 130 actually use a single amplifier AMP, they operate, as shown in FIG. 2, in the same way as a circuit (e.g., a sigma-delta ADC circuit) in which the order of the ADC is increased using two amplifiers AMP. Rather, according to the present embodiment, while relatively further reducing the size of the circuit, there is an effect of increasing the voltage measurement speed to reduce the voltage measurement time and also to improve the voltage measurement accuracy.

[0088] In accordance with the present disclosure, when measuring a voltage of a battery cell or the like, by increasing the order of an analog-to-digital converter (ADC) while not increasing the number of amplifiers (AMP), it is possible to relatively reduce a size of a circuit, to increase a voltage measurement speed to reduce a voltage measurement time and to improve voltage measurement accuracy.

Claims

1. An apparatus for measuring a voltage, comprising:

a primary integrator circuit configured to operate as a first integral stage of a sigma-delta analog-to-digital converter, ADC, circuit by a switching according to a control signal of a controller;
a secondary integrator circuit configured to operate as a second integral stage by a switching of the controller;
a comparator configured to compare final voltages modulated through the primary integrator circuit and the secondary integrator circuit; and
a digital filter configured to delay an output of

the comparator by a specified number of clocks according to a switching of the controller, pass the delayed output through a digital-to-analog converter, DAC, to feed the delayed output back to the primary and secondary integrator circuits, and receive the delayed output signal of the comparator as an input,
wherein an output of the digital filter becomes a final measured value.

2. The apparatus of claim 1, wherein:

the sigma-delta ADC includes an amplifier (AMP) for an integrator;
the amplifier (AMP) is used as an amplifier (AMP) for an integrator of the primary integrator circuit when the primary integrator circuit operates; and
the amplifier (AMP) is used as an amplifier (AMP) for an integrator of the secondary integrator circuit when the secondary integrator circuit operates.

3. The apparatus of claim 1, or 2, wherein the controller outputs an ST signal to operate the primary integrator circuit and outputs an ND signal to operate the secondary integrator circuit, and the primary integrator circuit operates when the ST signal is in a high section, and the secondary integrator circuit operates when the ND signal, which is an inverted signal of the ST signal, is in a high section so that the controller sequentially operates the primary integrator circuit and the secondary integrator circuit.

4. The apparatus of claim 1, 2, or 3, wherein:

the primary integrator circuit includes an integrating circuit formed of a first switching capacitor part and the amplifier (AMP);
the first switching capacitor part includes first, second, and third switching parts;
the first switching part includes:

first and second switches (SW1, SW2) having first contact points commonly connected to a positive (+) terminal of a battery cell (CELL); and
third and fourth switches (SW3, SW4) having first contact points commonly connected to a negative (-) terminal of the battery cell (CELL); and
second contact points of the first and third switches (SW1, SW3) are commonly connected;
second contact points of the second and fourth switches (SW2, SW4) are commonly connected;
one ends of insulating capacitors (C1-1, C1-2) having the same value are connected in series to the second contact points of the first and third switches (SW1, SW3) and to the second contact points of the second and fourth switches (SW2, SW4); and
a fifth switch (SW5) and a sixth switch (SW6) are connected in series to the other ends of the insulating capacitors (C1-1, C1-2) to be connected to one input terminal and the other input terminal of the amplifier (AMP).

5. The apparatus of claim 4, wherein:

the first and fourth switches (SW1, SW4) are simultaneously switched on/off by an STX1 signal;
the second and third switches (SW2, SW3) are simultaneously switched on/off by an STX2 signal which is an inverted signal of the STX1 signal; and
the fifth and sixth switches (SW5, SW6) are simultaneously switched on/off by the ST signal.

6. The apparatus of any one of claims 1 to 5, wherein:

the secondary integrator circuit includes an integrating circuit formed of a second switching capacitor part and the amplifier (AMP);
the second switching capacitor part includes fourth, fifth, sixth, and seventh switching parts;
the fourth switching part includes:

a seventeenth switch (SW17) having a first contact point which receives an amplifier positive output voltage (VOUTP);
an eighteenth switch (SW18) having a first contact point which receives the reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the seventeenth switch (SW17);
an insulating capacitor (C5-1) having one end connected to the second contact point at which the seventeenth and eighteenth switches (SW17, SW18) are commonly connected;
a nineteenth switch (SW19) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C5-1); and
a twentieth switch (SW20) having a first contact point commonly connected to the second contact point of the nineteenth switch (SW19) and the other end of the insulating capacitor (C5-1) and having a second contact point connected to the one input terminal of the amplifier (AMP); and

the amplifier positive output voltage (VOUTP) is a voltage that is feedback of a positive voltage output from the amplifier (AMP).

7. The apparatus of claim 6, wherein the seventeenth and nineteenth switches (SW17, SW19) are simultaneously switched on/off by an NDQ1 signal, and the eighteenth and twentieth switches (SW18, SW20) are simultaneously switched on/off by an NDQ2 signal.

8. The apparatus of claim 6, or 7, wherein the sixth switching part includes:

a twenty-sixth switch (SW26) having a first contact point which receives an amplifier negative output voltage (VOUTN);
a twenty-seventh switch (SW27) having a first contact point which receives the reference voltage (VCM) and having a second contact point commonly connected to a second contact point of the twenty-sixth switch (SW26);
an insulating capacitor (C5-2) having one end connected to the second contact point at which the twenty-sixth and twenty-seventh switches (SW26, SW27) are commonly connected;
a twenty-eighth switch (SW28) having a first contact point which receives the reference voltage (VCM) and having a second contact point connected to the other end of the insulating capacitor (C5-2); and
a twenty-ninth switch (SW29) having a first contact point commonly connected to the second contact point of the twenty-eighth switch (SW28) and the other end of the insulating capacitor (C5-2) and having a second contact point connected to the other input terminal of the amplifier (AMP),
wherein the amplifier negative output voltage (VOUTN) is a voltage that is feedback of a negative voltage output from the amplifier (AMP).

9. The apparatus of any one of claims 1 to 8, wherein:

a capacitor (C2-1) and a fifteenth switch (SW15), which are connected in series, are connected between one input terminal and one output terminal of the amplifier (AMP); a capacitor (C4-1) and a twenty-fifth switch (SW25), which are connected in series, are connected between the one input terminal and the one output terminal; a reset switch is connected between the one input terminal and the one output terminal; and
a capacitor (C2-2) and a sixteenth switch (SW16), which are connected in series, are connected between the other input terminal and the other output terminal of the amplifier (AMP); a capacitor (C4-2) and a thirty-fourth (SW34), which are connected in series, are connected between the other input terminal and the other output terminal; and a reset switch (RST) is connected between the other input terminal and the other output terminal.

10. The apparatus of any one of claims 1 to 9, comprising:

a voltage output circuit,
wherein the voltage output circuit includes:

a first D flip-flop which receives one output and the other output of the comparator;
a second D flip-flop connected to one output terminal and the other output terminal of the first D flip-flop; and
a digital filter configured to filter and output voltages output from one output terminal and the other output terminal of the second D flip-flop,
a first DAC (DAC1) is connected parallel to the one output terminal and the other output terminal of the first D flip-flop to feed a first positive measured voltage (DAC1P) and a first negative measured voltage (DAC1N) back to the secondary integrator circuit, and
a second DAC (DAC2) is connected parallel to the one output terminal and the other output terminal of the second D flip-flop to feed a second positive measured voltage (DAC2P) and a second negative measured voltage (DAC2N) back to the primary integrator circuit.

FIG.1

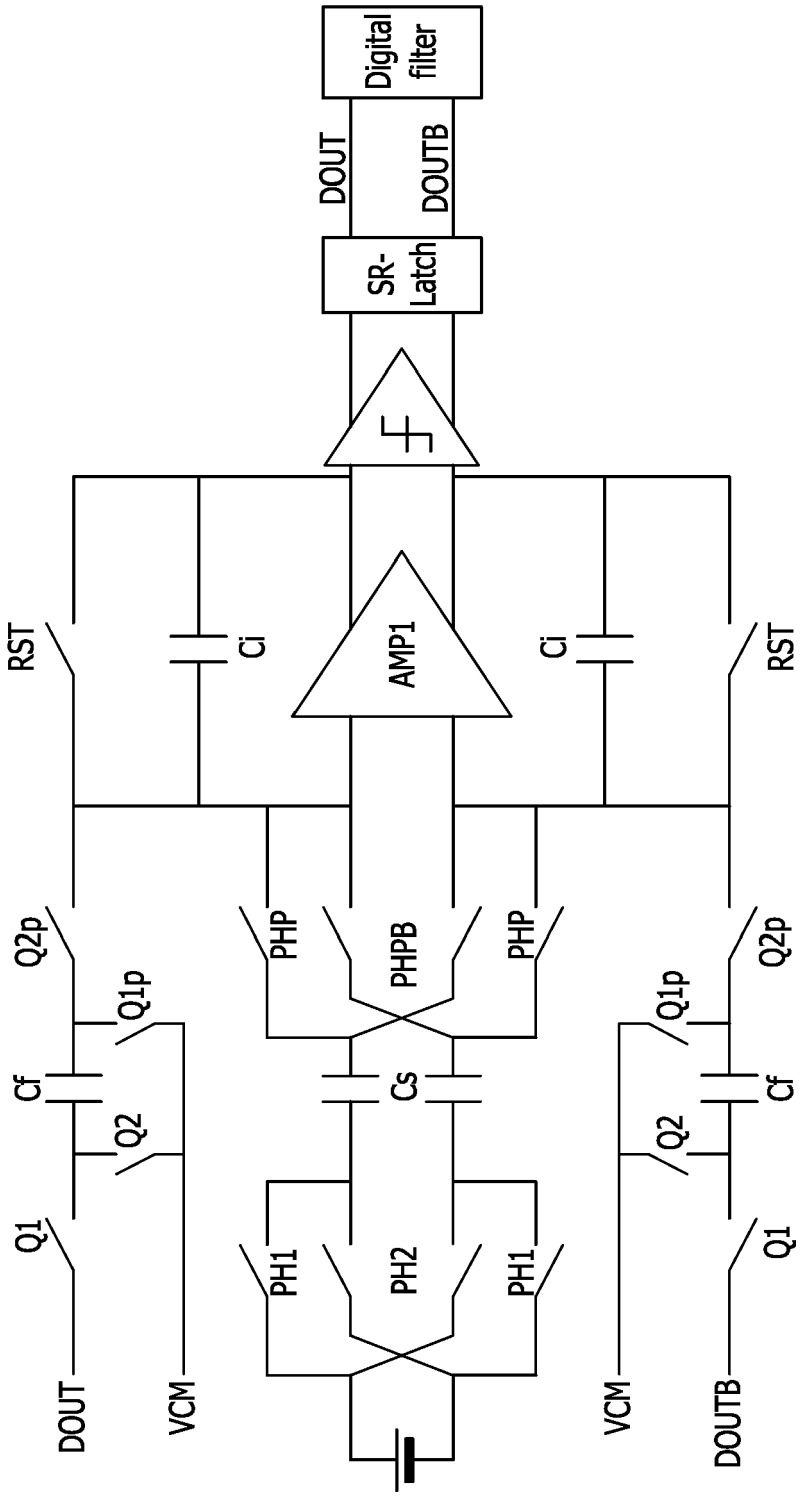

Digital filter
DOUT
DOUTB
SR-Latch
RST
Ci
AMP1
Ci
RST
Q2p
Q1p
PHP
PHPB
PHP
Q1p
Q2p
Cf
Q2
Cs
Q2
Cf
Q1
PH1
PH2
PH1
Q1
DOUT
VCM
VCM
DOUTB

FIG.2

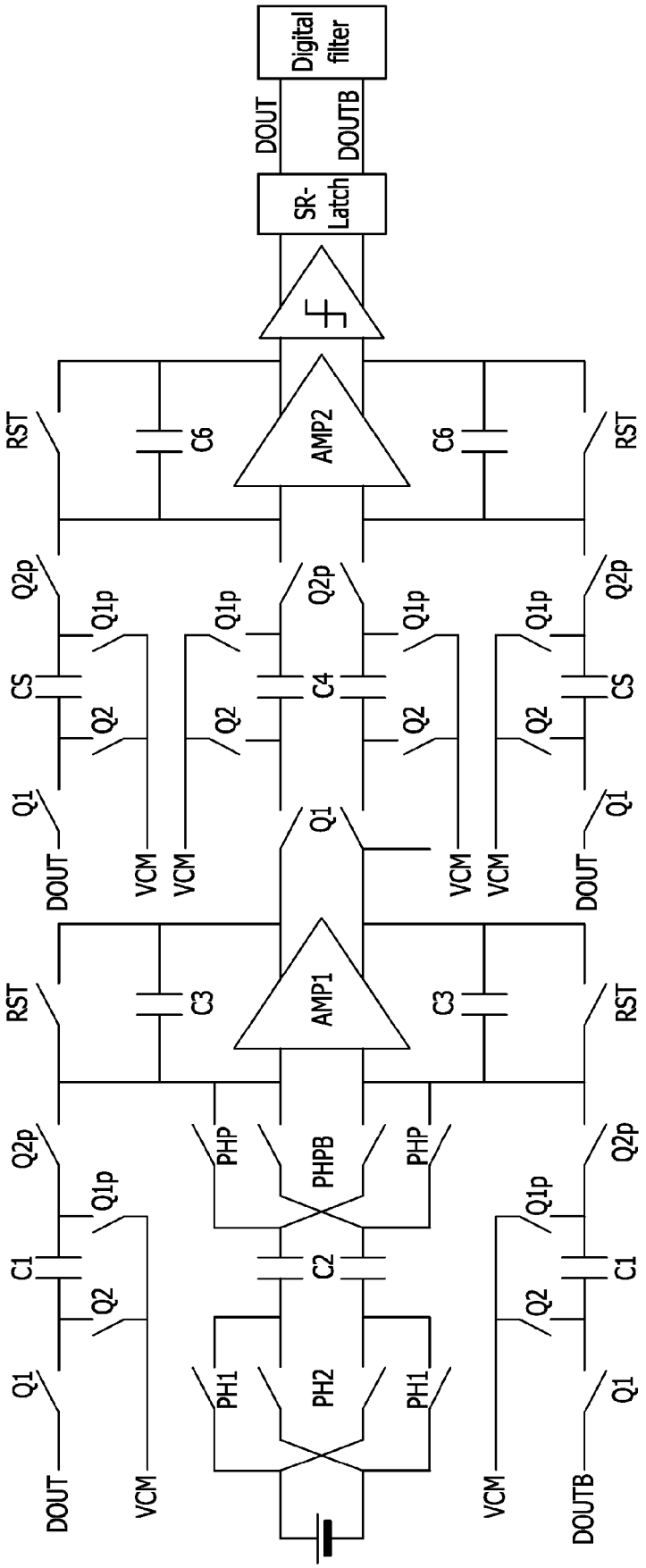

Digital filter
DOUT
DOUTB
SR-Latch
AMP2
AMP1
C6
C3
C4
C5
C2
C1
RST
Q2p
Q1p
Q2
Q1
PHP
PHPB
PH1
PH2
VCM
DOUT
DOUTB

FIG.3

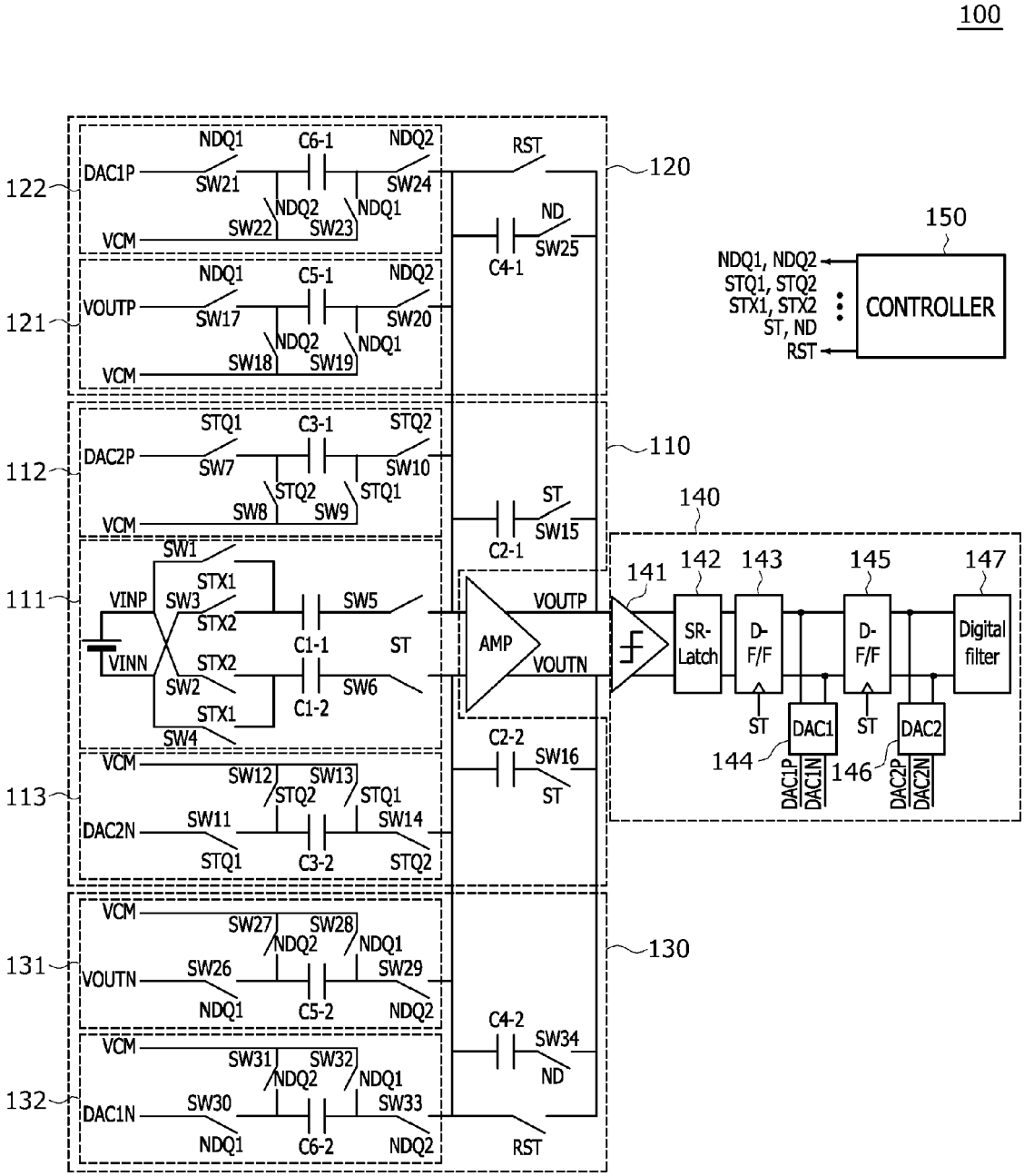
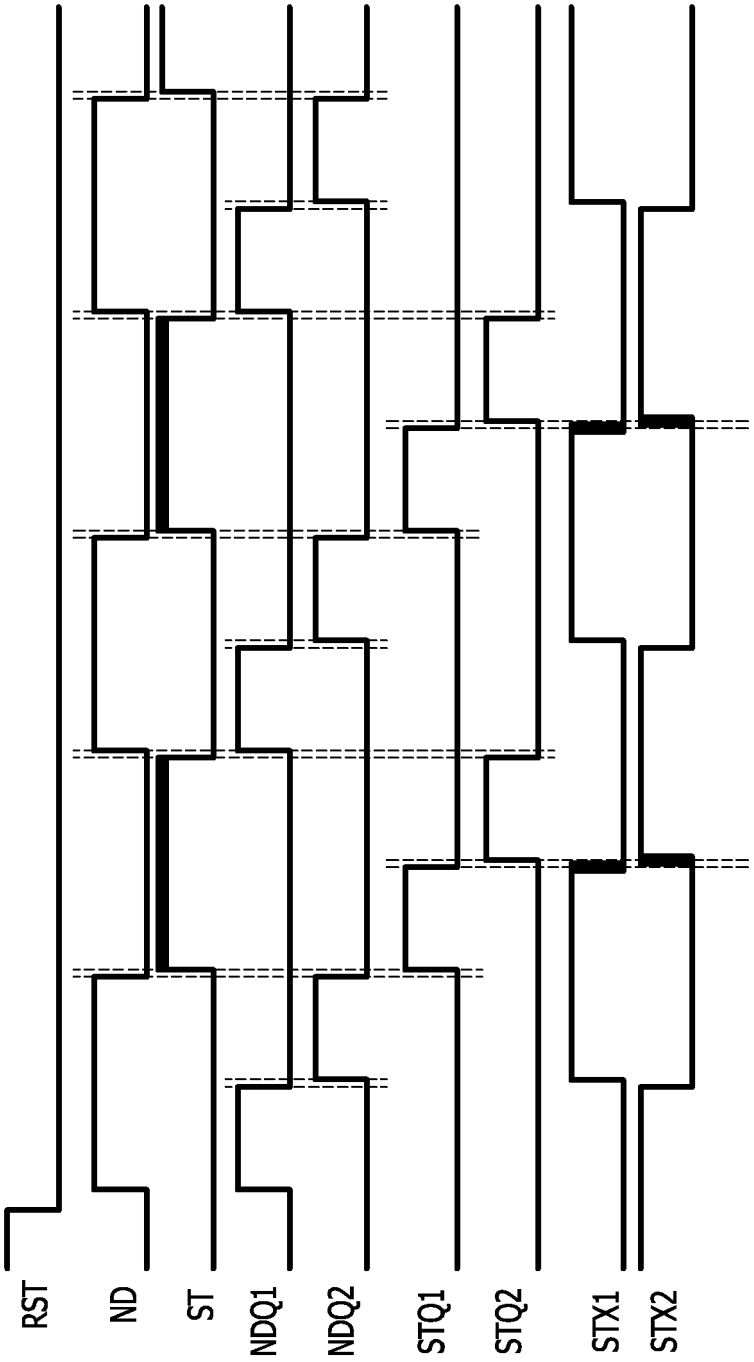

100
120
150
NDQ1, NDQ2
STQ1, STQ2
STX1, STX2
ST, ND
RST
CONTROLLER
122
121
112
111
113
131
132
110
130
140
DAC1P
VOUTP
DAC2P
VINP
VINN
DAC2N
VOUTN
DAC1N
VCM
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
SW19
SW20
SW21
SW22
SW23
SW24
SW25
SW26
SW27
SW28
SW29
SW30
SW31
SW32
SW33
SW34
C1-1
C1-2
C2-1
C2-2
C3-1
C3-2
C4-1
C4-2
C5-1
C5-2
C6-1
C6-2
AMP
141
142
143
145
147
SR-Latch
D-F/F
Digital filter
144
146
DAC1
DAC2
DAC1P
DAC1N
DAC2P
DAC2N

FIG.4



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EUROPEAN SEARCH REPORT

Application Number
EP 23 15 9308

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	ZIERHOFER C.M.: "Analysis of a Switched-Capacitor Second-Order Delta-Sigma Modulator Using Integrator Multiplexing", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING, vol. 53, no. 8, 28 August 2006 (2006-08-28), pages 787-791, XP055844366, 345 East 47 street , New York N Y 10017 , USA ISSN: 1057-7130, DOI: 10.1109/TCSII.2006.876409 * section II; figures 1,2 *	1-10	INV. H03M3/00 G01R31/3835
X	US 2016/285471 A1 (IMAIZUMI EIKI [JP]) 29 September 2016 (2016-09-29) * paragraph [0056] - paragraph [0061]; figures 6,7 *	1-10	
A	US 10 698 036 B2 (PANASONIC IP MAN CO LTD [JP]) 30 June 2020 (2020-06-30) * abstract; figure 3 *	4,5	TECHNICAL FIELDS SEARCHED (IPC) H03M G01R
A	US 2014/043032 A1 (MAKINO RYOSEI [JP] ET AL) 13 February 2014 (2014-02-13) * abstract; figure 1 *	4,5	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	15 August 2023	Galardi, Leonardo

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 23 15 9308

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15-08-2023

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REFERENCES CITED IN THE DESCRIPTION

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