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(54) **SOLID-STATE IMAGING DEVICE, METHOD OF DRIVING SAID SOLID-STATE IMAGING DEVICE, MOVABLE OBJECT COMPRISING SAID SOLID-STATE IMAGING DEVICE**

FESTKÖRPERBILDGEBUNGSVORRICHTUNG, VERFAHREN ZUR ANSTEUERUNG DER FESTKÖRPERBILDGEBUNGSVORRICHTUNG, UND BEWEGLICHES OBJEKT MIT DER FESTKÖRPERBILDGEBUNGSVORRICHTUNG

DISPOSITIF D'IMAGERIE À SEMI-CONDUCTEURS, PROCÉDÉ DE COMMANDE DUDIT DISPOSITIF D'IMAGERIE À SEMI-CONDUCTEURS, ET OBJET MOBILE COMPRENANT LEDIT DISPOSITIF D'IMAGERIE À SEMI-CONDUCTEURS

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a solid-state imaging device, a method of driving the solid-state imaging device, an imaging system, and a movable object.

Description of the Related Art

[0002] As photon detector, an avalanche photo diode (APD) and a single photon avalanche diode (SPAD) in which charges generated by photon incidence are amplified by avalanche breakdown are known. These photon detectors are used for capturing or ranging as a photon count sensor that counts the number of detected photons. In general, the sensor using the SPAD is formed of a photon detector, a quench element, a waveform shaper, and a signal processing circuit. An avalanche current generated by the photon detector detecting photons causes a voltage drop through the quench element and generates a photon detection signal. The photon detection signal is shaped into a pulse-like waveform by the waveform shaper, and the shaped signal is input to the signal processing circuit. Japanese Patent Application Laid-Open No. 2006-179587 discloses that detection response speed is improved by performing switching between a Geiger mode and a non-Geiger mode of a photon detector in accordance with a photon detection signal or a control signal.

[0003] When signal processing is performed on a photon detection signal, it is desirable to hold the photon detection signal for a certain period of time. However, the method disclosed in Japanese Patent Application Laid-Open No. 2006-179587 does not consider to hold a photon detection signal, and signal processing that can be performed on a photon detection signal by the post-stage signal processing circuit is limited to very simple processing. For example, in a photon count sensor having two-dimensionally arranged pixels, although each pixel can perform counting of the number of photons independently, it is difficult to perform calculation other than simple counting such as a filtering process. Further, it is difficult to perform signal processing on a plurality of pixels simultaneously. Prior art can be found e.g. in document GB-A-2 509 545 disclosing an avalanche photodetector, the output of which is delayed and used to control quenching, in document US-B-9 671 284 disclosing a single photon avalanche diode circuit avalanche photodetector, the output of which is delayed and used to control quenching, with variable hold-off time and dual delay regime and in US-B-7 115 963 disclosing a circuitry for image sensors with avalanche photodiodes. Further, prior art can be found e.g.in document GB-A-2 269 O10 disclosing a photon counting APD with active quench and reset, in document US-A-2010/214654 disclosing an apparatus for the detection of light in a scanning microscope, in non-patent literature Cronin, D et al: "Intelligent System for Optimal Hold-Off Time Selection in an Active Quench and Reset IC", IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, Vol. 13, No. 4, 1 July 2007 (2007-07-01), pages911-918, and in document US-A-2018/006071 disclosing an imaging device, imaging system and movable object.

SUMMARY OF THE INVENTION

[0004] The present invention intends to provide a solid-state imaging device and a method of driving the same that can hold a signal detected by a photon detector and perform various signal processing.

[0005] According to aspects of the present invention, provided are a solid-state imaging device according to claim 1, an imaging system according to claim 10, and a movable object according to claim 12.

[0006] Further, according to another aspect of the present invention, a method of driving a solid-state imaging device according to claim 9 is provided.

[0007] Further features of the present invention will become apparent from the following description of exemplary embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008]

FIG. 1 is a block diagram illustrating a general configuration of a solid-state imaging device according to a first example useful for understanding the present invention.

FIG. 2 is a circuit diagram illustrating a configuration example of a pixel of the solid-state imaging device according to the first example useful for understanding the present invention.

FIG. 3 is a timing chart illustrating a method of driving the solid-state imaging device according to the first example useful for understanding the present invention.

FIG. 4 is a circuit diagram illustrating a configuration example of a pixel of a solid-state imaging device according to a first embodiment of the present invention.

FIG. 5 is a timing chart illustrating a method of driving the solid-state imaging device according to the first embodiment of the present invention.

FIG. 6 is a block diagram illustrating a general configuration of an imaging system according to a second embodiment of the present invention.

FIG. 7A is a diagram illustrating a configuration example of an imaging system according to a third embodiment of the present invention.

FIG. 7B is a diagram illustrating a configuration ex-

ample of a movable object according to the third embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS AND EXAMPLES

[First example]

[0009] A solid-state imaging device and a method of driving the same according to a first example useful for understanding the present invention will be described with reference to FIG. 1 to FIG. 3.

[0010] First, the structure of the solid-state imaging device according to the present example will be described by using FIG. 1 and FIG. 2. FIG. 1 is a block diagram illustrating a general configuration of the solid-state imaging device according to the present example. FIG. 2 is a circuit diagram illustrating a configuration example of a pixel of the solid-state imaging device according to the present example.

[0011] As illustrated in FIG. 1, a solid-state imaging device 100 according to the present example includes a pixel region 10, a vertical scanning circuit 20, a horizontal scanning circuit 30, an output circuit 40, and a control circuit 50.

[0012] In the pixel region 10, a plurality of pixels 12 arranged in a matrix over a plurality of rows and a plurality of columns are provided. The number of pixels 12 forming the pixel region 10 is not particularly limited. For example, the pixel region 10 may be formed of several thousand rows by several thousand columns of the pixels 12 as seen in general digital cameras. Alternatively, the pixel region 10 may be formed of a plurality of pixels 12 arranged in one row or one column. Alternatively, the pixel region 10 may be formed of a single pixel 12.

[0013] On each row of the pixel arrays in the pixel region 10, a control line 14 is arranged extending in a first direction (the horizontal direction in FIG. 1). Each control line 14 is connected to the pixels 12 aligned in the first direction, respectively, to form a signal line common to these pixels 12. The first direction in which the control line 14 extends may be referred to as a row direction or the horizontal direction. Each of the control lines 14 may include a plurality of signal lines used for supplying multiple types of control signal to the pixels 12.

[0014] On each column of the pixel arrays of the pixel region 10, a data line 16 is arranged extending in a second direction (the vertical direction in FIG. 1) crossing the first direction. Each data line 16 is connected to the pixels 12 aligned in the second direction, respectively, to form a signal line common to these pixels 12. The second direction in which the data line 16 extends may be referred to as a column direction or the vertical direction. Each of the data lines 16 may include a plurality of signal lines used for transferring digital signals output from the pixels 12 on a bit basis.

[0015] The control line 14 on each row is connected to the vertical scanning circuit 20. The vertical scanning circuit 20 is a circuit unit that supplies control signals used for driving the pixels 12 to the pixels 12 via the control lines 14. The vertical scanning circuit 20 sequentially scans the pixels 12 within the pixel region 10 on a row-by-row basis and outputs a pixel signal of each pixel 12 to the horizontal scanning circuit 30 via the data line 16.

[0016] The data line 16 on each column is connected to the horizontal scanning circuit 30. The horizontal scanning circuit 30 is a circuit unit that selects a pixel signal of the pixel 12 on each column output on a row-by-row basis from the pixel region 10 and sequentially outputs the selected pixel signal to the output circuit 40. The horizontal scanning circuit 30 includes a plurality of holding portions corresponding to a plurality of columns of the pixel region 10 and holds a pixel signal of the pixel 12 on each column output on a row-by-row basis from the pixel region 10 at a holding portion on the corresponding column. The horizontal scanning circuit 30 sequentially scans holding portions on respective columns and sequentially outputs pixel signals held in the holding portions on respective columns to the output circuit 40.

[0017] The output circuit 40 is a circuit unit that includes a transmitter circuit 42 and outputs the pixel signal output from the horizontal scanning circuit 30 to the outside of the solid-state imaging device 100. The transmitter circuit 42 may be formed of SERializer/DESerializer (SerDes) transmitter circuit such as a low voltage differential signaling (LVDS) circuit, a scalable low voltage signaling (SLVS) circuit, or the like, for example. Note that an external interface circuit forming the output circuit 40 is not particularly limited.

[0018] The control circuit 50 is a circuit unit used for supplying control signals that control the operation of the vertical scanning circuit 20 and the horizontal scanning circuit 30 and the timing thereof. Note that at least some of the control signals that control the operation of the vertical scanning circuit 20 and the horizontal scanning circuit 30 and the timing thereof may be supplied from the outside of the solid-state imaging device 100.

[0019] As illustrated in FIG. 2, each of the pixels 12 includes a photon detector D, a quench element Mq, a waveform shaper INV, and a signal processing circuit 18. The photon detector D may be formed of a photodiode such as an avalanche photo diode (APD) or a single photon avalanche diode (SPAD) in which charges generated by photon incidence are amplified by avalanche breakdown. The quench element Mq may be formed of a p-channel MOS transistor, for example. The waveform shaper INV may be formed of an inverter circuit, for example. The signal processing circuit 18 includes a counter circuit that counts the number of pulses output from the waveform shaper INV

[0020] The anode of the photodiode forming the photon detector D is connected to the node to which a voltage Vss is supplied. The cathode of the photodiode forming the photon detector D is connected to the drain (primary node) of the p-channel MOS transistor forming the quench element Mq. The source of the p-channel MOS

transistor forming the quench element Mq is connected to the node to which a voltage Vdd is supplied. The input terminal of the waveform shaper INV is connected to the connection node (node N) between the photon detector D and the quench element Mq. The output terminal of the waveform shaper INV is connected to the input terminal of the signal processing circuit 18. The output terminal of the signal processing circuit 18 is connected to the data line 16.

[0021] The gate (control node) of the p-channel MOS transistor forming the quench element Mq is supplied with a mode switch signal PMODE from the vertical scanning circuit 20 or the control circuit 50 via a control line 14a. The signal processing circuit 18 is supplied with a select signal PSEL from the vertical scanning circuit 20 via a control line 14b. The control lines 14a and 14b are signal lines forming the control line 14 described using FIG. 1. Note that the vertical scanning circuit 20 or the control circuit 50 that supplies the mode switch signal PMODE is a control unit that controls the quench element Mq so as to hold an output signal when the photon detector transitions from a Geiger mode to a non-Geiger mode.

[0022] The voltage Vss and the voltage Vdd are set so as to be able to apply, to the photon detector D, a reverse bias voltage which is sufficient for operation in a Geiger mode. In one example, a negative high voltage is applied as the voltage Vss, and a positive voltage around a power source voltage is applied as the voltage Vdd. In the present example, the photodiode forming the photon detector D is operated in a Geiger mode, that is, used as a single photon avalanche diode (SPAD).

[0023] Thereby, the photon detector D is in a state where a reverse bias voltage corresponding to the potential difference between the voltage Vdd and the voltage Vss is applied. This reverse bias voltage is a voltage higher than the breakdown voltage of the photodiode forming the photon detector D and is high enough to cause avalanche amplification (Geiger mode). However, since no carrier as a seed exists in a state where no photon enters the photon detector D, no avalanche amplification occurs, and no current flows in the photon detector D (standby state).

[0024] Once photons enter the photon detector D in a standby state, carriers excited by incident photons are generated inside the photon detector D. The carriers generated inside the photon detector D are accelerated by a strong electric field inside the photon detector D and causes an avalanche amplification, and a large avalanche current occurs (Geiger mode operation). Such avalanche current flows through the quench element Mq, thereby a voltage drop is caused by the quench element Mq, and the voltage between the terminals of the photon detector D decreases. Thereby, the photon detector D exits the Geiger mode (non-Geiger mode), and the avalanche amplification stops. Carriers at the node (node N) on the cathodes side of the photon detector D are gradually drained via the quench element Mq connected as a load. Thereby, the potential at the node N returns to the initial value again.

[0025] Such a series of operations causes the node N to transition from the standby state to a voltage-dropped state resulted by a flow of a large current in the Geiger mode due to photon incidence and then return to the standby state. Such a potential change at the node N is input to the waveform shaper INV as a signal Sig_A. The waveform shaper INV shapes the waveform of the input signal Sig_A to a pulse-like signal Sig_D and outputs the pulse-like signal Sig_D to the signal processing circuit 18. The signal processing circuit 18 counts the number of pulses superimposed on the signal Sig_D output from the waveform shaper INV Further, the signal processing circuit 18 performs predetermined signal processing on the signal Sig_D. The signal processing circuit 18 outputs an output signal DOUT, which is a signal resulted from signal processing, to the data line 16 in response to the select signal PSEL output from the vertical scanning circuit 20.

[0026] During a period when the mode switch signal PMODE is at a low level (or an on-state or an active state), the quench element Mq is in a relatively low resistance state and operates as a quench resistor (detection mode). On the other hand, during a period when the mode switch signal PMODE is at a high level (or an off-state or an inactive state), the quench element Mq is in a relatively high resistance state, blocks a current flowing into the quench element Mq, and holds the potential of the node N (hold mode).

[0027] Next, a method of driving the solid-state imaging device according to the present example will be described by using FIG. 3. FIG. 3 is a timing chart illustrating the method of driving the solid-state imaging device according to the present example. The timing chart of FIG. 3 illustrates the timing when a photon enters the photon detector D, the mode switch signal PMODE, the signal Sig_A, the signal Sig_D, the count value in the counter, the select signal PSEL, and the output signal DOUT.

[0028] At time t10, the mode switch signal PMODE is at a low level, and the quench element Mq is in the detection mode. No photon has entered the photon detector D, the signal Sig_A is a predetermined potential indicating the standby state, and the signal Sig_D is at a low level. Further, at the time t10, the count value of the counter is zero, and the select signal PSEL is at a low level.

[0029] At time t11, incidence of a photon occurs. In response, avalanche amplification occurs in the photon detector D with carriers excited with the incident photon being as a seed, and a flow of an avalanche current causes the potential at the node N to decrease. In response to the decrease of the potential at the node N, the potential of the signal Sig_A decreases.

[0030] On and after the time t11, the potential of the signal Sig_A gradually increases as electrons generated in the photon detector D are gradually drained via the quench element Mq.

[0031] In response to the decrease of the potential of the signal Sig_A, the signal Sig_D transitions from the

low level to the high level at time t12. The counter of the signal processing circuit 18 increments the count value by one in response to a rising edge of the signal Sig_D. Thereby, the count value in the counter becomes one.

[0032] At time t13, the vertical scanning circuit 20 controls the mode switch signal PMODE from the low level to the high level. Thereby, the quench element Mq is in a high resistance state, draining of electrons generated in the photon detector D stops, and the increase of the potential of the signal Sig_A stops. That is, the signal Sig_A is held at a constant value.

[0033] At time 114, the vertical scanning circuit 20 controls the mode switch signal PMODE from the high level to the low level. Thereby, the quench element Mq is in a low resistance state (on-state), that is, in the detection mode. In response to the transition of the quench element Mq to the low resistance state, draining of electrons via the quench element Mq is resumed, and the potential of the signal Sig_A gradually increases to a predetermined potential indicating the standby state.

[0034] At time t15, when the potential of the signal Sig_A increases to a predetermined value, the signal Sig_D transitions from the high level to the low level and returns to the standby state.

[0035] At subsequent time t16, another incidence of a photon occurs. In response, avalanche amplification occurs in the photon detector D with carriers excited by the incident photon being as a seed, and a flow of an avalanche current causes the potential at the node N to decrease. In response to the decrease of the potential at the node N, the potential of the signal Sig_A decreases.

[0036] On and after the time t16, the potential of the signal Sig_A gradually increases as electrons generated in the photon detector D are gradually drained via the quench element Mq.

[0037] In response to the decrease of the potential of the signal Sig_A due to incidence of a photon, the signal Sig_D transitions from the low level to the high level at time t17. The counter of the signal processing circuit 18 increments the count value by one in response to the rising edge of the signal Sig_D. Thereby, the count value in the counter becomes two.

[0038] At time t18, the vertical scanning circuit 20 controls the mode switch signal PMODE from the low level to the high level. Thereby, the quench element Mq is in a high resistance state, draining of electrons generated in the photon detector D stops, and the increase of the potential of the signal Sig_A stops. That is, the signal Sig_A is held at a constant value.

[0039] At time t19, the vertical scanning circuit 20 controls the select signal PSEL from the low level to the high level. Thereby, the output signal DOUT indicating the count value of two in the counter of the signal processing circuit 18 is output to the data line 16.

[0040] In FIG. 3, the signal waveforms of the signal Sig_A and the signal Sig_D when the resistance of the quench element Mq is constant (detection mode) are illustrated by dotted lines. In this case, the potential of the signal Sig_A continuously increases toward the potential of the standby state and is unable to be held at a constant value. Thus, signal processing that needs to be held for a certain period of time cannot be performed on the signal Sig_A.

[0041] In contrast, in the method of driving the solid-state imaging device according to the present example, the potential of the signal Sig_A can be held at a constant level during the period of time t13 to time t14 and a period on and after time t18 in which the mode switch signal PMODE is controlled to the high level. Therefore, according to the present example, signal processing that needs to be held for a certain period of time can be performed on the signal Sig A.

[0042] That is, when signal processing that needs to be held for a certain period of time is performed on the signal Sig_A, the mode switch signal PMODE is held at the low level. Thereby, during a period in which the signal processing circuit 18 performs signal processing, that is, a period in which the signal processing circuit 18 does not accept input, the photon detector D can be held in the hold mode, and power consumption can be reduced. The process performed by the signal processing circuit 18 is not particularly limited, which may be, for example, a filtering process, signal processing performed simultaneously on the plurality of pixels 12, or the like.

[0043] Further, when the signal processing circuit 18 performs only the process that requires substantially no period for holding an input signal, for example, a simple counting process, it is possible to set a longer period for detecting photons and increase detection sensitivity of photons by setting a shorter period of the hold mode.

[0044] Further, an operation in a non-hold mode in which the mode switch signal PMODE is maintained at the high level during an integration period from the start to the end of integration of count values in the counter may be used. This integration period is a period determined from an exposure condition such as a framerate, an aperture, a set ISO sensitivity, a shutter speed, or the like. The solid-state imaging device of the present example can perform switching between an operation having the hold mode described in the present example and an operation in the non-hold mode.

[0045] An example of selection of the operation having the hold mode described in the present example and the operation in the non-hold mode will be described. For example, the operation in the non-hold mode is used when the set ISO sensitivity is relatively high (a high sensitivity mode), and the operation having the hold mode described in the present example is used when the set ISO sensitivity is relatively low (a low sensitivity mode).

[0046] When the set ISO sensitivity is set relatively high, it is often the case of capturing a low light amount capturing scene. In such a low light amount scene, it is preferable to shorten a period in which the photon detector D is in a non-Geiger mode to enable detection of a small amount of incident photons.

[0047] On the other hand, when the set ISO sensitivity

is set relatively low, it is often the case of capturing a high light amount capturing scene. When operated in the non-hold mode, an SPAD tends to require time to return to a Geiger mode from a non-Geiger mode and be unable to detect photons entering the photon detector D during the time period. Therefore, increase of a signal value of the output signal DOUT of the pixel 12 no longer responds to increase of an incident light amount. That is, the linearity of the output signal DOUT of the pixel 12 relative to an incident light amount decreases as the incident light amount increases.

[0048] Accordingly, in such a high light amount scene, during the operation having the hold mode described in the present example, that is, the integration period, a period in which the mode switch signal PMODE is at the high level is provided for n times. Each of the n times of periods is referred to as a sub-integration period. By deriving the ratio of a count value to the number n, it is possible to estimate the amount of light entering the photon detector D. That is, in each of the n times of sub-integration periods, as the frequency of a photon entering the photon detector D increases, the count value in the counter approaches n. For example, when the count value becomes n, this indicates that photons enter the photon detector D in all the sub-integration periods, which indicates that the amount of light entering the photon detector D is large.

[0049] When a signal of the solid-state imaging element is used to generate an image, the luminance at an image position corresponding to the pixel 12 can be defined as the maximum value (typically, white). In such a way, by using the mode switch signal PMODE to provide sub-integration periods, it is possible to derive a ratio of the count value in the counter relative to the number of times of sub-integration periods. Thereby, the linearity of a signal value of the output signal DOUT of the pixel 12 relative to an increase of the incident light mount can be increased.

[0050] As discussed above, according to the present example, a signal detected by the photon detector can be held for a desired time period, and various signal processing can be performed in the post-stage signal processing circuit.

[First Embodiment]

[0051] A solid-state imaging device and a method of driving the same according to a first embodiment of the present invention will be described with reference to FIG. 4 and

[0052] FIG. 5. The same components as those in the solid-state imaging device according to the first example will be labeled with the same references, and the description thereof will be omitted or simplified.

[0053] First, the structure of the solid-state imaging device according to the present embodiment will be described by using FIG. 4. FIG. 4 is a circuit diagram illustrating a configuration example of a pixel of the solid-state imaging device according to the present embodiment.

[0054] As illustrated in FIG. 4, the pixel 12 of the solid-state imaging device according to the present embodiment further includes a quench element control circuit 22 in addition to the photon detector D, the quench element Mq, a waveform shaper INV, and the signal processing circuit 18. Other configurations of the solid-state imaging device according to the present embodiment are basically the same as the solid-state imaging device according to the first example.

[0055] The anode of the photodiode forming the photon detector D is connected to the node to which a voltage Vss is supplied. The cathode of the photodiode forming the photon detector D is connected to the drain of the p-channel MOS transistor forming the quench element Mq. The source of the p-channel MOS transistor forming the quench element Mq is connected to the node to which a voltage Vdd is supplied. The gate of the p-channel MOS transistor forming the quench element Mq is connected to the output terminal of the quench element control circuit 22. The input terminal of the waveform shaper INV is connected to the connection node (node N) between the photon detector D and the quench element Mq. The output terminal of the waveform shaper INV is connected to the input terminal of the signal processing circuit 18 and the input terminal of the quench element control circuit 22. The output terminal of the signal processing circuit 18 is connected to the data line 16.

[0056] The signal processing circuit 18 is supplied with the select signal PSEL from the vertical scanning circuit 20 via the control line 14b. Further, the signal processing circuit 18 and the quench element control circuit 22 are supplied with a control signal CLK from the vertical scanning circuit 20 or the control circuit 50 via a control line 14c. The control lines 14b and 14c are signal lines forming the control line 14 described using FIG. 1. The control signal CLK is a timing signal that determines operation timings of the solid-state imaging device, which may be a signal based on a clock signal, for example. Note that the quench element control circuit 22 is a control unit that controls the quench element so that the photon detector holds an output signal when transitioning from a Geiger mode to a non-Geiger mode.

[0057] As described in the first example, the node N transitions from the standby state to a voltage-dropped state resulted by a flow of a large current in the Geiger mode due to photon incidence and then returns to the standby state. Such a potential change at the node N is input to the waveform shaper INV as a signal Sig_A. The waveform shaper INV shapes the waveform of the input signal Sig_A to a pulse-like signal Sig_D and outputs the pulse-like signal Sig_D to the signal processing circuit 18 and the quench element control circuit 22.

[0058] The signal processing circuit 18 performs counting of the number of pulses or predetermined signal processing in synchronization with the control signal CLK. For example, when the signal Sig_D is at a high

level at the timing of a falling edge of the control signal CLK, the signal processing circuit 18 counts this pulse. Further, the signal processing circuit 18 performs predetermined signal processing on the signal Sig_D in accordance with the timing of the control signal CLK. The signal processing circuit 18 outputs an output signal DOUT, which is a signal resulted from signal processing, to the data line 16 in response to the select signal PSEL output from the vertical scanning circuit 20.

[0059] The quench element control circuit 22 detects a rising edge of the signal Sig_D output from the waveform shaper INV and controls a quench element control signal PMq output to the gate of the quench element Mq from a high level to a low level. Further, the quench element control circuit 22 detects a rising edge of the control signal CLK and controls a quench element control signal PMq output to the gate of the quench element Mq from a low level to a high level. The control signal CLK is an example of a periodic signal whose signal value changes periodically. Further, in the present embodiment, such a periodic signal is input commonly to the quench element control circuit 22 and the signal processing circuit 18.

[0060] During a period when the quench element control signal PMq is at a high level, the quench element Mq is in a relatively low resistance state and operates as a quench resistor (detection mode). On the other hand, during a period when the quench element control signal PMq is at a low level, the quench element Mq is in a relatively high resistance state, blocks a current flowing to the quench element Mq, and holds the potential of the node N (hold mode).

[0061] Next, a method of driving the solid-state imaging device according to the present embodiment will be described by using FIG. 5. FIG. 5 is a timing chart illustrating the drive method of the solid-state imaging device according to the present embodiment. The timing chart of FIG. 5 illustrates the timing when a photon enters the photon detector D, the control signal CLK, the quench element control signal PMq, the signal Sig_A, the signal Sig_D, the count value in the counter, the select signal PSEL, and the output signal DOUT.

[0062] At time t20, the quench element control signal PMq is at a low level, and the quench element Mq is in the detection mode. No photon has entered the photon detector D, the signal Sig_A is a predetermined potential illustrating the standby state, and the signal Sig_D is at a low level. Further, at the time t20, the count value of the counter is zero, and the select signal PSEL is at a low level.

[0063] At time t21, incidence of a photon occurs. In response, avalanche amplification occurs in the photon detector D with carriers excited by the incident photon being as a seed, and a flow of an avalanche current causes the potential at the node N to decrease. In response to the decrease of the potential at the node N, the potential of the signal Sig_A decreases.

[0064] On and after the time t21, the potential of the signal Sig_A gradually increases as electrons generated in the photon detector D are gradually drained via the quench element Mq.

[0065] At time t22, in response to the decrease of the potential of the signal Sig_A, the signal Sig_D transitions from the low level to the high level.

[0066] At time t23, the quench element control circuit 22 detects the rising edge of the signal Sig_D supplied from the waveform shaper INV and controls the quench element control signal PMq from the low level to the high level. Thereby, the quench element Mq is in a high resistance state, draining of electrons generated in the photon detector D stops, and the increase of the potential of the signal Sig_A stops. That is, the signal Sig_A is held at a constant value. The quench element control circuit 22 maintains the quench element control signal PMq at the high level while the control signal CLK is at the low level.

[0067] At time t24, the signal processing circuit 18 increments the count value by one in response to the falling edge of the control signal CLK. Thereby, the count value in the counter becomes one.

[0068] At time t25, the quench element control circuit 22 detects the rising edge of the control signal CLK and controls the quench element control signal PMq from the high level to the low level. Thereby, the quench element Mq is in a low resistance state, that is, in the detection mode. In response to the transition of the quench element Mq to the low resistance state, draining of electrons via the quench element Mq is resumed, and the potential of the signal Sig_A gradually increases to a predetermined potential indicating the standby state.

[0069] At time t26, when the potential of the signal Sig_A increases to a predetermined value, the signal Sig_D transitions from the high level to the low level, and returns to the standby state.

[0070] At subsequent time t27, another incidence of a photon occurs. In response, avalanche amplification occurs in the photon detector D with carriers excited by the incident photon being as a seed, and a flow of an avalanche current causes the potential at the node N to decrease. In response to the decrease of the potential at the node N, the potential of the signal Sig_A decreases.

[0071] On and after the time t27, the potential of the signal Sig_A gradually increases as electrons generated in the photon detector D are gradually drained via the quench element Mq.

[0072] At time t28, in response to the decrease of the potential of the signal Sig_A due to incidence of a photon, the signal Sig_D transitions from the low level to the high level.

[0073] At time t29, the quench element control circuit 22 detects the rising edge of the signal Sig_D supplied from the signal processing circuit 18 and controls the quench element control signal PMq from the low level to the high level. Thereby, the quench element Mq is in a high resistance state, draining of electrons generated in the photon detector D stops, and the increase of the potential of the signal Sig_A stops. That is, the signal Sig_A

is held at a constant value.

[0074] At time t30, the signal processing circuit 18 increments the count value by one in response to the falling edge of the control signal CLK. Thereby, the count value in the counter becomes two.

[0075] At time t31, the vertical scanning circuit 20 controls the select signal PSEL from the low level to the high level. Thereby, the output signal DOUT indicating the count value of two in the counter of the signal processing circuit 18 is output to the data line 16.

[0076] Note that, while the case where incidence of a photon occurs in a period in which the control signal CLK is at a high level has been assumed in the example described above, the quench element Mq is in a hold mode when incidence of a photon occurs in a period in which the control signal CLK is at a high level, and the signals Sig_A and Sig_D do not change. That is, in the solid-state imaging device according to the present embodiment, detection of a photon and signal processing on the signal Sig_D are enabled in synchronization with the control signal CLK.

[0077] In FIG. 5, the signal waveforms of the signal Sig_A and the signal Sig_D when the resistance of the quench element Mq is constant (detection mode) are illustrated by doted lines. In this case, the potential of the signal Sig_A continuously increases toward the potential of the standby state and is unable to be held at a constant value. Thus, signal processing that needs to be held for a certain period of time cannot be performed on the signal Sig_A.

[0078] In contrast, in the method of driving the solid-state imaging device according to the present embodiment, the potential of the signal Sig_A can be held at a constant level during the period of time t23 to time t25 and a period on and after time t29 in which the quench element control signal PMq is controlled to the high level. Therefore, according to the present embodiment, signal processing that needs to be held for a certain period of time can be performed on the signal Sig_A.

[0079] In particular, in the present embodiment, since the quench element Mq is switched to the hold mode in accordance with the level of the signal Sig_D, switching of the quench element Mq to the hold mode can be performed independently on a pixel 12 basis immediately after photon detection. Therefore, the present embodiment is a more preferable form than the first example in terms of reduction of consumption power.

[0080] Further, since the quench element Mq is switched to the detection mode when the control signal CLK becomes a high level, the present embodiment is a more preferable form also when signal processing across a plurality of pixels 12 is performed, such as when detection results at a certain timing of the plurality of pixels 12 are intended to be acquired at the same time, for example.

[0081] Further, while the same control signal CLK is input to the quench element control circuit 22 and the signal processing circuit 18 in the present embodiment, the embodiment is not limited to this example. For example, separate control signals may be supplied to the signal processing circuit 18 and the quench element control circuit 22. Further, as another example, a frequency division circuit, which divides the frequency of the control signal CLK, is provided in the pre-stage of the quench element control circuit 22. Further, a signal resulted by dividing the frequency of the control signal CLK may be input from the frequency division circuit to the quench element control circuit 22. Including the above form in which a signal resulted by dividing the frequency of the control signal CLK is input to the quench element control circuit 22, a form in which a signal based on the control signal CLK is input to the quench element control circuit 22 is preferable.

[0082] As discussed above, according to the present embodiment, a signal detected by the photon detector can be held for a desired time period, and various signal processing can be performed on the post-stage signal processing circuit. Further, detection of photons or signal processing can be performed in response to a timing signal, and a synchronous system of photo-counting can be realized.

[0083] Note that, also in the present embodiment, as described in the first example, an operation having the hold mode described in the present embodiment or an operation in the non-hold mode can be appropriately used. For example, the operation in the non-hold mode is used when the set ISO sensitivity is relatively high (a high sensitivity mode), and the operation having the hold mode described in the present embodiment is used when the set ISO sensitivity is relatively low (a low sensitivity mode).

[0084] During the operation having the hold mode described in the present embodiment, that is, the integration period, n times of sub-integration periods are provided. In the present embodiment, these sub-integration periods are respective periods in which the control signal CLK is at the high level. By deriving the ratio of a count value to the number n, it is possible to estimate the amount of light entering the photon detector D. That is, in each of the n times of sub-integration periods, as the frequency of a photon entering the photon detector D increases, the count value in the counter approaches n. For example, when the count value becomes n, this indicates that photons enter the photon detector D in all the sub-integration periods, which indicates that the amount of light entering the photon detector D is large.

[0085] When a signal of the solid-state imaging element is used to generate an image, the luminance at an image position corresponding to the pixel 12 can be defined as the maximum value (typically, white). In such a way, by using the mode switch signal PMODE to provide sub-integration periods, it is possible to derive a ratio of the count value in the counter relative to the number of times of sub-integration periods. Thereby, the linearity of a signal value of the output signal DOUT of the pixel 12 relative to an increase of the incident light mount can be

increased. Further, an increase in the frequency of the control signal CLK allows the linearity to be higher.

[Second Embodiment]

[0086] An imaging system according to a second embodiment of the present invention will be described with reference to FIG. 6. FIG. 6 is a block diagram illustrating a general configuration of the imaging system according to the present embodiment.

[0087] The solid-state imaging device 100 described in the first example and the first embodiment described above can be applied to various imaging systems. Examples of applicable imaging systems may include a digital still camera, a digital camcorder, a surveillance camera, a copying machine, a fax machine, a mobile phone, an on-vehicle camera, an observation satellite, and the like. In addition, a camera module including an optical system such as a lens and an imaging device is also included in the imaging system. FIG. 6 illustrates a block diagram of a digital still camera as an example out of these examples.

[0088] The imaging system 200 illustrated as an example in FIG. 6 includes an imaging device 201, a lens 202 that captures an optical image of an object onto the imaging device 201, an aperture 204 for changing a light amount passing through the lens 202, and a barrier 206 for protecting the lens 202. The lens 202 and the aperture 204 form an optical system that converges a light onto the imaging device 201. The imaging device 210 is the solid-state imaging device 100 described in the first example (not claimed) or the first embodiment and converts an optical image captured by the lens 202 into image data.

[0089] The imaging system 200 further includes a signal processing unit 208 that processes an output signal output from the imaging device 201. The signal processing unit 208 preforms an AD-conversion that converts an analog signal output by the imaging device 201 into a digital signal. In addition, the signal processing unit 208 performs various correction and compression other than above, if necessary, and outputting image data. An AD-conversion unit, which is a part of the signal processing unit 208, may be formed on a semiconductor substrate on which the imaging device 201 is provided or a semiconductor substrate on which the imaging device 201 is not provided. Further, the imaging device 201 and the signal processing unit 208 may be formed on the same semiconductor substrate.

[0090] The imaging system 200 further includes a memory unit 210 for temporarily storing image data therein and an external interface unit (external I/F unit) 212 for communicating with an external computer or the like. The imaging system 200 further includes a storage medium 214 such as a semiconductor memory for performing storage or readout of imaging data and a storage medium control interface unit (storage medium control I/F unit) 216 for performing storage or readout on the storage medium 214. Note that the storage medium 214 may be embedded in the imaging system 200 or may be removable.

[0091] The imaging system 200 further includes a general control/operation unit 218 that controls various operations and the entire digital still camera and a timing generation unit 220 that outputs various timing signals to the imaging device 201 and the signal processing unit 208. Here, the timing signal or the like may be input from the outside, and the imaging system 200 may include at least the imaging device 201 and the signal processing unit 208 that processes an output signal output from the imaging device 201.

[0092] The imaging device 201 outputs an imaging signal to the signal processing unit 208. The signal processing unit 208 performs predetermined signal processing on an imaging signal output from the imaging device 201 and outputs image data. The signal processing unit 208 uses an imaging signal to generate an image.

[0093] As discussed above, according to the present embodiment, the imaging system to which the solid-state imaging device 100 according to the first example (not claimed) or first embodiment is applied can be realized.

[Third Embodiment]

[0094] An imaging system and a movable object according to a third embodiment of the present invention will be described with reference to FIG. 7A and FIG. 7B. FIG. 7A is a diagram illustrating a configuration of an imaging system according to the present embodiment. FIG. 7B is a diagram illustrating a configuration of a movable object according to the present embodiment.

[0095] FIG. 7A illustrates an example of an imaging system related to an on-vehicle camera. The imaging system 300 includes an imaging device 310. The imaging device 310 is the solid-state imaging device 100 described in any of the above first example (not claimed) and first embodiment. The imaging system 300 includes an image processing unit 312 that performs image processing on a plurality of image data acquired by the imaging device 310 and a parallax acquisition unit 314 that calculates a parallax (a phase difference of parallax images) from the plurality of image data acquired by the imaging system 300. Further, the imaging system 300 includes a distance acquisition unit 316 that calculates a distance to the object based on the calculated parallax and a collision determination unit 318 that determines whether or not there is a collision possibility based on the calculated distance. Here, the parallax acquisition unit 314 and the distance acquisition unit 316 are an example of a distance information acquisition unit that acquires distance information on the distance to the object. That is, the distance information is information on a parallax, a defocus amount, a distance to an object, or the like. The collision determination unit 318 may use any of the distance information to determine the collision possibility. The distance information acquisition unit may be

implemented by dedicatedly designed hardware or may be implemented by a software module. Further, the distance information acquisition unit may be implemented by a Field Programmable Gate Array (FPGA), an Application Specific Integrated Circuit (ASIC), or the like, or may be implemented by combination thereof.

[0096] The imaging system 300 is connected to the vehicle information acquisition device 320 and can acquire vehicle information such as a vehicle speed, a yaw rate, a steering angle, or the like. Further, the imaging system 300 is connected to a control ECU 330, which is a control device that outputs a control signal for causing a vehicle to generate braking force based on a determination result by the collision determination unit 318. Further, the imaging system 300 is also connected to an alert device 340 that issues an alert to the driver based on a determination result by the collision determination unit 318. For example, when the collision probability is high as the determination result of the collision determination unit 318, the control ECU 330 performs vehicle control to avoid a collision or reduce damage by applying a brake, pushing back an accelerator, suppressing engine power, or the like. The alert device 340 alerts a user by sounding an alert such as a sound, displaying alert information on a display of a car navigation system or the like, providing vibration to a seat belt or a steering wheel, or the like.

[0097] In the present embodiment, an area around a vehicle, for example, a front area or a rear area is captured by using the imaging system 300. FIG. 7B illustrates the imaging system when a front area of a vehicle (a capturing area 350) is captured. The vehicle information acquisition device 320 transmits an instruction to the imaging system 300 or the imaging device 310. Such a configuration can further improve the ranging accuracy.

[0098] Although the example of control for avoiding a collision to another vehicle has been described, the embodiment is applicable to automatic driving control for following another vehicle, automatic driving control for not going out of a traffic lane, or the like. Furthermore, the imaging system is not limited to a vehicle such as the subject vehicle and can be applied to a movable object (moving apparatus) such as a ship, an airplane, or an industrial robot, for example. In addition, the imaging system can be widely applied to a device which utilizes object recognition, such as an intelligent transportation system (ITS), without being limited to movable objects.

[Modified Embodiments]

[0099] The present invention is not limited to the embodiments described above, and various modifications are possible.

[0100] Further, while a solid-state imaging device in which the pixels 12 are arranged two-dimensionally inside the pixel region 10 has been assumed in the embodiments described above, the arrangement of the pixels 12 is not limited to be two-dimensional. For example, a solid-state imaging device may be formed of a single pixel 12, or the pixels 12 may be arranged one-dimensionally or three-dimensionally.

[0101] Further, while each of the control lines 14 is used as a signal line common to all the pixels 12 on each row and each of the data lines 16 is used as a signal line common to all the pixels 12 on each column in the embodiments described above, the arrangement of the control lines 14 and the data lines 16 is not limited thereto. For example, a common control line 14 or a common data line 16 may be arranged on a block basis in a unit of i row(s) by j column(s) (i and j are both natural numbers).

[0102] Further, the imaging systems illustrated in the above second and third embodiments are examples of an imaging system to which the photoelectric conversion device of the present invention may be applied, and an imaging system to which the photoelectric conversion device of the present invention can be applied is not limited to the configuration illustrated in FIG. 6 and FIG. 7A.

[0103] While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments but by the scope of the following claims.

Claims

1. A solid-state imaging device comprising:

a photon detector (D) that operates in a Geiger mode and outputs an analog output signal as a result of an avalanche amplification in accordance with the incidence of a photon;
a quench element (Mq) that causes the photon detector to transition to a non-Geiger mode in which the avalanche amplification does not occur; and
a signal processing circuit (18) that performs a predetermined process on the output signal,
characterized by
a control unit (22) that is supplied with a control signal (CLK) and a digital signal which is shaped into a pulse-like waveform from the analog output signal from the photon detector and switches, in accordance with the control signal and the digital signal, the quench element between a state in which the quench element has a relatively low resistance and the photon detector detects the photon in the Geiger mode, and a hold state in which the quench element has a relatively high resistance and a potential of a node between the photon detector and the quench element is controlled to hold the photon detector in the non-Geiger mode, wherein
the control unit (22) switches the quench element from the low resistance state to the high

resistance state when the photon detector transitions from the Geiger mode to the non-Geiger mode, and then switches the quench element from the high resistance state to the low resistance state;
the control signal is a periodic signal whose signal value changes periodically from a first level to a second level; and
the signal processing circuit performs the predetermined process in synchronization with the control signal.

2. The solid-state imaging device according to claim 1 , wherein the control unit switches the quench element from the high resistance state to the low resistance state in response to transition of the control signal, which determines an operation timing, from the first level to the second level.

3. The solid-state imaging device according to claim 2, wherein the control unit sets the quench element in the high resistance state during a period in which the control signal is at the first level.

4. The solid-state imaging device according to any one of claims 1 to 3, wherein the quench element is a transistor, the low resistance state corresponds to a state where the transistor is in an on-state, and the high resistance state corresponds to a state where the transistor is in an off-state.

5. The solid-state imaging device according to any one of claims 1 to 4,

wherein the signal processing circuit includes a counter that performs integration of the number of times of a change of the output signal,
wherein the solid-state imaging device is capable of selecting an operation mode out of a plurality of operation modes including the hold state and the non-hold state,
wherein in the hold state, the control unit controls the quench element so that the photon detector holds the output signal when transitioning from the Geiger mode to the non-Geiger mode over a period from start to end of the integration performed by the counter, and
wherein in the non-hold state, the control unit controls the quench element so that the photon detector does not hold the output signal when transitioning from the Geiger mode to the non-Geiger mode over a period from start to end of the integration performed by the counter and the photon detector transitions from the non-Geiger mode to the Geiger mode.

6. The solid-state imaging device according to any of claims 1 to 5, wherein:

the photon detector (D) outputs the output signal resulting from avalanche amplification of the photon;
the quench element comprises a transistor (Mq) having a drain connected to the photon detector (D) and a source connected to a node to which a voltage V_{DD} is supplied;
the control unit (22) supplies a signal to the gate of the transistor to cause the transistor to be in the relatively low resistance state at a set predetermined cycle, wherein
the photon may be detected when the transistor is in the relatively low resistance state.

7. The solid-state imaging device according to claim 6, wherein the control signal is a signal resulting from dividing the frequency of a clock signal.

8. The solid-state imaging device according to claim 7, wherein the analog output signal is held at a constant value by the quench element in the hold state.

9. A method of driving a solid-state imaging device including a photon detector (D) that outputs an analog output signal as a result of an avalanche amplification in accordance with an incidence of a photon if the photon detector operates in a Geiger mode; a quench element (Mq) that causes the photon detector to transition to a non-Geiger mode in which the avalanche amplification does not occur; and a signal processing circuit (18) that performs a predetermined process on the output signal in synchronization with a control signal (CLK), the method being **characterized by** comprising:

when the photon detector transitions from the Geiger mode to the non-Geiger mode in accordance with a digital signal which is shaped into a pulse-like waveform from the analog output signal from the photon detector and the control signal (CLK), switching the quench element from a relatively low resistance state to a relatively high resistance state, wherein
the quench element is switched from the low resistance state to the high resistance state such that a potential of a node between the photon detector and the quench element is controlled to hold the photon detector in the non-Geiger mode when the photon detector transitions from the Geiger mode to the non-Geiger mode, and then the quench element is switched from the high resistance state to the low resistance state;
the control signal is a periodic signal whose signal value changes periodically from a first level to a second level.

10. An imaging system comprising a plurality of pixels each including a solid-state imaging device accord-

ing to any one of claims 1 to 8.

11. The imaging system according to claim 10, further comprising
a signal processing unit that processes a signal output from the solid-state imaging devices.

12. A movable object comprising:

the solid-state imaging device according to any one of claims 1 to 8;
a distance information acquisition unit that acquires distance information on a distance to an object, from parallax images based on a signal from the solid-state imaging device; and
a control unit that controls the movable object based on the distance information.

Patentansprüche

1. Festkörperabbildungseinrichtung, die aufweist:

einen Photonendetektor (D), der in einem Geigermodus arbeitet und ein Ausgabesignal als ein Ergebnis einer Lawinenverstärkung gemäß dem Einfall eines Photons ausgibt;
ein Quenchelement (Mq), das veranlasst, dass der Photonendetektor in einen Nicht-Geigermodus übergeht, in dem die Lawinenverstärkung nicht auftritt; und
eine Signalverarbeitungsschaltung (18), die einen vorbestimmten Prozess an dem Ausgabesignal durchführt,
gekennzeichnet durch
eine Steuerungseinheit (22), der ein Steuerungssignal und ein digitales Signal, das aus dem Ausgabesignal von dem Photonendetektor in eine impulsartige Wellenform geformt ist, zugeführt werden, und die gemäß dem Steuerungssignal und dem digitalen Signal das Quenchelement zwischen einem Zustand, in dem das Quenchelement einen relativ niedrigen Widerstand hat und der Photonendetektor das Photon in dem Geigermodus erfasst, und einem Haltezustand, in dem das Quenchelement einen relativ hohen Widerstand hat und ein Potential eines Knotens zwischen dem Photonendetektor und dem Quenchelement so gesteuert ist, dass der Photonendetektor in dem Nicht-Geigermodus gehalten wird, schaltet, wobei
die Steuerungseinheit (22) das Quenchelement von dem Zustand niedrigen Widerstands zu dem Zustand hohen Widerstands schaltet, wenn der Photonendetektor von dem Geigermodus zu dem Nicht-Geigermodus übergeht, und dann das Quenchelement von dem Zustand hohen Widerstands zu dem Zustand niedrigen Widerstands schaltet;
das Steuerungssignal ein periodisches Signal (PMq) ist, dessen Signalwert periodisch von einem ersten Niveau zu einem zweiten Niveau wechselt; und
die Signalverarbeitungsschaltung den vorbestimmten Prozess synchron mit dem Steuerungssignal durchführt.

2. Festkörperabbildungseinrichtung nach Anspruch 1, wobei die Steuerungseinheit das Quenchelement von dem Zustand hohen Widerstands zu dem Zustand niedrigen Widerstands als Reaktion auf einen Übergang des Steuerungssignals von dem ersten Niveau zu dem zweiten Niveau, das einen Betriebszeitpunkt bestimmt, schaltet.

3. Festkörperabbildungseinrichtung nach Anspruch 2, wobei die Steuerungseinheit das Quenchelement in den Zustand hohen Widerstands während einer Periode, in der das Steuerungssignal auf dem ersten Niveau ist, einstellt.

4. Festkörperabbildungseinrichtung nach einem der Ansprüche 1 bis 3, wobei das Quenchelement ein Transistor ist, der Zustand niedrigen Widerstands einem Zustand entspricht, in dem der Transistor eingeschaltet ist, und der Zustand hohen Widerstands einem Zustand entspricht, in dem der Transistor ausgeschaltet ist.

5. Festkörperabbildungseinrichtung nach einem der Ansprüche 1 bis 4,

wobei die Signalverarbeitungsschaltung einen Zähler enthält, der eine Integration der Anzahl an Malen einer Änderung des Ausgangssignals integriert,
wobei die Festkörperabbildungseinrichtung in der Lage ist, einen Betriebsmodus aus einer Vielzahl von Betriebsmodi einschließlich einem Haltemodus und einem Nicht-Haltemodus auszuwählen,
wobei die Steuerungseinheit in dem Haltemodus das Quenchelement so steuert, dass der Photonendetektor das Ausgabesignal über eine Periode von einem Start bis zu einem Ende der Integration, die durch den Zähler durchgeführt wird, hält, wenn er von dem Geigermodus zu dem Nicht-Geigermodus übergeht, und
wobei die Steuerungseinheit in dem Nicht-Haltemodus das Quenchelement so steuert, dass der Photonendetektor das Ausgabesignal nicht über eine Periode vom Start bis zum Ende der Integration, die durch den Zähler durchgeführt wird, hält, wenn er von dem Geigermodus zu dem Nicht-Geigermodus übergeht, und der Photonendetektor von dem Nicht-Geigermodus

zu dem Geigermodus übergeht.

6. Festkörperabbildungseinrichtung nach einem der Ansprüche 1 bis 5, wobei:

der Photonendetektor (D) ein Signal, das aus einer Lawinenverstärkung des Photons resultiert, ausgibt;
das Quenchelement einen Transistor (Mq) mit einer Drain, die mit dem Photonendetektor (D) verbunden ist, und einer Source, die mit einem Knoten, dem eine Spannung V_{DD} zugeführt wird, verbunden ist, aufweist;
die Steuerungseinheit (22) dem Gate des Transistors ein Signal zuführt, um den Transistor zu veranlassen, in dem Zustand relativ niedrigen Widerstands bei einem eingestellten vorbestimmten Zyklus zu sein, wobei
ein Photon erfasst werden kann, wenn der Transistor in dem eingeschalteten Zustand ist.

7. Festkörperabbildungseinrichtung nach Anspruch 6, wobei das Steuerungssignal ein Signal ist, das vom Teilen der Frequenz eines Taktsignals resultiert.

8. Festkörperabbildungseinrichtung nach einem der Ansprüche 1 bis 7, wobei das Analogsignal durch das Quenchelement in dem Haltezustand bei einem konstanten Wert gehalten wird.

9. Verfahren zum Steuern einer Festkörperabbildungseinrichtung, die einen Photonendetektor (D), der in einem Geigermodus arbeitet und ein Ausgabesignal als ein Ergebnis einer Lawinenverstärkung gemäß dem Einfall eines Photons ausgibt; ein Quenchelement (Mq), das den Photonendetektor veranlasst, in einen Nicht-Geigermodus überzugehen, in dem die Lawinenverstärkung nicht auftritt; und eine Signalverarbeitungsschaltung (18), die einen vorbestimmten Prozess an dem Ausgabesignal synchron mit einem Steuerungssignal (CLK) durchführt, enthält, wobei das Verfahren **dadurch gekennzeichnet ist, dass** es aufweist:
wenn der Photonendetektor von dem Geigermodus zu dem Nicht-Geigermodus gemäß einem digitalen Signal, das aus dem Ausgabesignal von dem Photonendetektor in eine impulsartige Wellenform geformt ist, und dem Steuerungssignal übergeht:

Schalten des Quenchelements von einem Zustand relativ niedrigen Widerstands zu einem Zustand relativ hohen Widerstands, wodurch das Ausgabesignal bei einem konstanten Wert gehalten wird, wobei
das Quenchelement von dem Zustand niedrigen Widerstands zu dem Zustand hohen Widerstands so geschaltet wird, dass ein Potential eines Knotens zwischen dem Photonendetektor und dem Quenchelement so gesteuert wird, dass der Photonendetektor indem Nicht-Geigermodus gehalten wird, wenn der Photonendetektor von dem Geigermodus zu dem Nicht-Geigermodus übergeht, und das Quenchelement dann von dem Zustand hohen Widerstands zu dem Zustand niedrigen Widerstands geschaltet wird
das Steuerungssignal ein periodisches Signal ist, dessen Signalwert sich periodisch von einem ersten Niveau zu einem zweiten Niveau ändert.

10. Abbildungssystem mit einer Vielzahl von Pixeln, die jeweils eine Festkörperabbildungseinrichtung nach einem der Ansprüche 1 bis 8 aufweisen.

11. Abbildungssystem nach Anspruch 10, ferner mit einer Signalverarbeitungseinheit, die ein Signal, das von den Festkörperabbildungseinrichtungen ausgegeben wird, verarbeitet.

12. Bewegliches Objekt, das aufweist:

die Festkörperabbildungseinrichtung nach einem der Ansprüche 1 bis 8;
eine Abstandsinformationserhalteeinheit, die eine Abstandsinformation über einen Abstand zu einem Objekt von Parallaxbildern, die auf einem Signal von der Festkörperabbildungseinrichtung basieren, erhält; und
eine Steuerungseinheit, die das bewegliche Objekt basierend auf der Abstandsinformation steuert.

Revendications

1. Dispositif d'imagerie à semi-conducteurs comprenant :

un détecteur de photon (D) qui fonctionne dans un mode Geiger et délivre en sortie un signal de sortie analogique en résultat d'une amplification en avalanche en fonction de l'incidence d'un photon ;
un élément d'extinction (Mq) qui amène le détecteur de photon à passer dans un mode non-Geiger dans lequel l'amplification en avalanche ne se produit pas ; et
un circuit de traitement de signal (18) qui effectue un processus prédéterminé sur le signal de sortie,
caractérisé par
une unité de commande (22) à laquelle sont fournis un signal de commande (CLK) et un signal numérique qui est façonné en une forme d'onde de type impulsion à partir du signal de

sortie analogique provenant du détecteur de photon et qui commute, conformément au signal de commande et au signal numérique, l'élément d'extinction entre un état dans lequel l'élément d'extinction a une résistance relativement faible et le détecteur de photon détecte le photon dans le mode Geiger, et un état de maintien dans lequel l'élément d'extinction a une résistance relativement élevée et un potentiel d'un noeud entre le détecteur de photon et l'élément d'extinction est commandé pour maintenir le détecteur de photon dans le mode non-Geiger, dans lequel

l'unité de commande (22) commute l'élément d'extinction de l'état de faible résistance à l'état de résistance élevée lorsque le détecteur de photon passe du mode Geiger au mode non-Geiger, et commute alors l'élément d'extinction de l'état de résistance élevée à l'état de faible résistance ;

le signal de commande est un signal périodique dont la valeur de signal change périodiquement d'un premier niveau à un second niveau ; et

le circuit de traitement du signal effectue le processus prédéterminé en synchronisation avec le signal de commande.

2. Dispositif d'imagerie à semi-conducteurs selon la revendication 1, dans lequel l'unité de commande commute l'élément d'extinction de l'état de résistance élevée à l'état de faible résistance en réponse à un passage du signal de commande, qui détermine un cadencement de fonctionnement, du premier niveau au second niveau.

3. Dispositif d'imagerie à semi-conducteurs selon la revendication 2, dans lequel l'unité de commande établit l'élément d'extinction dans l'état de résistance élevée pendant une période pendant laquelle le signal de commande est au premier niveau.

4. Dispositif d'imagerie à semi-conducteurs selon l'une quelconque des revendications 1 à 3, dans lequel l'élément d'extinction est un transistor, l'état de faible résistance correspond à un état dans lequel le transistor est dans un état passant, et l'état de résistance élevée correspond à un état dans lequel le transistor est dans un état bloqué.

5. Dispositif d'imagerie à semi-conducteurs selon l'une quelconque des revendications 1 à 4,

dans lequel le circuit de traitement de signal comporte un compteur qui effectue une intégration du nombre de changements du signal de sortie,

dans lequel le dispositif d'imagerie à semi-conducteurs est capable de sélectionner un mode de fonctionnement parmi une pluralité de modes de fonctionnement comportant l'état de maintien et l'état de non-maintien,

dans lequel, dans l'état de maintien, l'unité de commande commande l'élément d'extinction de sorte que le détecteur de photon maintien le signal de sortie lors du passage du mode Geiger au mode non-Geiger sur une période allant du début à la fin de l'intégration effectuée par le compteur, et

dans lequel, dans l'état de non-maintien, l'unité de commande commande l'élément d'extinction de sorte que le détecteur de photon ne maintient pas le signal de sortie lors du passage du mode Geiger au mode non-Geiger sur une période allant du début à la fin de l'intégration effectuée par le compteur et le détecteur de photons passe du mode non-Geiger au mode Geiger.

6. Dispositif d'imagerie à semi-conducteurs selon l'une quelconque des revendications 1 à 5, dans lequel :

le détecteur de photon (D) délivre en sortie le signal de sortie résultant de l'amplification en avalanche du photon ;

l'élément d'extinction comprend un transistor (Mq) ayant un drain connecté au détecteur de photon (D) et une source connectée à un noeud auquel une tension V_{DD} est fournie ;

l'unité de commande (22) fournit un signal à la grille du transistor pour amener le transistor à être dans l'état de résistance relativement faible selon un cycle prédéterminé défini, dans lequel le photon peut être détecté lorsque le transistor est dans l'état de résistance relativement faible.

7. Dispositif d'imagerie à semi-conducteurs selon la revendication 6, dans lequel le signal de commande est un signal résultant d'une division de la fréquence d'un signal d'horloge.

8. Dispositif d'imagerie à semi-conducteurs selon la revendication 7, dans lequel le signal de sortie analogique est maintenu à une valeur constante par l'élément d'extinction dans l'état de maintien.

9. Procédé d'attaque d'un dispositif d'imagerie à semi-conducteurs comportant un détecteur de photon (D) qui délivre en sortie un signal de sortie analogique en résultat d'une amplification en avalanche en fonction d'une incidence d'un photon si le détecteur de photon fonctionne dans un mode Geiger ; un élément d'extinction (Mq) qui amène le détecteur de photon à passer dans un mode non-Geiger dans lequel l'amplification en avalanche ne se produit pas ; et un circuit de traitement de signal (18) qui effectue un processus prédéterminé sur le signal de sortie en synchronisation avec un signal de commande

(CLK), le procédé étant **caractérisé en ce qu'**il comprend :

lorsque le détecteur de photon passe du mode Geiger au mode non-Geiger conformément à un signal numérique qui est façonné en une forme d'onde de type impulsion à partir du signal de sortie analogique provenant du détecteur de photon et au signal de commande (CLK), la commutation de l'élément d'extinction d'un état de résistance relativement faible à un état de résistance relativement élevée, dans lequel
l'élément d'extinction est commuté de l'état de faible résistance à l'état de résistance élevée de telle sorte qu'un potentiel d'un noeud entre le détecteur de photon et l'élément d'extinction est commandé pour maintenir le détecteur de photon dans le mode non-Geiger lorsque le détecteur de photon passe du mode Geiger au mode non-Geiger, et l'élément d'extinction est alors commuté de l'état de résistance élevée à l'état de faible résistance ;
le signal de commande est un signal périodique dont la valeur de signal change périodiquement d'un premier niveau à un second niveau.

10. Système d'imagerie comprenant une pluralité de pixels comportant chacun un dispositif d'imagerie à semi-conducteurs selon l'une quelconque des revendications 1 à 8.

11. Système d'imagerie selon la revendication 10, comprenant en outre
une unité de traitement de signal qui traite un signal délivré en sortie par les dispositifs d'imagerie à semi-conducteurs.

12. Objet mobile comprenant :

le dispositif d'imagerie à semi-conducteurs selon l'une quelconque des revendications 1 à 8 ;
une unité d'acquisition d'informations de distance qui acquiert des informations de distance concernant une distance par rapport à un objet, à partir d'images de parallaxe sur la base d'un signal provenant du dispositif d'imagerie à semi-conducteurs ; et
une unité de commande qui commande l'objet mobile sur la base des informations de distance.

FIG. 1

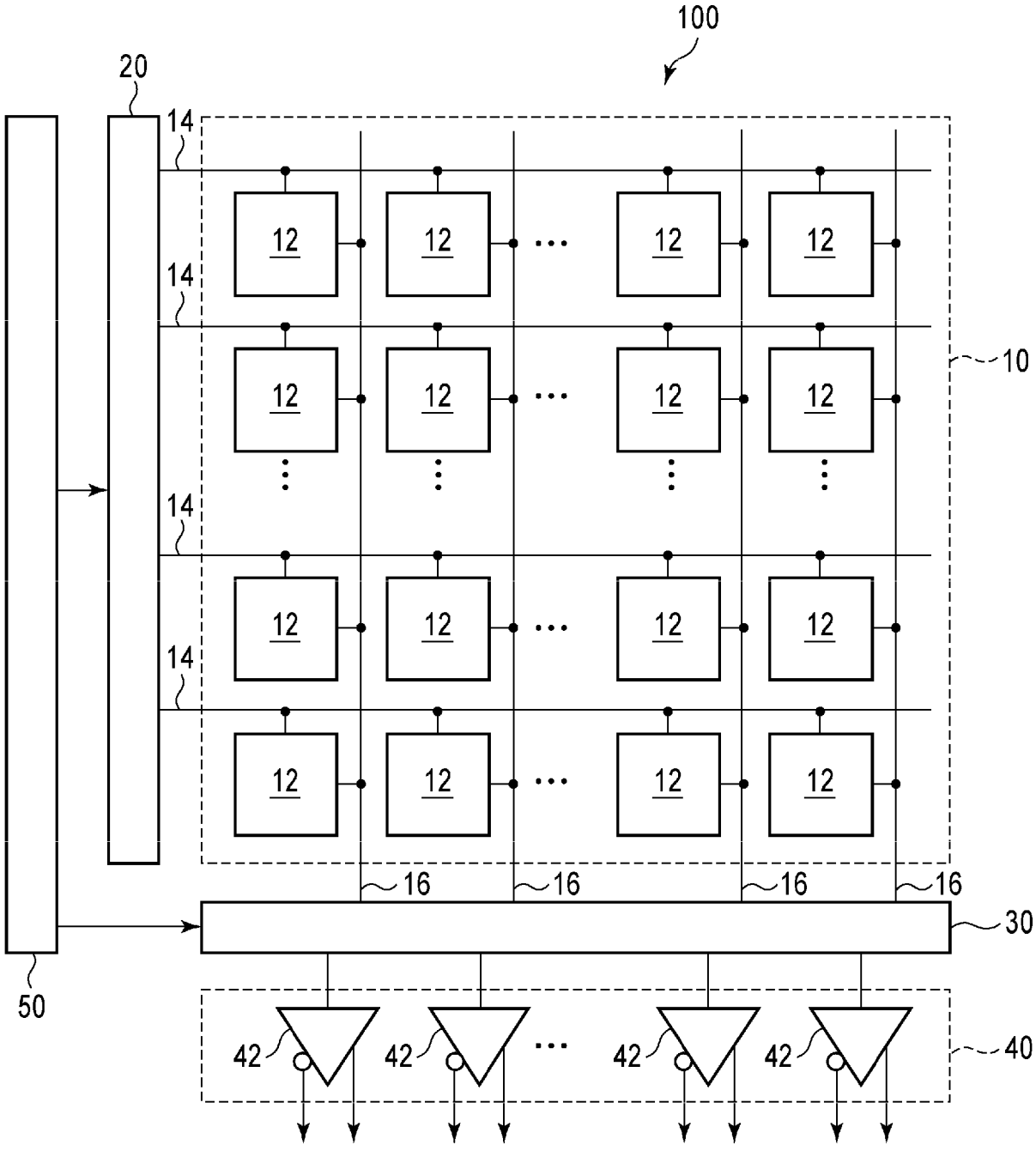


FIG. 2

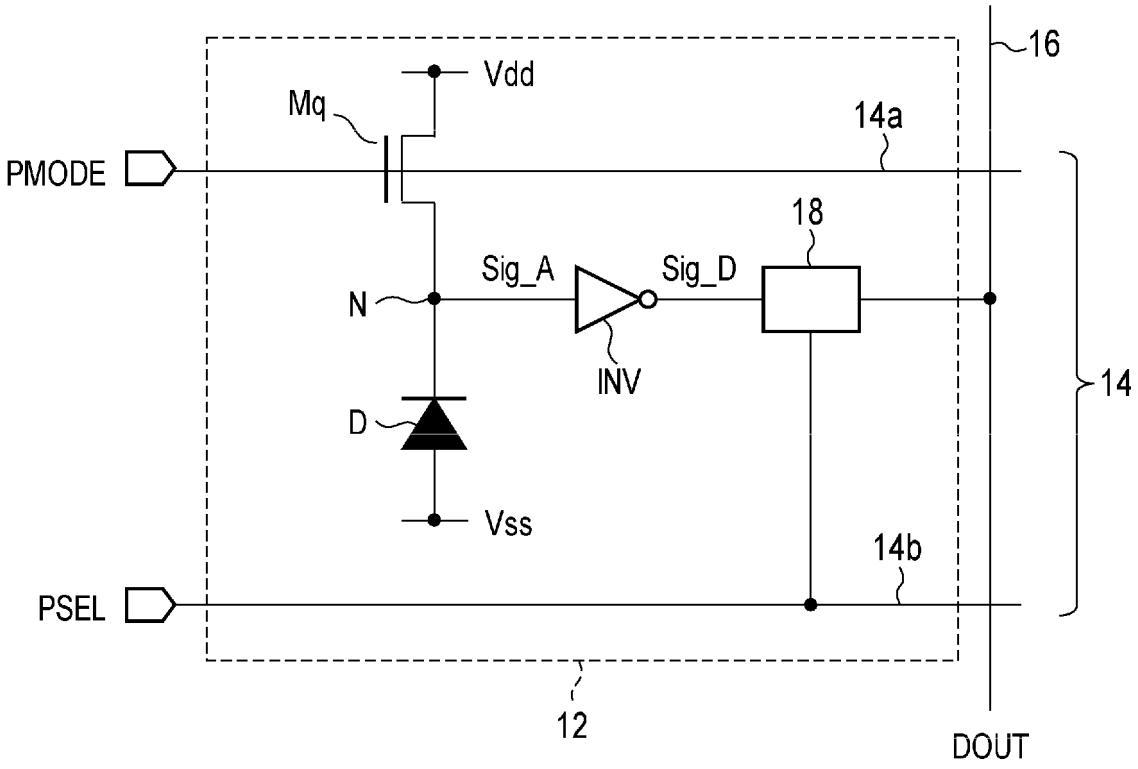


FIG. 3

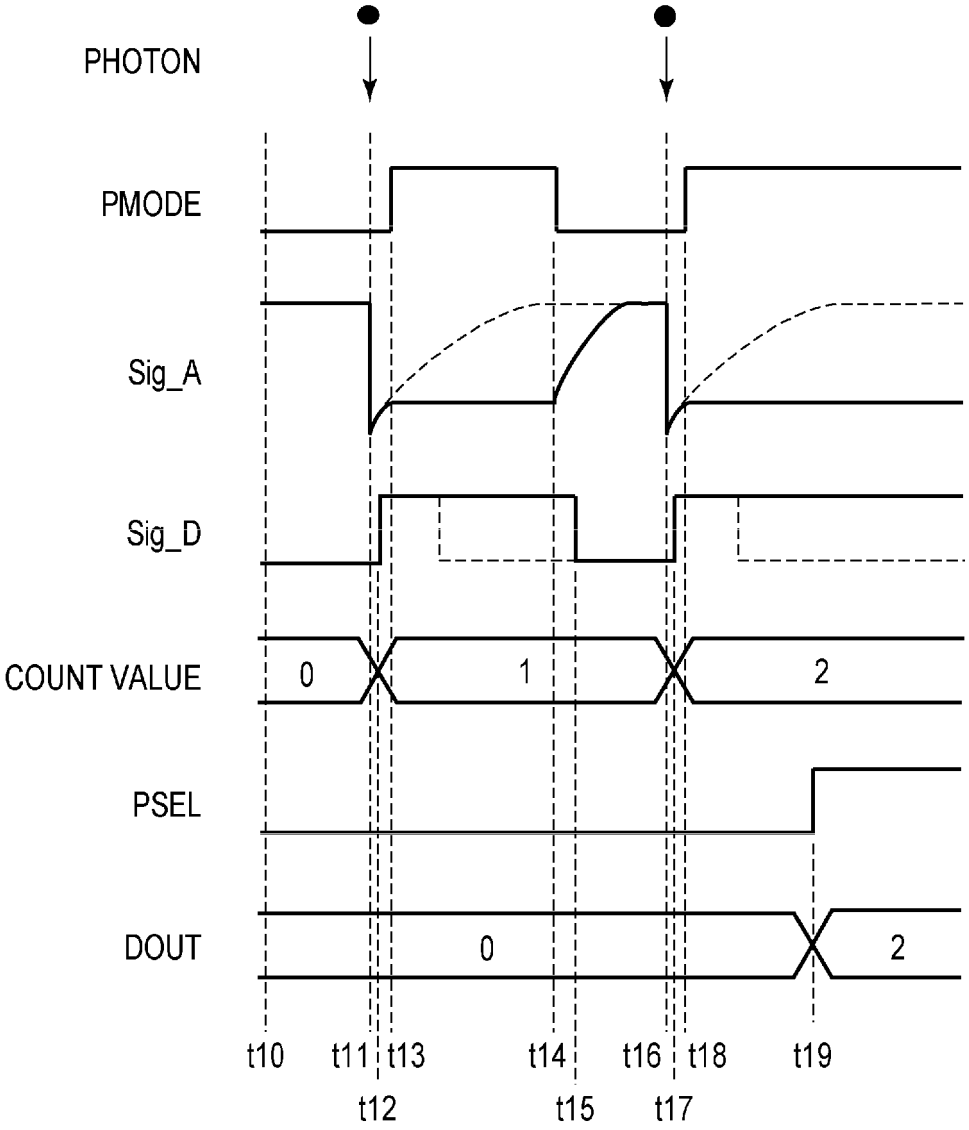

PHOTON
PMODE
Sig_A
Sig_D
COUNT VALUE
0
1
2
PSEL
DOUT
0
2
t10
t11
t12
t13
t14
t15
t16
t17
t18
t19

FIG. 4

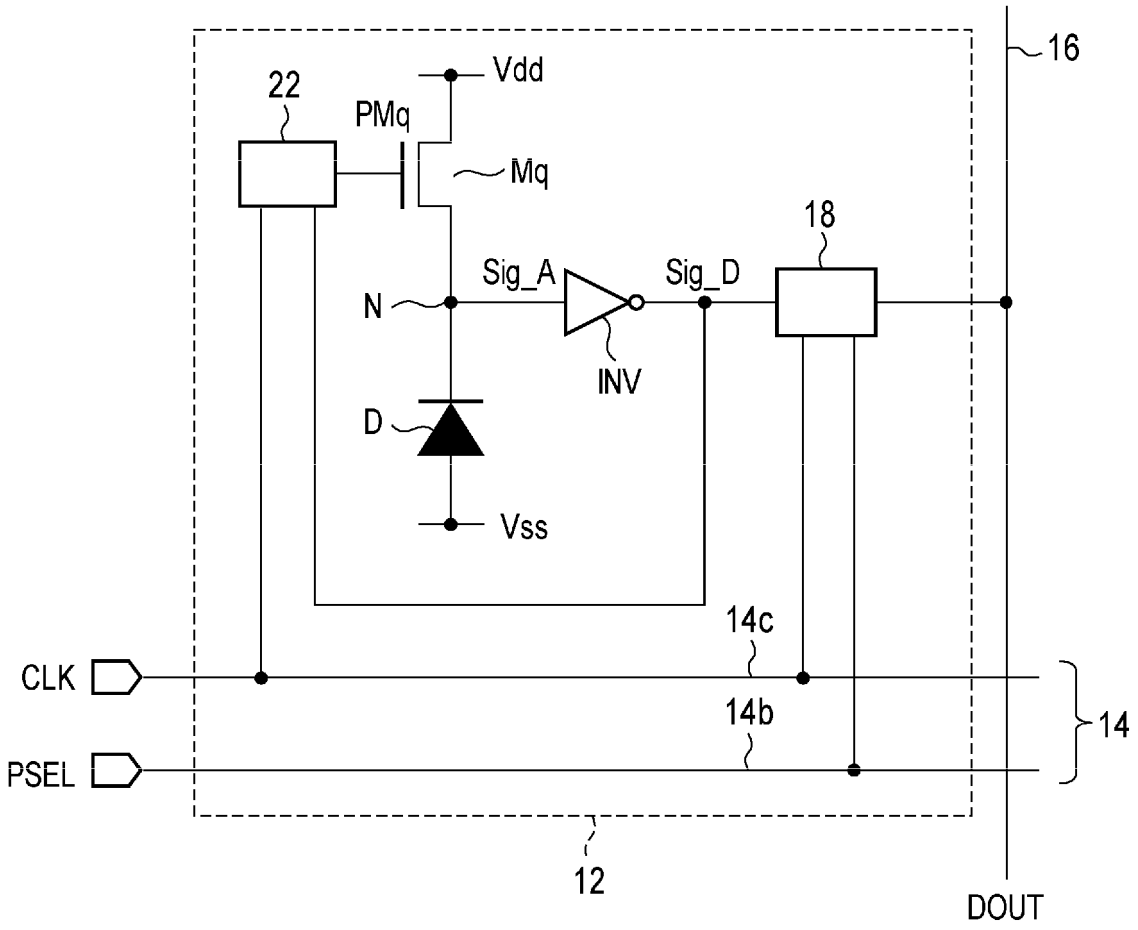

16
22
Vdd
PMq
Mq
18
Sig_A
Sig_D
N
INV
D
Vss
14c
CLK
14b
14
PSEL
12
DOUT

FIG. 5

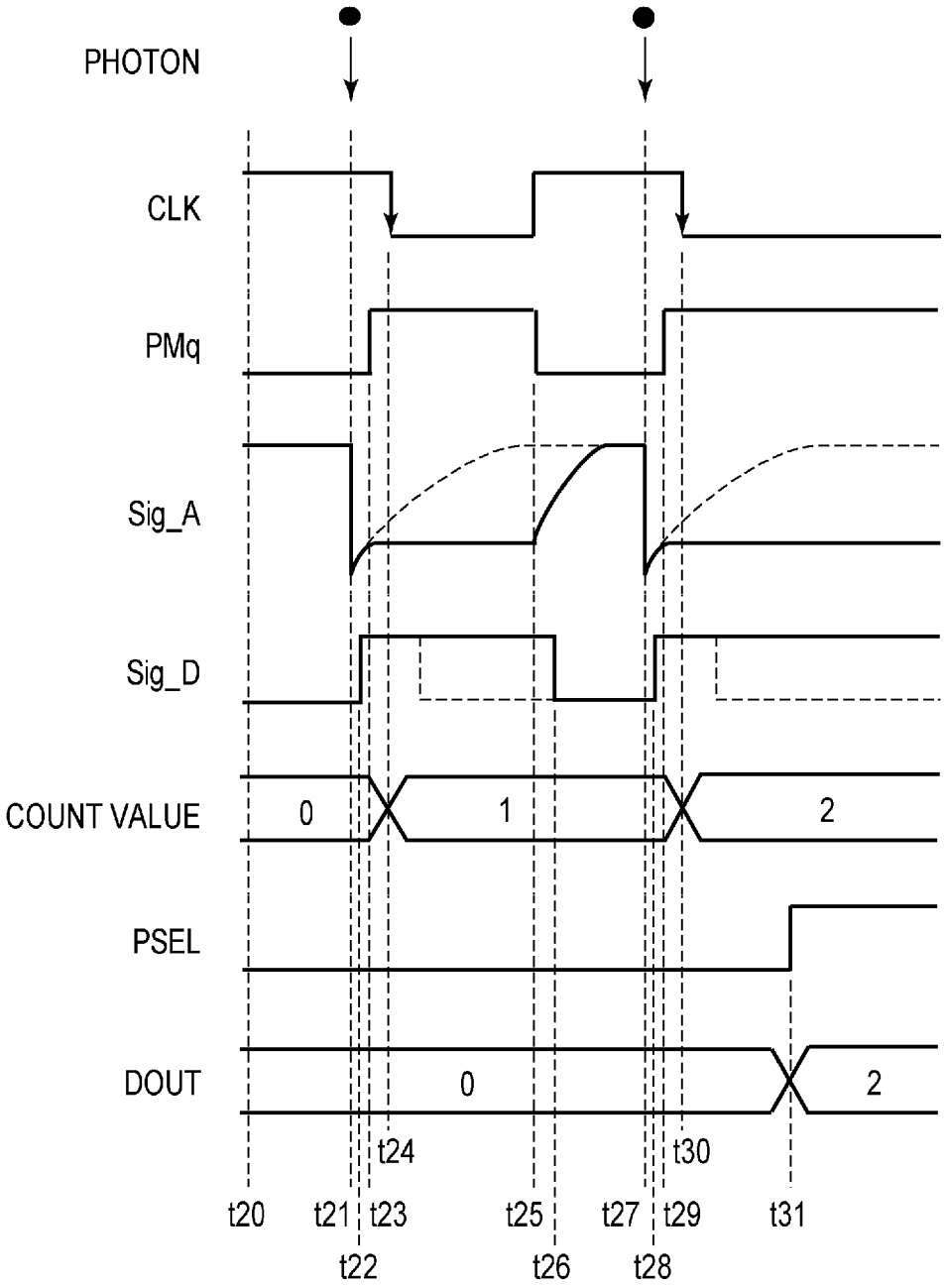

PHOTON
CLK
PMq
Sig_A
Sig_D
COUNT VALUE
0
1
2
PSEL
DOUT
0
2
t20
t21
t22
t23
t24
t25
t26
t27
t28
t29
t30
t31

FIG. 6

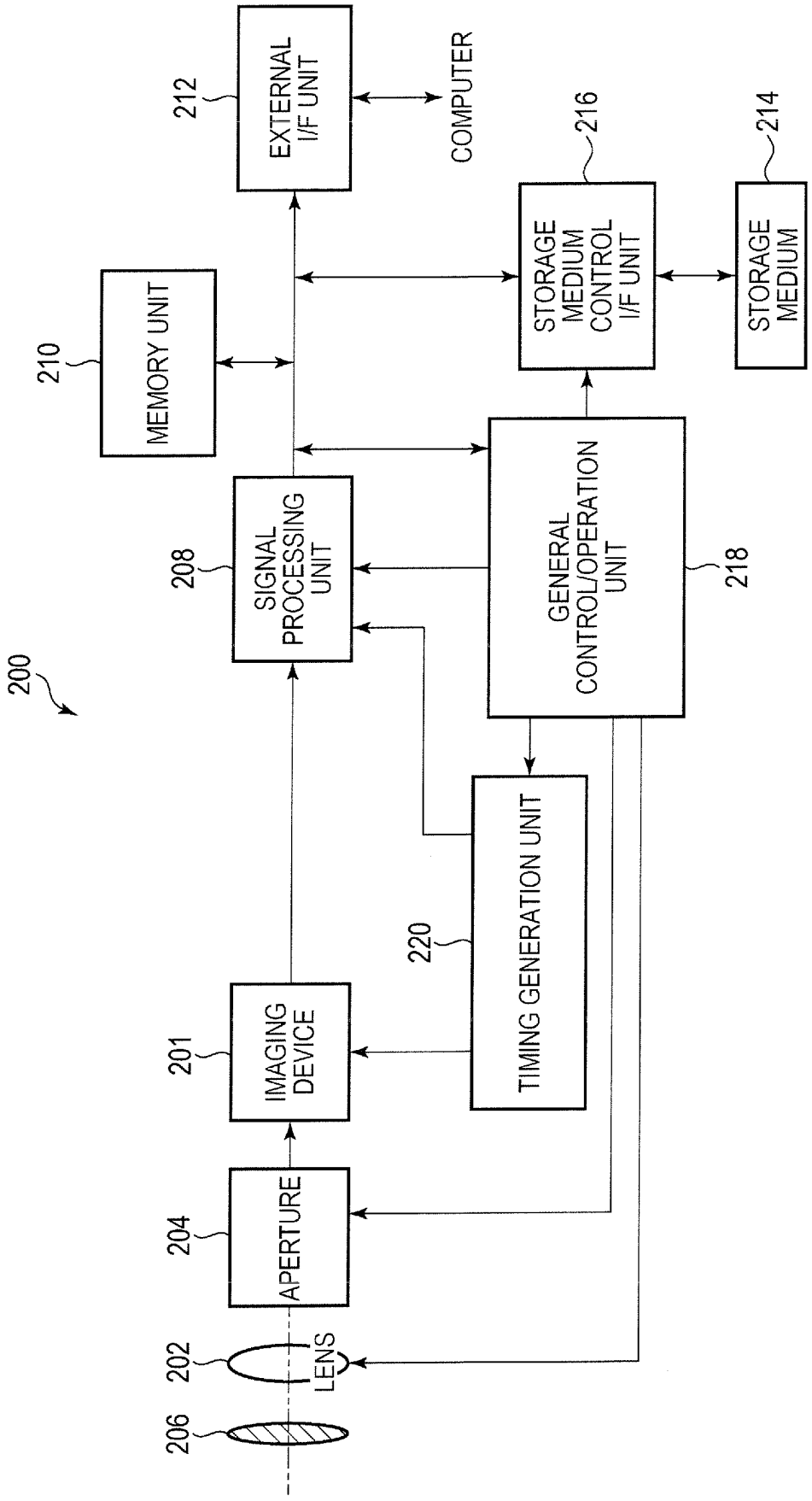
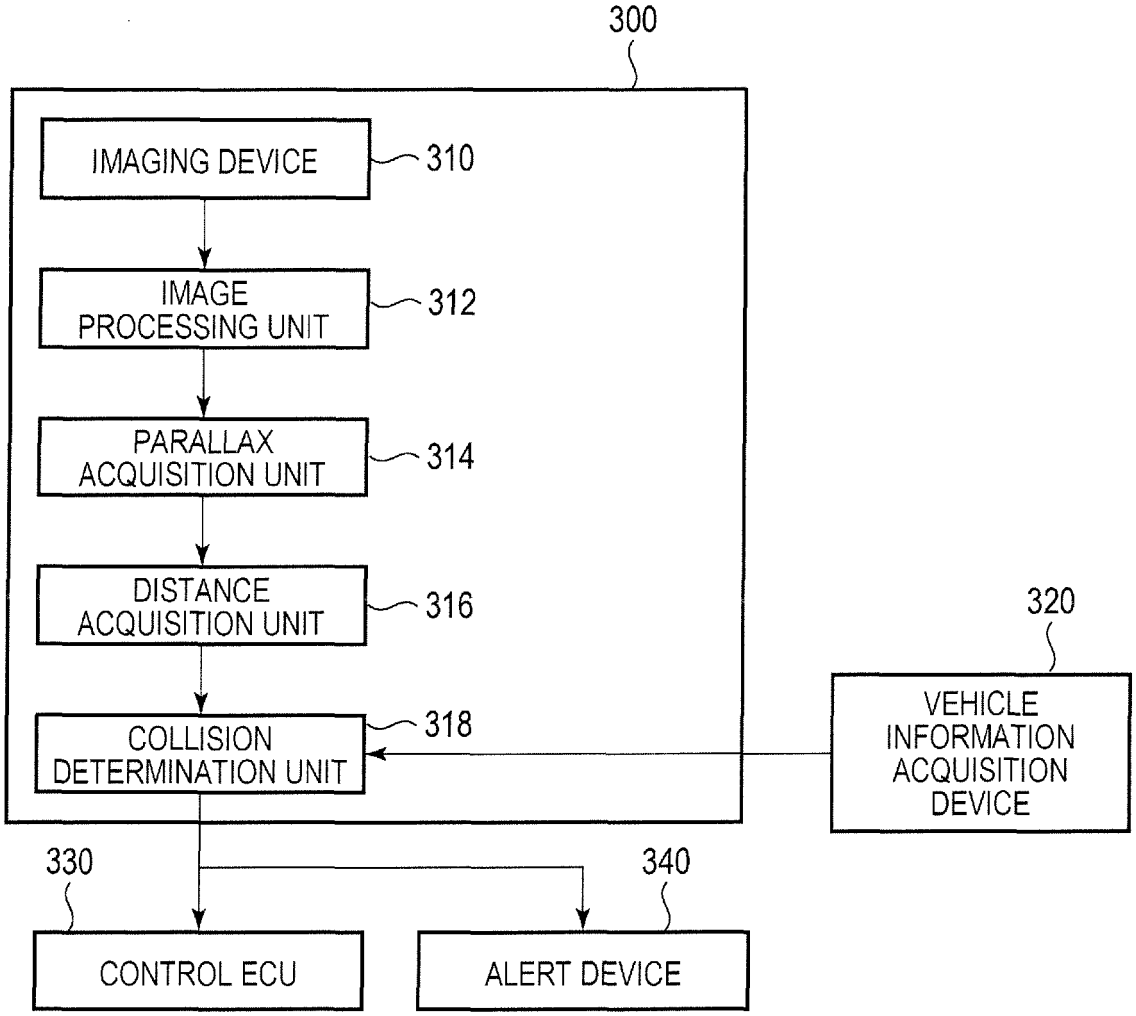

200
206
LENS
202
APERTURE
204
IMAGING DEVICE
201
TIMING GENERATION UNIT
220
SIGNAL PROCESSING UNIT
208
GENERAL CONTROL/OPERATION UNIT
218
MEMORY UNIT
210
EXTERNAL I/F UNIT
212
COMPUTER
STORAGE MEDIUM CONTROL I/F UNIT
216
STORAGE MEDIUM
214

FIG. 7A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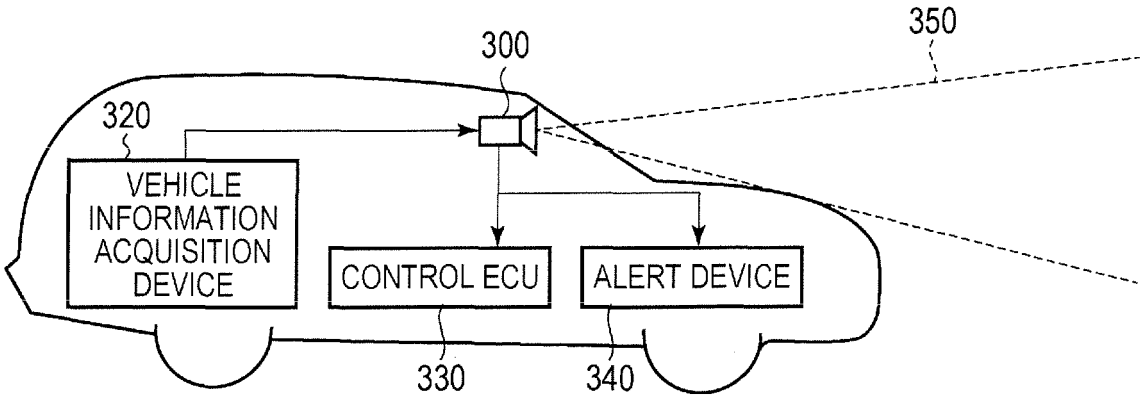
IMAGING DEVICE
310
IMAGE PROCESSING UNIT
312
PARALLAX ACQUISITION UNIT
314
DISTANCE ACQUISITION UNIT
316
COLLISION DETERMINATION UNIT
318
320
VEHICLE INFORMATION ACQUISITION DEVICE
330
340
CONTROL ECU
ALERT DEVICE

FIG. 7B


350
300
320
VEHICLE INFORMATION ACQUISITION DEVICE
CONTROL ECU
ALERT DEVICE
330
340

REFERENCES CITED IN THE DESCRIPTION

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