



(11) **EP 4 391 018 A1**

(12) **EUROPEAN PATENT APPLICATION**  
published in accordance with Art. 153(4) EPC

(43) Date of publication:  
**26.06.2024 Bulletin 2024/26**

(51) International Patent Classification (IPC):  
**H01L 21/02<sup>(2006.01)</sup>**

(21) Application number: **22858293.8**

(52) Cooperative Patent Classification (CPC):  
**H01L 21/02**

(22) Date of filing: **01.08.2022**

(86) International application number:  
**PCT/JP2022/029483**

(87) International publication number:  
**WO 2023/021972 (23.02.2023 Gazette 2023/08)**

(84) Designated Contracting States:  
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR**  
Designated Extension States:  
**BA ME**  
Designated Validation States:  
**KH MA MD TN**

(71) Applicant: **Shin-Etsu Handotai Co., Ltd.**  
**Tokyo 100-0004 (JP)**

(72) Inventor: **ISHIZAKI Junya**  
**Annaka-shi, Gunma 379-0196 (JP)**

(74) Representative: **Mooser, Sebastian Thomas**  
**Wuesthoff & Wuesthoff**  
**Patentanwälte und Rechtsanwalt PartG mbB**  
**Schweigerstraße 2**  
**81541 München (DE)**

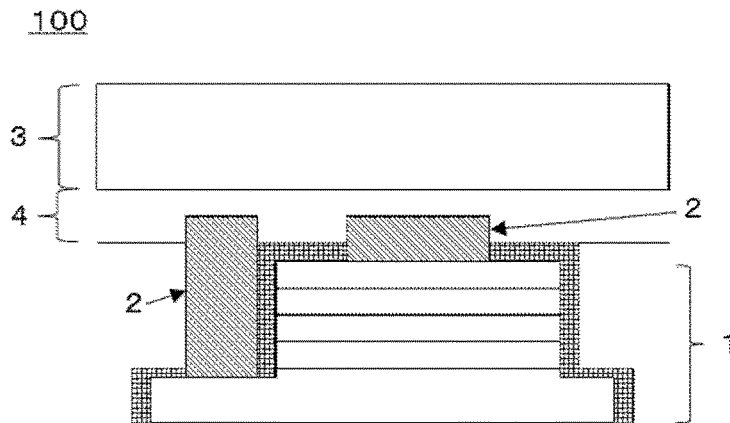
(30) Priority: **17.08.2021 JP 2021132721**

(54) **PROVISIONALLY BONDED WAFER AND METHOD FOR PRODUCING SAME**

(57) The present invention provides a temporarily bonded wafer in which an epitaxial functional layer having two or more electrodes with different polarities on one surface and a support substrate are temporarily bonded, in which the surface having the electrodes of the epitaxial functional layer and the support substrate are temporarily

bonded via an uncured thermosetting bonding material. This provides a technique to reduce bonding failure and delamination failure after removing the substrate after a bonding process, to improve the yield, and to easily remove the temporary support substrate.

[FIG. 1]



**EP 4 391 018 A1**

**Description**

## TECHNICAL FIELD

5 **[0001]** The present invention relates to a temporarily bonded wafer and a temporary bonding method for temporary bonding a semiconductor substrate to be mounted on a mounting substrate to a temporary support substrate for a temporary period.

## BACKGROUND ART

10 **[0002]** The technique to separate only an epitaxial functional layer, such as a light emitting element, from a starting substrate and transfer to another substrate is an important technique to mitigate a limitation due to a physical property of the starting substrate and improve a degree of design freedom for a device system. To realize the transfer, a technique is required to realize removing the starting substrate after bonding the epitaxial functional layer to a temporary support substrate and then transferring to a permanent substrate.

15 **[0003]** Patent Document 1 discloses a technique to perform thermo-compression bonding to a semiconductor epitaxial substrate and a temporary support substrate via a dielectric layer and a technique to separate the temporary support substrate and the epitaxial functional layer by wet etching. Patent Document 2 discloses a technique to insert a transparent conductive layer between an adhesive layer and a functional layer as one form of bonding, although not directly related to an improvement of bonding.

20 **[0004]** Patent Document 3 discloses a technique in which polyimide is used for temporary bonding; after a removal of a starting substrate, an electrode is formed on the surface where the substrate is removed.

## CITATION LIST

25

## PATENT LITERATURE

**[0005]**

30 Patent Document 1: JP 2021-27301 A  
 Patent Document 2: JP 4159421 B2  
 Patent Document 3: JP 2008-187160 A

## SUMMARY OF INVENTION

35

## TECHNICAL PROBLEM

40 **[0006]** However, in Patent Document 3, an electrode is formed after temporary bonding and removal of a starting substrate, thus causing a problem of delaminating due to heat treatment in forming ohmic contact. In particular, when a material system with a large lattice mismatch or materials with large differences in thermal expansion coefficient are combined to form a heterostructure, the delamination rate tends to be large due to the bimetallic effect during the heat treatment.

45 **[0007]** To lower the temperature for ohmic contact formation, it is required to dope a dopant impurity with a concentration close to the solid solubility limit. However, a doped crystal layer having a concentration close to the solid solubility limit tends to have a lower quality of a crystal when compared to a relatively low doped crystal layer. A high-doped layer is needed to be provided between the starting substrate and a functional layer. Since the functional layer is provided above a high-doped layer, the functional layer is affected by the quality of the high-doped layer. In other words, a high-doped layer with low quality provided under the functional layer decreases the quality of the functional layer.

50 **[0008]** Moreover, to avoid an effect of thermal deformation due to bimetal, there is an idea to select a material system with a small difference in a coefficient of thermal expansion. However, it is impossible to select a material with a small difference in coefficient of thermal expansion while maintaining the function of the functional layer. Thus, only a selectable technical option is to reduce the difference in coefficient of thermal expansion; in other words, to thin the film thickness of each layer. Although designing a thin film thickness is technically possible, such thinning the thickness is highly likely unable to sufficiently control a carrier behavior in the functional layer due to a thinned film thickness; thus, the design function of the functional layer is degraded.

55 **[0009]** Based on a background described above, when an electrode is formed, and ohmic contact is formed after the temporary bonding of a support substrate, suppressing delamination due to a bimetallic effect is extremely difficult.

**[0010]** The present invention has been made in view of the above-described problem. An object of the present invention

is to provide a technique for a temporarily bonded wafer in which the bonding failure and delamination failure after the removal of the starting substrate after a bonding process are reduced, the yield is improved, and the temporary support substrate can be easily removed.

5 SOLUTION TO PROBLEM

**[0011]** To achieve the object, the present invention provides a temporarily bonded wafer in which an epitaxial functional layer having two or more electrodes with different polarities on one surface and a support substrate are temporarily bonded, wherein the surface having the electrodes of the epitaxial functional layer and the support substrate are temporarily bonded via an uncured thermosetting bonding material.

**[0012]** Such a temporarily bonded wafer in which the support substrate is temporarily bonded to the surface where the electrodes are formed with a thermosetting bonding material in an uncured state has no bonding or delamination failure in the temporarily bonded area, and the temporary support substrate can be easily removed because the bonding material is bonded in an uncured state.

**[0013]** In addition, the epitaxial functional layer is preferably a light emitting element.

**[0014]** The inventive temporarily bonded wafer can be used for this purpose.

**[0015]** Moreover, the epitaxial functional layer preferably contains an AlGaInP-based or InGaN-based material.

**[0016]** In particular, the present invention can be suitably used for the epitaxial functional layer containing these materials.

**[0017]** Furthermore, the thermosetting bonding material is preferably any of benzocyclobutene (BCB) resin, polyimide (PI) resin, fluoro-resin, and epoxy resin.

**[0018]** Such a thermosetting bonding material can not only temporarily bond in a softened state but also delaminate easily.

**[0019]** In addition, the support substrate is preferably comprised of any of the materials: silicon, sapphire, GaP, GaAs, InP, SiC, quartz, glass, LiTaO<sub>3</sub>, and LiNbO<sub>3</sub>.

**[0020]** In the present invention, for example, such a support substrate can be used.

**[0021]** Moreover, the inventive temporarily bonded wafer can have no starting substrate on a surface of the epitaxial functional layer opposite to the surface having the electrodes.

**[0022]** In this way, the inventive temporarily bonded wafer can be a wafer on which the starting substrate is removed.

**[0023]** Furthermore, the present invention provides a method for manufacturing a temporarily bonded wafer, the method being a method for temporarily bonding of an epitaxial substrate in which an epitaxial functional layer is grown on the starting substrate to a support substrate, the method comprising:

(1) forming two or more electrodes with different polarities on one surface of the epitaxial functional layer of the epitaxial substrate; and

(2) temporarily bonding the support substrate to the surface on which the electrodes are formed via an uncured thermosetting bonding material.

**[0024]** By manufacturing the temporarily bonded wafer in this way, temporary bonding is performed after forming electrodes, thus not subjected to a thermal restriction accompanied with electrode formation. Consequently, a bonding failure and a delamination failure between the epitaxial functional layer and the temporarily support substrate can be prevented. Thus, the yield can be improved. Moreover, temporary bonding with the temporary support substrate is performed where the bonding material is in an uncured state; thus, the temporary support substrate can be removed with ease.

**[0025]** In addition, the epitaxial functional layer is preferably a light emitting element.

**[0026]** The present invention can be used for manufacturing the temporarily bonded wafer having such a purpose.

**[0027]** Moreover, the epitaxial functional layer preferably contains an AlGaInP-based or InGaN-based material.

**[0028]** In particular, the present invention can be suitably used for the epitaxial functional layer containing such material.

**[0029]** Furthermore, the thermosetting bonding material is preferably any of benzocyclobutene (BCB) resin, polyimide (PI) resin, fluoro-resin, and epoxy resin.

**[0030]** Such a thermosetting bonding material is not only temporarily bondable in the softened state but also easy to delaminate.

**[0031]** In addition, the support substrate is preferably comprised of any of the materials: silicon, sapphire, GaP, GaAs, InP, SiC, quartz, glass, LiTaO<sub>3</sub>, and LiNbO<sub>3</sub>.

**[0032]** The present invention, for example, can use such a support substrate.

**[0033]** Moreover, the inventive method for manufacturing a temporarily bonded wafer may comprise after (2), (3) removing the starting substrate from the epitaxial substrate.

**[0034]** In this way, the temporarily bonded wafer without the starting substrate can be manufactured.

## ADVANTAGEOUS EFFECTS OF INVENTION

**[0035]** As described above, the present invention can provide a technique for a temporarily bonded wafer in which the bonding failure and delamination failure after the removal of the starting substrate after a bonding process are reduced, the yield is improved, and the temporary support substrate can be easily removed.

## BRIEF DESCRIPTION OF DRAWINGS

**[0036]**

FIG. 1 is a view illustrating an example of a schematic view of a temporarily bonded wafer according to the present invention.

FIG. 2 is a view illustrating a schematic view in which an epitaxial substrate is manufactured by growing an epitaxial functional layer on a GaAs starting substrate in the first embodiment of a method for manufacturing a temporarily bonded wafer according to the present invention.

FIG. 3 is a view illustrating a schematic view in which a first electrode is formed on a GaP window layer in the first embodiment.

FIG. 4 is a view illustrating a schematic view in which an AlGaInP first cladding layer is exposed by dry etching in the first embodiment.

FIG. 5 is a view illustrating a schematic view in which a second electrode is formed on an AlGaInP first cladding layer in the first embodiment.

FIG. 6 is a view illustrating a schematic view in which the surface of an epitaxial functional layer, where an electrode is formed, is temporarily bonded to a support substrate via BCB resin, thereby manufacturing a temporarily bonded wafer in the first embodiment.

FIG. 7 is a view illustrating a schematic view in which a GaAs starting substrate is removed from a manufactured temporarily bonded wafer in the first embodiment.

FIG. 8 is a view illustrating a schematic view in which a temporarily bonded wafer having a GaAs starting substrate removed adheres to a silicon wafer via silicone; then, the support substrate is delaminated in the first embodiment.

FIG. 9 is a view illustrating a schematic view in which an epitaxial functional layer is grown on a sapphire starting substrate to manufacture an epitaxial substrate in the second embodiment of a method for manufacturing a temporarily bonded wafer according to the present invention.

FIG. 10 is a view illustrating a schematic view in which a first electrode is formed on a GaN contact layer in the second embodiment.

FIG. 11 is a view illustrating a schematic view in which a GaN first cladding layer is exposed by dry etching in the second embodiment.

FIG. 12 is a view illustrating a schematic view in which a second electrode is formed on a GaN first cladding layer in the second embodiment.

FIG. 13 is a view illustrating a schematic view in which the surface of an epitaxial functional layer, where an electrode is formed, is temporarily bonded to a support substrate via BCB resin, thereby manufacturing a temporarily bonded wafer in the second embodiment.

FIG. 14 is a view illustrating a schematic view in which a sapphire starting substrate is removed from a manufactured temporarily bonded wafer in the second embodiment.

FIG. 15 is a view illustrating a schematic view in which a temporarily bonded wafer having a sapphire starting substrate removed adheres to a silicon wafer via silicone; then, a support substrate is delaminated in the second embodiment.

## DESCRIPTION OF EMBODIMENTS

**[0037]** As described above, temporary bonding of a support substrate and then forming an electrode cause a problem of delamination due to heat treatment for the formation of ohmic contact. In particular, when a heterostructure is formed by combining a material system with a large lattice mismatch and a material with a large difference in coefficient of thermal expansion, the delamination rate tends to be enlarged due to a bimetallic effect at heat treatment.

**[0038]** To solve the above problem, the present inventors have earnestly studied and found out that by temporarily bonding the surface of an epitaxial functional layer having two or more electrodes of different polarities to a support substrate with a thermosetting bonding material in an uncured state, a temporarily bonded area has no delamination due to heat treatment during electrode formation, and since the thermosetting bonding material is bonded in an uncured state, the temporarily bonded support substrate can be removed very easily. Based on this finding, the present invention has been completed.

**[0039]** That is, the present invention is a temporarily bonded wafer in which the epitaxial functional layer having two or more electrodes with different polarities on one surface and a support substrate are temporarily bonded, wherein the surface having the electrodes of the epitaxial functional layer and the support substrate are temporarily bonded via an uncured thermosetting bonding material.

**[0040]** Hereinafter, the present invention will be described in detail. However, the present invention is not limited thereto.

[Temporarily bonded wafer]

**[0041]** FIG. 1 shows an example of the inventive temporarily bonded wafer. In the inventive temporarily bonded wafer 100, an epitaxial functional layer 1 has two electrodes 2 with different polarities on one surface, and the surface having electrodes 2 of the epitaxial functional layer 1 and a support substrate 3 are temporarily bonded via an uncured thermosetting bonding material 4.

**[0042]** A conventional temporarily bonded wafer has a structure in which an electrode is formed on one surface of an epitaxial functional layer, and the other surface (the opposite surface to the electrode formation surface) is temporarily bonded to a support substrate. This is because in the conventional method for manufacturing the temporarily bonded wafer, firstly, the epitaxial layer of an epitaxial substrate, in which the epitaxial functional layer is formed on the starting substrate, is temporarily bonded to a support substrate, then, the starting substrate is removed, and the electrode is formed on the surface where the starting substrate is removed. In contrast, the inventive temporarily bonded wafer, unlike the conventional temporarily bonded wafer, has a structure in which the electrodes are placed between the epitaxial functional layer and the support substrate. The reason for this structure is that the wafer is manufactured by temporary bonding after the formation of the electrodes, according to the inventive method for manufacturing the temporarily bonded wafer, as described later.

[Method for manufacturing temporarily bonded wafer]

**[0043]** Thus, the present invention provides a method for manufacturing a temporarily bonded wafer, the method being a method for temporarily bonding an epitaxial substrate in which an epitaxial functional layer is grown on a starting substrate to a support substrate, the method comprising:

- (1) forming two or more electrodes with different polarities on one surface of the epitaxial functional layer of the epitaxial substrate; and
- (2) temporarily bonding the support substrate to the surface on which the electrodes are formed via an uncured thermosetting bonding material.

**[0044]** Such a method for manufacturing the temporarily bonded wafer, unlike the conventional method in which heat treatment is performed to form an ohmic contact of electrodes (Ohmic heat treatment) to the wafer having a temporarily bonded portion, performs the electrode formation and ohmic heat treatment to the wafer before the formation of the temporarily bonded portion, then performs temporarily bonding with the support substrate. Consequently, heat treatment at a high temperature to form the electrodes does not cause delamination or thermal deformation at the temporarily bonded portion. Thus, the temporarily bonded wafer can be manufactured with an excellent yield. Furthermore, in the inventive method for manufacturing the temporarily bonded wafer, temporary bonding is performed via an uncured thermosetting bonding material. Thus, the support substrate is easily removed.

**[0045]** Hereinafter, the embodiments of the present invention will be described in detail with reference to drawings. However, the present invention is not limited thereto.

(First embodiment)

**[0046]** With reference to FIG. 2 to FIG. 8, a first embodiment of the inventive method for manufacturing a temporarily bonded wafer is described. In the first embodiment, the epitaxial functional layer contains an AlGaInP-based material.

**[0047]** Firstly, as illustrated in FIG. 2, a GaAs buffer layer 102 of the first conductivity type is laminated on a GaAs starting substrate 101 of the first conductivity type, then the following layers are grown sequentially on the substrate: a  $\text{Ga}_y\text{In}_{1-y}\text{P}$  ( $0.4 \leq y \leq 0.6$ ) first etching stop layer 103 of the first conductivity type having a thickness of e.g., 0.3  $\mu\text{m}$ ; a GaAs second etching stop layer 104 of the first conductivity type having a thickness of e.g., 0.3  $\mu\text{m}$ ; a  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 < x \leq 1, 0.4 \leq y \leq 0.6$ ) first cladding layer 105 of the first conductivity type having a thickness of e.g., 1.0  $\mu\text{m}$ ; a non-doped  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 \leq x \leq 0.6, 0.4 \leq y \leq 0.6$ ) active layer 106; a  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 < x \leq 1, 0.4 \leq y \leq 0.6$ ) second cladding layer 107 of the second conductivity type having a thickness of e.g., 1.0  $\mu\text{m}$ ; a  $\text{Ga}_y\text{In}_{1-y}\text{P}$  ( $0.45 \leq y \leq 1$ ) intermediate layer 108 of the second conductivity type having a thickness of e.g., 0.1  $\mu\text{m}$ ; a GaP window layer 109 of the second conductivity type having a thickness of e.g., 4  $\mu\text{m}$ ; thus an epitaxial substrate having a light emitting element structure, which is a sequentially

grown epitaxial functional layer, is provided. At this point, the AlGaInP first cladding layer 105 to the AlGaInP second cladding layer 107 are referred to as a double-hetero (DH) structure portion 111 (FIG. 3).

**[0048]** Then, as shown in FIG. 3, in a part of a region in the GaP window layer 109 of the second conductivity type, a first electrode 110 is formed. The use of highly reflective metal is suitable for the first electrode 110, and the electrode can be an Au-based electrode. For example, AuBe alloy can be used as the metal in contact with the GaP window layer 109, and Au can be laminated on the alloy. Thus, the first electrode 110 is formed.

**[0049]** The metal in contact with the GaP window layer 109 of the second conductivity type is not limited to AuBe alloys, but any metal or alloy can be selected as long as ohmic contact can be formed. In general, other than AuBe, an alloy such as AuZn is often selected.

**[0050]** Then, as shown in FIG. 4, after the formation of the first electrode 110, a part of a region other than the first electrode 110 formation region on the GaP window layer 109 of the second conductivity type is coated with a mask using a material having etching selectivity such as SiO<sub>2</sub> or SiN<sub>x</sub>, and the exposed portion is notched by a method such as dry etching, and then the AlGaInP first cladding layer 105 of the first conductivity type is exposed.

**[0051]** Then, as shown in FIG. 5, the GaP window layer 109 of the second conductivity type, the side surface of the notched portion, and the AlGaInP first cladding layer 105 of the first conductivity type are coated with SiO<sub>2</sub> or SiN<sub>x</sub> as a PSV (passivation) film 113, then, the first electrode 110 portion and a part of the AlGaInP first cladding layer 105 of the first conductivity type are exposed by a photolithography method. Then, the second electrode 112 is formed on the exposed portion on the AlGaInP first cladding layer 105 of the first conductivity type.

**[0052]** The use of a highly reflective metal is suitable for the second electrode 112, and the electrode can be an Au-based electrode. For example, an AuSi alloy can be used as the metal to come in contact with the AlGaInP first cladding layer 105 of the first conductivity type, and Au can be laminated on the metal. Thus, the second electrode 112 is formed.

**[0053]** Furthermore, the metal in contact with the AlGaInP cladding layer 105 of the first conductivity type is not limited to AuSi alloys, but any metal or alloy can be selected as long as ohmic contact can be formed. In general, other than AuSi, alloys such as AuGe are often selected.

**[0054]** In addition, the PSV film 113 is not necessarily formed before the formation of the second electrode 112, and the PSV film 113 may be formed after the formation of the second electrode 112. Furthermore, the same effect can be obtained without the formation of the PSV film 113.

**[0055]** After the formation of the first and second electrodes 110 and 112, to obtain ohmic contact, for example, RTA heat treatment is performed at 400°C for 5 minutes. Although the case of RTA treatment is shown here as an example, the treatment is not limited to this RTA treatment, but may also be performed at relatively low temperatures, e.g., approximately 350°C for 30 minutes.

**[0056]** Then, as shown in FIG. 6, after the formation of ohmic contact, the electrode formation side is spin-coated with a BCB resin 114, then faced each other with the support substrate 115 selected from such as silicon, and then pressurized in a vacuum atmosphere and retained at 150°C for 15 minutes, and then temporarily bonded to the support substrate 115. Since the BCB resin 114 is cured by retaining the temperature condition above 150°C, the BCB resin 114 is prevented from being cured by retaining the temperature at 150°C or less. The uncured BCB resin 114 can improve the delamination property of the support substrate 115 from the epitaxial substrate.

**[0057]** In addition, the thermosetting bonding material is not limited to benzocyclobutene (BCB) resin; for example, the material can be polyimide (PI) resin, fluororesin, and epoxy resin.

**[0058]** Moreover, the support substrate 115 is not limited to silicon, but any material with excellent surface flatness can be selected, such as sapphire, GaP, GaAs, InP, quartz, glass, LiTaO<sub>3</sub>, LiNbO<sub>3</sub>, rock crystal, and SiC.

**[0059]** Then, as shown in FIG. 7, after the temporarily bonding to the support substrate 115, the starting substrate is removed by a selective etching method. The GaAs starting substrate 101 is removed by ammonia hydrogen peroxide water. The GaInP first etching stop layer 103 is removed by diluted hydrochloric acid or hydrochloric acid-based etchant, and lastly, the GaAs second etching stop layer 104 is removed by sulfuric acid-hydrogen peroxide mixture, and then the AlGaInP first cladding layer 105 of the first conductivity type is exposed. Consequently, the temporarily bonded wafer can be manufactured.

**[0060]** Lastly, as shown in FIG. 8, after exposing the AlGaInP first cladding layer 105 of the first conductivity type on the temporarily bonded wafer, this layer is adhered to a silicon wafer 117 coated with silicone 116, then BCB resin 114 in a softened state is dissolved by BCB solvent, thus delaminating the support substrate 115 and then individually divided chips are produced.

(Second embodiment)

**[0061]** Using FIG. 9 to FIG. 15, a second embodiment of the inventive method for manufacturing a temporarily bonded wafer is described. In the second embodiment, the epitaxial functional layer includes InGaN-based material.

**[0062]** Firstly, as shown in FIG. 9, a GaN buffer layer 202 of the first conductivity type is laminated on a sapphire starting substrate 201, and then the following layers are grown sequentially on the substrate: a GaN first cladding layer

203 of the first conductivity type having a thickness, e.g., 1.0  $\mu\text{m}$ ; non-doped  $\text{In}_z\text{Ga}_{1-z}\text{N}$  ( $0 < z \leq 0.4$ ) active layer 204; an  $\text{Al}_v\text{Ga}_{1-v}\text{N}$  ( $0 \leq v \leq 0.4$ ) (GaN) second cladding layer 205 of the second conductivity type having a thickness of e.g., 1.0  $\mu\text{m}$ ; a GaN contact layer 206 of the second conductivity type having a thickness of e.g., 0.1  $\mu\text{m}$ ; thus an epitaxial substrate having a light emitting element structure, which is a sequentially grown epitaxial functional layer, is provided. At this point, the GaN first cladding layer 203 to the AlGaIn second cladding layer 205 are referred to as a double-hetero (DH) structure 208 (FIG. 10).

**[0063]** Then, as shown in FIG. 10, in a part of a region in the GaN contact layer 206 of the second conductivity type, a first electrode 207 is formed. The use of a highly reflective metal for the first electrode 207 is suitable, and the electrode can be an Ag-based electrode. Ag can be used as the metal in contact with the GaN contact layer 206, and Pd can be laminated on the metal. Thus, the first electrode 207 is formed.

**[0064]** Moreover, the metal in contact with the GaN contact layer 206 of the second conductivity type is not limited to an Ag-based metal, but any metal or alloy can be selected as long as ohmic contact can be formed. Generally, metals other than Ag, such as Au, and Ti, are often selected.

**[0065]** Then, as shown in FIG. 11, after the formation of the first electrode 207, a part of a region other than the first electrode 207 formation region on the GaN contact layer 206 of the second conductivity type is coated with a mask using a material having etching selectivity such as  $\text{SiO}_2$  or  $\text{SiNx}$ , and the exposed portion is notched by a method such as dry etching. Then, the GaN first cladding layer 203 of the first conductivity type is exposed.

**[0066]** Then, as shown in FIG. 12, the GaN contact layer 206, the side surface of the notched portion, the GaN first cladding layer 203 are coated with  $\text{SiO}_2$  or  $\text{SiNx}$  as a PSV film 210, then, the first electrode 207 portion and a part of the GaN first cladding layer 203 are exposed by a photolithography method. Then, the second electrode 209 is formed on the exposed portion of the GaN first cladding layer 203.

**[0067]** Moreover, the use of a highly reflective metal is suitable for the second electrode 209, and the electrode can be an Al-based electrode. For example, an Al metal can be used as the metal to come in contact with the GaN first cladding layer 203 of the first conductivity type, and Au can be laminated on the metal. Thus, the second electrode 209 is formed.

**[0068]** Furthermore, the metal in contact with the GaN first cladding layer 203 of the first conductivity type is not limited to Al metal, but any metal or alloy can be selected as long as ohmic contact can be formed. In general, other than Al, metals such as Ti or Au are often selected.

**[0069]** In addition, the PSV film 210 is not necessarily formed before the formation of the second electrode 209, and the PSV film 210 may be formed after the formation of the second electrode 209. Furthermore, the same effect can be obtained without the formation of the PSV film 210.

**[0070]** After the formation of the first and second electrodes 207 and 209, to obtain ohmic contact, for example, RTA heat treatment is performed at  $700^\circ\text{C}$  for 5 minutes.

**[0071]** Then, as shown in FIG. 13, after the formation of ohmic contact, the electrode formation side is spin-coated with BCB resin 211, faced each other with the support substrate 212 selected from such as silicon, and then pressurized in a vacuum atmosphere and retained approximately at  $150^\circ\text{C}$  for 15 minutes, and then temporarily bonded to the support substrate 212. Since the BCB resin 211 is cured by retaining the temperature condition above  $150^\circ\text{C}$ , the BCB resin 211 is prevented from being cured by retaining the temperature at  $150^\circ\text{C}$  or less. The uncured BCB resin 211 can improve the delamination property of the support substrate 212 from the epitaxial substrate.

**[0072]** In addition, the thermosetting bonding material is not limited to benzocyclobutene (BCB) resin; for example, the material can be polyimide (PI) resin, fluoro resin, and epoxy resin.

**[0073]** Moreover, the support substrate 212 is not limited to silicon, but any material with excellent surface flatness can be selected. Such as sapphire, GaP, GaAs, InP, quartz, glass,  $\text{LiTaO}_3$ ,  $\text{LiNbO}_3$ , rock crystal, and SiC can be selected.

**[0074]** Then, as shown in FIG. 14, after temporary bonding, the GaN buffer layer 202 is irradiated by a laser from the starting substrate side for ablation, thus, the sapphire starting substrate 201 is removed, and the GaN first cladding layer 203 of the first conductivity type is exposed. Consequently, the temporarily bonded wafer can be manufactured.

**[0075]** Lastly, as shown in FIG. 15, after the GaN first cladding layer 203 of the first conductivity type is exposed, this layer adheres with a silicon wafer 214 on which silicone 213 is coated, then BCB resin 211 in softened state is dissolved by BCB solvent, thus delaminating the support substrate 212, and then individually divided chips are produced.

## EXAMPLE

**[0076]** Hereinafter, the present invention will be specifically described with reference to Examples and Comparative Example. However, the present invention is not limited thereto.

(Example 1)

**[0077]** A GaAs buffer layer of the first conductivity type was laminated on a GaAs starting substrate of the first con-

ductivity type, and then the following layers were grown sequentially on the substrate: a  $\text{Ga}_y\text{In}_{1-y}\text{P}$  ( $0.4 \leq y \leq 0.6$ ) first etching stop layer of the first conductivity type having a thickness of 0.3  $\mu\text{m}$ ; a GaAs second etching stop layer of the first conductivity type having 0.3  $\mu\text{m}$ ; a  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 < x \leq 1, 0.4 \leq y \leq 0.6$ ) first cladding layer of the first conductivity type having a thickness of 1.0  $\mu\text{m}$ ; a non-doped  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 \leq x \leq 0.6, 0.4 \leq y \leq 0.6$ ) active layer; a  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 < x \leq 1, 0.4 \leq y \leq 0.6$ ) second cladding layer of the second conductivity type having a thickness of 1.0  $\mu\text{m}$ ; a  $\text{Ga}_y\text{In}_{1-y}\text{P}$  ( $0.45 \leq y \leq 1$ ) intermediate layer of the second conductivity type having a thickness of 0.1  $\mu\text{m}$ ; and a GaP window layer of the second conductivity type having a thickness of 4  $\mu\text{m}$ ; thus an epitaxial substrate having a light emitting element structure, which was a sequentially grown epitaxial functional layer, was provided (see FIG. 2).

[0078] Then, a first electrode was formed in a part of a region on the GaP window layer of the second conductivity type. The use of a highly reflective metal was suitable for the first electrode; thus, an Au-based electrode was used. In this technique, AuBe alloy was used for the metal in contact with the GaP window layer, and Au was laminated on the alloy. Thus, the first electrode was formed (see FIG. 3).

[0079] After the formation of the first electrode, a part of a region of the GaP window layer of the second conductivity type, other than the area where the first electrode was formed, was coated with  $\text{SiO}_2$ , and the exposed portion was notched by dry etching, thus, the AlGaInP first cladding layer of the first conductivity type was exposed (see FIG. 4).

[0080] The GaP window layer of the second conductivity type, the side surface of the notched portion, and the AlGaInP first cladding layer of the first conductivity type were coated with  $\text{SiO}_2$  as a PSV film, then the first electrode portion and a part of the AlGaInP first cladding layer of the first conductivity type were exposed by a photolithography method. Then, the second electrode was formed on the exposed portion of the AlGaInP first cladding layer of the first conductivity type. At this point, the second electrode was formed using AuSi alloy as the metal in contact with the AlGaInP first cladding layer of the first conductivity type and laminating Au on the alloy (see FIG. 5).

[0081] After the formation of the first and second electrodes, to obtain ohmic contact, RTA heat treatment was performed at 400°C for 5 minutes.

[0082] After the formation of ohmic contact, the electrode formation side was spin-coated with BCB resin, then faced each other with a support substrate made of silicon, and then pressurized in a vacuum atmosphere and retained approximately at 150°C for 15 minutes, and then temporarily bonded to the support substrate (see FIG. 6).

[0083] After the temporary bonding to the support substrate, the GaAs starting substrate was removed by ammonia hydrogen peroxide water, the GaInP first etching stop layer was removed by diluted hydrochloric acid or hydrochloric acid-based etchant, and lastly, the GaAs second etching stop layer was removed by sulfuric acid-hydrogen peroxide mixture. Thus, the AlGaInP first cladding layer of the first conductivity type was exposed (see FIG. 7)

[0084] After exposing the AlGaInP first cladding layer of the first conductivity type, the layer was adhered to a silicon wafer coated with silicone, then the BCB resin in a softened state was dissolved by BCB solvent, thus delaminating the support substrate, and then individually divided chips were produced (see FIG. 8).

(Example 2)

[0085] A GaN buffer layer of the first conductivity type was laminated on a sapphire starting substrate, and then the following layers were grown sequentially on the substrate: a GaN first cladding layer of the first conductivity type having a thickness of 1.0  $\mu\text{m}$ ; non-doped  $\text{In}_z\text{Ga}_{1-z}\text{N}$  ( $0 < z \leq 0.4$ ) active layer; an  $\text{Al}_v\text{Ga}_{1-v}\text{N}$  ( $0 \leq v \leq 0.4$ ) (GaN) second cladding layer of the second conductivity type having a thickness of 1.0  $\mu\text{m}$ ; a GaN contact layer of the second conductivity type having a thickness of 0.1  $\mu\text{m}$ ; thus, an epitaxial substrate having a light emitting element structure, which is a sequentially grown epitaxial functional layer, is provided (see FIG. 9).

[0086] Then, in a part of a region of the GaN contact layer of the second conductive type, using Ag as the metal in contact with the GaN contact layer and laminating Pd thereon, the first electrode was formed (see FIG. 10).

[0087] After the formation of the first electrode, a part of a region of the GaN contact layer of the second conductivity type, other than the area where the first electrode was formed, was coated with  $\text{SiO}_2$ , and the exposed portion was notched by dry etching, thus, the GaN first cladding layer of the first conductivity type was exposed (see FIG. 11).

[0088] The GaN contact layer, the side surface of the notched portion, and the GaN first cladding layer were coated with  $\text{SiO}_2$  as a PSV film, then the first electrode portion and a part of the GaN first cladding layer were exposed by a photolithography method. Then, the second electrode was formed on the exposed portion of the GaN first cladding layer by using an Al metal as the metal in contact with the GaN first cladding layer of the first conductivity type and laminating Au on the Al metal (see FIG. 12).

[0089] After the formation of the first and second electrodes, to obtain ohmic contact, RTA heat treatment was performed at 700°C for 5 minutes.

[0090] After the formation of ohmic contact, the electrode formation side was spin-coated with BCB resin, faced each other with the support substrate made of silicon, and then pressurized in a vacuum atmosphere and retained approximately at 150°C for 15 minutes, and then temporarily bonded to the support substrate (see FIG. 13).

[0091] After temporary bonding, the GaN buffer layer was irradiated by a laser from the starting substrate side for



ablation, thus, the starting substrate was removed, and the GaN first cladding layer of the first conductivity type was exposed (see FIG. 14).

**[0092]** After the GaN cladding layer of the first conductivity type was exposed, this layer adhered with a silicon wafer on which silicone was coated, then the BCB resin in a softened state was dissolved by BCB solvent, thus delaminating the support substrate and then individually divided chips were produced (see. FIG.15).

(Comparative Example)

**[0093]** After lamination of a GaAs buffer layer of the first conductivity type on a GaAs starting substrate of the first conductivity type, the following layers were grown sequentially: a  $\text{Ga}_y\text{In}_{1-y}\text{P}$  ( $0.4 \leq y \leq 0.6$ ) first etching stop layer of the first conductivity type having a thickness of 0.3  $\mu\text{m}$ ; a GaAs second etching stop layer of the first conductivity type having a thickness of 0.3  $\mu\text{m}$ ; a  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 < x \leq 1, 0.4 \leq y \leq 0.6$ ) first cladding layer of the first conductivity type having a thickness of 1.0  $\mu\text{m}$ ; a non-doped  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 \leq x \leq 0.6, 0.4 \leq y \leq 0.6$ ) active layer; a  $(\text{Al}_x\text{Ga}_{1-x})_y\text{In}_{1-y}\text{P}$  ( $0 < x \leq 1, 0.4 \leq y \leq 0.6$ ) second cladding layer of the second conductivity type having a thickness of 1.0  $\mu\text{m}$ ; a  $\text{Ga}_y\text{In}_{1-y}\text{P}$  ( $0.45 \leq y \leq 1$ ) intermediate layer of the second conductivity type having a thickness of 0.1  $\mu\text{m}$ ; a GaP window layer of the second conductivity type having a thickness of 4  $\mu\text{m}$ ; thus an epitaxial substrate having a light emitting element structure, which was a sequentially grown epitaxial functional layer, was provided.

**[0094]** The epitaxial substrate was spin-coated with 1.0  $\mu\text{m}$  of BCB resin, faced and superimposed with a sapphire wafer, and thermocompression-bonded. Thereby, an epitaxial bonded substrate in which the epitaxial substrate and the sapphire wafer was bonded with each other via BCB was manufactured. During the bonding, the curing process was performed by retaining at 250°C for 1 hour.

**[0095]** The GaAs substrate was removed by ammonia hydrogen peroxide water and the GaInP first etching stop layer was exposed. By switching the etchant to hydrochloric acid-based, the GaInP first etching stop layer was removed, and the GaAs second etching stop layer was exposed. By switching the etchant to sulfuric acid-hydrogen peroxide mixture-based, the GaAs second etching stop layer was removed, and the first cladding layer was exposed. By performing the processes above, the epitaxial bonded substrate having only a double-hetero layer and a window layer was manufactured.

**[0096]** After removing the starting substrate, AuBe-based was used as the metal in contact with the starting substrate-removal surface (first cladding layer), and Au was laminated on the top to form the first electrode.

**[0097]** After forming the first electrode, a part of a region of the first cladding layer, other than the area where the first electrode was formed, was notched by dry-etching, and the second cladding layer was exposed on the notched portion.

**[0098]** The AlGaInP first cladding layer, the side surface of the notched portion, and the AlGaInP second cladding layer were coated with a passivation (PSV) film; then, the first electrode portion and a part of the AlGaInP second cladding layer were exposed by a photolithography method. Then, the second electrode made of Au was formed on the exposed portion of the second cladding layer.

**[0099]** After forming the first and second electrodes, RTA heat treatment was performed at 400°C for 5 minutes to obtain ohmic contact.

**[0100]** After adhesion with a silicone-coated wafer, a laser was irradiated from the support substrate side for ablation, and then the support substrate and the element were separated.

(Comparison of results between Examples and Comparative Example)

**[0101]** Temporarily bonded wafers manufactured in Examples 1 and 2, and Comparative Example were compared in light of area yield, doping level, area yield when P-CVD is adopted, and leakage failure rate as follows.

[Area yield]

**[0102]** Table 1 shows a comparison of yield (ratio of adhesive area). In Example 1 and Example 2, since the electrode formation process and the element separation process were completed before temporary bonding, the temporarily bonded area was not delaminated or deformed by an ohmic heat treatment, and the process was performed to a wafer with excellent flatness and warpage. Consequently, the yield of the electrode formation process and the element separation process was maintained at a comparable level with the non-bonded wafers. On the other hand, in Comparative Example, a wafer having a temporarily bonded portion was applied to high-temperature RTA heat treatment, and the temporarily bonded portion was delaminated or deformed. Thus, a sufficient yield was not obtained.

[Table 1]

	Example 1	Example 2	Comparative Example
Effective Area	97%~99%	96%~99%	10~47%

[Doping Level]

**[0103]** Even with applying curing treatment, a BCB film loses bonding strength when the film exceeds the softening point. Therefore, a high temperature processing should not be performed. To form ohmic contact, it is required to employ one of the following methods: the process is performed at a temperature higher than the softening point of BCB; and the metal contact layer is highly doped to avoid high-temperature treatment. However, heat treatment above the BCB softening point tends to induce deformation of the BCB bonded layer, leading to a decrease in an element yield. On the other hand, a highly doped contact layer easily induces an element degradation during energization through electromigration effect during energization, leading to performance degradation. When the process for electrode formation and element separation is performed in a wafer state where a BCB bonded wafer has not been formed, it is possible to effectively avoid the thermal restriction and the restrictions in designing an epitaxial substrate. Therefore, it is possible to increase the degree of freedom in design and avoid quality degradation of the element due to the process restriction.

**[0104]** Doping levels required for the first and the second electrode contact layers in Example 1, Example 2, and Comparative Example are shown in Table 2. In Examples, high-temperature heat treatment during electrode formation is possible. Consequently, ohmic contact can be obtained at the doping level of 10 to the power of seventeen. On the other hand, in Comparative Example, an ohmic heat treatment for electrode formation is performed on a wafer including a BCB temporarily bonded portion; thus, when a high-temperature treatment is performed, the temporarily bonded portion is delaminated. Consequently, in Comparative Example, heat treatment at a low temperature is needed to maintain a high yield. Thus, the doping level of 10 to the power of eighteen level is needed.

**[0105]** When a cladding layer having a doping level of 10 to the power of eighteen is formed, a defect tends to occur in an active layer due to electromigration during energization; it is highly possible that the element is degraded by energizing. A light-emitting element doped at 10 to the power of eighteen level shows a satisfied quality only in the initial characteristic but cannot show a satisfied quality in the transient characteristic. In Examples, since an epitaxial layer having a one-digit lower doping level can be introduced, the problem produced in Comparative Example, in which an unsatisfactory transient characteristic is produced, can be avoided.

[Table 2]

	Example 1	Example 2	Comparative Example
First electrode contact layer	1~5E+17[/cm <sup>3</sup> ]	1~3E+17[/cm <sup>3</sup> ]	1~2E+18[/cm <sup>3</sup> ]
Second electrode contact layer	1~5E+17[/cm <sup>3</sup> ]	1~5E+17[/cm <sup>3</sup> ]	1~2E+18[/cm <sup>3</sup> ]

[Area yield when P-CVD is adopted]

**[0106]** To form SiO<sub>2</sub> as a PSV film, a film-forming method such as P-CVD is needed, and a heat environment of 400°C or more is needed due to a factor of the material reaction system. When the film-forming is performed by P-CVD after BCB bonding (Comparative Example), the film-forming needs to be performed under the condition of the BCB softening point. Thus, deformation of the BCB film is likely to occur during film-forming. Deformation of the BCB film is manifested as an uplift (delamination) phenomenon of the epitaxial layer, eventually leading to delamination of the uplift portions, thereby decreasing the yield.

**[0107]** Table 3 shows the yield when the P-CVD process is introduced (adhesive area ratio). As shown in Table 3, high yields were obtained in Examples; by contrast, in Comparative Example, in which the PSV film formation process was performed after the temporary bonding, the yield was decreased due to the occurrence of the delamination at the bonding portion during PSV film-forming process.

[Table 3]

	Example 1	Example 2	Comparative Example
Effective Area	97%~100%	95%~100%	16~68%

[Leakage failure rate]

**[0108]** If the PSV film is only a hard mask, a film-forming method other than a P-CVD method, e.g., a physical film-forming method, can be selected. However, in the PSV film formation, the physical film-forming method has a poor coverage rate at the side surface, thus having a problem that cannot suppress a leakage occurring at the side surface.

**[0109]** Therefore, as shown in Table 4, Comparative Example that cannot adopt the most suitable P-CVD method for the PSV film-forming had a higher leakage failure rate compared with Example 1 and Example 2, which were able to adopt the P-CVD method.

[Table 4]

	Example 1	Example 2	Comparative Example
Leakage failure rate	0.01%~3.75%	0.01%~4.11%	58~100%

**[0110]** It should be noted that the present invention is not limited to the above-described embodiments. The embodiments are just examples, and any examples that have substantially the same feature and demonstrate the same functions and effects as those in the technical concept disclosed in claims of the present invention are included in the technical scope of the present invention.

**Claims**

1. A temporarily bonded wafer in which an epitaxial functional layer having two or more electrodes with different polarities on one surface and a support substrate are temporarily bonded, wherein the surface having the electrodes of the epitaxial functional layer and the support substrate are temporarily bonded via an uncured thermosetting bonding material.
2. The temporarily bonded wafer according to claim 1, wherein the epitaxial functional layer is a light emitting element.
3. The temporarily bonded wafer according to claim 1 or 2, wherein the epitaxial functional layer contains an AlGaInP-based or InGaN-based material.
4. The temporarily bonded wafer according to any one of claims 1 to 3, wherein the thermosetting bonding material is any of benzocyclobutene (BCB) resin, polyimide (PI) resin, fluororesin, and epoxy resin.
5. The temporarily bonded wafer according to any one of claims 1 to 4, wherein the support substrate is comprised of any of the materials: silicon, sapphire, GaP, GaAs, InP, SiC, quartz, glass, LiTaO<sub>3</sub>, and LiNbO<sub>3</sub>.
6. The temporarily bonded wafer according to any one of claims 1 to 5, wherein the wafer does not have a starting substrate on a surface of the epitaxial functional layer opposite to the surface having the electrodes.
7. A method for manufacturing a temporarily bonded wafer, the method being a method for temporarily bonding an epitaxial substrate in which an epitaxial functional layer is grown on a starting substrate to a support substrate, the method comprising:
  - (1) forming two or more electrodes with different polarities on one surface of the epitaxial functional layer of the epitaxial substrate; and
  - (2) temporarily bonding the support substrate to the surface on which the electrodes are formed via an uncured thermosetting bonding material.
8. The method for manufacturing a temporarily bonded wafer according to claim 7, wherein the epitaxial functional layer is a light emitting element.

**EP 4 391 018 A1**

9. The method for manufacturing a temporarily bonded wafer according to claim 7 or 8, wherein the epitaxial functional layer contains an AlGaInP-based or InGaN-based material.

5 10. The method for manufacturing a temporarily bonded wafer according to any one of claims 7 to 9, wherein the thermosetting bonding material is any of benzocyclobutene (BCB) resin, polyimide (PI) resin, fluororesin, and epoxy resin.

10 11. The method for manufacturing a temporarily bonded wafer according to any one of claims 7 to 10, wherein the support substrate is comprised of any of the materials: silicon, sapphire, GaP, GaAs, InP, SiC, quartz, glass, LiTaO<sub>3</sub>, and LiNbO<sub>3</sub>.

15 12. The method for manufacturing a temporarily bonded wafer according to any one of claims 7 to 11, the method further comprising: after (2),  
(3) removing the starting substrate from the epitaxial substrate.

20

25

30

35

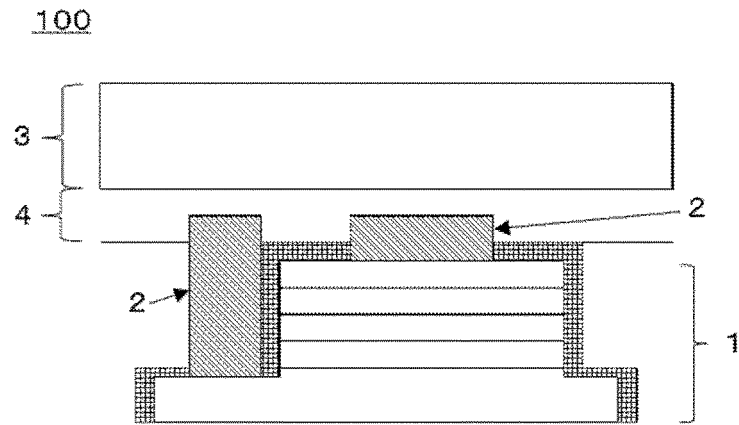
40

45

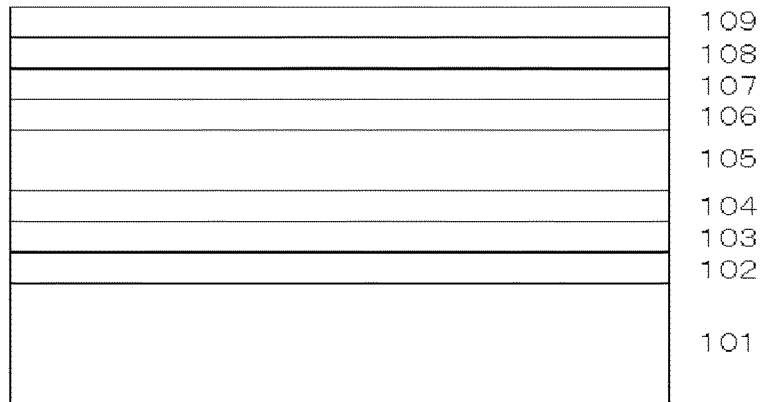
50

55

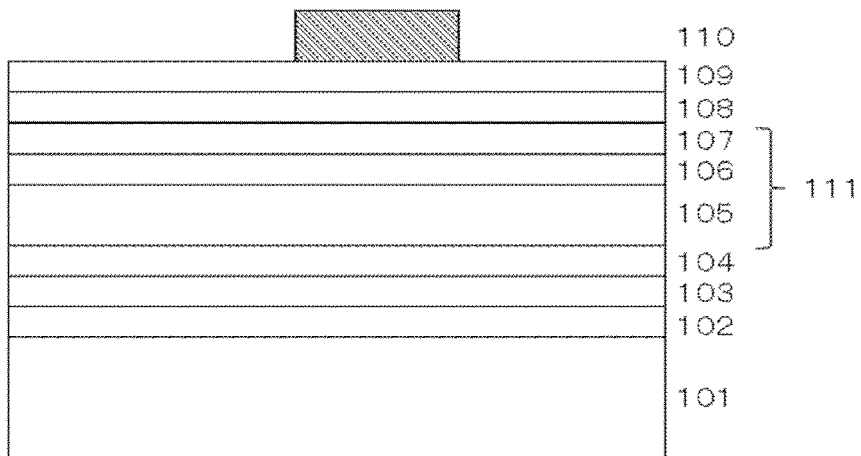
[FIG. 1]



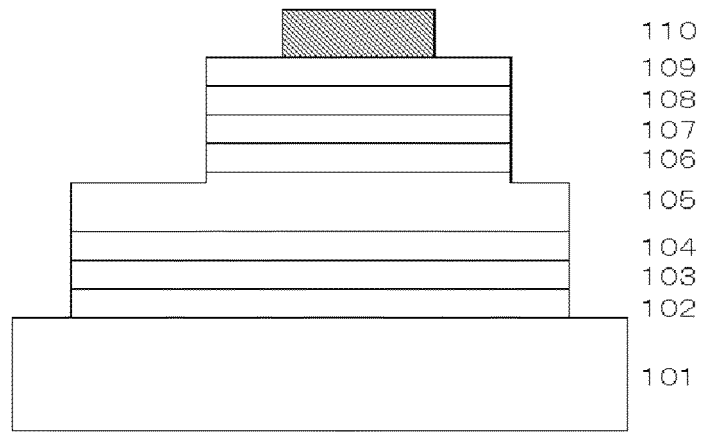
[FIG. 2]



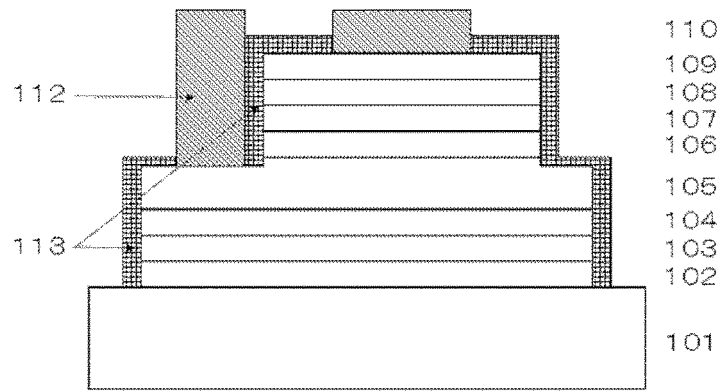
[FIG. 3]



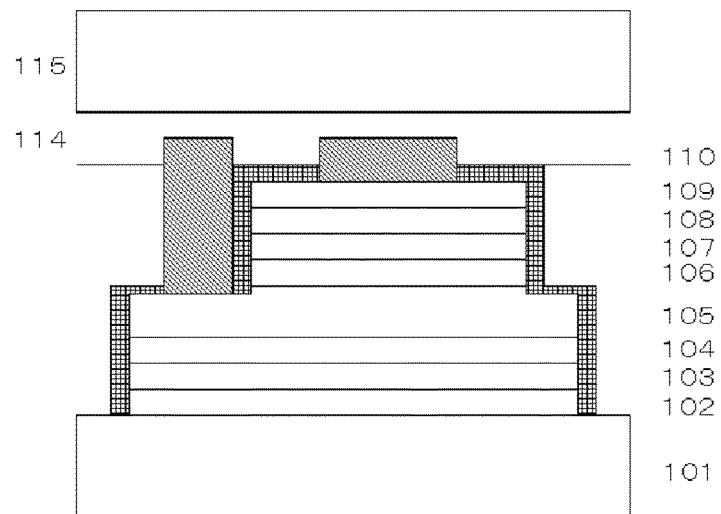
[FIG. 4]



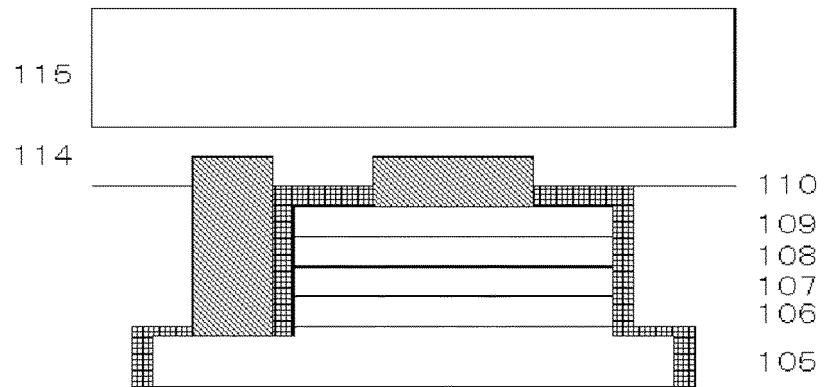
[FIG. 5]



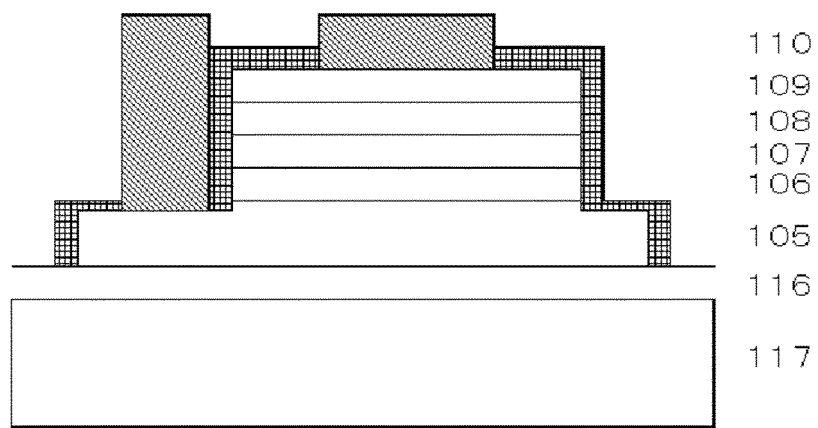
[FIG. 6]



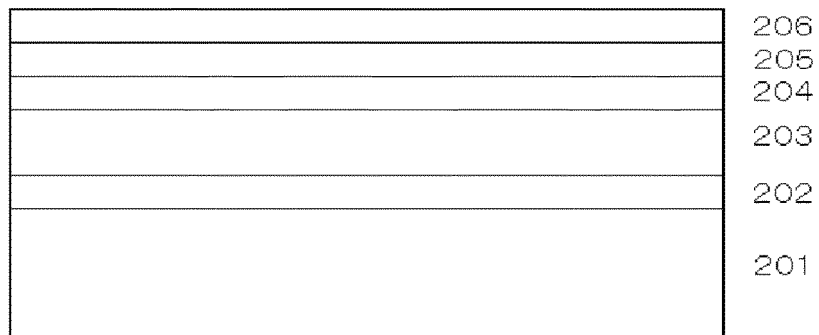
[FIG. 7]



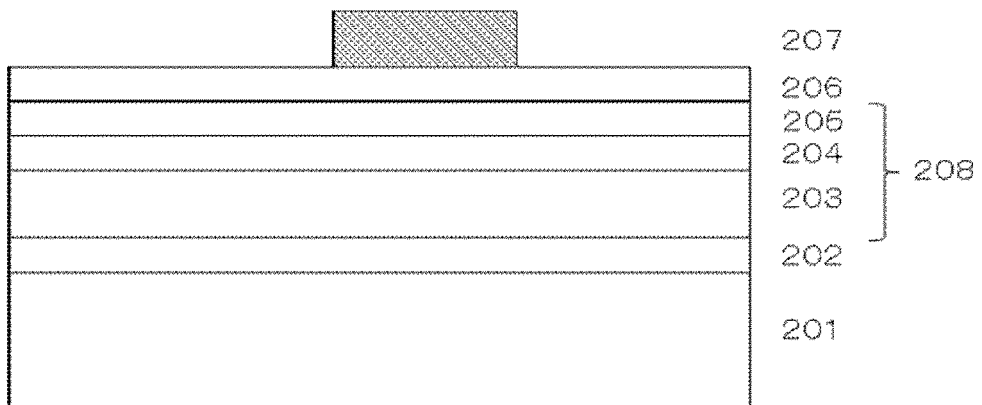
[FIG. 8]



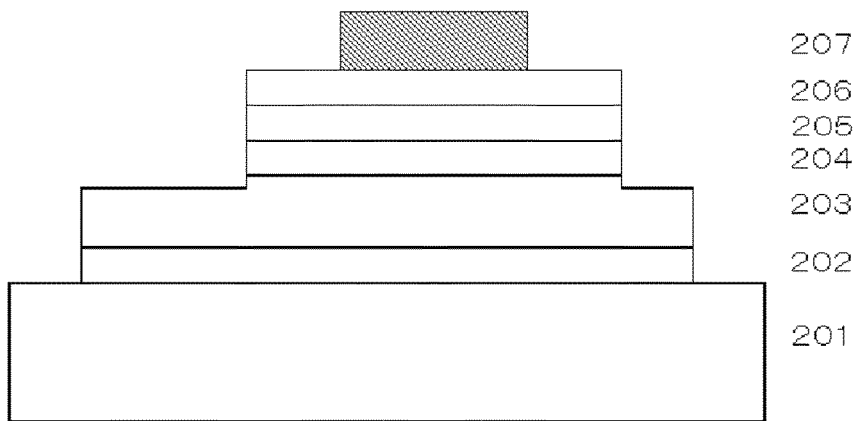
[FIG. 9]



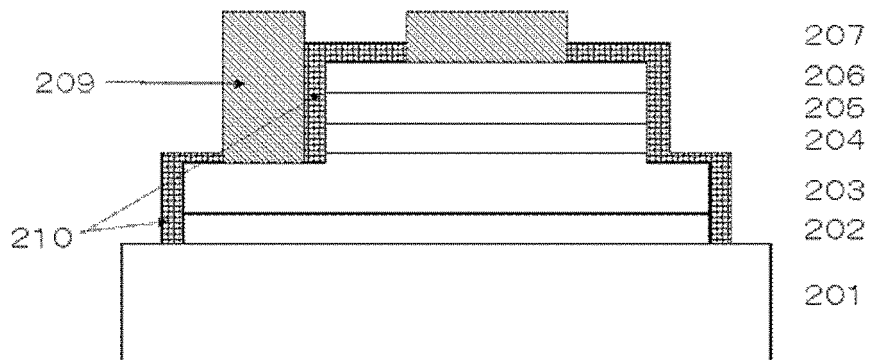
[FIG. 10]



[FIG. 11]

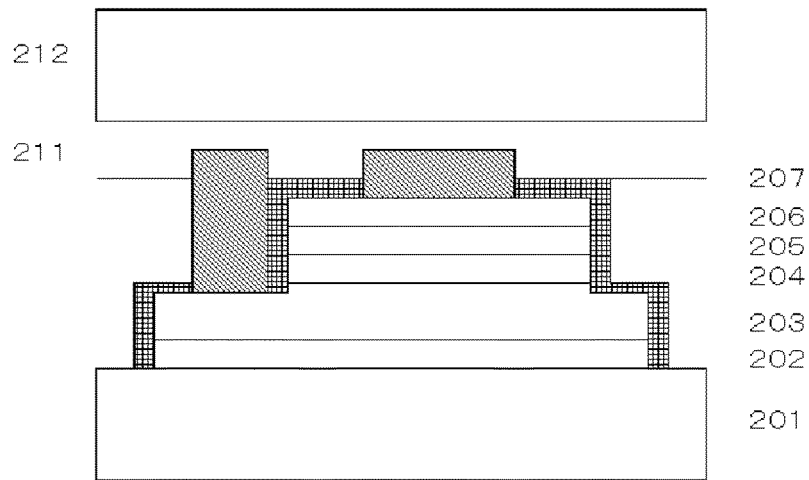


[FIG. 12]

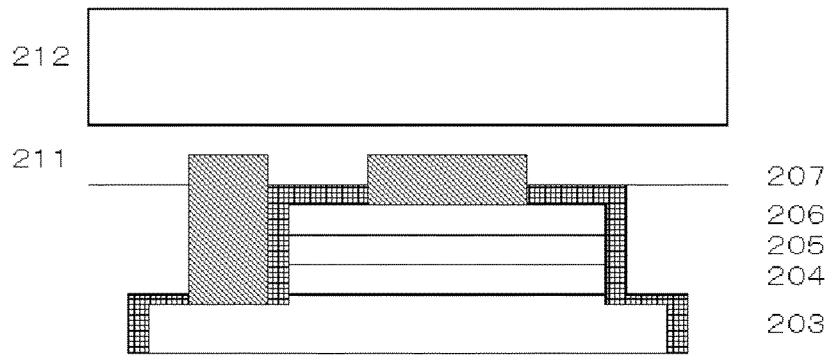




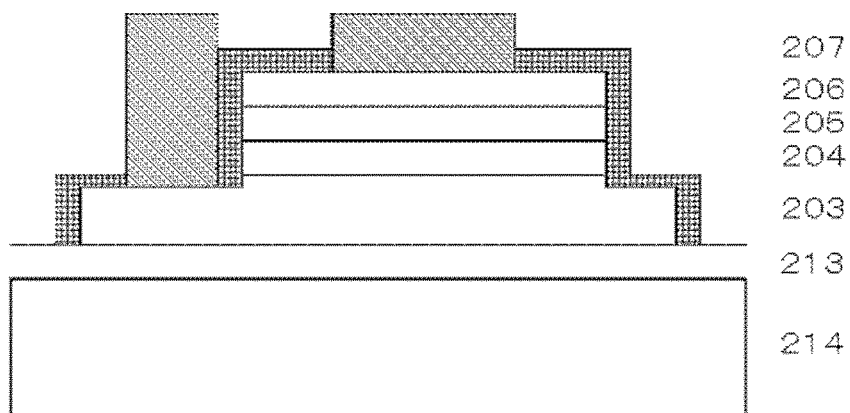
[FIG. 13]



[FIG. 14]



[FIG. 15]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2022/029483

5

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
H01L 21/02(2006.01)i FI: H01L21/02 B; H01L21/02 C  According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols) H01L21/02		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2022 Registered utility model specifications of Japan 1996-2022 Published registered utility model applications of Japan 1994-2022		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2007-42664 A (SHIN ETSU HANDOTAI CO., LTD.) 15 February 2007 (2007-02-15)	1-3, 5-9, 11-12
Y	paragraphs [0001], [0019]-[0044], fig. 1-8	4, 10
Y	WO 2019/013212 A1 (SHIN-ETSU CHEMICAL CO., LTD.) 17 January 2019 (2019-01-17)	4, 10
A	paragraph [0033], fig. 1	1-3, 5-9, 11-12
Y	WO 2021/024768 A1 (SHIN ETSU HANDOTAI CO., LTD.) 11 February 2021 (2021-02-11)	4, 10
A	paragraph [0029], fig. 3	1-3, 5-9, 11-12
Y	JP 2008-187160 A (ROHM CO., LTD.) 14 August 2008 (2008-08-14)	4, 10
A	paragraphs [0044], [0045], fig. 3, 4	1-3, 5-9, 11-12
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search <b>14 September 2022</b>		Date of mailing of the international search report <b>04 October 2022</b>
Name and mailing address of the ISA/JP <b>Japan Patent Office (ISA/JP) 3-4-3 Kasumigaseki, Chiyoda-ku, Tokyo 100-8915 Japan</b>		Authorized officer  Telephone No.

10

15

20

25

30

35

40

45

50

55

INTERNATIONAL SEARCH REPORT  
Information on patent family members

International application No.  
**PCT/JP2022/029483**

5  
10  
15  
20  
25  
30  
35  
40  
45  
50  
55

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
JP 2007-42664 A	15 February 2007	(Family: none)	
WO 2019/013212 A1	17 January 2019	US 2020/0227263 A1 paragraph [0035], fig. 1 EP 3654366 A1 CN 110892506 A KR 10-2020-0026822 A	
WO 2021/024768 A1	11 February 2021	(Family: none)	
JP 2008-187160 A	14 August 2008	US 2008/0164486 A1 paragraphs [0051], [0052], fig. 3, 4	

Form PCT/ISA/210 (patent family annex) (January 2015)

**REFERENCES CITED IN THE DESCRIPTION**

*This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.*

**Patent documents cited in the description**

- JP 2021027301 A [0005]
- JP 4159421 B [0005]
- JP 2008187160 A [0005]