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(54) **METHOD FOR FORMING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE**

(71) Applicant: **CHANGXIN MEMORY TECHNOLOGIES, INC.**, Hefei City (CN)

(72) Inventor: **CHIH-CHENG LIU**, Hefei (CN)

(73) Assignee: **CHANGXIN MEMORY TECHNOLOGIES, INC.**, Hefei City (CN)

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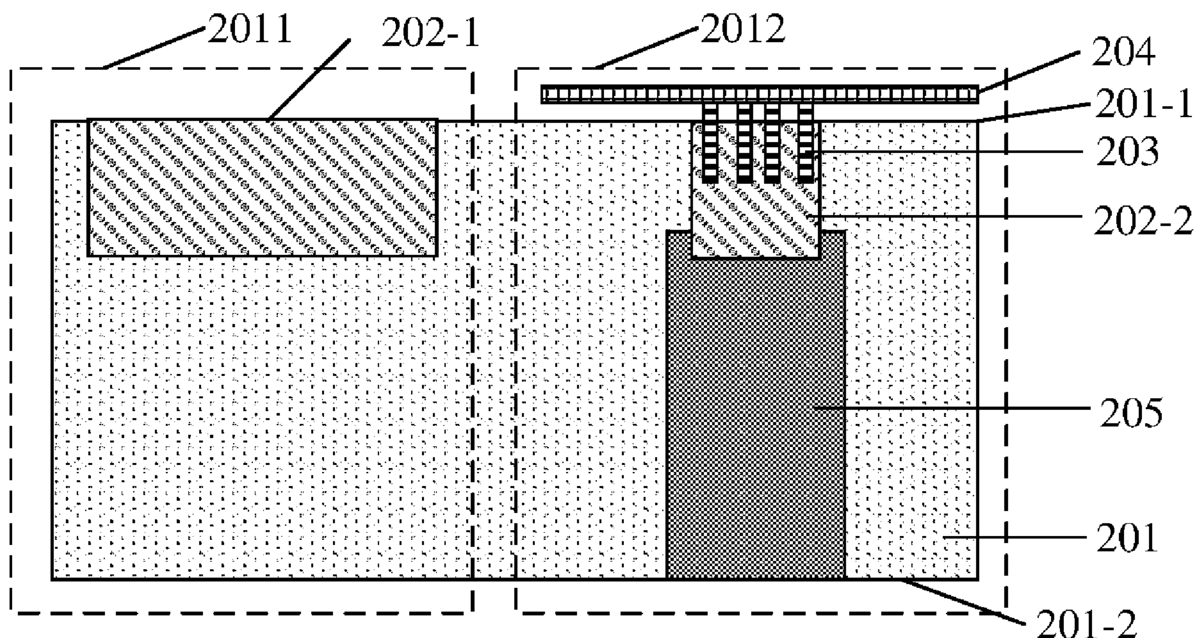
(52) **U.S. Cl.**
CPC ***H01L 21/76898*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 23/535*** (2013.01); ***H01L 21/743*** (2013.01)

(57) **ABSTRACT**

In a method for forming a semiconductor device, a substrate is provided; a word line is formed in the substrate by taking a first face of the substrate as an upper surface; a connecting layer electrically connected to one end of the word line is formed in part of the substrate and on the substrate; a first conducting layer is formed on the connecting layer; and a conducting plug is formed in the substrate by taking a second face of the substrate as an upper surface. The conducting plug is electrically connected to another end of the word line and electrically connected to the first conducting layer via the word line. The first face and the second face are two faces of the substrate opposite to each other in a thickness direction of the substrate.



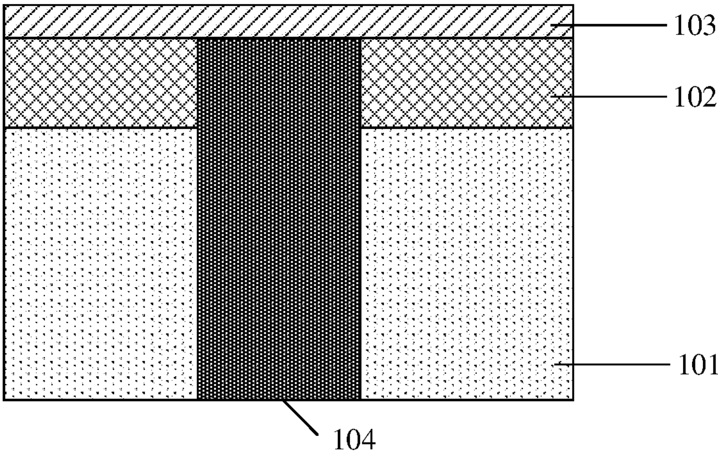


FIG. 1

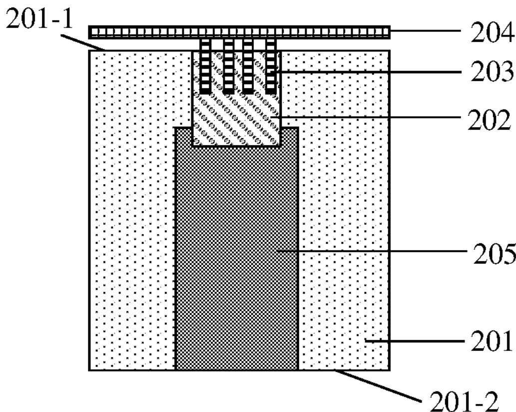


FIG. 2A

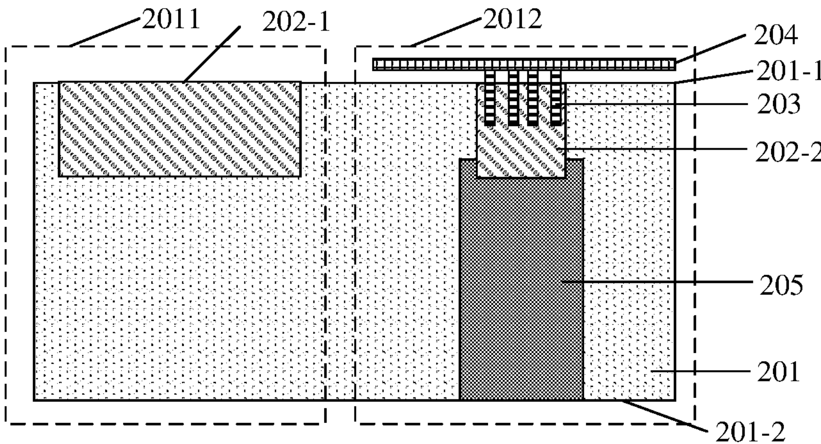


FIG. 2B

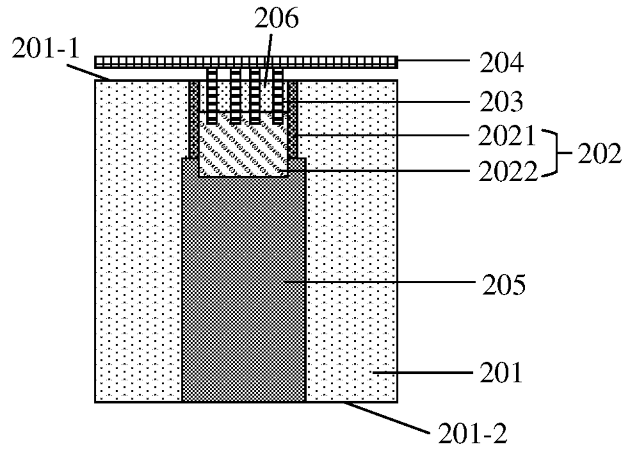


FIG. 2C

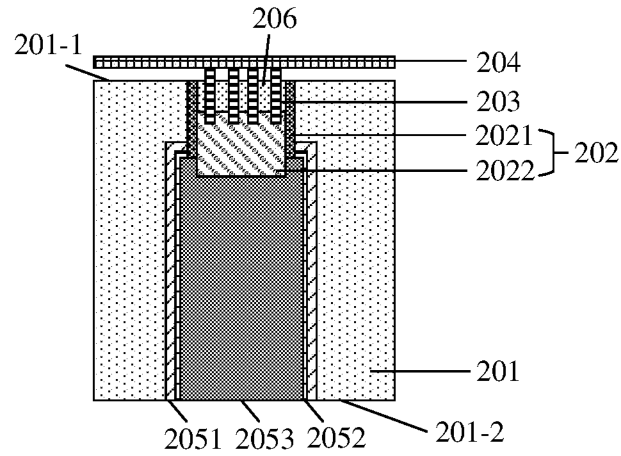


FIG. 2D

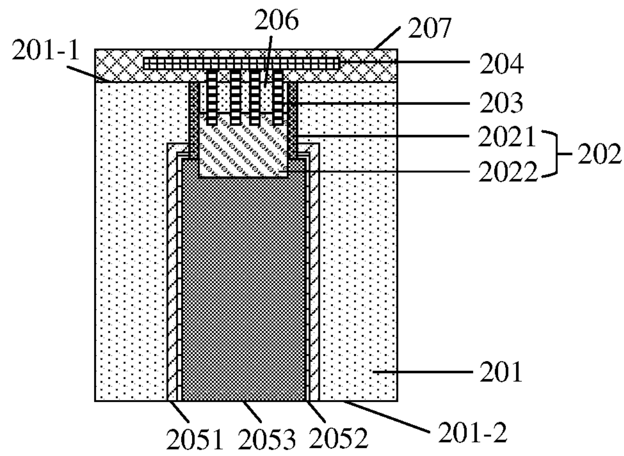


FIG. 2E

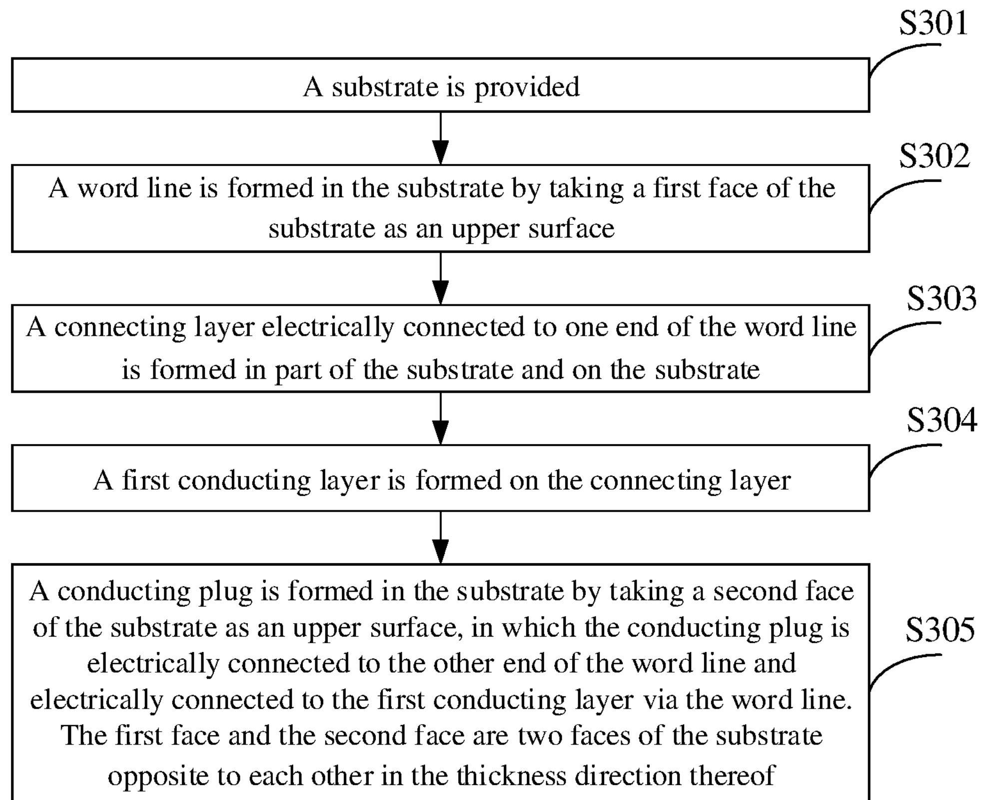


FIG. 3

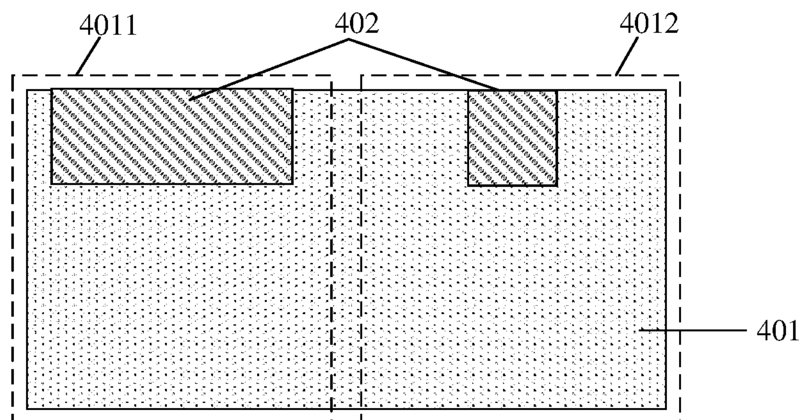


FIG. 4A

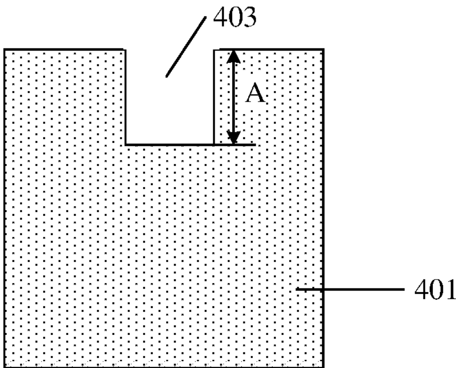


FIG. 4B

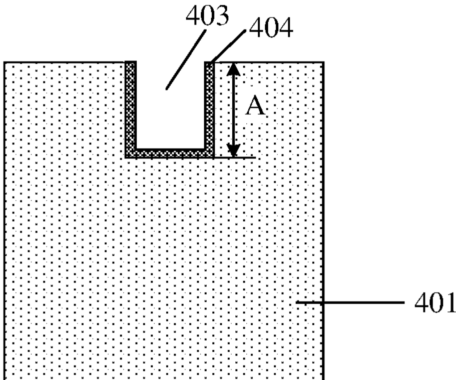


FIG. 4C

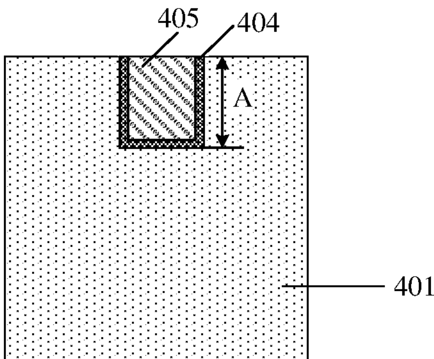


FIG. 4D

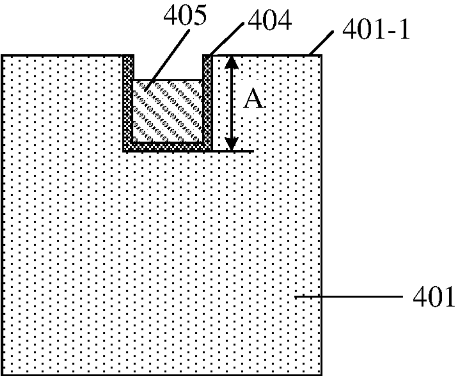


FIG. 4E

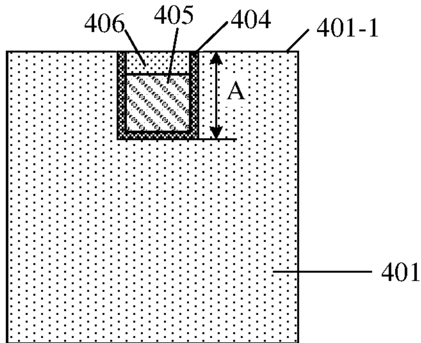


FIG. 4F

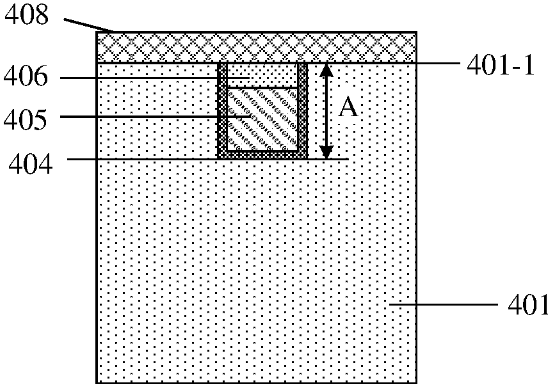


FIG. 4G

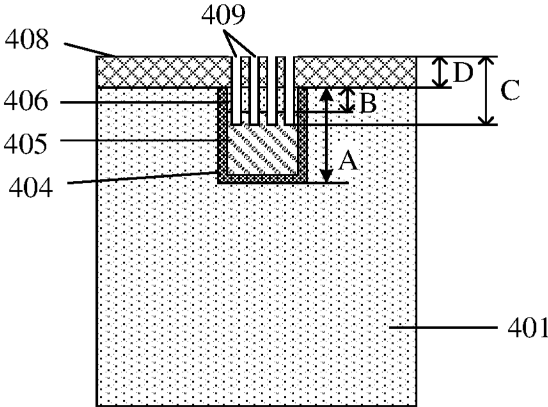


FIG. 4H

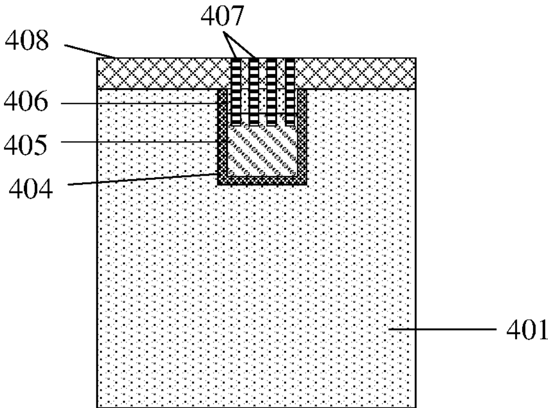


FIG. 4I

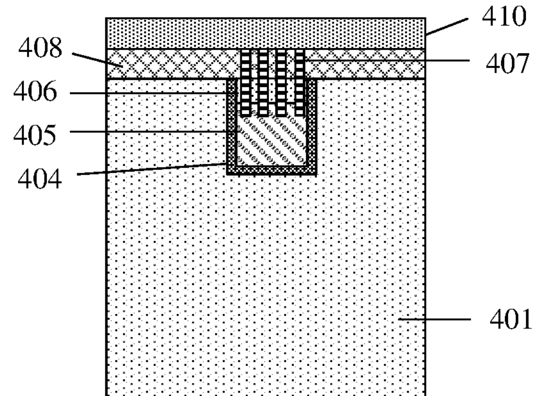


FIG. 4J

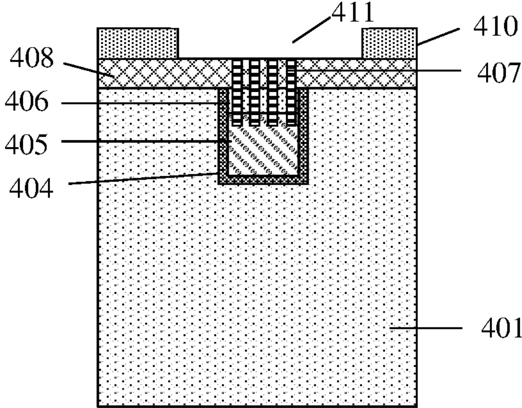


FIG. 4K

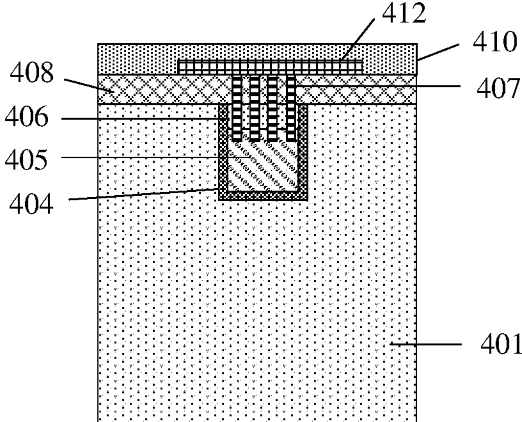


FIG. 4L

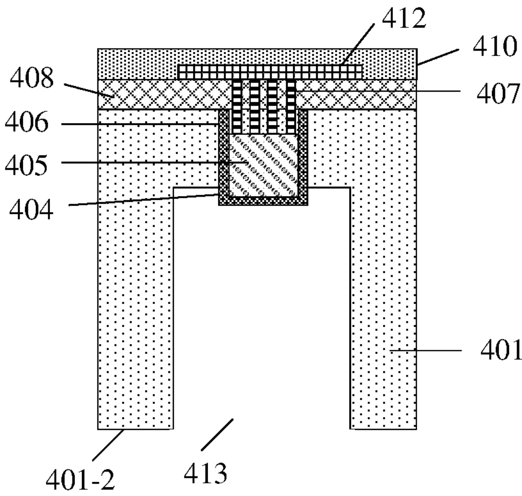


FIG. 4M

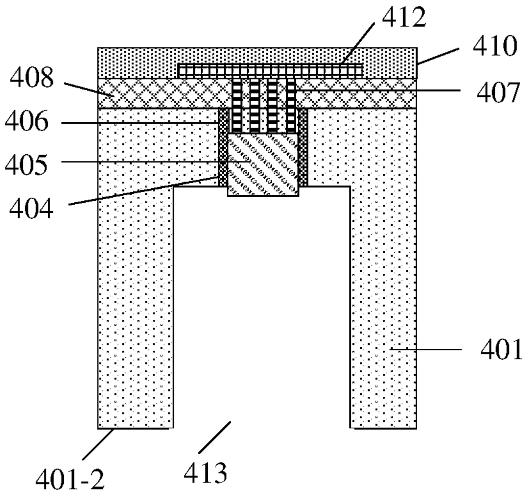


FIG. 4N

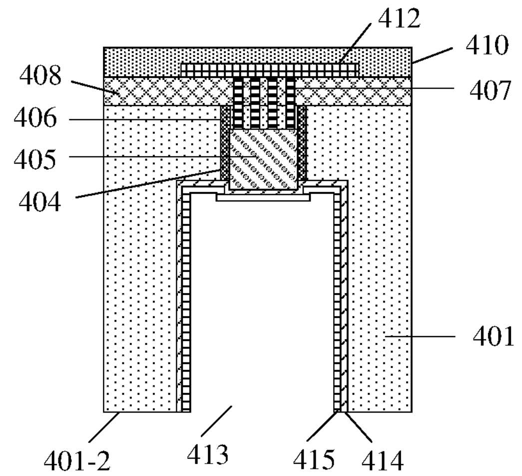


FIG. 4O

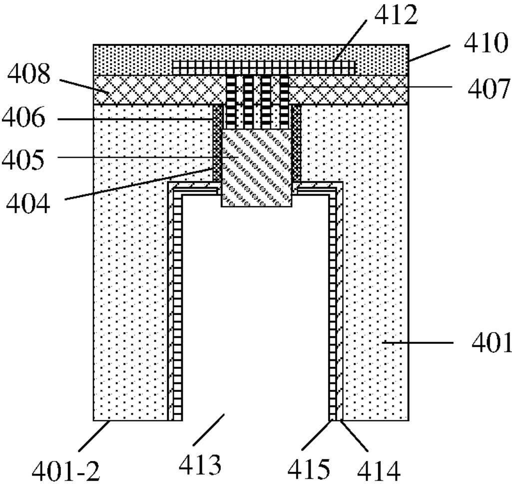


FIG. 4P

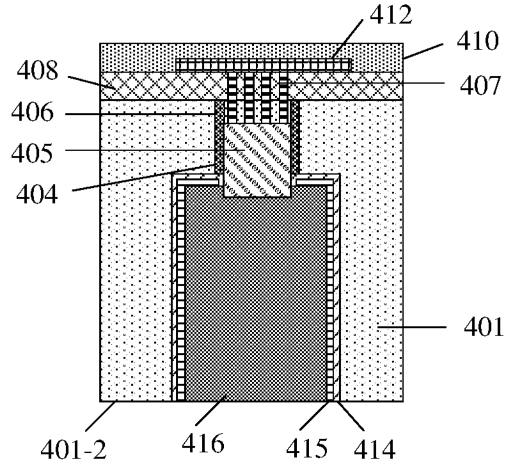


FIG. 4Q

METHOD FOR FORMING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a continuation application of International Application No. PCT/CN2022/081991 filed on Mar. 21, 2022, which claims priority to Chinese Patent Application No. 202210013825.1 filed on Jan. 7, 2022. The disclosures of the above-referenced applications are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] In the related art, when through silicon via (TSV) technology is used to stack dynamic random access memory (DRAM) chips in a DRAM, TSVs penetrate through the whole substrate and connect to a metal layer.

SUMMARY

[0003] Embodiments of the disclosure provide a method for forming a semiconductor device and the semiconductor device.

[0004] In a first aspect, embodiments of the disclosure provide a method for forming a semiconductor device. The method includes:

[0005] providing a substrate;

[0006] forming a word line in the substrate by taking a first face of the substrate as an upper surface;

[0007] forming a connecting layer electrically connected to one end of the word line in part of the substrate and on the substrate;

[0008] forming a first conducting layer on the connecting layer; and

[0009] forming a conducting plug in the substrate by taking a second face of the substrate as an upper surface, in which the conducting plug is electrically connected to another end of the word line and electrically connected to the first conducting layer via the word line, and the first face and the second face are two faces of the substrate opposite to each other in a thickness direction of the substrate.

[0010] In a second aspect, embodiments of the disclosure provide a semiconductor device, and the semiconductor device includes at least:

[0011] a substrate;

[0012] a word line located in the substrate, in which the word line is close to a first face of the substrate;

[0013] a connecting layer located in part of the substrate and on the substrate and electrically connected to one end of the word line;

[0014] a first conducting layer located on the connecting layer; and

[0015] a conducting plug located in the substrate and electrically connected to another end of the word line, in which the conducting plug is electrically connected to the first conducting layer via the word line, and the conducting plug is close to a second face of the substrate, and wherein the first face and the second face are two faces of the substrate opposite to each other in a thickness direction of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] In the drawings (which are not necessarily drawn to scale), similar reference numerals may describe similar parts in different views. Similar reference numerals with different letter suffixes may represent different examples of similar parts. The various embodiments discussed herein are generally shown in the accompanying drawings by way of example, but not limitation.

[0017] FIG. **1** is a partial structural schematic diagram of a TSV technology in the related art;

[0018] FIG. **2**A is a first partial structural schematic diagram of the semiconductor device provided by embodiments of the disclosure;

[0019] FIG. **2**B is a second partial structural schematic diagram of the semiconductor device provided by embodiments of the disclosure;

[0020] FIG. **2**C is a third partial structural schematic diagram of the semiconductor device provided by embodiments of the disclosure;

[0021] FIG. **2**D is a fourth partial structural schematic diagram of the semiconductor device provided by embodiments of the disclosure;

[0022] FIG. **2**E is a fifth partial structural schematic diagram of the semiconductor device provided by embodiments of the disclosure;

[0023] FIG. **3** is a flowchart of the method for forming a semiconductor device provided by embodiments of the disclosure;

[0024] FIG. **4**A is a first partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0025] FIG. **4**B is a second partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0026] FIG. **4**C is a third partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0027] FIG. **4**D is a fourth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0028] FIG. **4**E is a fifth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0029] FIG. **4**F is a sixth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0030] FIG. **4**G is a seventh partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0031] FIG. **4**H is an eighth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0032] FIG. **4**I is a ninth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0033] FIG. **4**J is a tenth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0034] FIG. **4**K is an eleventh partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0035] FIG. **4**L is a twelfth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0036] FIG. **4**M is a thirteenth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0037] FIG. **4**N is a fourteenth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0038] FIG. **4**O is a fifteenth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure;

[0039] FIG. **4**P is a sixteenth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure; and

[0040] FIG. **4**Q is a seventeenth partial structural schematic diagram corresponding to a method for forming a semiconductor device provided by embodiments of the disclosure.

DETAILED DESCRIPTION

[0041] Specific technical solutions of the disclosure will be further described in detail below with reference to the drawings in embodiments of the disclosure. The following embodiments are used to illustrate the disclosure, but not to limit the scope of the disclosure.

[0042] In the following description, suffixes such as "module" or "unit" used to denote elements are used only for the benefit of the description of the disclosure and have no specific meaning in themselves. Therefore, "module" or "unit" can be used in a mixed way.

[0043] In the related art, DRAM chips are stacked by a TSV technology for high-speed and broadband applications. FIG. **1** is a partial structural schematic diagram of a TSV technology in the related art. As shown in FIG. **1**, a dielectric layer **102** and a metal layer **103** are provided on the surface of a substrate **101**, and a through silicon via **104** penetrates through both the substrate **101** and the dielectric layer **102**, and is connected to the metal layer **103**. In this case, the structure of a semiconductor device may be destroyed when bonding by the TSV, causing failure problems when devices are subsequently interconnected.

[0044] Embodiments of the disclosure provide a semiconductor device. FIG. **2**A to FIG. **2**E are partial structural schematic diagrams of the semiconductor device provided by the embodiments of the disclosure. As shown in FIG. **2**A, the semiconductor device includes a substrate **201**, a word line **202**, a connecting layer **203**, a first conducting layer **204** and a conducting plug **205**. The word line **202** is located in the substrate **201**, and the word line is close to a first face **201-1** of the substrate. The connecting layer **203** is located in part of the substrate **201** and on the substrate **201** and electrically connected to one end of the word line **202**. The first conducting layer **204** is located on the connecting layer **203**. The conducting plug **205** is located in the substrate **201** and electrically connected to the other end of the word line **202**, and the conducting plug **205** is electrically connected to the first conducting layer **204** via the word line **202**, and the conducting plug **205** is close to a second face **201-2** of the substrate **201**. The first face **201-1** and the second face **201-2** are two faces of the substrate **201** opposite to each other in the thickness direction thereof.

[0045] In some embodiments, the substrate **201** includes at least an array region **2011** and a peripheral region **2012**. The word line **202** includes a word line **202-1** in the array region **2011** and a word line **202-2** in the peripheral region **2012**. The connecting layer **203** is located at the peripheral region **2012** and electrically connected to one end of the word line **202-2** in the peripheral region **2012**, as shown in FIG. **2**B.

[0046] In some embodiments, the word line **202** includes a word line dielectric layer **2021** and a second conducting layer **2022**. The word line dielectric layer **2021** is located on the surface of the substrate **201**. The second conducting layer **2022** is located on the surface of the word line dielectric layer **2021**, and the surface of the second conducting layer **2022** is lower than the first face of the substrate **201**. In some embodiments, the semiconductor device further includes an isolation layer **206** located on the second conducting layer **2022**, and the surface of the isolation layer **206** is flush with the first face **201-1** of the substrate **201**, as shown in FIG. **2**C.

[0047] In some embodiments, the conducting plug **205** includes a liner **2051**, a buffer layer **2052** and a third conducting layer **2053**. The liner **2051** is located on the surface of the substrate **201**. The buffer layer **2052** is located on the surface of the liner **2051**. The third conducting layer **2053** is located on the surface of the buffer layer **2052** and electrically connected to the second conducting layer **2022**, as shown in FIG. **2**D.

[0048] In some embodiments, the semiconductor device further includes a dielectric layer **207**. The dielectric layer **207** is located on the word line **202**, the isolation layer **206** and the substrate **201**. The first conducting layer **204** and part of the connecting layer **203** are located in the dielectric layer **207**, as shown in FIG. **2**E.

[0049] In some embodiments, the dielectric layer **207** may include a first dielectric layer and a second dielectric layer (not shown in the drawings), in which the part of the connecting layer **203** is located in the first dielectric layer, and the first conducting layer **204** is located in the second dielectric layer. Materials of the first dielectric layer and the second dielectric layer are the same or different.

[0050] In the semiconductor device provided by the embodiments of the disclosure, the word line is formed by taking the first face of the substrate as an upper surface, and the connecting layer connected to the first conducting layer is formed in the word line. The conducting plug is formed by taking the second face of the substrate as an upper surface, and the conducting plug is electrically connected to the first conducting layer via the word line and the connecting layer. According to the embodiments of the disclosure, an indirect connection between the conducting plug and the first conducting layer is realized via the buried word line in the substrate, so that the conducting plug does not penetrate through the whole semiconductor substrate and does not destroy the structure of the semiconductor substrate, thus improving the yield and performance of semiconductor devices.

[0051] Based on the semiconductor device provided by the foregoing embodiments, embodiments of the disclosure provide a method for forming a semiconductor device. Reference may be made to FIG. **3**, which is a flowchart of the method for forming a semiconductor device provided by embodiments of the disclosure. The semiconductor device provided by the embodiments of the disclosure can be formed by the following operations.

[0052] At S**301**, a substrate is provided.

[0053] At S**302**, a word line is formed in the substrate by taking a first face of the substrate as an upper surface.

[0054] At S**303**, a connecting layer electrically connected to one end of the word line is formed in part of the substrate and on the substrate.

[0055] At S**304**, a first conducting layer is formed on the connecting layer.

[0056] At S**305**, a conducting plug is formed in the substrate by taking a second face of the substrate as an upper surface, in which the conducting plug is electrically connected to the other end of the word line and electrically connected to the first conducting layer via the word line. The first face and the second face are two faces of the substrate opposite to each other in the thickness direction thereof.

[0057] Referring to FIG. **4**A to FIG. **4**Q, the method for forming a semiconductor device provided by embodiments of the disclosure is described in detail below.

[0058] As shown in FIG. **4**A to FIG. **4**E, S**301** and S**302** are performed, in which a substrate **401** is provided, and a word line **402** is formed in the substrate **401** by taking a first face **401-1** of the substrate **401** as an upper surface.

[0059] In some embodiments, the substrate **401** may be made of a semiconductor material, for example, one or more of silicon, germanium, a silicon-germanium compound or a silicon-carbon compound.

[0060] In some embodiments, a substrate **401** includes at least an array region **4011** and a peripheral region **4012**. The operation that a word line **402** is formed in the substrate **401** means that the word line **402** is formed in both the array region **4011** and the peripheral region **4012** by taking a first face **401-1** of the substrate **401** as an upper surface, as shown in FIG. **4**A.

[0061] It should be noted that, in order to accurately demonstrate the method for forming a semiconductor device provided by the embodiments of the disclosure, the peripheral region **4012** of the substrate **401** is taken as an example in the following drawings, to illustrate the method for forming a semiconductor device provided by the embodiments of the disclosure.

[0062] In some embodiments, the word line **402** is formed in the peripheral region **4012** by the following operations.

[0063] At S**3021**, a first groove having a first thickness is formed in the peripheral region.

[0064] Referring to FIG. **4**B, a first groove **403** is formed in the peripheral region **4012** of the substrate by wet etching or dry etching. The first groove **403** has a first thickness A in a direction perpendicular to the surface of the substrate **401**.

[0065] At S**3022**, a word line dielectric layer covering a sidewall of the first groove is formed.

[0066] In embodiments of the disclosure, as shown in FIG. **4**C, a word line dielectric layer **404** covering a sidewall of the first groove **403** may be formed by physical vapor deposition (PVD), chemical vapor deposition (CVD), or atomic layer deposition (ALD). The material of the word line dielectric layer **404** may include at least one of silicon carbide (SiC), hafnium oxide (HfO_2), hafnium oxide nitride (HfON), aluminium oxide (Al_2O_3), zirconia (ZrO_2), or silicon dioxide (SiO_2) or other inorganic oxides.

[0067] At S**3023**, a second conducting layer is filled in the first groove having the word line dielectric layer.

[0068] At S**3024**, the second conducting layer is etched back to form the second conducting layer, the surface of which is lower than the first face of the substrate, to obtain the word line.

[0069] Referring to FIG. **4**D and FIG. **4**E, a second conducting layer **405** may be filled in the first groove **403** having the word line dielectric layer **404** by physical vapor deposition, chemical vapor deposition or atomic layer deposition. After the second conducting layer **405** is formed, the second conducting layer **405** is etched back by wet etching or dry etching to form the second conducting layer **405**, the surface of which is lower than the first face **401-1** of the substrate **401**. The second conducting layer **405** having the surface lower than the first face **401-1** and the word line dielectric layer **404** constitute the word line **402**.

[0070] In some embodiments, the second conducting layer **405** of the word line **402** may include at least one of titanium nitride (TiN), tantalum nitride (TaN), hafnium nitride (HfN), aluminum tantalum nitride (TaAlN) or aluminum titanium nitride (TiAlN), tungsten, polysilicon, or other materials.

[0071] In some embodiments, after the second conducting layer **405** having the surface lower than the first face **401-1** is formed, the method for forming a semiconductor device provided by the embodiments of the disclosure further includes forming an isolation layer **406** on the second conducting layer **405**. The surface of the isolation layer **406** is flush with the first face **401-1** of the substrate **401**.

[0072] As shown in FIG. **4**F, the isolation layer **406** may be formed in a remaining first groove **403** by physical vapor deposition, chemical vapor deposition or atomic layer deposition. The isolation layer **406** may be made of silicon nitride (SiN) or other materials.

[0073] In the embodiments of the disclosure, an indirect connection between the conducting plug and the first conducting layer is realized by forming the buried word line in the substrate, and the problem of interconnection failure caused by the conducting plug penetrating through the whole substrate is avoided.

[0074] Referring to FIG. **4**G to FIG. **4**I, S**303** is performed, in which a connecting layer **407** electrically connected to one end of the word line **402** is formed in part of the substrate **401** and on the substrate **401**.

[0075] In some embodiments, the second conducting layer **405** etched back and the word line dielectric layer **404** constitute the word line **402**, and the connecting layer **407** is electrically connected to one end of the second conducting layer **405** of the word line **402**, that is, the connecting layer **407** is electrically connected to the word line **402**.

[0076] In some embodiments, the connecting layer may be formed by the following operations.

[0077] At S**3031**, a first dielectric layer is formed on the isolation layer, the word line dielectric layer and the substrate.

[0078] Referring to FIG. **4**G, a first dielectric layer **408** covering the isolation layer **406**, the word line dielectric layer **404** and the substrate **401** is formed by physical vapor deposition, chemical vapor deposition or atomic layer deposition.

[0079] In some embodiments, the material of the first dielectric layer **408** may include at least one of zirconia (ZrO_2), hafnium oxide (HfO_2), titanium zirconium oxide ($TiZrO_4$), ruthenium oxide (RuO_4), antimony oxide (Sb_2O_3 or Sb_2O_5), aluminium oxide (Al_2O_3) or other materials.

[0080] At S**3032**, a second groove penetrating through the first dielectric layer and the isolation layer and penetrating through part of the word line in its thickness direction is formed in the first dielectric layer, the isolation layer and the word line, in which the thickness of the second groove is

greater than the sum of the second thickness and the thickness of the first dielectric layer.

[0081] In some embodiments, the distance between the surface of the word line **402** and the first face **401-1** of the substrate **401** in a direction perpendicular to the substrate **401** is a second thickness B.

[0082] In some embodiments, before forming a second groove **409**, a photoresist layer (not shown in the drawings) having a preset pattern may be formed on the surface of the first dielectric layer **408**. The isolation layer **406**, the word line **402** and the first dielectric layer **408** are etched based on the photoresist layer having the preset pattern by wet etching or dry etching, to form the second groove **409** penetrating through the isolation layer **406** and the first dielectric layer **408** and penetrating through part of the word line **402** in its thickness direction.

[0083] In some embodiments, the distance between the surface of the word line **402** and the first face **401-1** of the substrate **401** is the second thickness B, the thickness of the second groove **409** is represented by C, and the thickness of the first dielectric layer **408** is represented by D. In the embodiments of the disclosure, the thickness C of the second groove **409** is greater than the sum of the second thickness B and the thickness D of the first dielectric layer **408**. In the embodiments of the disclosure, as shown in FIG. **4**H, the sum of the first thickness A of the first groove **403** and the thickness D of the first dielectric layer **408** is greater than the thickness C of the second groove **409**.

[0084] In the embodiments of the disclosure, the number of the second grooves **409** is not limited.

[0085] At S**3033**, the second groove is filled to form the connecting layer electrically connected to one end of the word line.

[0086] Referring to FIG. **4**I, a connecting layer **407** may be formed in the second groove **409** by physical vapor deposition, chemical vapor deposition or atomic layer deposition.

[0087] In the embodiments of the disclosure, one end of the connecting layer **407** is located inside the word line **402**, and the connecting layer **407** is connected to the word line **402**.

[0088] In some embodiments, the material of the connecting layer **407** may include at least one of titanium nitride (TiN), tantalum nitride (TaN), hafnium nitride (HfN), aluminum tantalum nitride (TaAlN), aluminum titanium nitride (TiAlN) or other materials.

[0089] In the embodiments of the disclosure, after the connecting layer is formed, the conducting plug is electrically connected to the first conducting layer via the word line and the connecting layer, thus realizing the indirect connection between the conducting plug and the first conducting layer and improving the performance of the semiconductor device.

[0090] Referring to FIG. **4**J to FIG. **4**L, S**304** is performed, in which a first conducting layer **412** is formed on the connecting layer **407**. In embodiments of the disclosure, the first conducting layer **412** may be formed by the following operations.

[0091] At S**3041**, a second dielectric layer is formed on the surface of the first dielectric layer having the connecting layer.

[0092] At S**3042**, a fourth groove penetrating through the second dielectric layer is formed, in which the fourth groove exposes the connecting layer.

[0093] At S**3043**, the fourth groove is filled to form the first conducting layer, in which the first conducting layer is electrically connected to the connecting layer.

[0094] Referring to FIG. **4**J, a second dielectric layer **410** may be formed on the surface of the first dielectric layer **408** having the connecting layer **407** by physical vapor deposition, chemical vapor deposition or atomic layer deposition.

[0095] In some embodiments, the materials of the first dielectric layer **408** and the second dielectric layer **410** may be the same or different. For example, the material of the second dielectric layer **410** may also include at least one of zirconia (ZrO_2), hafnium oxide (HfO_2), titanium zirconium oxide ($TiZrO_4$), ruthenium oxide (RuO_4), antimony oxide (Sb_2O_3 or Sb_2O_5), aluminium oxide (Al_2O_3) or other materials.

[0096] In some embodiments, after the second dielectric layer **410** is formed, a fourth groove **411** is formed in the second dielectric layer **410** by wet etching or dry etching.

[0097] In some embodiments, before forming the fourth groove **411**, a photoresist layer (not shown in the drawings) having a preset pattern may be formed on the surface of the second dielectric layer **410**, and then the second dielectric layer **410** is etched based on the photoresist layer with the preset pattern by wet etching or dry etching to form the fourth groove **411**. As shown in FIG. **4**K, the fourth groove **411** penetrates through the second dielectric layer **410** to expose the connecting layer **407**.

[0098] In the embodiments of the disclosure, after the fourth groove **411** is formed, the fourth groove **411** is filled to form a first conducting layer **412**. The material of the first conducting layer **412** may include at least one of titanium nitride (TiN), tantalum nitride (TaN), hafnium nitride (HfN), aluminum tantalum nitride (TaAlN), aluminum titanium nitride (TiAlN) or other materials.

[0099] In the embodiments of the disclosure, the surface of the first conducting layer **412** may be lower than the surface of the second dielectric layer **410**, and after the first conducting layer **412** is formed, the remaining fourth groove **411** is filled, as shown in FIG. **4**L. The filling material may be the same as or different from the material of the second dielectric layer **410**.

[0100] In some embodiments, while the first conducting layer **412** is formed on the surface of the connecting layer **407**, a first conducting layer (the first conducting layer in the array region, not shown in the drawings) is formed in the array region (not shown in the drawings) of the substrate **401**. The first conducting layer in the array region is electrically connected to a source or a drain in the array region.

[0101] Referring to FIG. **4**M and FIG. **4**N, S**305** is performed, in which a conducting plug is formed in the substrate **401** by taking a second face **401-2** of the substrate **401** as an upper surface. The conducting plug is electrically connected to the other end of the word line **402** and is electrically connected to the first conducting layer **412** via the word line **402**.

[0102] In some embodiments, the first face **401-1** and the second face **401-2** of the substrate **401** are two faces of the substrate opposite to each other in the thickness direction thereof.

[0103] In some embodiments, the conducting plug can be formed by the following operations.

[0104] At S**3051**, a third groove is formed in the substrate by taking the second face of the substrate as the upper surface, in which part of the word line dielectric layer is exposed by the third groove.

[0105] Referring to FIG. **4**M, the substrate **401** is etched by wet etching or dry etching by taking the second face **401-2** of the substrate **401** as the upper surface to form a third groove **413** until part of the word line dielectric layer **404** is exposed by the third groove **413**.

[0106] At S**3052**, the part of the word line dielectric layer exposed in the third groove is removed to expose the second conducting layer.

[0107] In some embodiments, after the third groove **413** is formed, the word line dielectric layer **404** exposed in the third groove **413** is removed until the second conducting layer **405** is exposed, as shown in FIG. **4**N.

[0108] At S**3053**, the third groove exposing the second conducting layer is filled to form the conducting plug electrically connected to the other end of the second conducting layer.

[0109] In some embodiments, the conducting plug can be formed in the third groove **413** by the following operations.

[0110] At S1, a liner and a buffer layer covering sequentially the surface of the third groove are formed.

[0111] At S2, part of the liner and part of the buffer layer covering the second conducting layer are removed to expose the second conducting layer.

[0112] At S3, a third conducting layer covering the buffer layer and the exposed second conducting layer is formed, in which the third conducting layer fills up the third groove.

[0113] Referring to FIG. **4**O to FIG. **4**Q, a liner **414** and a buffer layer **415** covering sequentially the surface of the third groove **413** may be formed by physical vapor deposition, chemical vapor deposition or atomic layer deposition. Then, part of the liner **414** and part the buffer layer **415** covering the second conducting layer **405** are removed to expose the second conducting layer **405**. Then, a third conducting layer **416** covering the buffer layer **415** and the exposed second conducting layer **405** is formed by physical vapor deposition, chemical vapor deposition or atomic layer deposition. The third conducting layer **416** fills up the remaining third groove **413**.

[0114] In some embodiments, the liner **414**, the buffer layer **415** and the third conducting layer **416** together constitute a conducting plug.

[0115] In some embodiments, the materials of the third conducting layer **416** and the second conducting layer **405** may be the same or different. The material of the third conducting layer **416** may include at least one of copper (Cu), titanium nitride (TiN), tantalum nitride (TaN), hafnium nitride (HfN), aluminum tantalum nitride (TaAlN), aluminum titanium nitride (TiAlN), or other materials.

[0116] According to the embodiments of the disclosure, the word line is formed by taking the first face of the substrate as an upper surface, the connecting layer connected to the first conducting layer is formed in the word line, the conducting plug is formed by taking the second face of the substrate as an upper surface, and the conducting plug is electrically connected to the first conducting layer via the word line and the connecting layer. In this way, according to the embodiments of the disclosure, an indirect connection between the conducting plug and the first conducting layer is realized via the buried word line in the substrate, so that the conducting plug does not penetrate through the whole semiconductor substrate and does not destroy the structure of the semiconductor substrate, thus improving the yield and performance of semiconductor devices.

[0117] In the several embodiments provided by the disclosure, it should be understood that the disclosed device and method may be implemented in a non-target way. The above-described device embodiments are only illustrative. For example, the division of the units is only a logical function division, and there may be other division modes in actual implementation, such as, multiple units or components may be combined or integrated into another system, or some features may be ignored or not be executed. In addition, the components shown or discussed are coupled, or directly coupled to each other.

[0118] The units described above as separate components may or may not be physically separate. The components shown as units may or may not be physical units. That is, they may be located in one place or distributed to multiple network units. Some or all of the units may be selected according to actual requirements to achieve the purposes of the solutions of the embodiments of the disclosure.

[0119] The above are only some embodiments of the disclosure, but the protection scope of the disclosure is not limited to this. Changes or replacements can be easily thought of by any person skilled in the art and such changes or replacements should be covered by the protection scope of the disclosure. Therefore, the protection scope of the disclosure should be subject to the protection scope of the claims.

[0120] In the method for forming a semiconductor device and the semiconductor device provided by embodiments of the disclosure, a word line is formed by taking a first face of a substrate as an upper surface, a connecting layer connected to a first conducting layer is formed in the word line, a conducting plug is formed by taking a second face of the substrate as an upper surface, and the conducting plug is electrically connected to the first conducting layer via the word line and the connecting layer. In this way, according to the embodiments of the disclosure, an indirect connection between the conducting plug and the first conducting layer is realized via the buried word line in the substrate, so that the conducting plug does not penetrate through the whole semiconductor substrate and does not destroy the structure of the semiconductor substrate, thus improving the yield and performance of semiconductor devices.

What is claimed is:

1. A method for forming a semiconductor device, comprising:

providing a substrate;

forming a word line in the substrate by taking a first face of the substrate as an upper surface;

forming a connecting layer electrically connected to one end of the word line in part of the substrate and on the substrate;

forming a first conducting layer on the connecting layer; and

forming a conducting plug in the substrate by taking a second face of the substrate as an upper surface, wherein the conducting plug is electrically connected to another end of the word line and electrically connected to the first conducting layer via the word line, and wherein the first face and the second face are two faces of the substrate opposite to each other in a thickness direction of the substrate.

2. The method according to claim **1**, wherein the substrate comprises at least an array region and a peripheral region;
wherein forming the word line in the substrate comprises:
forming the word line in both the array region and the peripheral region by taking the first face of the substrate as the upper surface; and
wherein forming the connecting layer electrically connected to one end of the word line in the part of the substrate and on the substrate comprises:
forming the connecting layer electrically connected to one end of the word line in the peripheral region.

3. The method according to claim **2**, wherein the word line is formed in the peripheral region by the following operations:
forming a first groove having a first thickness in the peripheral region;
forming a word line dielectric layer covering a sidewall of the first groove;
filling a second conducting layer in the first groove having the word line dielectric layer; and
etching back the second conducting layer to form the second conducting layer, a surface of which is lower than the first face of the substrate, to obtain the word line.

4. The method according to claim **3**, wherein the method further comprises:
forming an isolation layer on the word line, wherein a surface of the isolation layer is flush with the first face of the substrate.

5. The method according to claim **3**, wherein forming the connecting layer electrically connected to one end of the word line in the peripheral region comprises:
forming the connecting layer electrically connected to the second conducting layer in the peripheral region.

6. The method according to claim **4**, wherein a distance between a surface of the word line and the first face of the substrate is a second thickness; and
wherein forming the connecting layer electrically connected to one end of the word line in the peripheral region comprises:
forming a first dielectric layer on the isolation layer, the word line dielectric layer and the substrate;
forming a second groove penetrating through the first dielectric layer and the isolation layer and penetrating through part of the word line in its thickness direction, in the first dielectric layer, the isolation layer and the word line, wherein a thickness of the second groove is greater than a sum of the second thickness and a thickness of the first dielectric layer; and
filling the second groove to form the connecting layer electrically connected to one end of the word line.

7. The method according to claim **3**, wherein forming the conducting plug in the substrate comprises:
forming a third groove in the substrate by taking the second face of the substrate as the upper surface, wherein part of the word line dielectric layer is exposed by the third groove;
removing the part of the word line dielectric layer exposed in the third groove to expose the second conducting layer; and
filling the third groove exposing the second conducting layer to form the conducting plug electrically connected to another end of the second conducting layer.

8. The method according to claim **7**, wherein forming the conducting plug electrically connected to the other end of the second conducting layer comprises:
forming a liner and a buffer layer covering sequentially a surface of the third groove;
removing part of the liner and part of the buffer layer covering the second conducting layer to expose the second conducting layer; and
forming a third conducting layer covering the buffer layer and the exposed second conducting layer, wherein the third conducting layer fills up the third groove.

9. The method according to claim **1**, wherein forming the first conducting layer on a surface of the connecting layer comprises:
forming a second dielectric layer on a surface of the first dielectric layer having the connecting layer;
forming a fourth groove penetrating through the second dielectric layer, wherein the fourth groove exposes the connecting layer;
filling the fourth groove to form the first conducting layer, wherein the first conducting layer is electrically connected to the connecting layer.

10. The method according to claim **2**, wherein when forming the first conducting layer on a surface of the connecting layer, the method further comprises:
forming the first conducting layer in the array region, wherein the first conducting layer in the array region is electrically connected to a source or a drain in the array region.

11. A semiconductor device, comprising:
a substrate;
a word line located in the substrate, wherein the word line is close to a first face of the substrate;
a connecting layer located in part of the substrate and on the substrate and electrically connected to one end of the word line;
a first conducting layer located on the connecting layer;
a conducting plug located in the substrate and electrically connected to another end of the word line, wherein the conducting plug is electrically connected to the first conducting layer via the word line, and the conducting plug is close to a second face of the substrate, and wherein the first face and the second face are two faces of the substrate opposite to each other in a thickness direction of the substrate.

12. The semiconductor device according to claim **11**, wherein the substrate comprises at least an array region and a peripheral region;
the word line comprises the word line in the array region and the word line in the peripheral region, the connecting layer is located at the peripheral region, and the connecting layer is electrically connected to one end of the word line in the peripheral region.

13. The semiconductor device according to claim **11**, wherein the word line comprises:
a word line dielectric layer located on a surface of the substrate; and
a second conducting layer located on a surface of the word line dielectric layer, wherein a surface of the second conducting layer is lower than the first face of the substrate.

14. The semiconductor device according to claim **13**, further comprising:

an isolation layer located on the second conducting layer, wherein a surface of the isolation layer is flush with the first face of the substrate.

15. The semiconductor device according to claim **13**, wherein the conducting plug comprises:

a liner located on a surface of the substrate;

a buffer layer located on a surface of the liner;

a third conducting layer located on a surface of the buffer layer, wherein the third conducting layer is electrically connected to the second conducting layer.

16. The semiconductor device according to claim **14**, further comprising:

a dielectric layer located on the word line, the isolation layer and the substrate, wherein the first conducting layer and part of the connecting layer are located in the dielectric layer.

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