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(54) SEMICONDUCTOR DEVICE HAVING DOPED SEED LAYER AND METHOD OF MANUFACTURING THE SAME

(71) Applicant: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)

(72) Inventors: **Chi-Ming CHEN**, Zhubei City (TW); **Po-Chun LIU**, Hsinchu City (TW); **Chung-Yi YU**, Hsinchu (TW); **Chia-Shiung TSAI**, Hsinchu (TW); **Ru-Liang LEE**, Hsinchu (TW)

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(63) Continuation of application No. 17/074,952, filed on Oct. 20, 2020, now Pat. No. 11,721,752, which is a continuation of application No. 16/687,219, filed on Nov. 18, 2019, now Pat. No. 11,329,148, which is a continuation of application No. 14/158,157, filed on Jan. 17, 2014, now Pat. No. 10,483,386.

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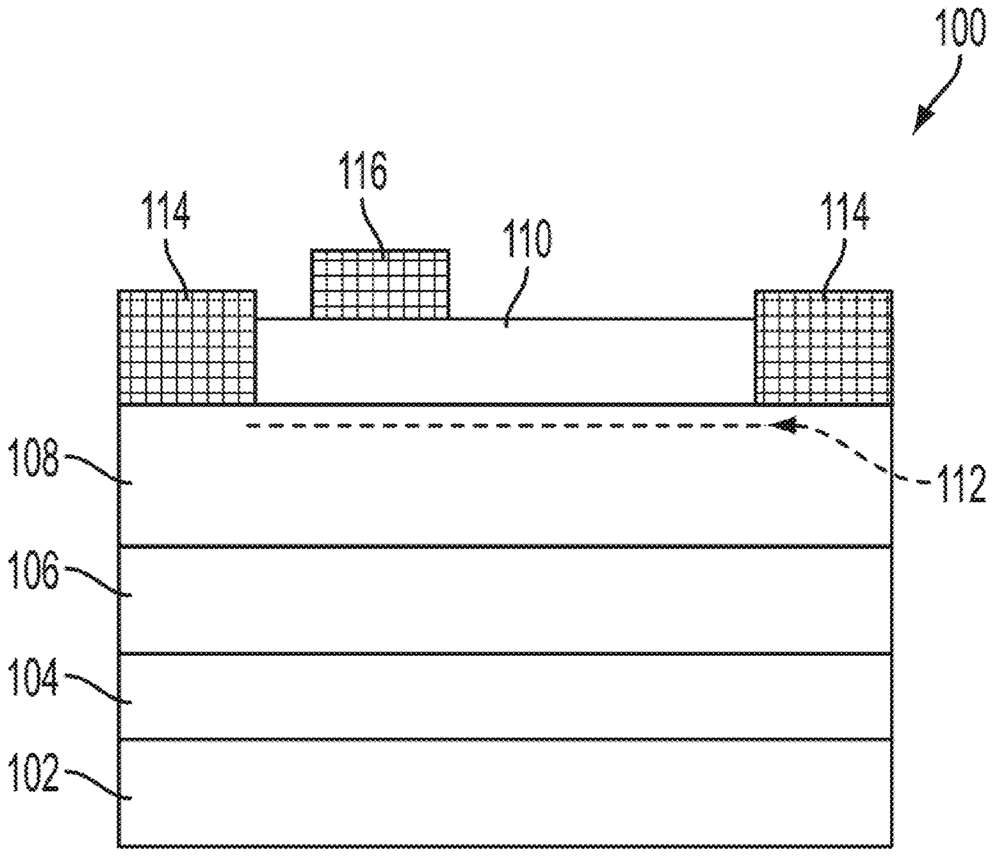
(57) ABSTRACT

A semiconductor device includes a substrate and a seed layer over the substrate. The seed layer includes a first seed sublayer having a first lattice structure, wherein the first seed sublayer includes AlN, and the first seed sublayer is doped with carbon, and a second seed sublayer over the first seed layer, wherein the second seed layer has a second lattice structure different from the first lattice structure, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm. The semiconductor device further includes a graded layer over the seed layer. The graded layer includes a first graded sublayer including AlGaN, having a first Al:Ga ratio; and a second graded sublayer over the first graded sublayer, wherein the second graded sublayer includes AlGaN having a second Al:Ga ratio. The semiconductor device further includes a two-dimensional electron gas (2-DEG) over the graded layer.



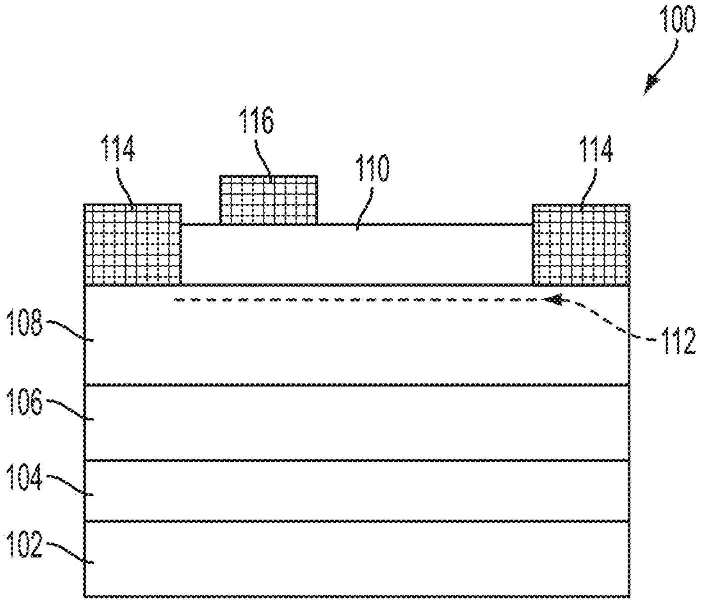


FIG. 1

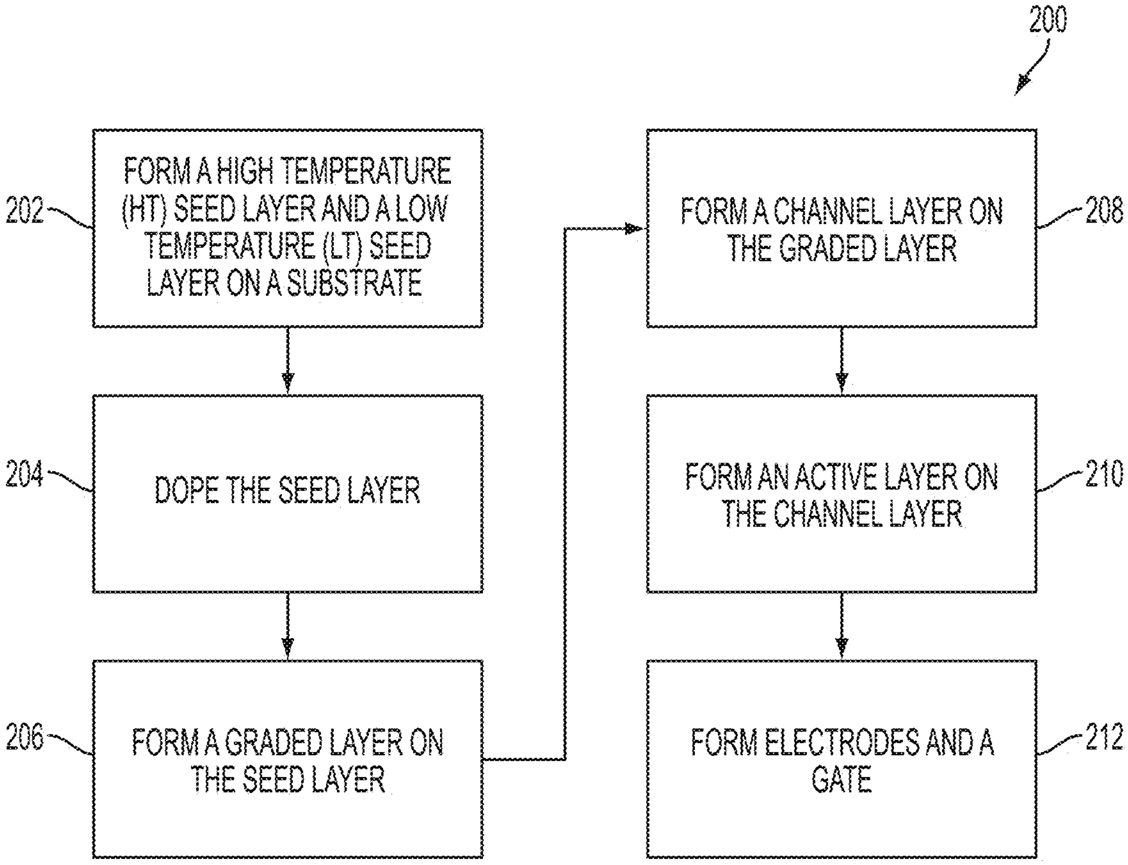

200
202
FORM A HIGH TEMPERATURE (HT) SEED LAYER AND A LOW TEMPERATURE (LT) SEED LAYER ON A SUBSTRATE
204
DOPE THE SEED LAYER
206
FORM A GRADED LAYER ON THE SEED LAYER
208
FORM A CHANNEL LAYER ON THE GRADED LAYER
210
FORM AN ACTIVE LAYER ON THE CHANNEL LAYER
212
FORM ELECTRODES AND A GATE

FIG. 2

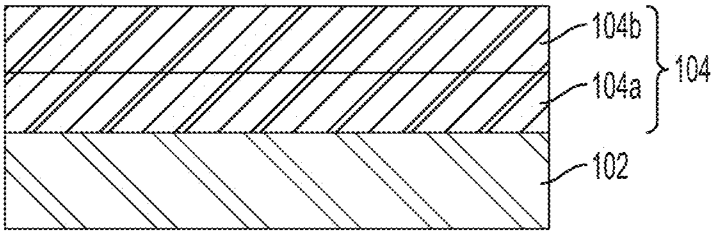


FIG. 3A

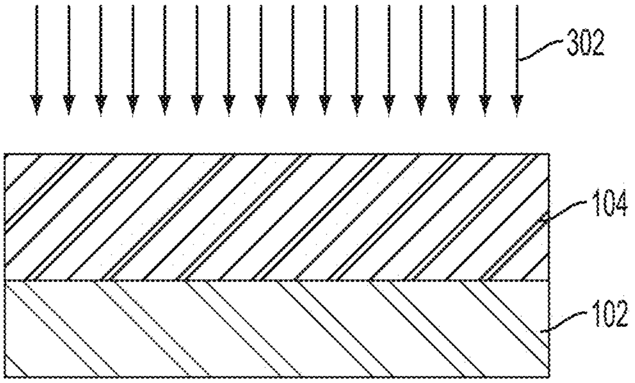


FIG. 3B

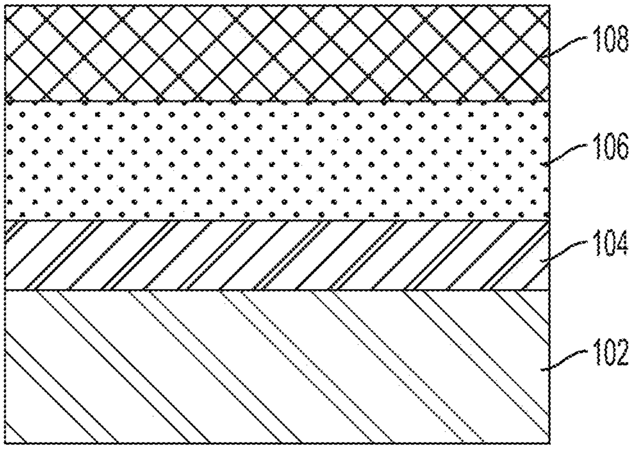


FIG. 3C

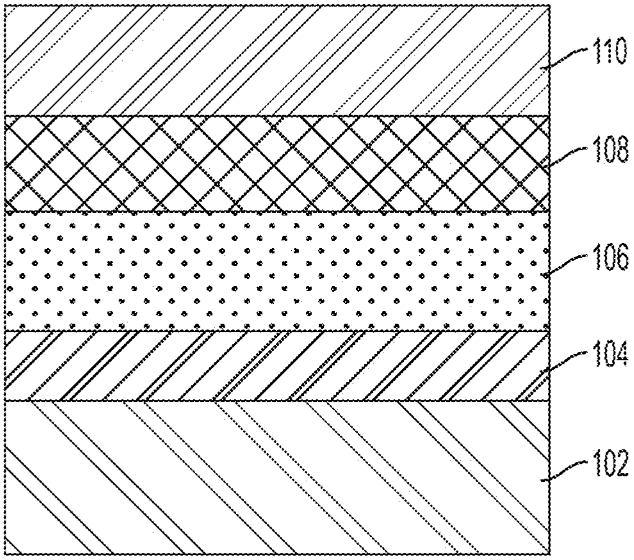


FIG. 3D

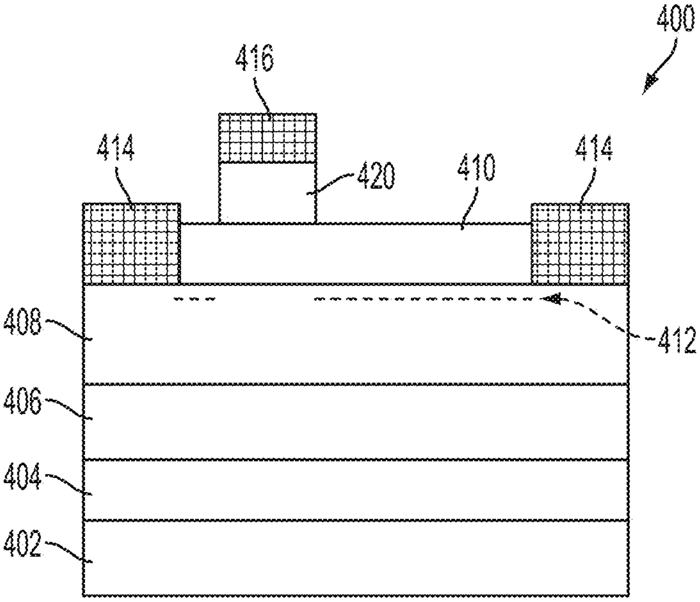


FIG. 4

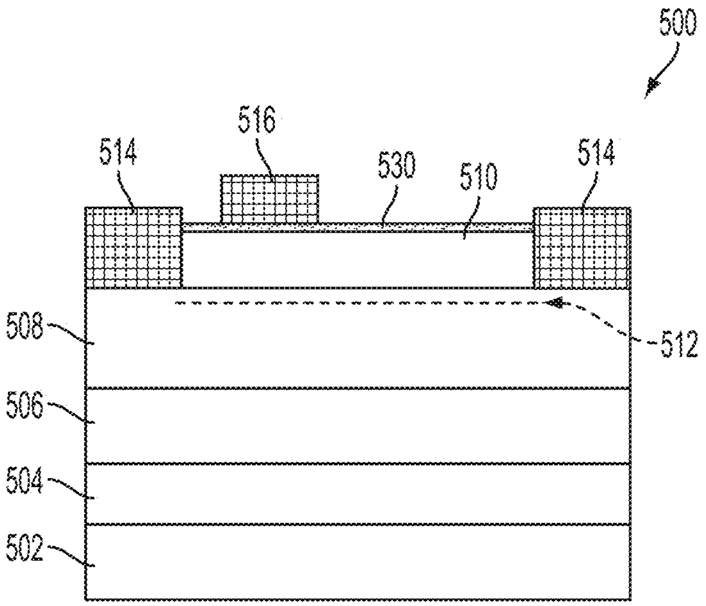


FIG. 5

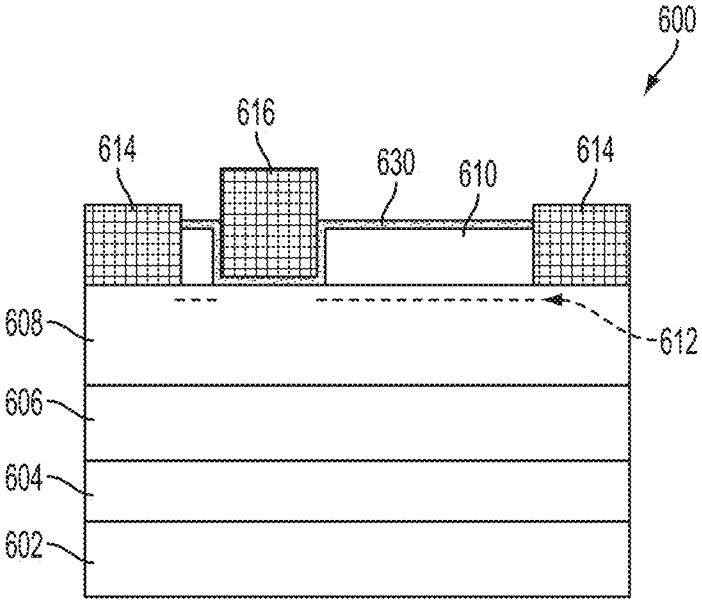


FIG. 6

SEMICONDUCTOR DEVICE HAVING DOPED SEED LAYER AND METHOD OF MANUFACTURING THE SAME

PRIORITY CLAIM

[0001] The present application is a continuation of U.S. application Ser. No. 17/074,952, filed Oct. 20, 2020, which is a continuation of U.S. application Ser. No. 16/687,219, filed Nov. 18, 2019, now U.S. Pat. No. 11,329,148, issued May 10, 2022, which is a continuation of U.S. application Ser. No. 14/158,157, filed Jan. 17, 2014, now U.S. Pat. No. 10,483,386, issued Nov. 19, 2019, which are incorporated herein by reference in their entireties.

RELATED APPLICATIONS

[0002] The instant application is related to the following U.S. patent applications:

[0003] U.S. patent application Ser. No. 13/944,713; filed Jul. 17, 2013, now U.S. Pat. No. 9,093,511, issued Jul. 25, 2015;

[0004] U.S. patent application Ser. No. 13/944,494, filed Jul. 17, 2013, now U.S. Pat. No. 8,901,609. Issued Dec. 2, 2014; and

[0005] U.S. patent application Ser. No. 13/944,625, filed Jul. 17, 2013, now U.S. Pat. No. 8,866,192, issued Oct. 21, 2014.

[0006] The entire contents of the above-referenced applications are incorporated by reference herein.

BACKGROUND

[0007] In semiconductor technology, Group III-Group V (or III-V) semiconductor compounds are used to form various integrated circuit devices, such as high power field-effect transistors, high frequency transistors, high electron mobility transistors (HEMTs), or metal-insulator-semiconductor field-effect transistors (MISFETs). A HEMT is a field effect transistor incorporating a junction between two materials with different band gaps (i.e., a heterojunction) as the channel instead of a doped region, as is generally the case for metal oxide semiconductor field effect transistors (MOSFETs). In contrast with MOSFETs, HEMTs have a number of attractive properties including high electron mobility and the ability to transmit signals at high frequencies, etc.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] One or more embodiments are illustrated by way of example, and not by limitation, in the figures of the accompanying drawings, wherein elements having the same reference numeral designations represent like elements throughout. It is emphasized that, in accordance with standard practice in the industry various features may not be drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features in the drawings may be arbitrarily increased or reduced for clarity of discussion. The drawings, which are incorporated herein, include the following in which:

[0009] FIG. **1** is a cross-sectional view of a high electron mobility transistor (HEMT) in accordance with one or more embodiments;

[0010] FIG. **2** is a flow chart of a method of making an HEMT in accordance with one or more embodiments;

[0011] FIGS. **3**A-**3**D are cross-sectional view of a HEMT at various stages of production in accordance with one or more embodiments;

[0012] FIG. **4** is a cross-sectional view of an enhanced HEMT (E-HEMT) in accordance with one or more embodiments;

[0013] FIG. **5** is a cross-sectional view of a depletion metal-insulator-semiconductor field-effect transistor (D-MISFET) in accordance with one or more embodiments; and

[0014] FIG. **6** is a cross-sectional view of an enhanced metal-insulator-semiconductor field-effect transistor (E-MISFET) in accordance with one or more embodiments.

DETAILED DESCRIPTION

[0015] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are examples and are not intended to be limiting.

[0016] FIG. **1** is a cross-sectional view of a high electron mobility transistor (HEMT) **100** in accordance with one or more embodiments. HEMT **100** includes a substrate **102**. A seed layer **104** is over substrate **102**. In some embodiments, seed layer **104** includes multiple layers. A graded layer **106** is over seed layer **104**. A channel layer **108** is over graded layer **106**. An active layer **110** is over channel layer **108**. Due to a band gap discontinuity between channel layer **108** and active layer **110**, a two dimension electron gas (2-DEG) **112** is formed in the channel layer near an interface with the active layer. Electrodes **114** are over channel layer **108** and a gate **116** is over active layer **110** between the electrodes.

[0017] Substrate **102** acts as a support for HEMT **100**. In some embodiments, substrate **102** is a silicon substrate. In some embodiments, substrate **102** includes silicon carbide (SiC), sapphire, or another suitable substrate material. In some embodiments, substrate **102** is a silicon substrate having a (111) lattice structure. In some embodiments, substrate **102** is doped.

[0018] In some embodiments, substrate **102** is doped with p-type dopants. In some embodiments, the p-type dopants include boron, aluminum, gallium, indium, titanium, boron di-fluoride, combinations thereof, or other suitable p-type dopants. The dopant concentration ranges from about 1×10^{18} ions/cm^3 to about 1×10^{23} ions/cm^3. In some embodiments, the p-type dopants are implanted using an ion implantation process to implant dopants directly into substrate **102**. In some embodiments, the p-type dopants are introduced using a plasma enhanced chemical vapor etching (PECVE) process, a reactive ion etching (RIE) process, an ion implantation (IMP) or another suitable material removal process to remove a top portion of substrate **102** and then a doped layer is grown over the remaining portion of the substrate. In some embodiments, an anneal process is performed following the introduction of the p-type dopants. In some embodiments, the anneal process is performed at a temperature ranging from about 900° C. to about 1100° C., for a duration of up to 60 minutes.

[0019] The introduction of the p-type dopants helps to reduce a concentration of electrons present at a top surface of the substrate. The lower electron concentration enables a higher voltage to be applied to gate **116** without damaging HEMT **100**. As a result, HEMT **100** is able to be used in higher voltage applications in comparison with HEMTs which do not include substrate **102** having a doped top surface, as described above.

[0020] Seed layer **104** helps to compensate for a mismatch in lattice structures between substrate **102** and graded layer **106**. In some embodiments, seed layer **104** includes multiple layers. In some embodiments, seed layer **104** includes a same material formed at different temperatures. In some embodiments, seed layer **104** includes a step-wise change in lattice structure. In some embodiments, seed layer **104** includes a continuous change in lattice structure. In some embodiments, seed layer **104** is formed by epitaxially growing the seed layer on substrate **102**.

[0021] Seed layer **104** is doped with carbon. In some embodiments, a concentration of carbon dopants ranges from about 2×10^{17} atoms/cm^3 to about 1×10^{20} atoms/cm^3. In some embodiments, seed layer **104** is doped using an ion implantation process. In some embodiments, seed layer **104** is doped using an in-situ doping process. In some embodiments, seed layer **104** is formed using molecular oriented chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), atomic layer deposition (ALD), physical vapor deposition (PVD) or another suitable formation process. In some embodiments, the in-situ doping process includes introducing the carbon dopants during formation of seed layer **104**. In some embodiments, a source of the carbon dopants includes a hydrocarbon (C_cH_y) such as CH_4, C_7H_7, $C_{16}H_{10}$, or another suitable hydrocarbon. In some embodiments, the source of the carbon dopants includes CBr_4, CCl_4, or another suitable carbon source.

[0022] Doping seed layer **104** with carbon helps to trap silicon atoms to help prevent the silicon atoms from substrate **102** from diffusing into graded layer **106**. By trapping the silicon atoms, an inversion current within HEMT **100** is reduced in comparison with HEMTs which do not include carbon in seed layer. The inversion current causes an HEMT to experience degradation in performance over time due to silicon diffusion into seed layer **104**. The carbon dopants occupy locations in a lattice structure of seed layer **104** which would enable silicon atoms to diffuse into the seed layer, thus reducing a number of available diffusion routes for silicon into the seed layer.

[0023] In at least one example, seed layer **104** includes a first layer of aluminum nitride (AlN) and a second layer of AlN over the first layer of AlN. The second layer of AlN is formed at a high temperature, ranging from about 1000° C. to about 1300° C., and has a thickness ranging from about 50 nanometers (nm) to about 200 nm. If the thickness of the first layer of AlN is too small, subsequent layers formed on the first layer of AlN will experience a high stress at the interface with the first AlN layer due to lattice mismatch increasing a risk of layer separation. If the thickness of the first layer of AlN is too great, the material is wasted and production costs increase. The first layer of AlN is formed at a low temperature, ranging from about 900° C. to about 1000° C., and has a thickness ranging from about 20 nm to about 80 nm. The lower temperature provides a different lattice structure in the second AlN layer in comparison with the first AlN layer. The lattice structure in the second AlN layer is more different from a lattice structure of substrate **102** than the first AlN layer. If the thickness of the second layer of AlN is too small, subsequent layers formed on the second layer of AlN will experience a high stress at the interface with the second layer of AlN due to lattice mismatch increasing the risk of layer separation. If the thickness of the second layer of AlN is too great, the material is wasted and production costs increase.

[0024] Graded layer **106** provides additional lattice matching between seed layer **104** and channel layer **108**. In some embodiments, graded layer **106** is doped with p-type dopants to reduce the risk of electron injection from substrate **102**. Electron injection occurs when electrons from substrate **102** diffuse into channel layer **108**. By including p-type dopants, the electrons are trapped by the positively charged dopants and do not negatively impact performance of 2-DEG **112** in channel layer **108**. In some embodiments, the p-type dopant concentration in graded layer **106** is greater than or equal to 1×10^{17} ions/cm^3. In some embodiments, the p-type dopants include carbon, iron, magnesium, zinc or other suitable p-type dopants. In some embodiments, graded layer **106** includes aluminum gallium nitride ($Al_xGa_{1-x}N$), where x is the aluminum content ratio in the graded layer. In some embodiments, the graded layer includes multiple layers each having a decreased ratio x (from a layer adjoining seed layer **104** to a layer that adjoins SLS **108**, or from the bottom to the top portions of the graded layer). In some embodiments, graded layer has a thickness ranging from about 550 nm to about 1050 nm. If graded layer **106** is too thin, electrons from substrate **102** will be injected into channel layer **110** at high voltages, negatively impacting 2-DEG **112** or a lattice mismatch between seed layer **104** and channel layer **108** will result in a high stress in the channel layer and increase a risk of layer separation. If graded layer **106** is too thick, material is wasted and production costs increase. In some embodiments, the graded layer is formed at a temperature ranging from about 1000° C. to about 1200° C. In some embodiments, a p-type dopant concentration of graded layer **106** increases from a bottom of the graded layer to a top of the graded layer.

[0025] In at least one example, graded layer **106** includes three graded layers. A first graded layer adjoins seed layer **104**. The first graded layer includes $Al_xGa_{1-x}N$, where x ranges from about 0.7 to about 0.9. A thickness of the first graded layer ranges from about 50 nm to about 200 nm. A second graded layer is on the first graded layer. The second graded layer includes $Al_xGa_{1-x}N$, where x ranges from about 0.4 to about 0.6. A thickness of the second graded layer ranges from about 150 nm to about 250 nm. A third graded layer is on the second graded layer. The third graded layer includes $Al_xGa_{1-x}N$, where x ranges from about 0.15 to about 0.3. A thickness of the third graded layer ranges from about 350 nm to about 600 nm.

[0026] Channel layer **108** is used to help form a conductive path for selectively connecting electrodes **114**. In some embodiments, channel layer **108** has a dopant concentration of p-type dopants of less than or equal to 1×10^{17} ions/cm^3. In some embodiments, channel layer **108** includes undoped GaN. In some embodiments, channel layer **108** has a thickness ranging from about 0.5 μm to about 5.0 μm. If a thickness of channel layer **108** is too thin, the channel layer will not provide sufficient charge carriers to allow HEMT **100** to function properly. If the thickness of channel layer **108** is too great, material is wasted and production costs increase. In some embodiments, channel layer **108** is formed by an epitaxial process. In some embodiments, channel layer **108** is formed at a temperature ranging from about 1000° C. to about 1200° C.

[0027] Active layer **110** is used to provide the band gap discontinuity with channel layer **108** to form 2-DEG **112**. In some embodiments, active layer **110** includes AlN. In some embodiments, active layer **110** includes a mixed structure, e.g., $Al_xGa_{1-x}N$, where x ranges from about 0.1 to 0.3. In some embodiments where active layer **110** includes an AlN layer and a mixed structure layer, a thickness of the AlN layer ranges from about 0.5 nm to about 1.5 nm. If active layer **110** is too thick, selectively controlling the conductivity of the channel layer is difficult. If active layer **110** is too thin, an insufficient amount of electrons are available for 2-DEG **112**. In some embodiments, active layer **110** is formed using an epitaxial process. In some embodiments, active layer **110** is formed at a temperature ranging from about 1000° C. to about 1200° C.

[0028] 2-DEG **112** acts as the channel for providing conductivity between electrodes **114**. Electrons from a piezoelectric effect in active layer **110** drop into channel layer **108**, and thus create a thin layer of highly mobile conducting electrons in the channel layer.

[0029] Electrodes **114** act as a source and a drain for HEMT **100** for transferring a signal into or out of the HEMT. Gate **116** helps to modulate conductivity of 2-DEG **112** for transferring the signal between electrodes **114**.

[0030] HEMT **100** is normally conductive meaning that a positive voltage applied to gate **116** will reduce the conductivity between electrodes **114** along 2-DEG **112**.

[0031] FIG. **2** is a flow chart of a method **200** of making an HEMT in accordance with one or more embodiments. Method **200** begins with operation **202** in which a low temperature (LT) seed layer and a high temperature (HT) seed layer are formed on a substrate, e.g., substrate **102**. The LT seed layer is formed on the substrate and the HT seed layer is formed on the LT seed layer.

[0032] In some embodiments, LT seed layer and HT seed layer include AlN. In some embodiments, the formation of LT seed layer and HT seed layer are performed by an epitaxial growth process. In some embodiments, the epitaxial growth process includes a metal-organic chemical vapor deposition (MOCVD) process, a molecular beam epitaxy (MBE) process, a hydride vapor phase epitaxy (HVPE) process or another suitable epitaxial process. In some embodiments, the MOCVD process is performed using aluminum-containing precursor and nitrogen-containing precursor. In some embodiments, the aluminum-containing precursor includes trimethylaluminium (TMA), triethylaluminium (TEA), or other suitable chemical. In some embodiments, the nitrogen-containing precursor includes ammonia, tertiarybutylamine (TBAm), phenyl hydrazine, or other suitable chemical. In some embodiments, the LT seed layer or the HT seed layer includes a material other than AlN. In some embodiments, the HT seed layer has a thickness ranging from about 50 nm to about 200 nm. In some embodiments, the HT seed layer is formed at a temperature ranging from about 1000° C. to about 1300° C. In some embodiments, the LT seed layer has a thickness ranging from about 20 nm to about 80 nm. In some embodiments, the LT seed layer is formed at a temperature ranging from about 900° C. to about 1000° C.

[0033] FIG. **3**A is a cross-sectional view of a HEMT following operation **202**. The HEMT includes seed layer **104** on substrate **102**. Seed layer **104** includes a HT seed layer **104***a* on substrate **102** and a LT seed layer **104***b* on the HT seed layer.

[0034] In operation **204**, the seed layer is doped with carbon. In some embodiments, the seed layer is doped to a carbon dopant concentration ranging from about 2×10^{17} atoms/cm^3 to about 1×10^{20} atoms/cm^3. In some embodiments, the seed layer is doped using ion implantation process. In some embodiments, the ion implantation process is performed at an implantation energy ranging from about 30 kilo-electron volts (KeV) to about 150 (KeV). In some embodiments, the ion implantation process is performed using an implantation angle ranging from about 5-degrees to about 10-degrees. In some embodiments, the seed layer is doped using an in-situ doping process. In some embodiments, operations **202** and **204** are combined into a single operation. In some embodiments, at least one layer of the seed layer is formed using MOCVD, MBE, ALD, PVD or another suitable formation process. In some embodiments, the in-situ doping process includes introducing the carbon dopants during formation of at least one layer of the seed layer. In some embodiments, the carbon dopants are introduced using a carbon source including a hydrocarbon (C_xH_y) such as CH_4, C_7H_7, $C_{16}H_{10}$, or another suitable hydrocarbon. In some embodiments, the carbon is introduced using an ion implantation process and a hydrocarbon as a carbon source. In some embodiments, the carbon dopants are introduced using a carbon source including a carbon halide, such as CBr_4, CCl_4, or another suitable carbon source. In some embodiments, the carbon is introduced using an in-situ process and a carbon halide as a carbon source.

[0035] FIG. **3**B is a cross-sectional view of a HEMT following operation **204**. The HEMT includes seed layer **104** on substrate **102**. Seed layer **104** is doped using a dopant process **302**. Dopant process **302** introduces carbon into seed layer **104**.

[0036] Returning to FIG. **2**, method **200** continues with operation **206** in which a graded layer is formed on the LT seed layer. In some embodiments, the graded layer includes an aluminum-gallium nitride ($Al_xGa_{1-x}N$) layer. In some embodiments, the graded aluminum gallium nitride layer has two or more aluminum-gallium nitride layers each having a different ratio x decreased from the bottom to the top. In some embodiments, each of the two or more aluminum-gallium nitride layers is formed by performing an epitaxial process. In some embodiments, the epitaxial process includes a MOCVD process, an MBE process, a HVPE process or another suitable epitaxial process. In some embodiments, the MOCVD process uses an aluminum-containing precursor, a gallium-containing precursor, and a nitrogen-containing precursor. In some embodiments, the aluminum-containing precursor includes TMA, TEA, or other suitable chemical. In some embodiments, the gallium-containing precursor includes trimethylgallium (TMG), triethylgallium (TEG), or other suitable chemical. In some embodiments, the nitrogen-containing precursor includes ammonia, TBAm, phenyl hydrazine, or other suitable chemical. In some embodiments, the graded aluminum gallium nitride layer has a continuous gradient of the ratio x gradually decreased from the bottom to the top. In some embodiments, x ranges from about 0.5 to about 0.9. In some embodiments, the graded layer is formed at a temperature ranging from about 1000° C. to about 1200° C. In some embodiments, the graded layer is doped with p-type dopants, such as carbon, iron, magnesium, zinc or other suitable p-type dopants.

[0037] In at least one embodiment, a first graded layer is formed on the LT seed layer. The first graded layer adjoins seed layer **104**. The first graded layer includes $Al_xGa_{1-x}N$, where x ranges from about 0.7 to about 0.9. A thickness of the first graded layer ranges from about 50 nm to about 200 nm. In some embodiments, the first graded layer is formed using epitaxy. In some embodiments, the first graded layer is formed at a temperature ranging from about 1000° C. to about 1200° C. A second graded layer is formed on the first graded layer. The second graded layer includes $Al_xGa_{1-x}N$, where x ranges from about 0.4 to about 0.6. A thickness of the second graded layer ranges from about 150 nm to about 250 nm. In some embodiments, the second graded layer is formed using epitaxy. In some embodiments, the second graded layer is formed at a temperature ranging from about 1000° C. to about 1200° C. A third graded layer is formed on the second graded layer. The third graded layer includes $Al_xGa_{1-x}N$, where x ranges from about 0.15 to about 0.3. A thickness of the third graded layer ranges from about 350 nm to about 600 nm. In some embodiments, the third graded layer is formed using epitaxy. In some embodiments, the third graded layer is formed at a temperature ranging from about 1000° C. to about 1200° C.

[0038] In operation **208**, a channel layer is formed on the graded layer. In some embodiments, the channel layer includes p-type dopants. In some embodiments, the channel layer includes GaN, and the P-type doping is implemented by using dopants including carbon, iron, magnesium, zinc or other suitable p-type dopants. In some embodiments, the channel layer is formed by performing an epitaxial process. In some embodiments, the epitaxial process includes a MOCVD process, an MBE process, a HVPE process or another suitable epitaxial process. In some embodiments, the channel layer has a thickness ranging from about 0.2 μm to about 1.0 μm. In some embodiments, the dopant concentration in the channel layer is equal to or less than about 1×10^{17} ions/cm^3. In some embodiments, the channel layer is undoped. In some embodiments, the channel layer is formed at a temperature ranging from about 1000° C. to about 1200° C.

[0039] FIG. **3**C is a cross-sectional view of a HEMT following operation **208**. The HEMT includes graded layer **106** on seed layer **104**. For the sake of simplicity, seed layer **104** and graded layer **106** are shown as single layers in the remaining cross-sectional views. Channel layer **108** is also on graded layer **106**.

[0040] Returning to FIG. **2**, in operation **210** an active layer is formed on the channel layer. In some embodiments, the active layer includes AlN, $Al_xGa_{1-x}N$, combinations thereof or other suitable materials. In some embodiments, x ranges from about 0.1 to about 0.3. In some embodiments, the active layer is formed by performing an epitaxial process. In some embodiments, the epitaxial process includes a MOCVD process, an MBE process, a HVPE process or another suitable epitaxial process. In some embodiments, the active layer has a thickness ranging from about 10 nm to about 40 nm. In some embodiments where the active layer includes both AlN and $Al_xGa_{1-x}N$, the AlN layer has a thickness ranging from about 0.5 nm to about 1.5 nm and the $Al_xGa_{1-x}N$ layer has a thickness ranging from about 10 nm to about 40 nm. In some embodiments, the active layer is formed at a temperature ranging from about 1000° C. to about 1200° C.

[0041] FIG. **3**D is a cross-sectional view of the HEMT following operation **210** in accordance with one or more embodiments. The HEMT includes active layer **110** on channel layer **108**. 2-DEG **112** is formed in channel layer **108** due to the band gap discontinuity between active layer **110** and the channel layer.

[0042] Returning to FIG. **2**, in operation **212** electrodes and a gate are formed on the active layer. The electrodes are formed over the other portion of the channel layer, and the gate is formed over the active layer. In some embodiments, a patterned mask layer (i.e., a photoresistive layer) is formed on the upper surface of the active layer, and an etching process is performed to remove a portion of the active layer to form openings partially exposing an upper surface of the other portion of the channel layer. A metal layer is then deposited over the patterned active layer and fills the openings and contacts the other portion of the channel layer. Another patterned photoresist layer is formed over the metal layer, and the metal layer is etched to form the electrodes over the openings and the gate over the upper surface of the active layer. In some embodiments, the metal layer for forming the electrodes or the gate includes one or more conductive materials. In some embodiments, the electrodes or the gate include one or more layers of conductive materials. In at least one embodiment, the electrodes or the gate include at least one barrier layer contacting the other portion of the channel layer and/or the active layer.

[0043] Following operation **212**, the HEMT has a structure similar to HEMT **100**.

[0044] FIG. **4** is a cross-sectional view of an enhanced HEMT (E-HEMT) **400** in accordance with one or more embodiments. E-HEMT **400** is similar to HEMT **100**. Similar elements have a same reference number as HEMT **100** increased by 300. In comparison with HEMT **100**, E-HEMT **400** includes a semiconductor material **420** between gate **416** and active layer **410**. In some embodiments, semiconductor material **420** is a group III-V semiconductor material such as GaN, AlGaN, InGaN, or another suitable group III-V semiconductor material. In some embodiments, semiconductor material **420** is doped with p-type or n-type dopants. In some embodiments, the p-type dopants include carbon, iron, magnesium, zinc or other suitable p-type dopants. In some embodiments, the n-type dopants include silicon, oxygen or other suitable n-type dopants. In comparison with HEMT **100**, E-HEMT **400** is normally non-conductive between electrodes **414**. As a positive voltage is applied to gate **416**, E-HEMT **400** provides an increased conductivity between electrodes **414**.

[0045] FIG. **5** is a cross-sectional view of a depletion metal-insulator-semiconductor field-effect transistor (D-MISFET) **500** in accordance with one or more embodiments. D-MISFET **500** is similar to HEMT **100**. Similar elements have a same reference number as HEMT **100** increased by 400. In comparison with HEMT **100**, D-MISFET **500** includes a dielectric layer **530** between gate **516** and active layer **510**. In some embodiments, dielectric layer **530** includes silicon dioxide. In some embodiments, dielectric layer **530** includes a high-k dielectric layer having a dielectric constant greater than a dielectric constant of silicon dioxide. Similar to HEMT **100**, D-MISFET **500** is normally conductive between electrodes **514**. As a positive voltage is applied to gate **516**, D-MISFET **500** provides a decreased conductivity between electrodes **514**.

[0046] FIG. **6** is a cross-sectional view of an enhanced metal-insulator-semiconductor field-effect transistor (E-MISFET) **600** in accordance with one or more embodiments. E-MISFET **600** is similar to HEMT **100**. Similar elements have a same reference number as HEMT **100** increased by 500. In comparison with HEMT **100**, E-MISFET **600** gate **616** is in contact with channel layer **608** without intervening active layer **610**. E-MISFET **600** further includes a dielectric layer **630** between gate **616** and channel layer **608**. Dielectric layer **630** also separates sidewalls of gate **616** and active layer **610**. In some embodiments, dielectric layer **630** includes silicon dioxide. In some embodiments, dielectric layer **630** includes a high-k dielectric layer having a dielectric constant greater than a dielectric constant of silicon dioxide. In comparison with HEMT **100**, E-MISFET **600** is normally non-conductive between electrodes **614**. As a positive voltage is applied to gate **616**, E-MISFET **600** provides an increased conductivity between electrodes **614**.

[0047] An aspect of this description relates to a semiconductor device. The semiconductor device includes a doped substrate. The semiconductor device further includes a seed layer in direct contact with the substrate. The seed layer further includes a first seed sublayer having a first lattice structure, wherein the first seed layer comprises AlN, and the first seed layer is doped with carbon. The seed layer further includes a second seed sublayer over the first seed layer, wherein the second seed layer has a second lattice structure different from the first lattice structure. The semiconductor device further includes a graded layer in direct contact with the seed layer. The graded layer includes a first graded sublayer including AlGaN, wherein the first graded sublayer has a first Al:Ga ratio; a second graded sublayer over the first graded sublayer, wherein the second graded sublayer includes AlGaN, and the second graded sublayer has a second Al:Ga ratio different from the first Al:Ga ratio; and a third graded sublayer over the second graded sublayer, wherein the third graded sub layer includes AlGaN, and the third graded sublayer has a third Al:Ga ratio different from the second Al:Ga ratio. The semiconductor device further includes a channel layer over the graded layer, wherein a two-dimensional electron gas (2-DEG) is defined in the channel layer. The semiconductor device further includes an active layer over the channel layer. In some embodiments, the semiconductor device further includes a gate over the active layer. In some embodiments, the semiconductor device further includes a source electrode in direct contact with the channel layer. In some embodiments, the semiconductor device further includes a drain electrode in direct contact with the channel layer. In some embodiments, the semiconductor device further includes a dielectric layer over the active layer. In some embodiments, the dielectric layer covers an entirety of a topmost surface of the active layer. In some embodiments, the dielectric layer directly contacts the active layer. In some embodiments, the dielectric layer includes silicon dioxide. In some embodiments, the semiconductor device further includes a source electrode, wherein the active layer directly contacts a sidewall of the source electrode; and a drain electrode, wherein the active layer directly contacts a sidewall of the drain electrode.

[0048] An aspect of this description relates to a semiconductor device. The semiconductor device includes a substrate. The semiconductor device includes a seed layer in direct contact with the substrate. The seed layer includes a first seed sublayer having a first lattice structure, wherein the first seed sublayer comprises AlN, and the first seed sublayer is doped with carbon, and a second seed sublayer over the first seed layer, wherein the second seed layer has a second lattice structure different from the first lattice structure, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm. The semiconductor device further includes a graded layer in direct contact with the seed layer. The graded layer includes a first graded sublayer including AlGaN, wherein the first graded sublayer has a first Al:Ga ratio; and a second graded sublayer over the first graded sublayer, wherein the second graded sublayer includes AlGaN, and the second graded sublayer has a second Al:Ga ratio different from the first Al:Ga ratio. The semiconductor device further includes a two-dimensional electron gas (2-DEG) over the graded layer. In some embodiments, the semiconductor device further includes a source electrode; a drain electrode; and a gate, wherein the source electrode is closer to the 2-DEG than the gate. In some embodiments, the semiconductor device further includes a semiconductor layer between the gate and the 2-DEG. In some embodiments, the semiconductor device further includes a dielectric layer between the gate and the 2-DEG. In some embodiments, the dielectric layer contacts a sidewall of the gate. In some embodiments, the 2-DEG is a normally conductive 2-DEG. In some embodiments, the 2-DEG is a normally non-conductive 2-DEG.

[0049] An aspect of this description relates to a method of making a semiconductor device. The method includes growing a first seed sublayer over a substrate, wherein the first seed sublayer comprises AlN. The method further includes doping the first seed sublayer with carbon. The method further includes growing a second seed sublayer over the doped first seed sublayer, wherein the second seed sublayer comprises AlN, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm. The method further includes growing a first graded sublayer over the second seed sublayer, wherein the first graded sublayer comprises AlGaN, and the first graded sublayer has a first Al:Ga ratio. The method further includes growing a second graded sublayer over the first graded sublayer, wherein the second graded sublayer includes AlGaN, and the second graded sublayer has a second Al:Ga ratio different from the first Al:Ga ratio. The method further includes forming a two-dimensional electron gas (2-DEG) over the second graded sublayer. In some embodiments, the method further includes forming a gate over the 2-DEG. In some embodiments, forming the gate causes the 2-DEG to be a normally conductive 2-DEG. In some embodiments, forming the gate causes the 2-DEG to be a normally non-conductive 2-DEG. In some embodiments, the method further includes forming a semiconductor layer over the 2-DEG, wherein forming the gate comprises forming the gate over the semiconductor layer. In some embodiments, the method further includes forming a dielectric layer over the 2-DEG, wherein forming the gate comprises forming the gate over the dielectric layer. In some embodiments, forming the gate includes forming the gate having a sidewall in contact with the dielectric layer. In some embodiments, doping the first seed sublayer with carbon includes doping the first seed sublayer using a carbon source selected from the group consisting of at least one of CH_4, C_7H_7, $C_{16}H_{10}$, CBr_4, and CC_{l4}. In some embodiments, doping the first seed sublayer with carbon includes performing an in-situ doping during the growing of the first seed sublayer.

[0050] An aspect of this description relates to a semiconductor device. The semiconductor device includes a substrate. The semiconductor device further includes a seed layer in direct contact with the substrate. The seed layer includes a first seed sublayer having a first lattice structure, wherein the first seed sublayer comprises AlN, and the first seed sublayer is doped with carbon, and a second seed sublayer over the first seed layer, wherein the second seed layer has a second lattice structure different from the first lattice structure, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm. The semiconductor device further includes a graded layer in direct contact with the seed layer, wherein the graded layer comprises a plurality of layers of AlGaN, wherein each of the plurality of layers of AlGaN has a different Al:Ga ratio for each other of the plurality of layer of AlGaN. The semiconductor device further includes a selectively conductive two-dimensional electron gas (2-DEG) over the graded layer. In some embodiments, a dopant concentration of the carbon ranges from 2×10^{17} atoms/cm^3 to about 1×10^{20} atoms/cm^3. In some embodiments, the semiconductor device further includes a semiconductor layer over the selectively conductive 2-DEG; and a gate over the semiconductor layer. In some embodiments, the semiconductor device further includes a dielectric layer over the selectively conductive 2-DEG; and a gate over the dielectric layer.

[0051] It will be readily seen by one of ordinary skill in the art that the disclosed embodiments fulfill one or more of the advantages set forth above. After reading the foregoing specification, one of ordinary skill will be able to affect various changes, substitutions of equivalents and various other embodiments as broadly disclosed herein. It is therefore intended that the protection granted hereon be limited only by the definition contained in the appended claims and equivalents thereof.

What is claimed is:

1. A semiconductor device comprising:
a substrate;
a seed layer in direct contact with the substrate, wherein the seed layer comprises:
  a first seed sublayer having a first lattice structure, wherein the first seed sublayer comprises AlN, and the first seed sublayer is doped with carbon, and
  a second seed sublayer over the first seed sublayer, wherein the second seed sublayer has a second lattice structure different from the first lattice structure, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm;
a graded layer in direct contact with the seed layer, wherein the graded layer comprises:
  a first graded sublayer including AlGaN, wherein the first graded sublayer has a first Al:Ga ratio; and
  a second graded sublayer over the first graded sublayer, wherein the second graded sublayer includes AlGaN, and the second graded sublayer has a second Al:Ga ratio different from the first Al:Ga ratio; and
a two-dimensional electron gas (2-DEG) over the graded layer.

2. The semiconductor device of claim **1**, further comprising:
a source electrode;
a drain electrode; and
a gate, wherein the source electrode is closer to the 2-DEG than the gate.

3. The semiconductor device of claim **2**, further comprising a semiconductor layer between the gate and the 2-DEG.

4. The semiconductor device of claim **2**, further comprising a dielectric layer between the gate and the 2-DEG.

5. The semiconductor device of claim **4**, wherein the dielectric layer contacts a sidewall of the gate.

6. The semiconductor device of claim **1**, wherein the 2-DEG is a normally conductive 2-DEG.

7. The semiconductor device of claim **1**, wherein the 2-DEG is a normally non-conductive 2-DEG.

8. A method of making a semiconductor device, the method comprising:
growing a first seed sublayer over a substrate, wherein the first seed sublayer comprises AlN;
doping the first seed sublayer with carbon;
growing a second seed sublayer over the doped first seed sublayer, wherein the second seed sublayer comprises AlN, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm;
growing a first graded sublayer over the second seed sublayer, wherein the first graded sublayer comprises AlGaN, and the first graded sublayer has a first Al:Ga ratio;
growing a second graded sublayer over the first graded sublayer, wherein the second graded sublayer comprises AlGaN, and the second graded sublayer has a second Al:Ga ratio different from the first Al:Ga ratio; and
forming a two-dimensional electron gas (2-DEG) over the second graded sublayer.

9. The method of claim **8**, further comprising forming a gate over the 2-DEG.

10. The method of claim **9**, wherein forming the gate comprises causing the 2-DEG to be a normally conductive 2-DEG.

11. The method of claim **9**, wherein forming the gate comprises causing the 2-DEG to be a normally non-conductive 2-DEG.

12. The method of claim **9**, further comprising forming a semiconductor layer over the 2-DEG, wherein forming the gate comprises forming the gate over the semiconductor layer.

13. The method of claim **9**, further comprising forming a dielectric layer over the 2-DEG, wherein forming the gate comprises forming the gate over the dielectric layer.

14. The method of claim **13**, wherein forming the gate comprises forming the gate having a sidewall in contact with the dielectric layer.

15. The method of claim **8**, wherein doping the first seed sublayer with carbon comprises doping the first seed sublayer using a carbon source selected from the group consisting of at least one of CH_4, C_7H_7, $C_{16}H_{10}$, CBr_4, and CC_{l4}.

16. The method of claim **8**, wherein doping the first seed sublayer with carbon comprises performing an in-situ doping during the growing of the first seed sublayer.

17. A semiconductor device comprising:

a substrate;

a seed layer in direct contact with the substrate, wherein the seed layer comprises:

a first seed sublayer having a first lattice structure, wherein the first seed sublayer comprises AlN, and the first seed sublayer is doped with carbon, and

a second seed sublayer over the first seed sublayer, wherein the second seed sublayer has a second lattice structure different from the first lattice structure, and a thickness of the second seed sublayer ranges from about 50 nanometers (nm) to about 200 nm;

a graded layer in direct contact with the seed layer, wherein the graded layer comprises a plurality of layers of AlGaN, wherein each of the plurality of layers of AlGaN has a different Al:Ga ratio for each other of the plurality of layer of AlGaN; and

a selectively conductive two-dimensional electron gas (2-DEG) over the graded layer.

18. The semiconductor device of claim **17**, wherein a dopant concentration of the carbon ranges from 2×10^{17} atoms/cm^3 to about 1×10^{20} atoms/cm^3.

19. The semiconductor device of claim **17**, further comprising:

a semiconductor layer over the selectively conductive 2-DEG; and

a gate over the semiconductor layer.

20. The semiconductor device of claim **17**, further comprising:

a dielectric layer over the selectively conductive 2-DEG; and

a gate over the dielectric layer.

* * * * *