US 20240195306A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2024/0195306 A1**

Lidsky (43) **Pub. Date: Jun. 13, 2024**

(54) **DEEPLY INTEGRATED VOLTAGE REGULATOR ARCHITECTURES**

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(21) Appl. No.: **18/471,973**

(22) Filed: **Sep. 21, 2023**

Related U.S. Application Data

(63) Continuation of application No. 18/163,820, filed on Feb. 2, 2023, now Pat. No. 11,799,377, which is a continuation of application No. 17/811,042, filed on Jul. 6, 2022, now Pat. No. 11,601,059, which is a continuation of application No. 17/208,851, filed on Mar. 22, 2021, now Pat. No. 11,418,120, which is a continuation of application No. 16/727,909, filed on Dec. 26, 2019, now Pat. No. 10,958,172.

(60) Provisional application No. 62/785,143, filed on Dec. 26, 2018.

Publication Classification

(51) **Int. Cl.**

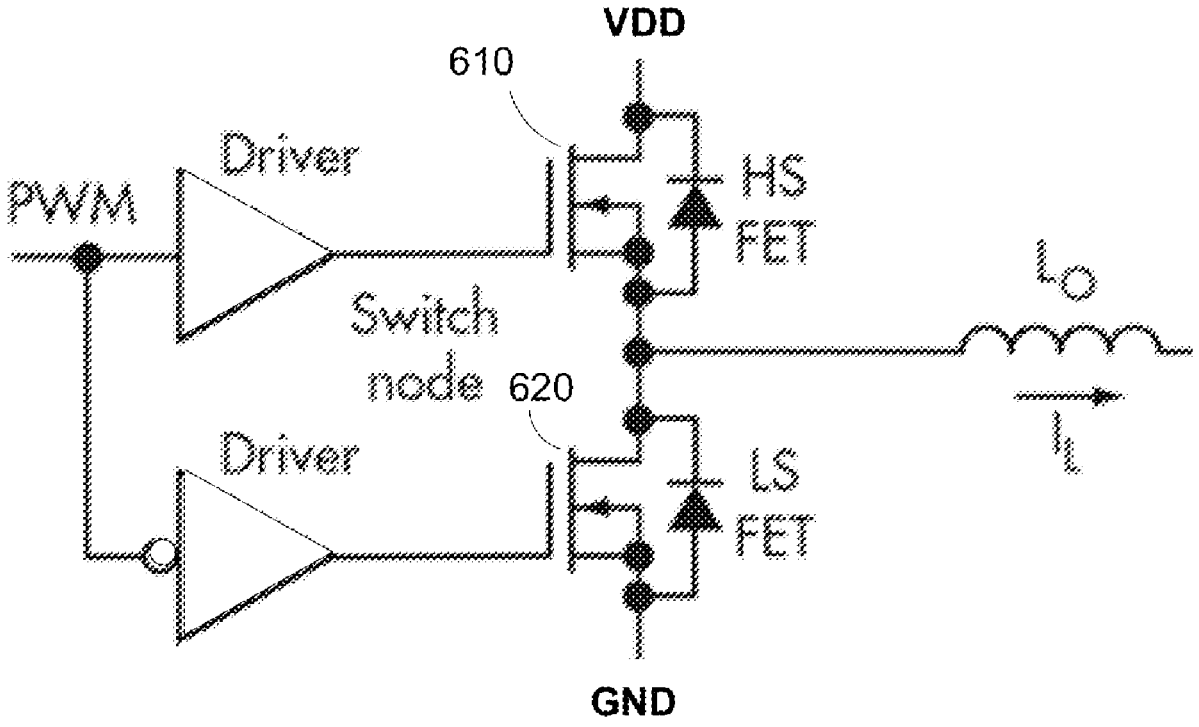
H02M 3/158	(2006.01)
H02M 1/00	(2006.01)
H02M 3/00	(2006.01)
H02M 3/07	(2006.01)

(52) **U.S. Cl.**

CPC ***H02M 3/1584*** (2013.01); ***H02M 3/003*** (2021.05); *H02M 1/0025* (2021.05); *H02M 3/07* (2013.01); *H02M 3/1586* (2021.05)

(57) **ABSTRACT**

A system is disclosed. The system includes a substrate, and a first chip on the substrate, where a load circuit is integrated on the first chip. The system also includes a second chip on the substrate, where a power delivery circuit is configured to deliver current to the load circuit according to a regulated voltage at a node. The power delivery circuit includes a first circuit configured to generate an error signal based at least in part on the regulated voltage, and a voltage generator including power switches configured to modify the regulated voltage according to the error signal, where the first circuit of the power delivery circuit is integrated on the first chip, and where at least a portion of the power switches of the power delivery circuit are integrated on the second chip.



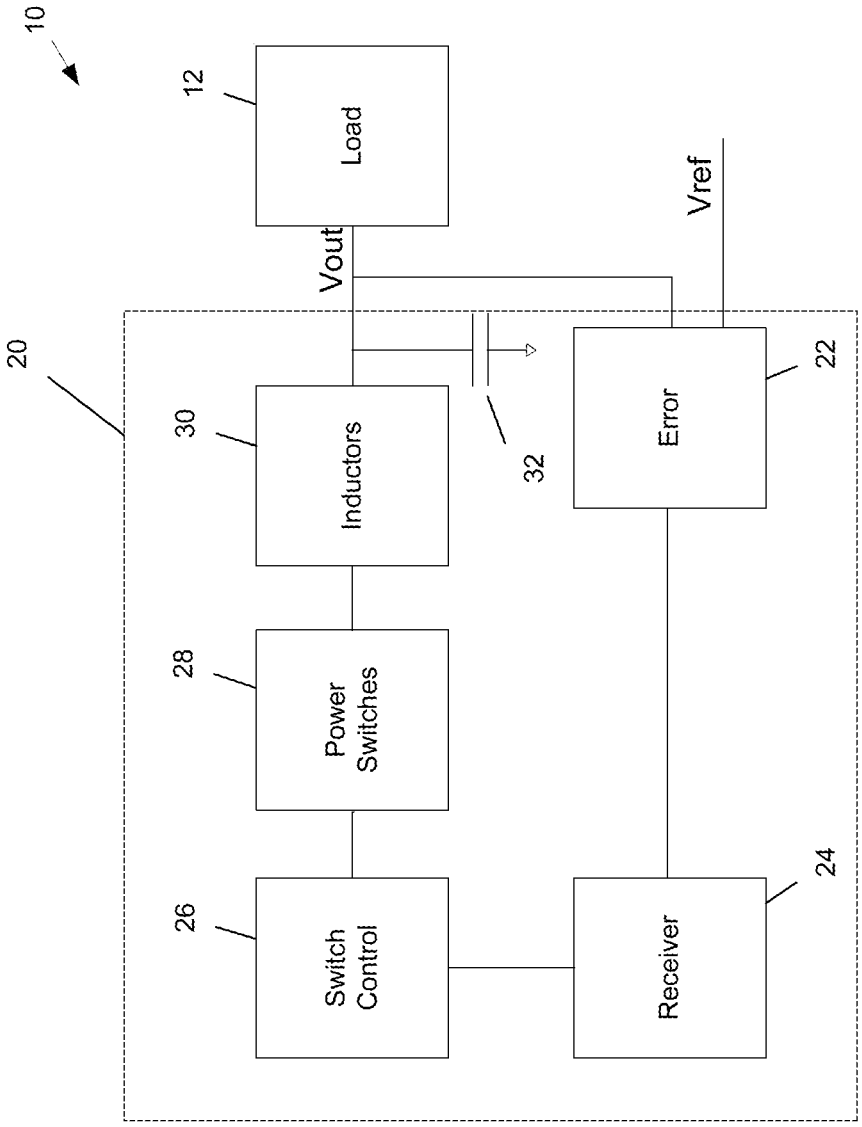

10
12
Load
Vout
Vref
20
30
Inductors
32
Error
22
28
Power Switches
26
Switch Control
Receiver
24

FIG. 1

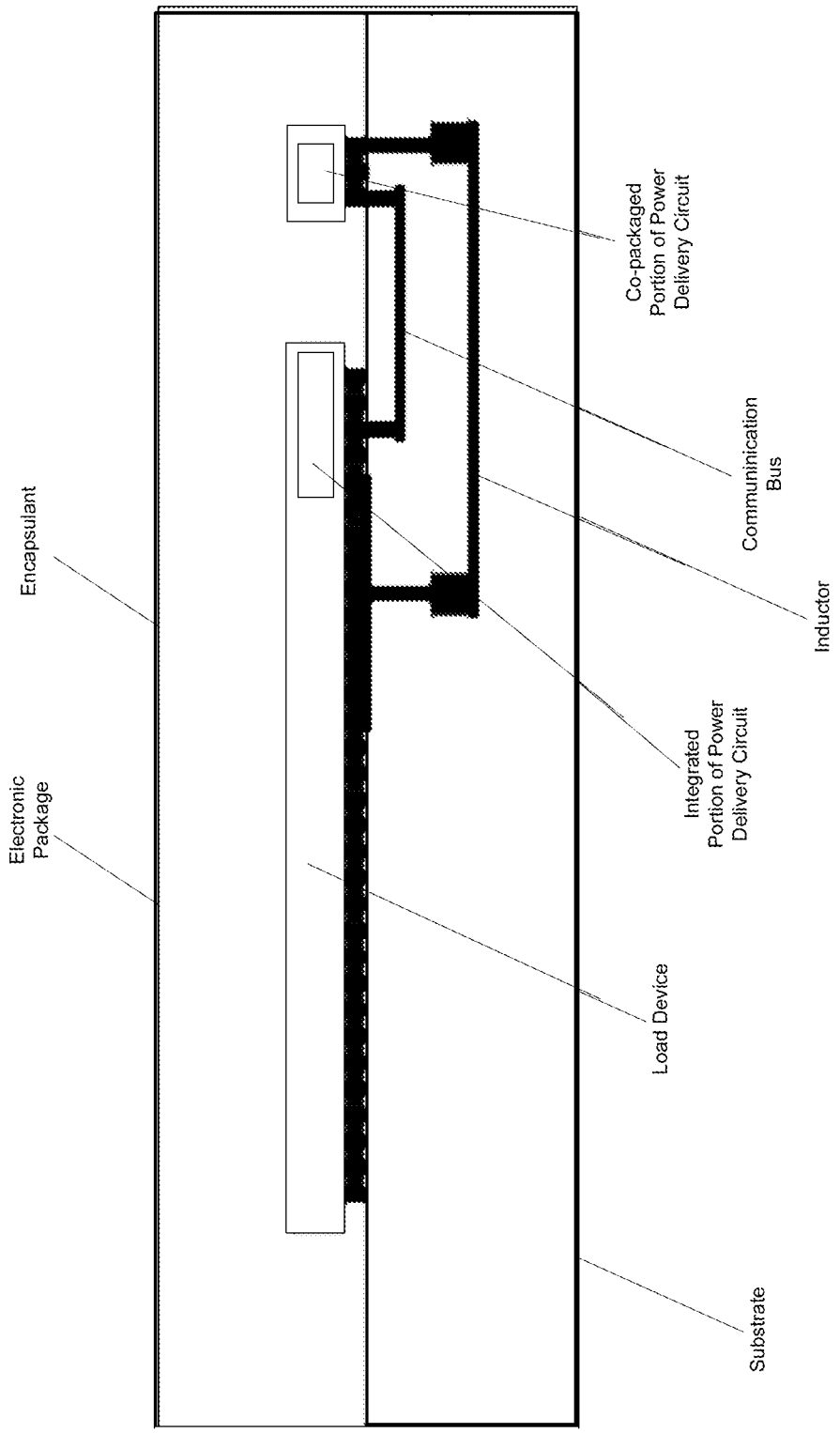

Co-packaged Portion of Power Delivery Circuit
Communication Bus
Inductor
Integrated Portion of Power Delivery Circuit
Load Device
Substrate
Encapsulant
Electronic Package

FIG. 2

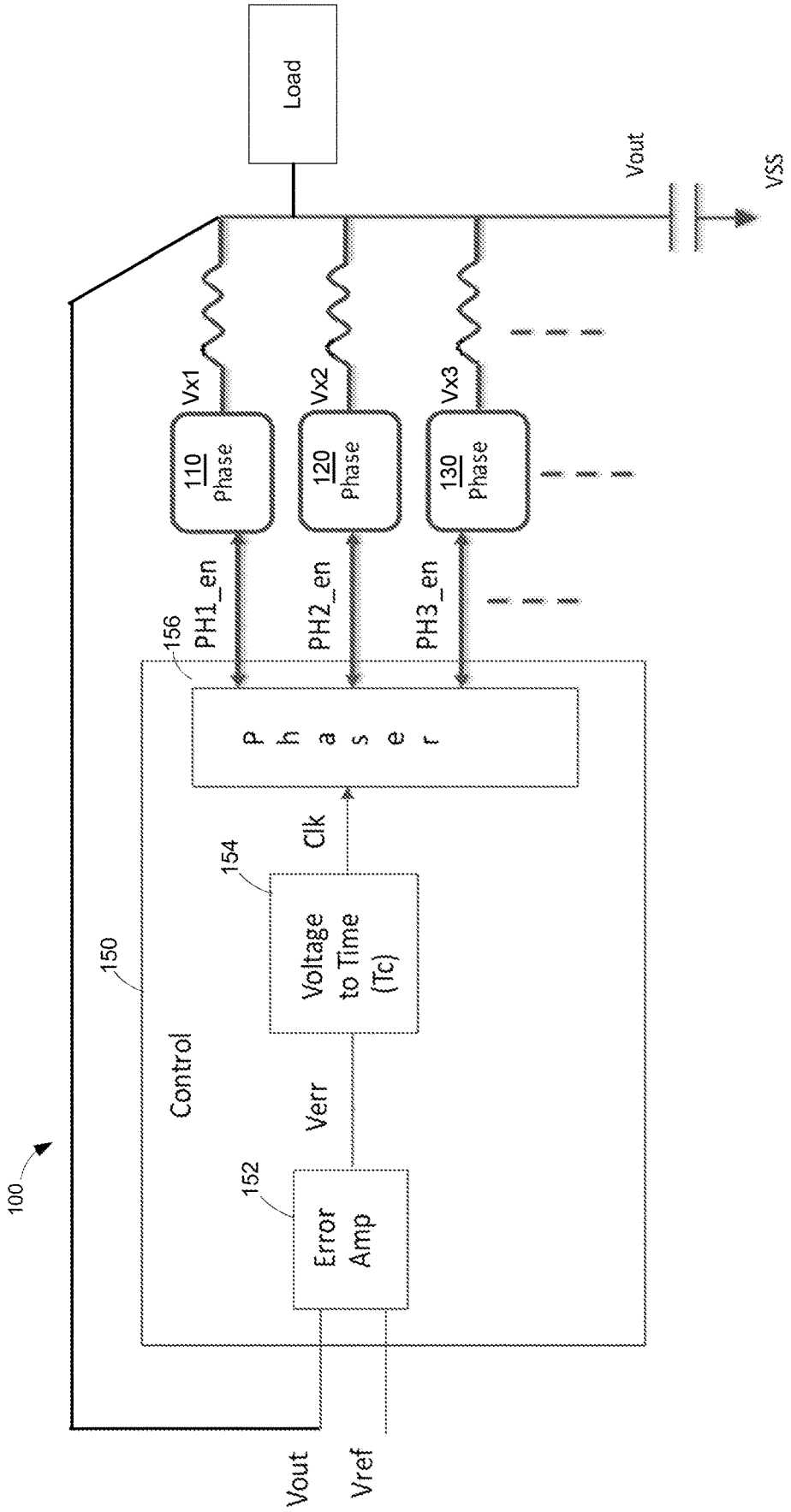

Load
Vout
VSS
Vx1
Vx2
Vx3
110 Phase
120 Phase
130 Phase
PH1_en
PH2_en
PH3_en
156
Phaser
Clk
154
Voltage to Time (Tc)
150
Control
Verr
152
Error Amp
100
Vout
Vref

FIG. 3

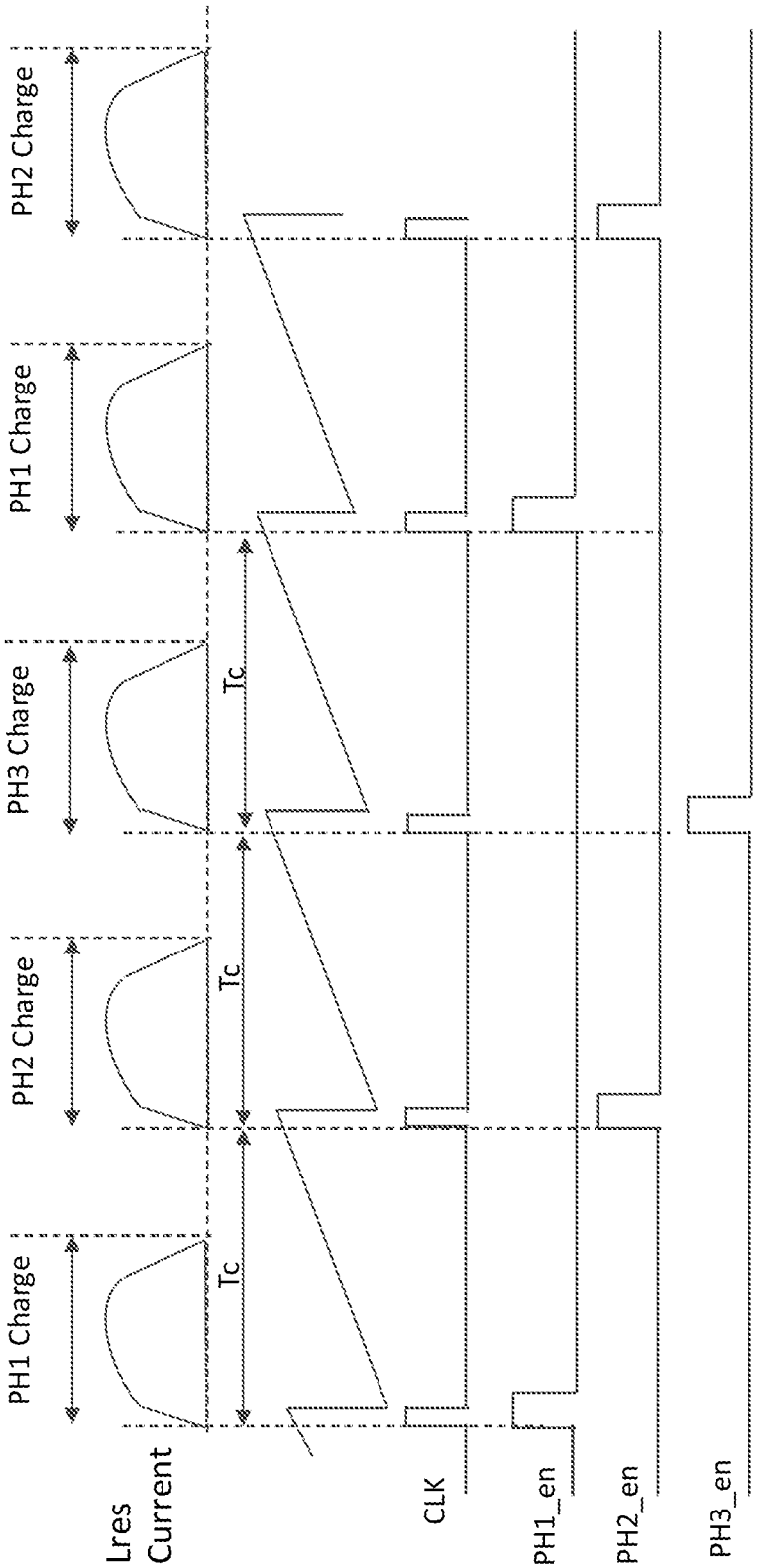

PH1 Charge
PH2 Charge
PH3 Charge
PH1 Charge
PH2 Charge
Tc
Tc
Tc
Lres Current
CLK
PH1_en
PH2_en
PH3_en

FIG. 4

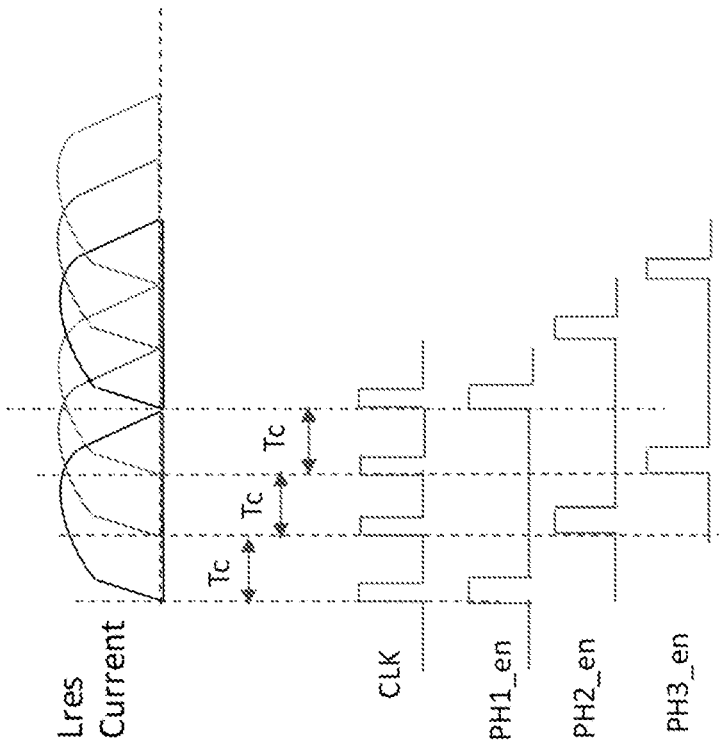

Lres Current
Tc
Tc
Tc
CLK
PH1_en
PH2_en
PH3_en

FIG. 5

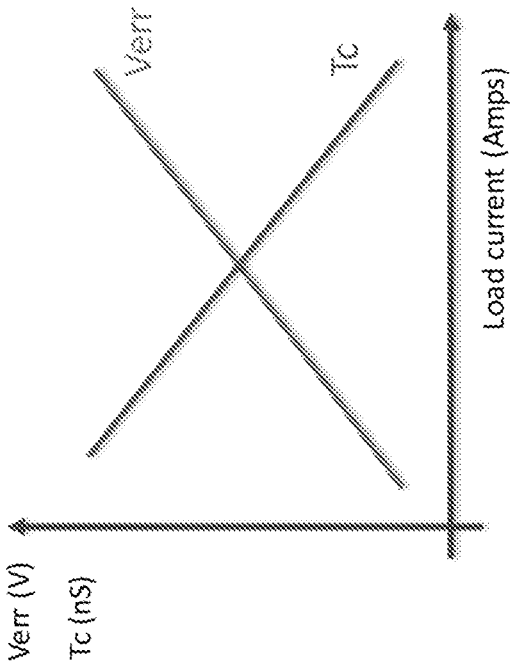

Verr
Tc
Load current (Amps)
Verr (V)
Tc (nS)

FIG. 6

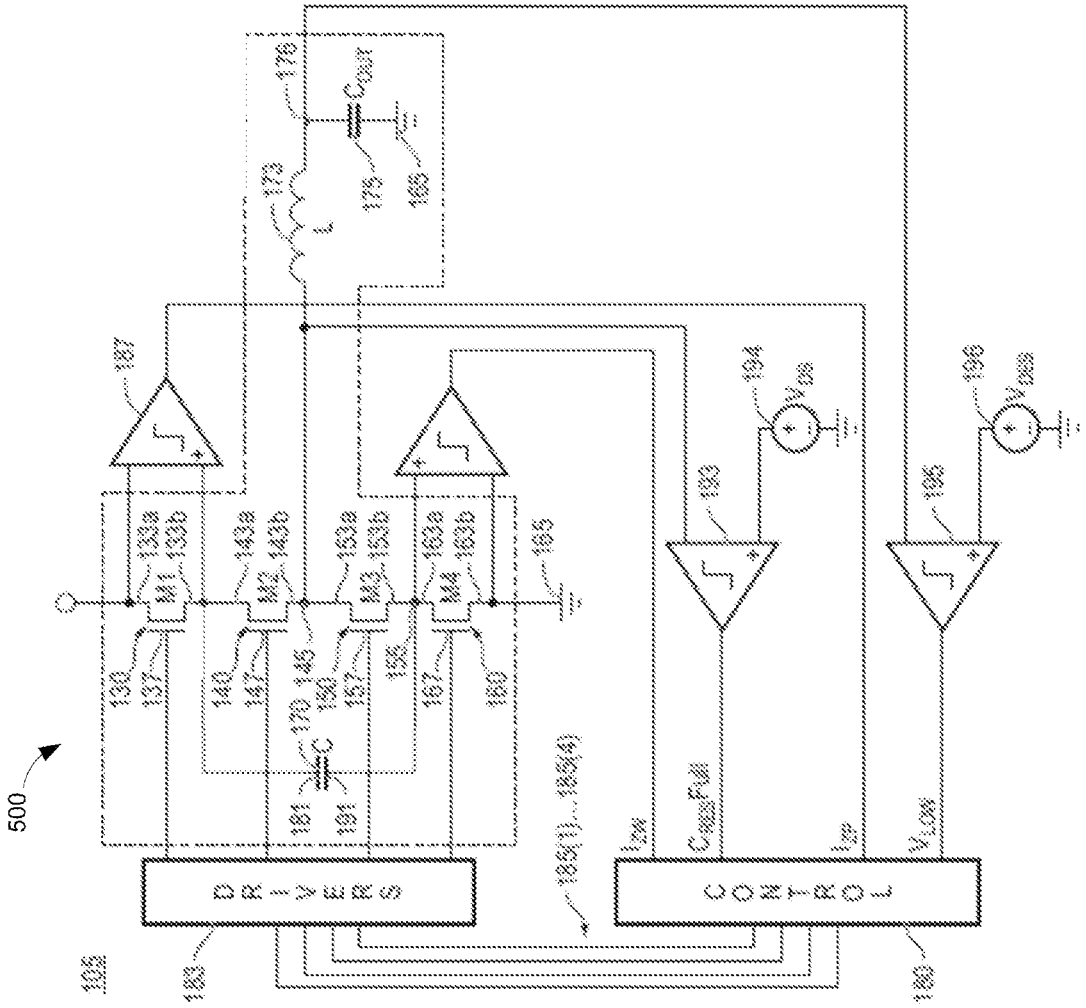

500
105
DRIVERS
CONTROL
183
180
185(1)...185(4)
M1
M2
M3
M4
130
137
140
147
150
157
155
167
160
133a
133b
143a
143b
153a
153b
163a
163b
165
170
181
191
187
193
194
195
196
173
L
175
176
C_{OUT}
I_{DN}
C_{REG} Full
I_{DP}
V_{LOW}
V_{DS}
V_{DSS}

FIG. 7A

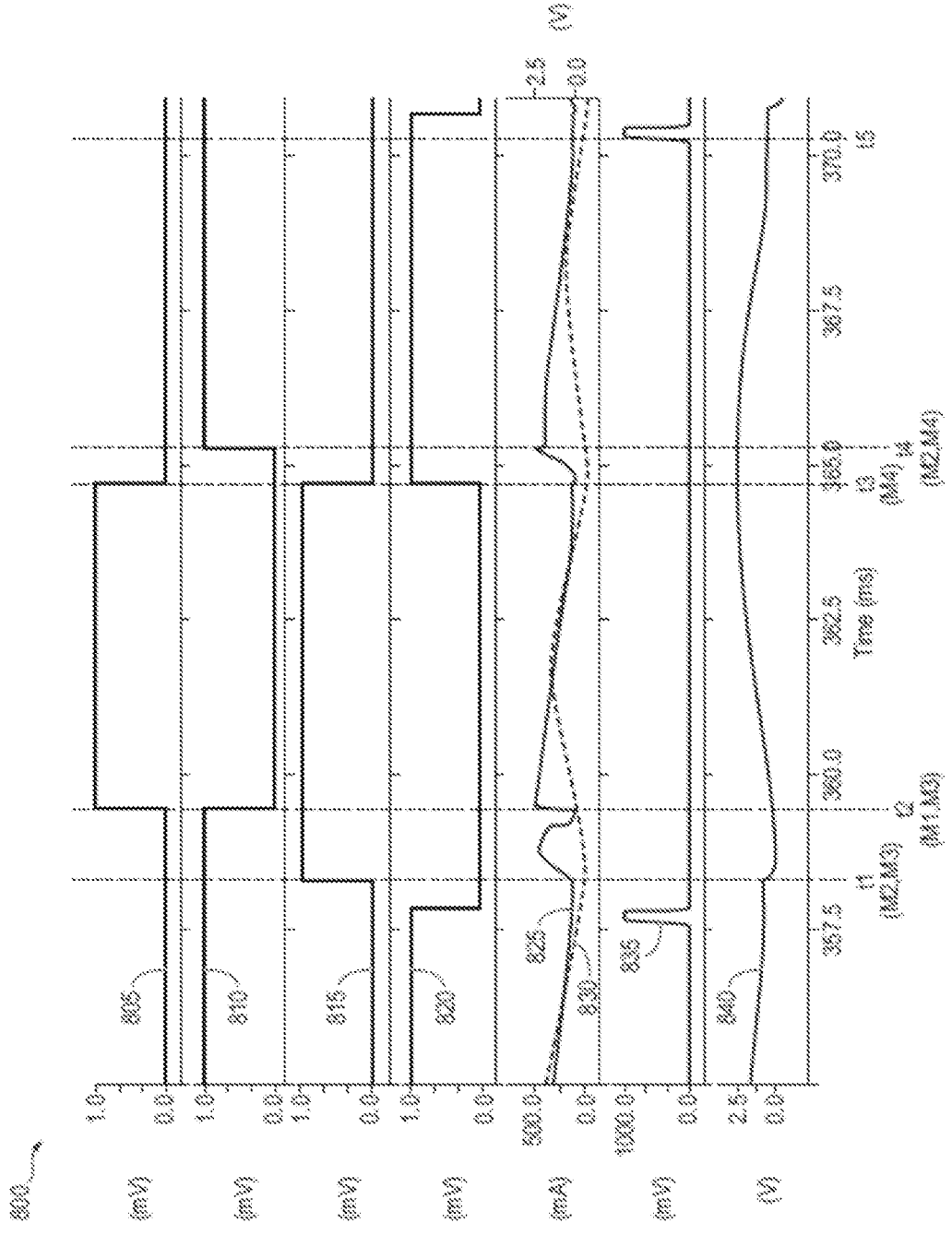

800
805
810
815
820
825
830
835
840
(mV)
(mA)
(V)
Time (ms)
t1 (M2,M3)
t2 (M1,M3)
t3 (M4)
t4 (M2,M4)
t5

FIG. 7B

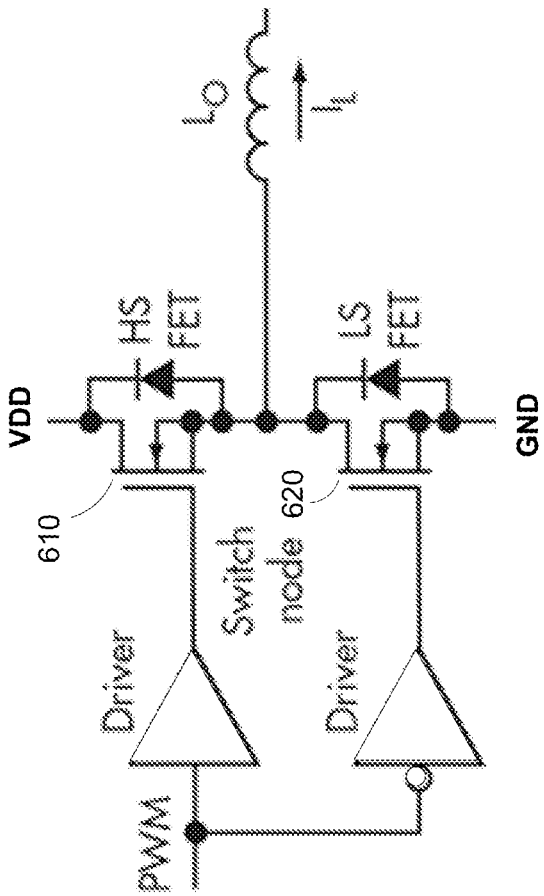

Lo
IL
HS FET
LS FET
VDD
GND
610
620
Switch node
Driver
Driver
PWM

FIG. 8

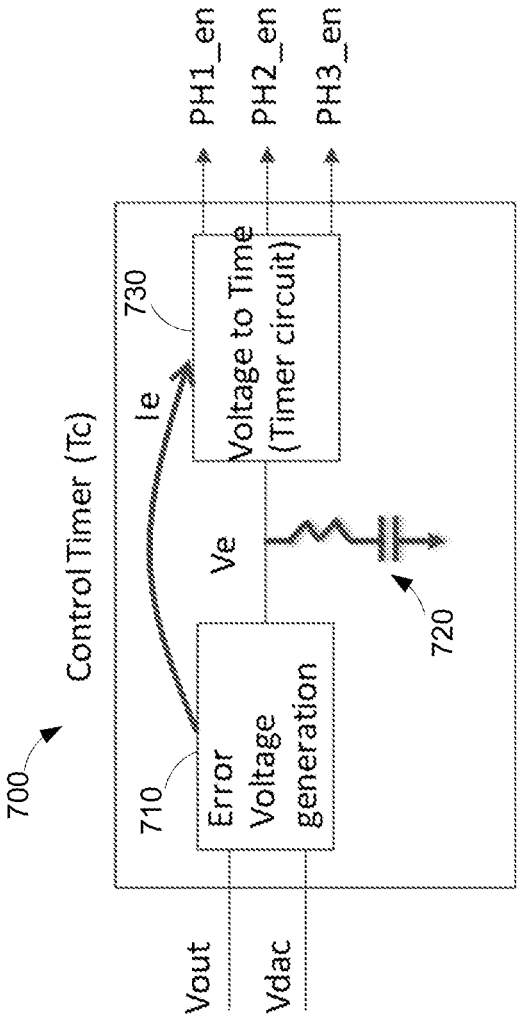

700
Control Timer (Tc)
710
Error Voltage generation
Ve
Ie
730
Voltage to Time (Timer circuit)
720
PH1_en
PH2_en
PH3_en
Vout
Vdac

FIG. 9

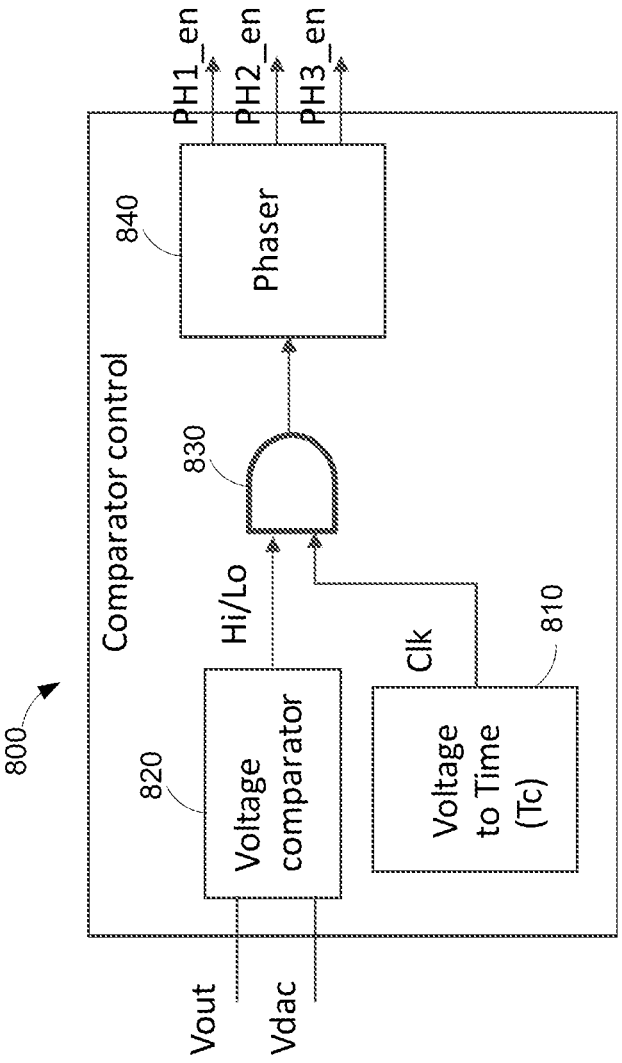

800
Comparator control
820
Voltage comparator
Hi/Lo
830
840
Phaser
PH1_en
PH2_en
PH3_en
Clk
810
Voltage to Time (Tc)
Vout
Vdac

FIG. 10

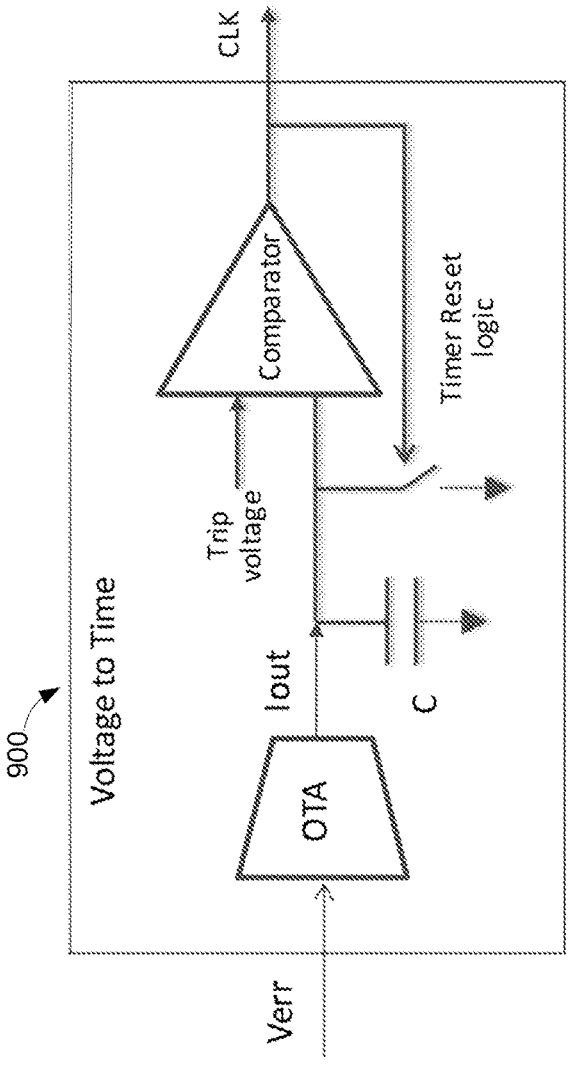

900
Voltage to Time
Verr
OTA
Iout
C
Trip voltage
Comparator
Timer Reset logic
CLK

FIG. 11

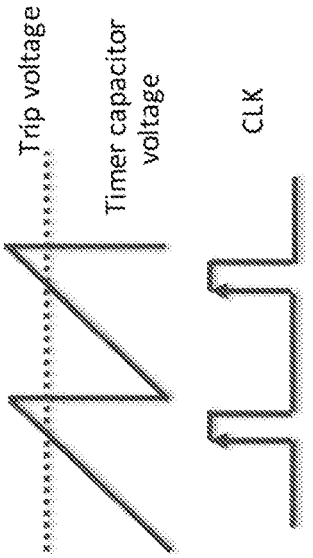

Trip voltage
Timer capacitor voltage
CLK

FIG. 12

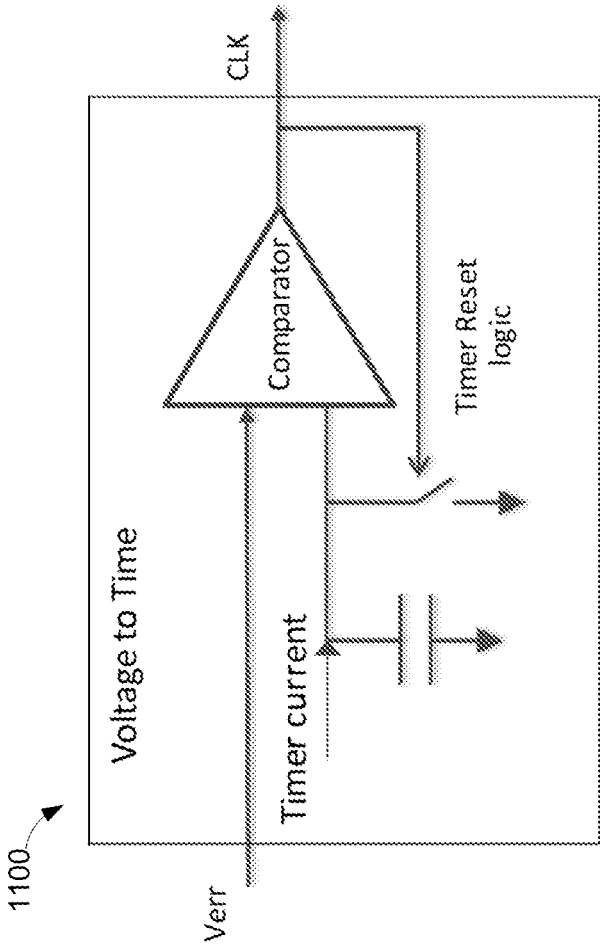

1100
Verr
Voltage to Time
Timer current
Comparator
CLK
Timer Reset logic

FIG. 13

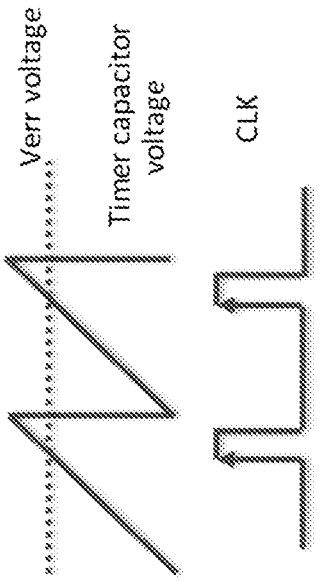

Verr voltage
Timer capacitor voltage
CLK

FIG. 14

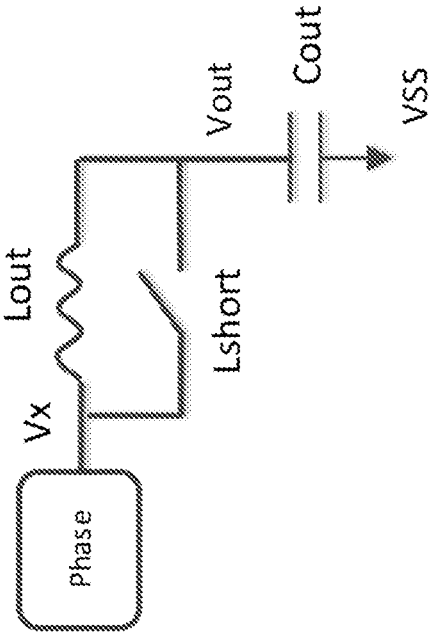


FIG. 16

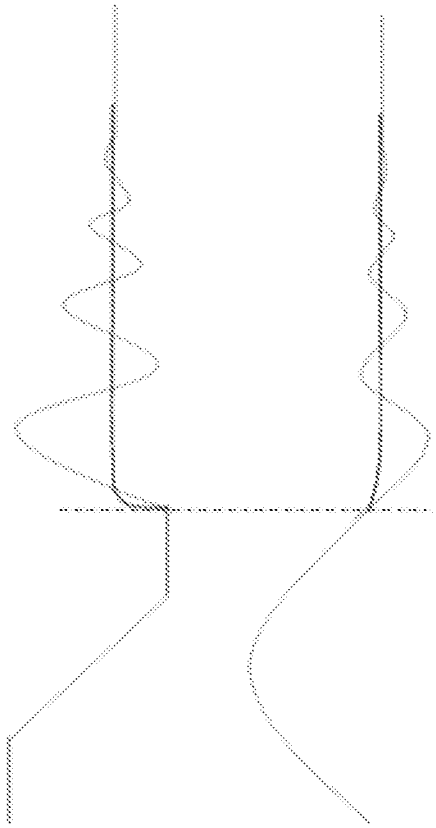


FIG. 15

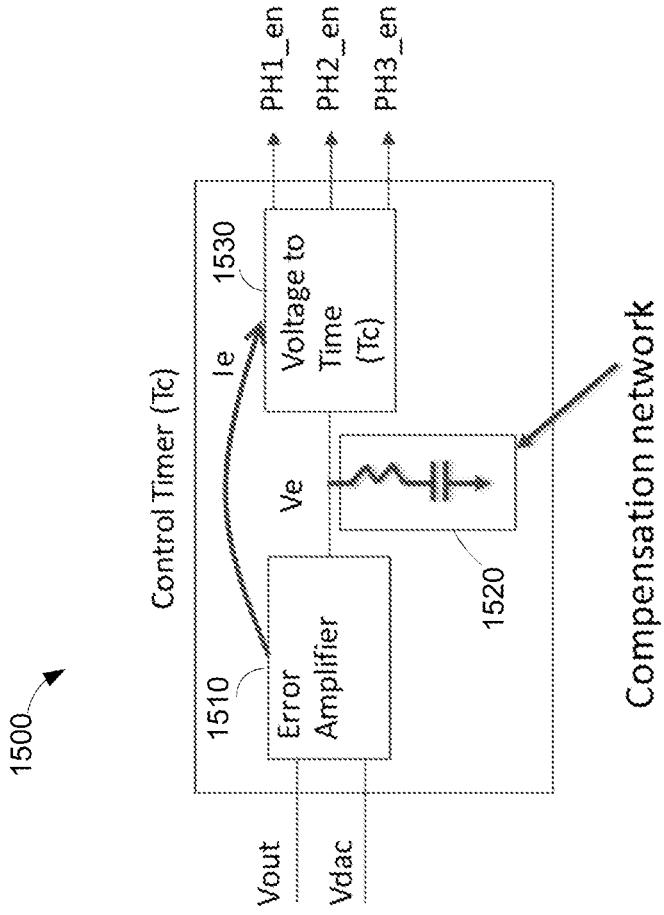
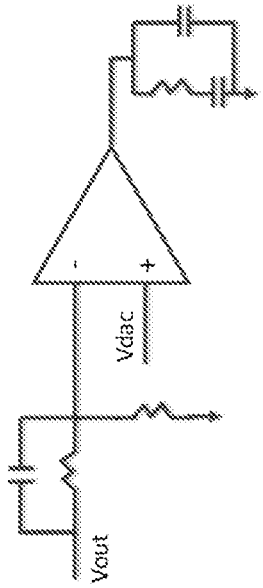
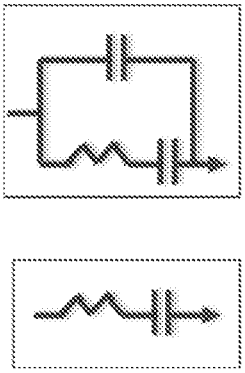

1500
Control Timer (Tc)
1510
Error Amplifier
Ie
1530
Voltage to Time (Tc)
Ve
1520
Compensation network
PH1_en
PH2_en
PH3_en
Vout
Vdac

FIG. 17



Type 3 Compensation

FIG. 18



Type 2

FIG. 19

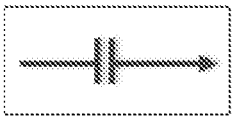


FIG. 20

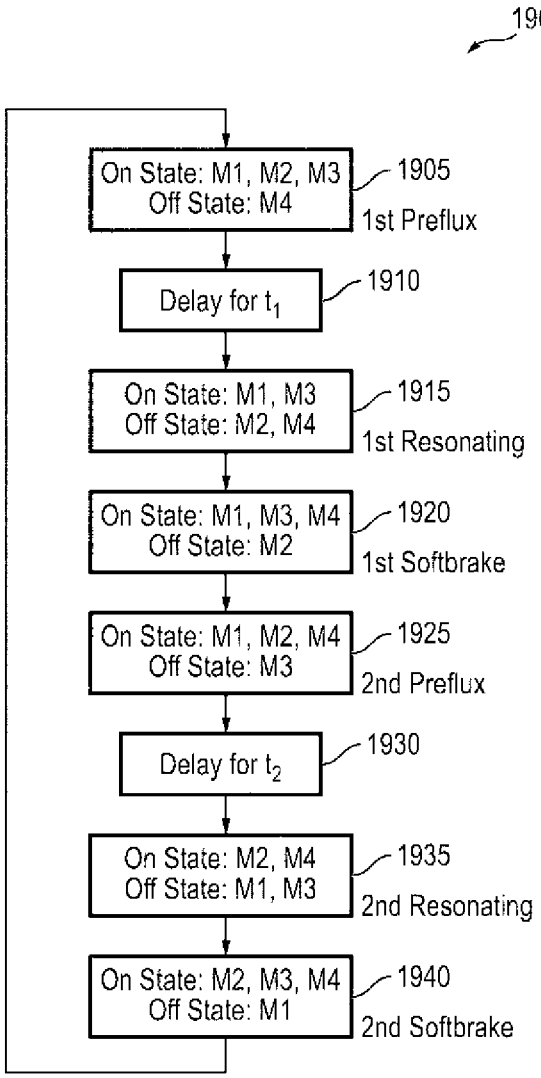

1900
On State: M1, M2, M3
Off State: M4
1905
1st Preflux
Delay for t_1
1910
On State: M1, M3
Off State: M2, M4
1915
1st Resonating
On State: M1, M3, M4
Off State: M2
1920
1st Softbrake
On State: M1, M2, M4
Off State: M3
1925
2nd Preflux
Delay for t_2
1930
On State: M2, M4
Off State: M1, M3
1935
2nd Resonating
On State: M2, M3, M4
Off State: M1
1940
2nd Softbrake

FIG. 21

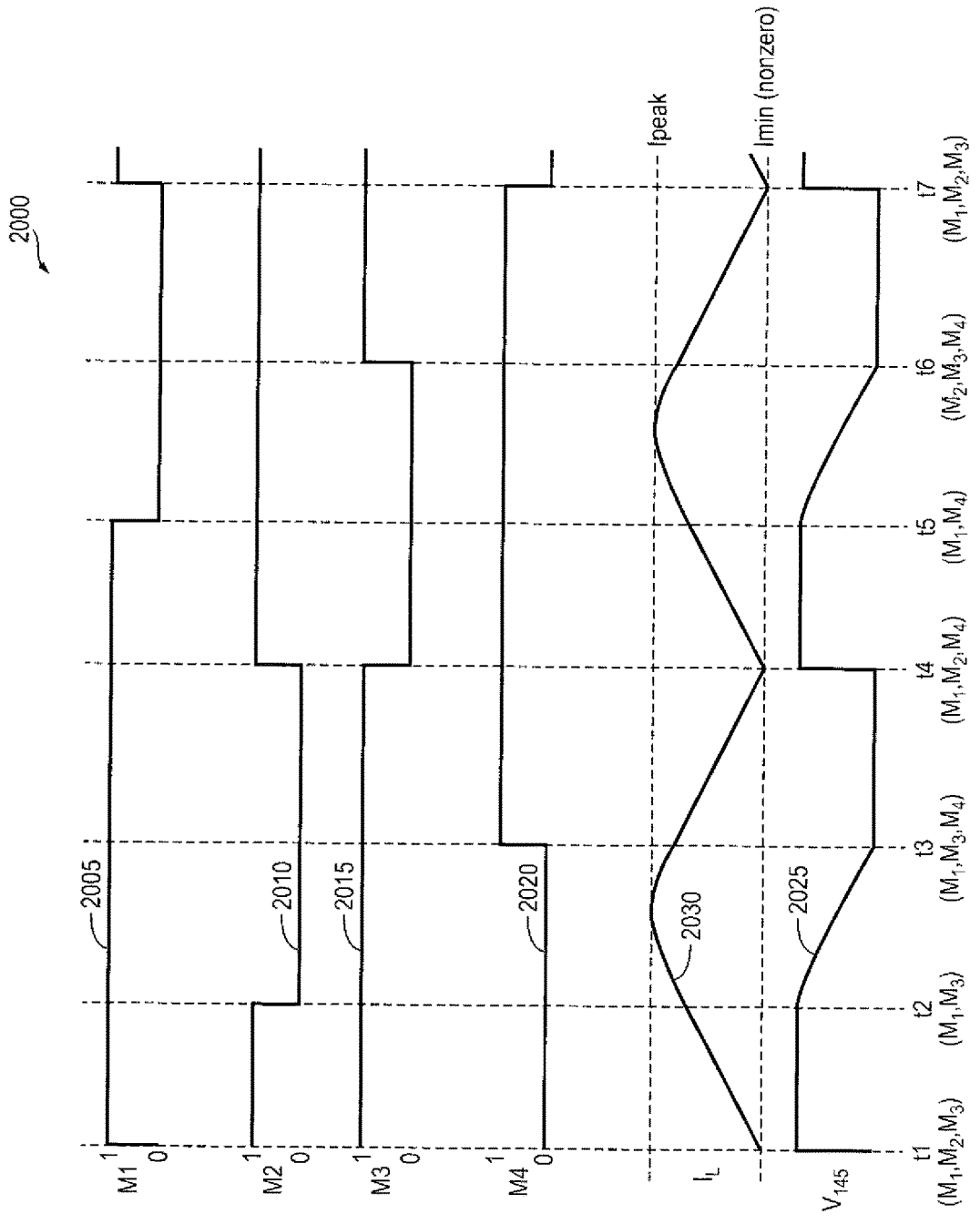

2000
2005
2010
2015
2020
2025
2030
M1
M2
M3
M4
1
0
I_L
V_{145}
Ipeak
Imin (nonzero)
t1 (M_1,M_2,M_3)
t2 (M_1,M_3)
t3 (M_1,M_3,M_4)
t4 (M_1,M_2,M_4)
t5 (M_1,M_4)
t6 (M_2,M_3,M_4)
t7 (M_1,M_2,M_3)

FIG. 22

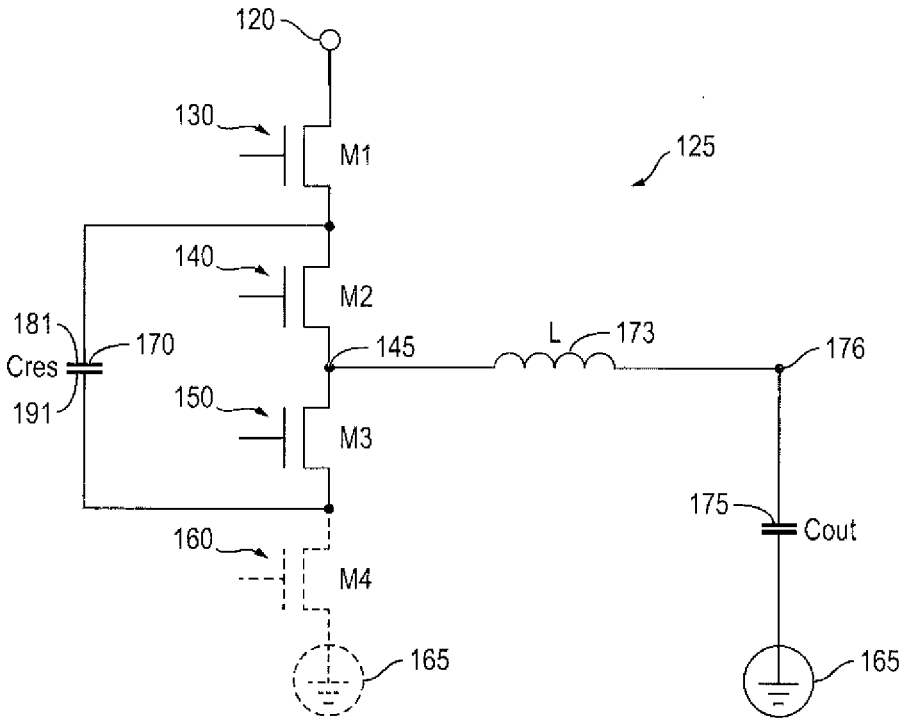

120
130
M1
125
140
M2
181
170
Cres
191
145
L
173
176
150
M3
175
Cout
160
M4
165
165

FIG. 23

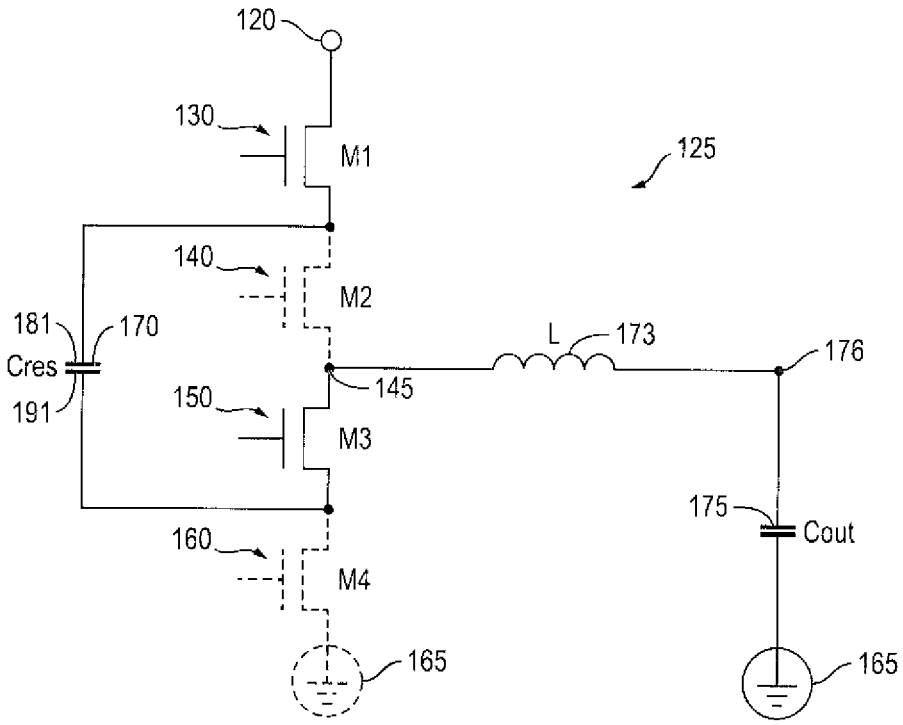

120
130
M1
125
140
M2
181
170
Cres
191
L
173
176
145
150
M3
175
Cout
160
M4
165
165

FIG. 24

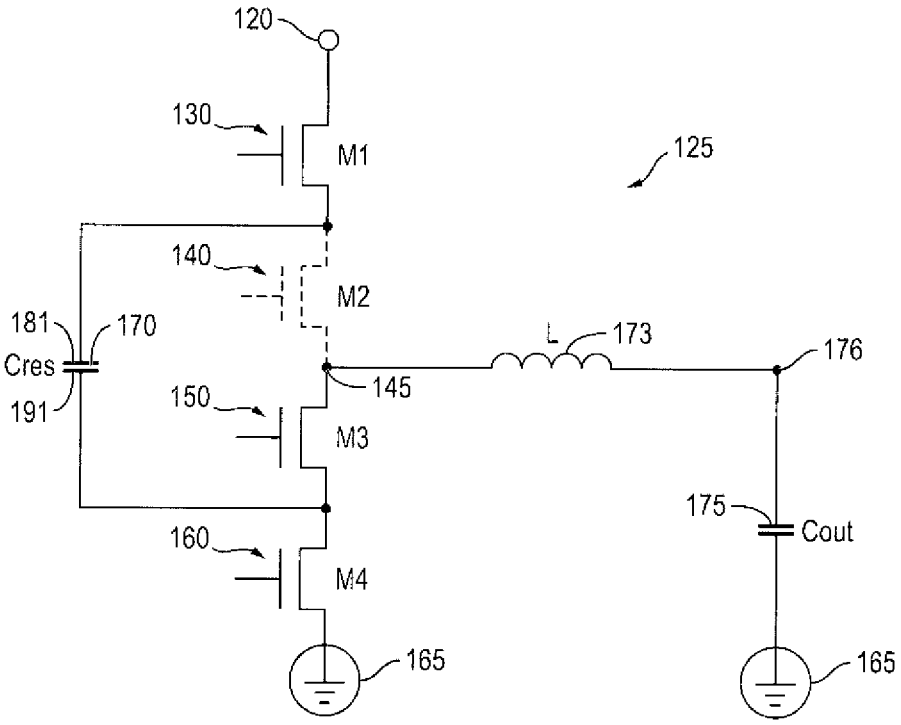

120
130
M1
125
140
M2
181
170
Cres
191
L
173
176
145
150
M3
175
Cout
160
M4
165
165

FIG. 25

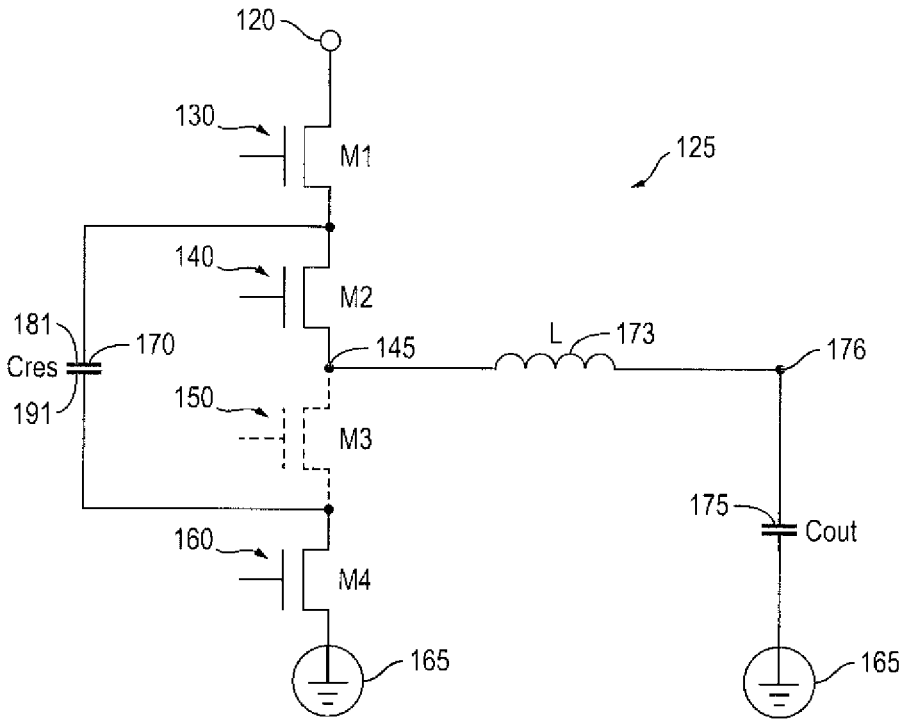

120
130
M1
125
140
M2
181
170
Cres
191
145
L
173
176
150
M3
175
Cout
160
M4
165
165

FIG. 26

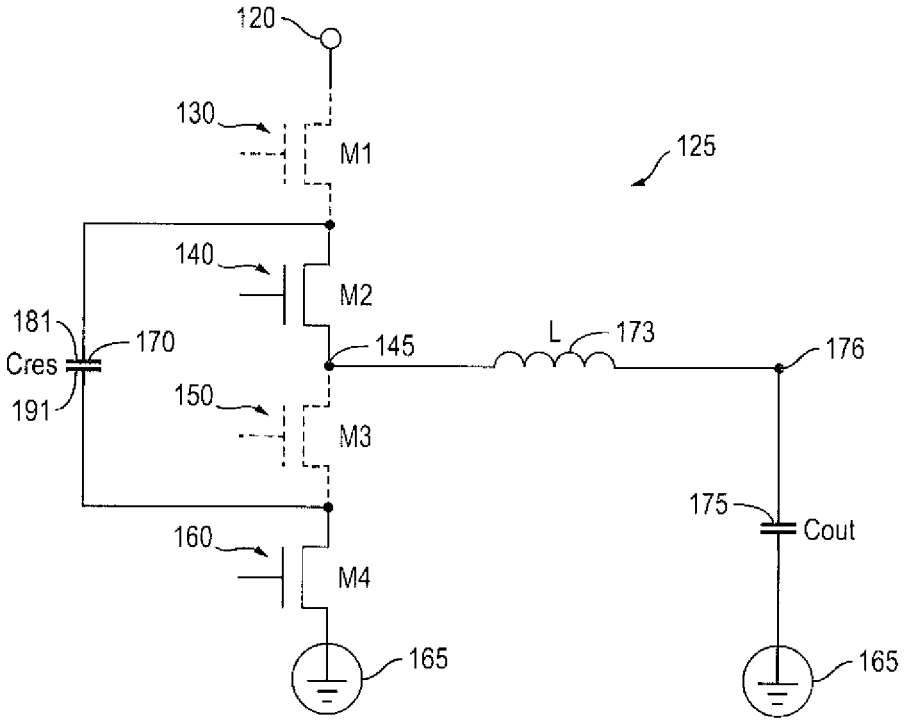

120
130
M1
125
140
M2
181
170
Cres
191
145
L
173
176
150
M3
175
Cout
160
M4
165
165

FIG. 27

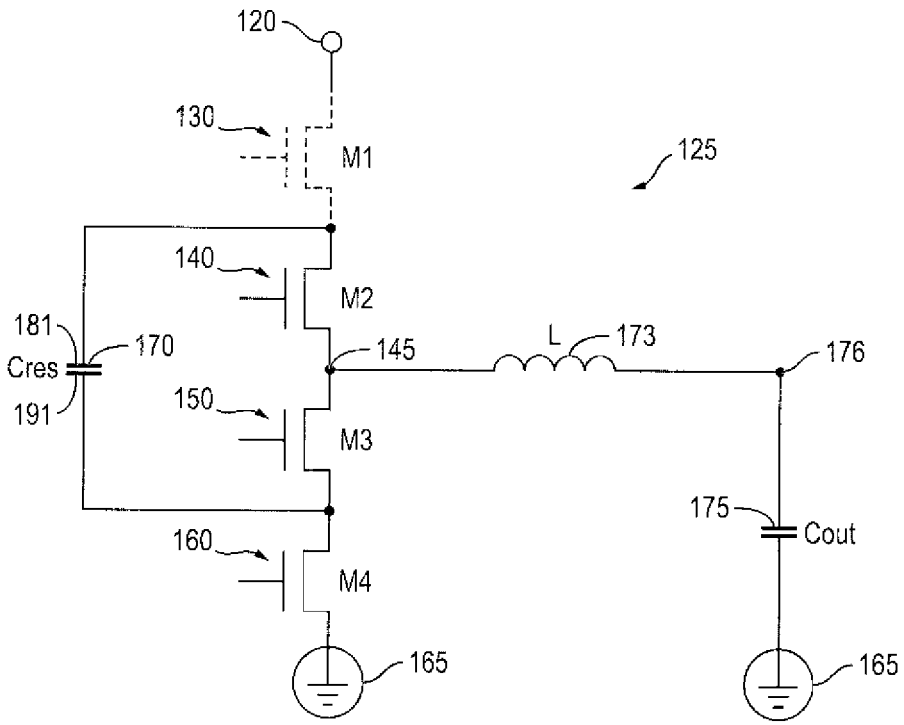

120
130
M1
125
140
M2
181
170
Cres
191
145
L
173
176
150
M3
175
Cout
160
M4
165
165

FIG. 28

DEEPLY INTEGRATED VOLTAGE REGULATOR ARCHITECTURES

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 18/163,820, filed Feb. 2, 2023, entitled DEEPLY INTEGRATED VOLTAGE REGULATOR ARCHITECTURES, which is a continuation of U.S. patent application Ser. No. 17/811,042, filed Jul. 6, 2022, entitled DEEPLY INTEGRATED VOLTAGE REGULATOR ARCHITECTURES, which is a continuation of U.S. patent application Ser. No. 17/208,851, filed Mar. 22, 2021, entitled DEEPLY INTEGRATED VOLTAGE REGULATOR ARCHITECTURES, which is a continuation of U.S. patent application Ser. No. 16/727,909, filed Dec. 26, 2019, entitled DEEPLY INTEGRATED VOLTAGE REGULATOR ARCHITECTURES, which claims the benefit of U.S. Provisional Application No. 62/785,143, filed Dec. 26, 2018, entitled INTEGRATED VOLTAGE REGULATOR, the disclosures of all of which are incorporated herein by reference in their entirety.

FIELD OF THE INVENTION

[0002] The present application generally pertains to power delivery circuits, and more particularly to circuits which deliver power to a load using multiple phases.

BACKGROUND OF THE INVENTION

[0003] New circuits have increased power needs. Therefore, power delivery systems having improved control schemes are needed.

BRIEF SUMMARY OF THE INVENTION

[0004] One inventive aspect is a system. The system includes a substrate, and a first chip on the substrate, where a load circuit is integrated on the first chip. The system also includes a second chip on the substrate, where a power delivery circuit is configured to deliver current to the load circuit according to a regulated voltage at a node. The power delivery circuit includes a first circuit configured to generate an error signal based at least in part on the regulated voltage, and a voltage generator including power switches configured to modify the regulated voltage according to the error signal, where the first circuit of the power delivery circuit is integrated on the first chip, and where at least a portion of the power switches of the power delivery circuit are integrated on the second chip.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** depicts an illustrative simplified schematic of a system.

[0006] FIG. **2** is a cross-sectional schematic view of a IC package.

[0007] FIG. **3** depicts an illustrative simplified schematic of a power delivery control circuit that can be used in a variety of electronic systems.

[0008] FIG. **4** is a waveform diagram illustrating wave forms for signals of the power delivery control circuit **100** illustrated in FIG. **1**.

[0009] FIG. **5** is a waveform diagram illustrating wave forms for signals of the power delivery control circuit **100** illustrated in FIG. **1**.

[0010] FIG. **6** is a diagram illustrating Tc (time between starts of phase pulses) and Verr (error voltage) dependence on load current.

[0011] FIG. **7**A is a schematic illustration of a power delivery engine.

[0012] FIG. **7**B illustrates one example of the waveforms for the power delivery engine **500** illustrated in FIG. **7**A.

[0013] FIG. **8** is a schematic illustration of a power delivery engine.

[0014] FIG. **9** is a schematic illustration of a control timer circuit.

[0015] FIG. **10** is a schematic illustration of a comparator mode control circuit.

[0016] FIGS. **11** and **12** illustrate an embodiment of a voltage to time circuit.

[0017] FIGS. **13** and **14** illustrate an embodiment of a voltage to time circuit.

[0018] FIGS. **15** and **16** illustrate an embodiment of inductor shorting.

[0019] FIG. **17** is a schematic illustration of a control timer circuit.

[0020] FIGS. **18-20** are schematic illustrations of compensation networks according to some embodiments.

[0021] FIG. **21** is a flowchart of a repetitive switching sequence providing a continuous current output for the switched regulation circuit in FIG. **5** according to an embodiment of the invention.

[0022] FIG. **22** is a timing diagram of voltages and currents within the switched regulation circuit of FIG. **7**A according to the switching sequence in FIG. **21**.

[0023] FIG. **23** is a schematic of the switched regulation circuit shown in FIG. **7**A in a particular switch configuration according to the switching sequence in FIG. **21**.

[0024] FIG. **24** is a schematic of the switched regulation circuit shown in FIG. **7**A in a particular switch configuration according to the switching sequence in FIG. **21**.

[0025] FIG. **25** is a schematic of the switched regulation circuit shown in FIG. **7**A in a particular switch configuration according to the switching sequence in FIG. **21**.

[0026] FIG. **26** is a schematic of the switched regulation circuit shown in FIG. **7**A in a particular switch configuration according to the switching sequence in FIG. **21**.

[0027] FIG. **27** is a schematic of the switched regulation circuit shown in FIG. **7**A in a particular switch configuration according to the switching sequence in FIG. **21**;

[0028] FIG. **28** is a schematic of the switched regulation circuit shown in FIG. **7**A in a particular switch configuration according to the switching sequence in FIG. **21**.

DETAILED DESCRIPTION OF THE INVENTION

[0029] Particular embodiments of the invention are illustrated herein in conjunction with the drawings.

[0030] FIG. **1** depicts an illustrative simplified schematic of system **10** including a power delivery circuit **20** that is coupled to a load **12**, which receives power from power delivery circuit **20**. For example, load **12** may receive current from power delivery circuit **20** via node Vout, where the voltage at node Vout is regulated by power delivery circuit **20**. Accordingly, as understood by those skilled in the art, load **12** is a load for power delivery circuit **20**.

[0031] The load **12** is integrated on a first semiconductor chip or die. A first portion of the power delivery circuit **20** is also integrated on the first semiconductor chip or die. In addition, a second portion of the power delivery circuit **20** is integrated on a second semiconductor chip or die.

[0032] In some embodiments, as described above, the load **12** can be any type of integrated circuit (e.g., a processor, DSP, AI computation, communication) and may contain digital and analog circuits. The load **12** may interface with the power delivery circuit **20**. The means of communication can include a communication bus coupled to either or both of the first and second portions of power delivery circuit **20**. For example, the load **12** can include any portion of a monitoring or control system that interfaces with one or more portions of the power delivery circuit **20**. The load **12** can also store information associated with the power delivery circuit **20** in a memory and communicate data associated with the power delivery circuit **20** to an external device.

[0033] The load **12**, can include circuitry that configures the power delivery circuit **20**. For example in can communicate the desired output voltage. It may also configure properties of the power delivery circuit **20** including compensation information, startup and shutdown information etc. The load can communicate to the power delivery circuit on either the second die or the first die. A dedicated communication connection may also be connected between parts of the power delivery circuit **20** on the first and second die.

[0034] Communication between circuits on the same die can often be much faster. Being able to change the voltage quickly can increase throughput and save power so one implementation enables the load to quickly change the voltage desired by communicating with the portion of the power delivery circuit on the first die. In some implementations, the desired voltage may also be communicated to the portion of the power delivery circuit **20** on the second die. This can enable optimal optimization of that circuitry. Other information that can be communicated to the power delivery circuit **20** include power states of the load, timing and rate of startup and shut down of the power delivery circuits. Other information that can be communicated from the power delivery circuit **20**, to the load **12** include status of the regulator, information about the output voltage, how much current is being provided, temperature and any fault conditions. This information may be used by the receiving circuit or component to modify the functionality of the receiving component. For example, the information may be used by the receiving circuit or component to modify the voltage generated by power delivery circuit **20**.

[0035] The power delivery circuit **20** includes error circuit **22**, error management circuit **24**, switch control circuit **26**, power switches **28**, inductors **38**, and capacitor **32**. In some embodiments, the power delivery circuit **20** forms or partly forms a voltage regulator circuit.

[0036] Error circuit **22** is configured to receive a reference voltage at node or bus Vref. The reference voltage is generated by another circuit, and has a voltage value equal or substantially equal to a target or desired voltage value of the voltage at node Vout, which is generated by power delivery circuit **20** for load **12**, such that the power delivery circuit **20** delivers current to the load **12** at a regulated voltage at node Vout, where the regulated voltage at node Vout is determined based on the reference voltage at node or bus Vref.

[0037] Error circuit **22** is configured to also receive the voltage at node Vout generated by power delivery circuit **20**. Based at least on the difference between the voltage at node Vout and the reference voltage, error circuit **22** generates an error signal which causes the power delivery circuit **20** to generate the voltage at node Vout so that the difference between the voltage at node Vout and the reference voltage is minimized, as understood by those of skill in the art.

[0038] In some embodiments, error circuit **22** comprises an operational amplifier having gain, bandwidth, and stability characteristics which contribute to stable generation of the voltage at node Vout.

[0039] Error circuit **22** may include an analog-to-digital converter configured to generate a digital representation of the difference between the analog voltage at node Vout and the analog reference voltage at node Vref as the error signal.

[0040] In some embodiments, error circuit **22** comprises an analog-to-digital converter configured to generate a digital representation of the voltage at node Vout, and a digital difference or subtraction circuit configured to receive the digital representation of the voltage at node Vout and to generate a digital error signal based on the difference between the digital representation of the voltage at node Vout and the reference voltage, as represented by a digital word received by error circuit **22** at node or bus Vref.

[0041] Alternatively, in some embodiments, error circuit **22** comprises an analog amplifier configured to receive the analog voltage at node Vout and an analog reference voltage at node Vref, and to generate an analog error signal. In some implementations, the analog error signal represents the difference between the analog voltage at node Vout and the analog reference voltage at node Vref. In some implementations, the analog error signal represents the difference between the analog voltage at node Vout and the analog reference voltage at node Vref multiplied by a gain factor. In some implementations the amplifier can include compensation as known in the art. For example the amplifier can be configured to have proportional, integral and/or differential processing of the analog voltage at node Vout. In other implementations the error circuit **22** can be, or include with other circuits, a comparator to generate an error signal indicating whether the analog voltage at node Vout is greater than or less than a reference voltage, such as the reference voltage at node Vref.

[0042] At least a portion of error circuit **22** may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of error circuit **22** is integrated on the first semiconductor chip or die. In some embodiments, at least a portion of error circuit **22** is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of error circuit **22** is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**.

[0043] It may be advantageous to integrate at least a portion of error circuit **22** on the first semiconductor chip or die at least because error circuit **22** or at least a portion of error circuit **22** comprises a sensor configured to sense the voltage at node Vout for power delivery circuit **20**. As understood by those of skill in the art, power delivery circuit **20** regulates the voltage at node Vout based on the difference between the voltage at node Vout and the voltage reference voltage at node Vref. Accordingly, it is advantageous for the sensor to be as close as possible to the optimum point of

sensing the voltage at node Vout, which is at the load, as understood by those of skill in the art, so that the sensed value is as accurate as possible. As understood by those of skill in the art, distance between the optimum point and the sensed point at node Vout allows for the sensed voltage to be different from the actual voltage at least because of, for example, noise and IR drop.

[0044] Error management circuit **24** is configured to receive the output(s) of error circuit **22** and to generate one or more signals based on the output of error circuit **22**. The one or more signals generated by error management circuit **24** influence the voltage at node Vout so as to minimize the difference between the voltage at node Vout and the reference voltage, as understood by those of skill in the art.

[0045] In some embodiments, the output of error management circuit **24** is a representation of the difference between the voltage at node Vout and the reference voltage.

[0046] The output of error management circuit **24** may include one or more of an analog voltage, a digital word, and another signal type. For example, in some embodiments, the output of error management circuit **24** may include a series of digital pulses, where the frequency of the pulses corresponds at least with the relationship (e.g. difference) between the voltage at node Vout and the reference voltage. In alternative embodiments, other signal mechanisms, for example encoding the difference between the voltage at node Vout and the reference voltage, are generated by error management circuit **24**.

[0047] In some embodiments, the error management circuit **24** receives a representation of the current being provided to the load, for example, from the load **12**, the error circuit **22**, or switch control circuit **26**, and the output of the error management circuit **24** is determined based on the current being drawn from or supplied to the load and a representation of the voltage at node Vout.

[0048] At least a portion of error management circuit **24** may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of error management circuit **24** is integrated on the first semiconductor chip or die. In some embodiments, at least a portion of error management circuit **24** is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of error management circuit **24** is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**. In some embodiments, all of error management circuit **24** is integrated on the second semiconductor chip or die.

[0049] Switch control circuit **26** is configured to receive the output of error management circuit **24** and to generate one or more signals based on the received output of error management circuit **24**. The one or more output signals generated by the switch control circuit **26**, for example, with power FET drivers, influences the voltage at node Vout so as to minimize the difference between the voltage at node Vout and the reference voltage, as understood by those of skill in the art.

[0050] In some embodiments, the output of switch control circuit **26** is based on the difference between the voltage at node Vout and the reference voltage. In some embodiments, the output of switch control circuit **26** is based additionally or alternatively on a current delivered to load **12**.

[0051] The output of switch control circuit **26** may include signals from power FET drivers which control the conductivity states of the power switches **28**. For example, in some embodiments, the output of switch control circuit **26** may include multiple series of digital pulses, where the frequency and the timing relationship among the multiple series corresponds with at least the difference between the voltage at node Vout and the reference voltage. In alternative embodiments, other signal mechanisms, for example corresponding with the difference between the voltage at node Vout and the reference voltage, are generated by switch control circuit **26**.

[0052] In some embodiments, the switch control circuit **26** includes current sense circuitry, which senses the current through power switches **28**. As understood by those of skill in the art, the sensed current may be used to influence when the power switches **28** should switch.

[0053] In some embodiments, switch control circuit **26** generates signals representing the current being delivered to the load for either or both of error circuit **22** and error management circuit **24**.

[0054] At least a portion of switch control circuit **26** may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of switch control circuit **26** is integrated on the first semiconductor chip or die. In some embodiments, at least a portion of switch control circuit **26** is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of switch control circuit **26** is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**. In some embodiments, all of switch control circuit **26** is integrated on the second semiconductor chip or die.

[0055] Power switches **28** are configured to receive the output of switch control circuit **26** and to cooperatively generate the voltage at node Vout with inductor(s) **30** and capacitor **32**, wherein the generated voltage is based on the received output of switch control circuit **26**. Accordingly, power switches **28**, inductor(s) **30**, and capacitor **32** collectively form a voltage generator driven and controlled by the output of switch control circuit **26**. Therefore, the output of switch control circuit **26** causes the power switches **28**, inductor(s) **30**, and capacitor **32** to influence the voltage at node Vout so as to minimize the difference between the voltage at node Vout and the reference voltage, as understood by those of skill in the art.

[0056] In some embodiments, power switches **28** are configured to selectively, alternately, and repetitively connect inductor(s) **30** to a positive power supply and to a negative power supply. In some embodiments, switch control circuitry **26**, power switches **28**, inductor(s) **30**, and capacitor **32** are arranged so as to form a synchronous buck converter topology, a full-bridge converter topology, a boost topology, a buck-boost or another type of power regulator circuit topology.

[0057] Power switches **28** may be integrated on the second semiconductor chip or die. In some embodiments, power switches **28** are discrete power devices or are integrated on another semiconductor die.

[0058] Inductors **38** and capacitor **32** collectively form an LC filter, as understood by those of skill in the art. In some embodiments, capacitor **32** is implemented as multiple physical capacitors connected in parallel. Inductors **38** and capacitor **32** or portions of inductors **38** and capacitor **32** may be formed on either of the first and second semiconductor chips or die. In some embodiments, the output

capacitor **32** is only located on the first semiconductor die. In some embodiments, the output capacitor **32** is a combination of capacitors some on the first semiconductor die, with some outside of the first semiconductor die. In some embodiments, either or both of inductors **38** and capacitor **32** are placed within a multi-chip or multi-die package carrying the first and second semiconductor chips or die, and are not integrated on either of the first and second semiconductor chips or die. In some embodiments, either or both of inductors **38** and capacitor **32** are placed outside of a multi-chip or multi-die package carrying the first and second semiconductor chips or die.

[0059] In some embodiments, power delivery system **20** is multi-phase. In such embodiments, inductor(s) **30** comprises multiple inductors, each connected to capacitor **32** and to a distinct pair of power switches of power switches **28**. Each distinct pair of power switches of power switches **28** is separately controlled by switch control circuitry **26** such that multi-phase power is delivered by power switches **28**, inductor(s) **30**, and capacitor **32** to load **12**.

[0060] In some embodiments, error management circuit **24** and switch control circuit **26** are integrated into a loop control circuit having the input functionality of error management circuit **24** and the output functionality of switch control circuit **26**.

[0061] In such embodiments, at least a portion of the loop control circuit may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of the loop control circuit is integrated on the first semiconductor chip or die. In some embodiments, at least a portion of the loop control circuit is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of the loop control circuit is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**.

[0062] As discussed above, at least in some embodiments, error circuit **22** receives analog voltages at nodes Vout and Vref, and switch control circuit **26** generates control signals at for power switches **28**. Accordingly, error circuit **22**, error management circuit **24**, and switch control circuit **26** may be considered as collectively generating the control signals. Accordingly, error circuit **22**, error management circuit **24**, and switch control circuit **26** may be collectively considered a control signal generator.

[0063] In such embodiments, at least a portion of the collective control signal generator control signal generator may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of the collective control signal generator is integrated on the first semiconductor chip or die. In some embodiments, at least a portion of the collective control signal generator is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of the collective control signal generator is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**.

[0064] As understood by those of skill in the art, the collective control signal generator converter may be segregated into an analog circuit portion and a digital circuit portion. At least a portion of the analog circuit portion may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of the analog circuit portion is integrated on the first semiconductor chip or die, for example, such that a digital signal is sent from the first semiconductor chip or die to the second semiconductor chip or die. In some embodiments, at least a portion of the analog circuit portion is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of the analog circuit portion is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**.

[0065] In some embodiments, the signal from the first die to the second die indicates when a phase should start a new pulse. The second die may take this signal and decide which phase should switch next so as to minimize the voltage ripple at the output voltage at the load **12**.

[0066] In some embodiments, system **10** also includes a reference voltage generation circuit (not shown), which is configured to generate the reference voltage at node Vref.

[0067] In such embodiments, at least a portion of the reference voltage generation circuit may be integrated on the first semiconductor chip or die, whereon the load **12** or at least a portion of the load **12** is also integrated. In some embodiments, all of the reference voltage generation circuit is integrated on the first semiconductor chip or die. In some embodiments, at least a portion of the collective analog-to-digital converter is integrated on the second semiconductor chip or die. In some embodiments, at least a portion of the reference voltage generation circuit is integrated on the second semiconductor chip or die with one or more other portions of the power delivery circuit **20**.

[0068] In some embodiments, current provided to load **12** may additionally or alternatively be used in any of error circuit **22**, error management circuit **24**, and switch control circuit **26** to generate the control signals for the power switches **28**. Sensing the current provided to load **12** can be done in either of the first and second die. The current provided to load **12** may also be sensed by sensing the voltage across the inductor(s) **30**.

[0069] FIG. **2** is a cross-sectional schematic view of a IC package **50** having power delivery system **20** and load **12**. As shown, IC package **50** includes first and second die **51** and **52** on substrate **55**. As understood by those of skill in the art, first and second die **51** and **52** may be electrically connected to one another, for example, through connectors on the first and second die and metal in the a package or printed circuit board. Additionally, first and second die **51** and **52** may be electrically connected to conductive pins or leads which extend so as to be exposed to components external to package **50** with one or more bond wires or other conductors. For example, first and second die **51** and **52** may be electrically connected with a communication bus.

[0070] Load **12** or at least a portion of load **12** may be integrated on the first die **51**. In addition, power switches **28** may be integrated on the second die **52**.

[0071] In some embodiments, a first portion of error circuit **22** is integrated on the first die **51**, where a second portion of error circuit **22** is integrated on the second die **52** along with error management circuit **24** and switch control circuit **26**.

[0072] In some embodiments, error circuit **22** is entirely integrated on the first die **51**, and error management circuit **24** and switch control circuit **26** are integrated on the second die **52**.

[0073] In some embodiments, a first portion of error management circuit **24** is integrated on the first die **51** along

with error circuit **22**, where a second portion of error management circuit **24** is integrated on the second die **52** along with switch control circuit **26**.

[0074] In some embodiments, error circuit **22** and error management circuit **24** are entirely integrated on the first die **51**, and switch control circuit **26** is integrated on the second die **52**.

[0075] In some embodiments, a first portion of switch control circuit **26** is integrated on the first die **51** along with error management **24** and error circuit **22**, where a second portion of switch control circuit **26** is integrated on the second die **52**.

[0076] In some embodiments, switch control circuit **26**, error circuit **22**, and error management circuit **24** are entirely integrated on the first die **51**.

[0077] In some embodiments, the inductors **30** are integrated on the second die **52**.

[0078] In some embodiments, the inductors **30** are external to both the first and second die **51** and **52**. For example, the inductors **30** may be formed by a metal on substrate **55** external to both the first and second die **51** and **52**, and electrically connected to either or both of the first and second die **51** and **52**. Alternatively, the inductors **30** may be connected external to package **50**, and electrically connected to either or both of the first and second die **51** and **52**.

[0079] In some embodiments, the capacitor **32** is integrated on the second die **52**.

[0080] In some embodiments, the capacitor **32** is external to both the first and second die **51** and **52**. For example, the capacitor **32** may be connected to substrate **55** external to both the first and second die **51** and **52**, and electrically connected to either or both of the first and second die **51** and **52**. Alternatively, the capacitor **32** may be connected external to package **50**, and electrically connected to first die **51** and/or to second die **52**.

[0081] In some embodiments, the capacitor **32** is integrated solely on the second die **52**.

[0082] In some embodiments power switches **28** are on integrated on the second die **52**. In some embodiments, for example, in embodiments using a boost regulator configuration, the power switches **28** are partially integrated on the second die **52**, and are partially integrated on the first die **51**.

[0083] In some embodiments only the power switches of the power delivery system **20** are integrated on the second die **52**, and the remainder of the power delivery system **20** is integrated on the first die **51**.

[0084] A separate fabrication process can be used to form the first and second die **51** and **52**, where the fabrication process of the first die is optimized for forming power semiconductors. This is one of the advantages of the disclosed allocations of circuitry onto the first and second die **51** and **52**. Circuitry that is preferentially fast can be integrated on to the second die **52**, where the process may be better for fast operation. The first die **51** can be in a process that is optimized for creating power switches.

[0085] In some embodiments, first and second die are positioned within 200-500 microns of one another. In some embodiments, the first and second die are close enough that the first and second die use high speed communications that enables the power delivery circuit **20** to deliver power to the load **12** without a capacitor **32** external to the first and second die or without a capacitor **32** external to package **50**. For example, capacitor **32** may be formed on the first die, on the second die, or within package **50** external to the first and second die. In some embodiments, capacitor **32** within the electronic package can be in the form of one or more discrete capacitors positioned within the electronic package.

[0086] In some embodiments the inductor that couples power to the load can be an air-core inductor, that is, an inductor without a magnetic core. Various embodiments can have a reduced need for capacitance of capacitor **32**, as compared to traditional architectures. Some embodiments have substantially reduced parasitics and delays, as compared to traditional architectures, allowing the power delivery circuit **20** to respond much faster to transient power requirements of the load **12**.

[0087] The load **12** and/or the portion of the power delivery circuit **20** integrated on the first die can communicate with and control the portion of the power delivery circuit **20** integrated on the second die via a communication bus. In some embodiments the communication bus is analog while in other embodiments it is digital, including but not limited to an I2C bus. In some configurations it is a high speed digital bus. In various embodiments the communication bus can be bi-directional such that the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die can send signals to the portion of the power delivery circuit **20** integrated on the second die, and the portion of the power delivery circuit **20** integrated on the second die can send signals to the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die. In some embodiments, the communication bus has one, two, three, four or more separate conductors. In some embodiments the communication bus has one or more of the following architectures and/or features:

[0088] In some multiphase embodiments, the number of phases of the power delivery circuit **20** is not communicated to the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die.

[0089] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to the portion of the power delivery circuit **20** integrated on the second die every time a pulse should be started (e.g., PWM Signal, off to high side on, or low side on to high side on, high side on to low side, or start a resonant pulse).

[0090] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to the portion of the power delivery circuit **20** integrated on the second die indicating which phase should be triggered next.

[0091] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to the portion of the power delivery circuit **20** integrated on the second die indicating information related to the output voltage. That information can contain one or more of: an error voltage, an absolute voltage, a current of the load, a digital representation of the output voltage, a digital representation of the error voltage, a processed (i.e., compensated version) of the error voltage that is an output of the compensation circuit, or any other information.

[0092] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to or receives a signal from

the portion of the power delivery circuit **20** integrated on the second die indicating the value of the reference voltage at node Vref.

[0093] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to the portion of the power delivery circuit **20** integrated on the second die indicating status information (e.g., how much current is being delivered, temperature, etc.).

[0094] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to the portion of the power delivery circuit **20** integrated on the second die indicating configuration information (e.g., desired voltage, compensation settings, power saving settings).

[0095] In some embodiments, the load **12** and/or the portion of the power delivery circuit **20** integrated on the first die sends a signal to or receives a signal from the portion of the power delivery circuit **20** integrated on the second die with information including:

[0096] A desired power state of the portion of the power delivery circuit **20** integrated on the first die (e.g. off, low power, high power, voltage of the integrated portion of the power delivery circuit).

[0097] On and off signals for each phase and/or each individual power switch integrated on the second die.

[0098] The state of one or more portions of the power delivery circuit **20** (e.g., current, temperature, voltage, current, error state, etc.).

[0099] FIG. **3** is a schematic illustration of a system including power delivery circuit **100** and load **175**. The system of FIG. **3** is an example embodiment of system **10** of FIG. **1**. Other embodiments can be used.

[0100] FIG. **3** depicts an illustrative simplified schematic of a power delivery control circuit **100** that can be used in a variety of electronic systems. As shown in FIG. **1**, the power delivery control circuit includes three phases **110**, **120**, and **130**, however in other embodiments the power delivery control circuit can have from one to any number of phases. Phases **110**, **120**, and **130** are collectively an embodiment of power switches **28** or power switches **28** and switch control **26** of system **10**. In some embodiments each phase can include one or more solid-state switches that regulate power delivered from a power source to a load. In various embodiments each phase can include an arrangement of sequentially coupled solid-state switches while in further embodiments each phase can include a pair of solid-state switches arranged in a synchronous buck converter topology, while in yet further embodiments each phase can be a full-bridge or other type of power regulator circuit.

[0101] As further illustrated in FIG. **3**, each phase is coupled to and controlled by a control circuit **150**. The control circuit **150** includes Vout and Vref nodes as inputs into an error amplifier **152**. Error amplifier **152** is an embodiment of error circuit **22** of system **10**. The error amplifier **152** generates an error voltage at node Verr based on the difference between Vout and Vref inputs. The error voltage can be used as an input into a Voltage to Time circuit **154**, which is an embodiment of error management circuit **24** of system **10**. In some embodiments, instead of using the error voltage as an input to the Voltage to Time circuit **154**, a signal that is derived from the error voltage can be used as an input. In one example the signal can be derived from a Type 2 compensation network. The Voltage to Time circuit **154** is configured to convert the error voltage, or the signal derived from the error voltage, to a controlled time (Tc). In some embodiments, the Voltage to Time circuit **154** sends a series of clock pulses to a phaser circuit **156**, where the time between the beginning of the pulses is equal or substantially equal to the controlled time (Tc). Phase circuit **156** is an embodiment of switch control circuit **26**.

[0102] When the phaser circuit **156** receives each clock pulse signal, it determines which of phases **110**, **120**, and **130** to trigger next and sends a trigger signal to the determined phase. For example, at very light loads only phase **110** may be repetitively triggered so the phaser circuit **156** only sends trigger voltages to phase **110** each time it receives a clock pulse signal. However, at large loads phase **120** may need to be triggered before all of the current or energy in phase **110** is delivered to the load so the phaser circuit **156** sends a first trigger signal to phase **110** and a second trigger signal to phase **120**, as illustrated in more detail herein.

[0103] In some embodiments, relatively large error voltages (e.g., when Vout is lower than Vref) indicate that more power is required at the load to raise Vout so the Voltage to Time Circuit decreases Tc so there is less time between triggering the phases **110**, **120**, and **130**. Similarly, when Vout is near Vref there is a relatively smaller error voltage that corresponds to an increase in Tc and a longer time between sequential phases, as described in more detail below.

[0104] In some configurations, the logic and control circuitry for one or more of the Voltage to Time circuit **154**, the phaser circuit **156**, and the phases **110**, **120**, and **130** are physically combined with or intermixed with or near one another.

[0105] FIG. **4** is a waveform diagram illustrating wave forms for signals of the power delivery control circuit **100** illustrated in FIG. **3**. Now referring to FIG. **5**, the waveforms for the power delivery control circuit illustrated in FIG. **3** are illustrated for a light load condition. The first waveform is the inductor current (Lres Current) the second waveform is the voltage, the third waveform is the clock pulse and the fourth, fifth and sixth are the trigger signals for triggering phase **1**, phase **2** and phase **3**, respectively.

[0106] As shown in FIG. **4**, for the given load condition, the Voltage to Time Circuit has set the time between the starts of the phase charging times as Tc. The phaser circuit triggers phase **110** to execute one cycle which causes an amount of charge or current or energy to be delivered to the inductor of the illustrated LC filter. After the time Tc has expired, the Voltage to Time Circuit **154** sends a second pulse to the phaser circuit **156**. In this case the phaser circuit **156** triggers phase **120** to execute one cycle which causes an amount of charge or current or energy to be delivered to the inductor of the illustrated LC filter. After the time Tc has expired, the Voltage to Time Circuit **154** sends a third pulse to the phaser circuit **156**. In this case the phaser circuit **156** triggers phase **130** to execute one cycle which causes an amount of charge or current or energy to be delivered to the inductor of the illustrated LC filter.

[0107] In some embodiments, the amount of charge or current or energy delivered to the inductor by each of the phases **110**, **120**, and **130** may be controlled. For example, the amount of charge or current or energy may be controlled by design of the components of the power delivery control circuit **100**, or may be controlled by controlling signals of the power delivery control circuit **100**. For example, phaser

circuit **156** may be configured to trigger phases **110**, **120**, and **130** by delivering pulses of variable widths, where the pulse width is controlled by a controller. Alternatively, each of phases **110**, **120**, and **130** may be configured to deliver a variable amount of charge or current or energy, where the amount is controlled by the controller. Other mechanisms of controlling the charge or current or energy delivered to the inductor by each of the phases **110**, **120**, **130** may additionally or alternatively be used.

[0108] After the time Tc has expired, the Voltage to Time Circuit **154** sends a fourth pulse to the phaser circuit **156**. In this case the phaser circuit **156** triggers phase **110** to execute one cycle which essentially sends a controlled amount of energy to the connected inductor and out to the load. After the time Tc has expired, the Voltage to Time Circuit **154** sends a fifth pulse to the phaser circuit **156**. In this case the phaser circuit **156** decides to trigger phase **120** to execute one cycle which essentially sends a controlled amount of energy to the connected inductor and out to the load.

[0109] In some embodiments the power delivery control circuit **100** and/or phaser circuit **156** may have one or more of the following features:

[0110] Charge mode control, where the phaser circuit **156** is configured to arbitrate which phase to fire next. In some embodiments, the charge delivered to the inductor during each cycle is controlled. In some embodiments, the current delivered to the output capacitor and load starts at zero and returns to zero in response to each pulse from the Voltage to Time Circuit **154**.

[0111] At light loads, the time between a phase being fired again can be large. During an 'off' time between firing of phases, the phase is does not deliver current to the inductor, and as such can be considered 'off' or 'shed'. In other words, phase shedding can be an automatic by product of this control scheme.

[0112] This auto phase shedding can also allow for portions of the phase to be turned off while the phase is shed. For example, a bias current to the phase may be turned down or off to reduce power consumption and heat.

[0113] In some embodiments some of the features of the power delivery control circuit **100** are:

[0114] Time based control loop architecture.

[0115] Each time a phase is 'fired' or 'triggered' it delivers a 'quantity of charge' to the output.

[0116] The control loop determines 'Tc', the time between successive phase triggering. The smaller the 'Tc', the quicker next phase gets fired. In other words, 'Tc' determines the rate at which 'quantities' of charge get delivered to the output.

[0117] A Control Timer circuit can be configured to monitor the output voltage and the commanded/desired voltage (DAC voltage) to calculate the precise 'Tc' required.

[0118] The Control Timer circuit can be digital, analog, or a combination thereof.

[0119] The power delivery control circuit can utilize digital technology, analog technology or a combination of digital and analog technologies. More specifically, in some embodiments signals such as, but not limited to, the error voltage and the output voltage can be analog signals or digitized signals. The timer can be a digital programmed timer or an analog timer that charges a capacitor. Similarly logic functions can be performed with digital data or analog comparators. Any combination of technologies can be employed and this disclosure is in no way limited to a particular digital or analog technology to perform any particular function.

[0120] FIG. **5** is a waveform diagram illustrating wave forms for signals of the power delivery control circuit **100** illustrated in FIG. **3**. Now referring to FIG. **5**, high load waveforms are illustrated for the power delivery circuit shown in FIG. **3**. As shown in FIG. **5**, phase **110**, phase **120** and phase **130** trigger pulses are much closer together such that a much higher average charge or current or energy is transferred to the load than for the low load case illustrated in FIG. **4**. More specifically, the charge or current or energy delivered by each phase overlaps in time with the charge or current or energy delivered by each adjacent phase as shown by the Lres Current waveform.

[0121] FIG. **6** is a diagram illustrating an example embodiment of Tc and Verr dependence on load current. In alternative embodiments, the Tc and Verr dependence on load current has characteristics which are not illustrated in FIG. **6**. For example, in some embodiments, the Tc and/or Verr dependence on load current is not linear. As shown in FIG. **6**, as load current increases, Verr increases, and Tc reduces. In addition, as illustrated in FIG. **5**, as load current increases, CLK pulses occur more frequently. At high enough load current conditions the output of the phases overlap to provide an increased output current and can seamlessly transition into continuous conduction mode (CCM) operation for delivering even higher current. In some embodiments a CCM circuit such as those disclosed in U.S. patent application Ser. No. 15/640,335 filed on Jun. 30, 2017 which is incorporated herein by reference in its entirety for all purposes, can be used with the power delivery control circuit **100**.

[0122] FIG. **7**A is a schematic illustration of a power delivery engine **500**. In this embodiment, power delivery engine **500** comprises a power regulator circuit. Now referring to FIG. **7**A a non-limiting example schematic of a power delivery engine **500** that can be used for each phase of the power delivery control circuit **100** illustrated in FIG. **3** is shown. In this example the power delivery engine **500** includes a plurality of sequentially coupled power switches M**1**, M**2**, M**3**, and M**4**.

[0123] FIG. **7**B illustrates one example of the waveforms for the power delivery engine **500** illustrated in FIG. **7**A. These circuits and others are described in more detail in U.S. Pat. No. 9,300,210 issued on Mar. 29, 2016, which is incorporated by reference herein in its entirety for all purposes.

[0124] Trace **805** illustrates a control voltage applied to first solid-state switch **130**. In the particular embodiment depicted, switches are turned on when approximately 1 volt is applied. At time t**1** trace **805** is at approximately 0 volts thus first solid-state switch **130** is off. Trace **810** illustrates a control terminal voltage applied to second solid-state switch **140**. At time t**1** trace **810** is at approximately 1 volt thus second solid-state switch is on. Trace **815** illustrates a control terminal voltage applied to third solid-state switch **150**. At time t**1** trace **815** transitions to approximately 1 volt thus third solid-state switch **150** transitions from off to on. Trace **820** illustrates a control terminal voltage applied to fourth solid-state switch **160**. At time t**1** trace **820** is at approximately 0 volts thus fourth solid-state switch is off.

[0125] Trace **825** illustrates a voltage at second junction **145**. At time t**1**, capacitor **170** is shorted. Trace **830** illustrates current through inductor **173**. At time t**1** inductor **173** is decoupled from the remainder of switched regulation circuit **125** thus the current in inductor **173** is zero. Trace **835** illustrates a comparator output corresponding to a zero current condition in inductor **173**, as discussed in more detail below. Trace **840** illustrates the voltage across capacitor **170**. At time t**1** capacitor **170** is shorted causing the voltage across capacitor **173** to decrease as the capacitor is discharged.

[0126] Now referring to FIG. **8** a non-limiting example schematic of a power delivery engine **600** that can be used in each phase of the circuit **100** illustrated in FIG. **3** is shown. In this example the power delivery engine **600** includes a two coupled power switches **610** and **620** arranged in a synchronous buck converter configuration, as known in the art. Other embodiments can have different power delivery engines including, but not limited to full bridge, buck, boost, buck boost, and other types of power control circuits known by one of skill in the art.

[0127] Now referring to FIG. **9** a transient performance boost circuit **700** is shown that can be used instead of control circuit **150** in the power delivery control circuit **100** illustrated in FIG. **3**.

[0128] In some embodiments the transient performance boost circuit **700** can include one or more of the following features:

[0129] For fast transient response, the error voltage generation **710** can incorporate multiple enhancement schemes.

[0130] One such scheme temporarily increases the GM of an error amplifier in the Error Voltage generation **710**. The increase in GM helps the control voltage "Ve" quickly ramp up or down in response to the error voltage seen at the input (Vout-Vdac).

[0131] Another scheme employs a feed forward signal (Ie) supplied from the error amplifier and delivered to the timer such that during a transient an error current bypasses the compensation network **720** and quickly changes the timer circuit **730** output (Increases or decreases the frequency of phase firing).

[0132] Another scheme employs a fixed offset in the timer circuit **730**. Detecting a transient, the offset can be either increased or decreased instantly such that the frequency change is instant giving a rapid response.

[0133] Another scheme employs multiple bands of frequency of operation. Timer circuit **730** is configured to generate a range of output frequencies corresponding with the functional range of control voltage (Ve). In a multiple frequency band scheme, timer circuit **730** is programmable so as to generate a different range of output frequencies for each frequency band. Accordingly, when using a multiple frequency band scheme, the frequency generated by timer circuit **730** is determined based on both the control voltage (Ve) and the programmed frequency band. Control of the output frequency is achieved through a combination of response to error voltage for fine control and frequency band selection for coarse control.

[0134] During transient conditions, bands can be hopped (band hopping) up or down to quickly achieve the desired operating frequency. For example, in response to the control voltage (Ve) saturating, by being driven outside its functional range, timer circuit **730** may be programmed by a controller to operate in an appropriate adjacent higher or lower frequency band. Alternatively or additionally, timer circuit **730** may be programmed by a controller to operate in a higher or lower frequency band in response to the control voltage (Ve) increasing or decreasing at a rate greater than a threshold.

[0135] In some embodiments bump type sequencing of each phase can be used when a plurality of serially coupled power devices are used, for example, as described in application Ser. No. 15/640,335 filed on Jun. 30, 2017 and U.S. Pat. No. 9,300,210 issued on Mar. 29, 2016, which are incorporated herein in their entirety by reference. The bump type sequencing can include one or more of the following features:

[0136] Each phase can deliver two types of "Bumps" or charge delivery sequences, named VDD bump and GND bump, a VDD bump caused by current sourced from or sunk by the VDD power supply being sunk by or sourced from the connected inductor, and a GND bump caused by current sourced from or sunk by the connected inductor being sunk by or sourced from the GND power supply.

[0137] The phases may collectively deliver these two bumps strictly in alternate sequence. VDD=>GND=>VDD=>GND and so on. For example, this may occur by each of the phases delivering alternating bumps (VDD=>GND=>VDD=>GND and so on.)

[0138] In some embodiments, an alternative bump sequence may be preferred.

[0139] For example, a VDD bump may excite the supply network more than a GND bump. Therefore, the phases in a multiphase system may collectively deliver more GND bumps than VDD bumps.

[0140] In some systems, a frequency of the VDD bumps and/or the GND bumps may be controlled through selection of a VDD/GND bump sequence.

[0141] In some embodiments the phase firings can be sequenced to achieve an arbitrary bump sequence. For instance a 3 phase system can deliver VDD=>VDD=>VDD=>GND=>GND=>GND sequence. Or it can also deliver VDD=>GND=>VDD=>GND=>VDD=>GND sequence. The bump sequence used can affect the frequency at which the input network is excited.

[0142] Depending on the input impedance network, an optimal choice of bump sequence can be programed to achieve the optimal supply noise characteristics.

[0143] The power supply switching frequency can be kept away from the input network resonant frequency (or where the input impedance is large).

[0144] This feature can also help during transient response at least because the current load on the power supplies are distributed in time. As a result, the bypass capacitance and low power bus impedance are sufficient to prevent unacceptable power supply transients. Therefore, the voltage difference between the positive and negative power supplies remains substantially fixed.

[0145] In some embodiments, the bump sequence of each of the phases is controlled using methods discussed in described in application Ser. No. 15/640,335

filed on Jun. 30, 2017 and U.S. Pat. No. 9,300,210 issued on Mar. 29, 2016, referenced above. To coordinate a collective bump sequence collectively generated by the multiple phases, a controller receives or determines a target collective bump sequence, and determines a bump sequence for each of the phases. The controller provides signals for each of the individual phases so as to cause each of the individual phases to operate with the bump sequence determined therefor by the controller. Accordingly, each of the individual phases operate with the bump sequence determined therefor, and the collective bump sequence generated by the multiple phases correspondence with the target collective bump sequence.

[0146] Now referring to FIG. **10**, a comparator mode control circuit **800** can be used instead of control circuit **150** in the power delivery control circuit **100** illustrated in FIG. **3**. The comparator mode control circuit **800** can combine the output of the timer **810** with the output of a comparator **820** so the decision to trigger the next phase includes the following conditions: 1) has the timer expired? and 2) is the output voltage below a threshold voltage? Both of these conditions must be true for the next phase to trigger. This feature can be particularly useful for semiconductor processes where a timer with a wide time range is difficult to make so at light loads the comparator can be relied upon such that the next phase will only be triggered if the output voltage goes below a threshold voltage. In some embodiments the comparator mode control can have one or more of the following features:

[0147] Comparator mode control circuit **800** may be used in addition to one or more other control schemes. For example, comparative mode control circuit **800** and control circuit **150** may both be used. Which control circuit is active to be determined, for example, based on load conditions. For example, comparator more control mode control circuit **800** may be used when the load is less than a threshold.

[0148] Band hopping along with a comparator can be used to provide a fast transient response.

[0149] The comparator mode control is also useful during Start up, Dynamic Voltage Scaling (DVS) Up and DVS Down. In comparator mode overshoot and undershoot is minimized based on the state of the comparator output.

[0150] In some embodiments, the comparator **820** is hysteretic.

[0151] In some embodiments a comparator control circuit can be included as a portion of the phaser circuit. More specifically, a comparator control circuit can use Vout and the clock signal to only allow the phaser to execute a phase if Vout is below a predetermined voltage and a clock signal is received from the Voltage to Time circuit. This feature can protect against the phaser sending trigger signals to one or more phases if Vout is above the predetermined voltage but due to transients or bandwidth limitations of the control circuit one or more clock signals are sent. Because Vout is above the predetermined voltage no phases will be triggered.

[0152] In some embodiments any logical combination of Vout and the timer output can be used as an input to the phaser. In various embodiments the comparator control circuit can be implemented via analog circuitry, digital circuitry or a combination thereof. In one example, the output voltage can be digitized, the timer can be digital and a digital processor can be used to make a logical decision whether or not to transmit a pulse to the phaser.

[0153] Now referring to FIGS. **11** and **12**, an embodiment of a voltage to time circuit **900** is illustrated. Voltage to time circuit **900** can be used with the power delivery control circuit shown in FIG. **3**. In some embodiments the voltage to time circuit **900** can have one or more of the following features:

[0154] The trip voltage can be dynamically changed to get faster response during a transient. For example, during a loading transient trip voltage can be decrease.

[0155] For DVS up transition, trip voltage can be decreased while for a DVS down transition, trip voltage can be increased.

[0156] The capacitance of capacitor C can be changed to increase or decrease the clock output frequency

[0157] FIGS. **13** and **14** illustrate an embodiment of a voltage to time circuit. Now referring to FIGS. **13** and **14**, an embodiment of a voltage to time circuit **1100** is illustrated. Voltage to time circuit **1100** can be used with the power delivery circuit shown in FIG. **3**. In some embodiments the voltage to time circuit can have one or more of the following features:

[0158] Timer current can be programmable to give control on the clock frequency range.

[0159] Timer current can be dynamically changed to improve transient response, for example, during loading transient, the timer current can be increased to generate faster clock frequency.

[0160] During DVS up, timer current can be increased.

[0161] The capacitance of capacitor C can be changed to increase or decrease the clock output frequency.

[0162] FIGS. **15** and **16** illustrate an embodiment of inductor shorting circuit Lshort. In this embodiment inductor shorting circuit Lshort is a switch. Now referring to FIGS. **15** and **16**, in some embodiments inductor shorting can be used to improve linearity of the power delivery circuit shown in FIG. **3**. Inductor shorting can include one or more of the following features:

[0163] During discontinuous current mode (DCM) operation, the phase circuit of FIG. **15** presents a high impedance to the switching node Vx. As a result, the voltage at switching node Vx and the current through the inductor ring based on the capacitances, resistances, and inductances of the circuit according to principles understood by those of skill in the art. The ringing may not be desired in some embodiments since it leaves the starting current in the inductor at the beginning of the next cycle, when switching node Vx is again driven by the phase, in an uncontrolled state. The uncontrolled state is at least partially influenced by previous data, such that the uncontrolled state causes non-linearity.

[0164] An inductor shorting circuit Lshort can be used such that while the inductor is not driven by the phase, the switching node Vx and the output Vout are shorted.

[0165] The shorting causes the inductor current to be equal or substantially equal to zero. This allows for the next cycle of that phase, when switching node Vx is again driven by the phase, to begin with a controlled and/or consistent zero or substantially zero or near zero current instead of starting in the uncontrolled state, which may be either a positive or a negative current.

[0166] To short the inductor, inductor shorting circuit Lshort becomes conductive while the phase connected

thereto is in a high impedance state (for example, as is common to multiple parallel coupled FETS and Buck architectures). Inductor shorting circuit Lshort may remain on for a small predetermined amount of time or may stay on until just before the phase is fired again.

[0167] The inductor shorting circuit Lshort shorts the output inductor and provides a low impedance path for charging the parasitic capacitance at switching node Vx to the voltage at node Vout.

[0168] Because Lout and Cout form an LC oscillator, without the inductor shorting circuit Lshort, the parasitic node may ring undesirably.

[0169] In another embodiment, the inductor shorting circuit Lshort can electrically short the switching node Vx to another voltage source (Supply for example) for a brief amount of time to charge the switching node Vx to the supply voltage, after which the inductor shorting circuit Lshort may be opened. By charging the switching Vx node to the supply voltage, the ringing may be greatly reduced and/or may be controlled such that the next cycle of the phase, when switching node Vx is again driven by the phase, begins with a consistent current instead of starting in the uncontrolled state.

[0170] Now referring to FIG. **9** a transient performance boost circuit **700** is shown that can be used instead of control circuit **150** in the power delivery control circuit **100** illustrated in FIG. **1**. In some embodiments the transient performance boost circuit **700** can include one or more of the following features:

[0171] FIG. **17** is a schematic illustration of a control timer circuit **1500**. Now referring to FIG. **17**, a control timer **1500** is shown that can be used instead of control circuit **150** in the power delivery control circuit **100** illustrated in FIG. **3**. In this embodiment, a compensation network **1520** is coupled between the Error Amplifier **1510** and the Voltage to Time circuit **1530**. In various embodiments the compensation network **1520** is used to improve the stability of the Verr signal to make the feedback loop more stable and reliable. In one example embodiment the compensation network **1520** can include a capacitor to ground as shown. In further embodiments, illustrated in FIGS. **18**, **19** and **20**, the compensation network can include a Type 3, a Type 2 or a Type 1 compensation circuit, respectively, as known by those of skill in the art. Other compensation networks can also be used and this disclosure is in no way limited to the disclosed example compensation networks. For example, as illustrated in FIG. **17**, another scheme employs a feed forward signal (Ie) from the error amplifier **1510** to the timer **1530** such that during a transient an error current bypasses the compensation network and quickly changes the timer output (e.g., increases or decreases the frequency of phase firing).

[0172] In some embodiments one or more telemetry features can be implemented for the power delivery control circuitry **100** illustrated in FIG. **3**. For example, in one embodiment telemetry circuitry can be configured to record digital or analog data from the power delivery and control circuitry that corresponds to the current output, voltage output or other characteristic of the power delivery and control circuitry. In some embodiments the power delivery and control circuitry **100** can be used in conjunction with an integrated circuit that includes a processor wherein the processor can be commanded to record the telemetry data and store the telemetry data in an associated memory. In various embodiments the telemetry data can be recorded only when commanded, or in other embodiments it can be recorded continually, for example when used in conjunction with a FIFO memory.

[0173] In some embodiments the telemetry circuitry can acquire data associated with the current output of the power delivery and control circuitry **100** by recording data representing the Verr signal generated by the Error Amplifier **152** since the Verr signal can be correlated to the output current. In other embodiments the telemetry circuitry can acquire data corresponding to the frequency of the clock pulses sent by the Voltage to Time (Tc) circuit **154** which can also be correlated with the output current. The accuracy of the telemetry data and how precisely it is correlated to the actual current delivered by the power delivery and control circuitry can be affected by how well controlled and/or known the characteristics of the components of the power delivery and control circuitry are. For example, the specific values of the capacitors, inductors and resistors can affect the accuracy of the data, therefore to improve the accuracy the tolerance on such components can be either highly controlled and/or the components can be characterized and the system can be trimmed to compensate for the characteristics, thereby improving the accuracy.

[0174] For simplicity, various peripheral electrical components are not shown in the figures.

Regulator with Continuous Current

[0175] In some embodiments power delivery control circuit **100** (see FIG. **3**) can be configured to provide continuous current and/or an increase in current to the load by continuously maintaining the current in the inductor of at least one of the phases **110**, **120**, **130** above zero, as described in more detail below.

[0176] Now referring simultaneously to FIGS. **7**A, and **19-26** an example switching sequence and timing diagram for an embodiment of switched regulation circuit **125** (see FIG. **7**A) with continuous and/or increased current is illustrated. More specifically, FIG. **7**A illustrates a simplified schematic of switched regulation circuit **125**; FIG. **21** illustrates an example switching sequence **1900** having sequential steps **1905** through **1940** for the four switches in switched regulation circuit **125**; FIG. **22** illustrates an example timing diagram showing the control signals delivered to each of the four solid-state switches as well as the current within inductor **173** (IL), and the voltage at second junction **145** (V**145**) during switching sequence **1900**; and FIGS. **23-28** illustrate simplified circuit schematics of each of the six different solid-state switch configurations described in switching sequence **1900**. In FIGS. **23-28** solid-state switches that are in an on state are depicted with solid lines and solid-state switches that are in an off state are depicted with dashed lines. The switching sequence illustrated in FIG. **21** is for example only and other switching sequences, timings and configurations are within the scope of this disclosure.

[0177] Now referring to FIG. **21**, switching sequence **1900** having sequential steps **1905** through **1940** is illustrated. In step **1905**, first, second and third solid-state switches M**1**, M**2** and M**3**, respectively, are controlled to be in an on state and fourth solid-state switch M**4** is controlled to be in an off state. A simplified schematic of switched regulation circuit **125** in step **1905** is illustrated in FIG. **23**. Step **1905** is a first

inductor prefluxing state where current in inductor **173** (see FIG. **7**A) is increased at a substantially linear rate by the application of the input voltage at first terminal **120** (Vin) across the inductor, at a time before capacitor **170** is charged.

[0178] Example currents and voltages within switched regulation circuit **125** for step **1905** are illustrated in timing diagram **2000** (see FIG. **22**). The logic levels for solid-state switch control signals M**1**, M**2**, M**3**, M**4** are indicated by traces **2005**, **2010**, **2015** and **2020**, respectively. A high logic level (sometimes noted as 1) indicates the switch (or composite switch) is in an on state, and a low logic level (sometimes noted as 0) indicates the switch is in an off state.

[0179] Timing diagram **2000** illustrates that first step **1905** occurs at time t**1**. At time t**1**, trace **2005** shows that a high logic level control signal is applied to first solid-state switch **130**, placing it in an on state. Trace **2010** illustrates that at time t**1** a high logic level control signal is applied to second solid-state switch **140**, placing it in an on state. Trace **2015** illustrates that at time t**1** a high logic level control signal is applied to third solid-state switch **150**, placing it in an on state. Trace **2020** illustrates that at time t**1** a low logic level control signal is applied fourth solid-state switch **160**, placing it in an off state.

[0180] Continuing to refer to timing diagram **2000**, at t**1** a voltage at second junction **145** (see FIG. **7**A) is illustrated by trace **2025** and is substantially equivalent to the Vin voltage (minus a relatively small voltage drop across M**1** and M**2**) at first node **120**. Current in inductor **170** (IL trace **2030**) increases rapidly, corresponding to the applied voltage and the characteristics of inductor **173**. For some embodiments, the voltage at node **176** (see FIG. **7**A) may change a relatively small amount compared with the voltage across the inductor and thus the current may increase substantially linear at a rate approximated by (Vin−Vout)/L where Vout is the voltage at node **176**. The current in inductor **173** continues to increase while in this switch state, the duration of which may be controlled by a timer, shown in step **1910** as a delay.

[0181] In some embodiments the timer in step **1910** can be fixed while in other embodiments it can be a variable timer. In one example the variable timer can use a lookup table to adjust according to different load conditions and demands on switched regulation circuit **125**. More specifically, in some embodiments the timer can be set proportional to a "duty factor" (e.g., Vout/Vin) such that a longer amount of time is selected when a higher Vout is required. In further embodiments the timer in step **1910** can be controlled by a feedback loop based on one or more characteristics of switched regulation circuit **125**. In some embodiments the timer may be adjusted by the feedback loop to energize inductor **173** with an appropriate amount of current so that the inductor current resonates to a predetermined current when the first resonating state is engaged (discussed in the next step **1915**). In further embodiments the timer can use a comparator that compares the current in the inductor to a programmable current threshold.

[0182] In other embodiments, the timer can be made utilizing a current on a capacitor wherein the current starts charging at the beginning of the preflux cycle and may be compared to a predetermined voltage. When the voltage on the capacitor reaches a specified voltage the timer indicates that the preflux cycle should end. In other embodiments the timer function can be performed utilizing logic gates.

[0183] In some embodiments, instead of a timer for setting the amount of preflux, the current in the inductor can be monitored during preflux (e.g., step **1905**) and the preflux cycle can be set to end when the current reaches a specified level. That specified current level can be adjusted on a cycle by cycle basis to optimize performance. Other timer techniques and timer architectures can be used and are within the scope of this disclosure.

[0184] Now referring to FIG. **21**, after the delay in step **1910**, the controller advances to step **1915** where first and third solid-state switches M**1** and M**3** remain on while the second solid-state switch M**2** is turned off and the fourth solid-state switch M**4** remains off. Thus, first and third solid-state switches, M**1**, M**3**, respectively, are on while second and fourth solid-state switches M**2**, M**4**, respectively, are off. A simplified schematic of switched regulation circuit **125** in step **1915** is illustrated in FIG. **24**. This state couples capacitor **170** in series with inductor **173** and the voltage at first terminal **120** (Vin) is applied directly to second junction **145**. Capacitor **170** now begins to charge. Capacitor **170** charges with a time constant set by capacitor **170** and inductor **173** values. Further, as capacitor **170** begins to charge, current flow in inductor **173** continues to increase as the voltage between second junction **145** and the output is positive. Because of the prefluxing operation in step **1905**, the current that was already flowing in inductor **173** continues to increase, as discussed in more detail below.

[0185] Step **1915** is illustrated in timing diagram **2000** (see FIG. **22**) at time t**2**. Now referring simultaneously to FIGS. **7**A and **20**, at time t**2**, second solid-state switch **140** (i.e., trace **2010**) turns off. The voltage at second junction **145** (i.e., trace **2025**) begins to decrease. Current in inductor **173** (trace **2030**) continues to build as capacitor **170** charges. Voltage in capacitor **170** increases towards Vin. As capacitor **170** becomes charged the current in inductor **173** (trace **2030**) peaks, then begins to decrease when the voltage at node **145** equals the voltage at node **176** and continues to decrease towards time t**3**. Thus, in step **1915**, capacitor **170** charges, causing a current to flow in inductor **173**, and increasing the voltage at output node **176** (Vout). When capacitor **170** is fully charged to the voltage at (Vin) **120**, the controller proceeds to step **1920** (see FIG. **21**) which is a first "soft braking" configuration that can be used to transition the current remaining in inductor **173**. Soft braking can enable a higher current per phase and/or a smaller capacitor **170** per phase as compared to the methodologies discussed above and as explained in more detail below.

[0186] In the first soft braking configuration (step **1920**) first, third and fourth solid-state switches M**1**, M**3** and M**4**, respectively, are on while second solid-state switch M**2** is turned off. A simplified schematic of switched regulation circuit **125** in step **1920** is illustrated in FIG. **25**. In this state inductor **173** is coupled to Vin (node **120**) through capacitor **170** and also to ground **165** through third and fourth solid-state switches, M**3** and M**4**, respectively, allowing the residual current in the inductor to continue to decrease down to a non-zero minimum current (Imin).

[0187] Step **1920** is illustrated in timing diagram **2000** (see FIG. **22**) at time t**3**. Now referring simultaneously to FIGS. **7**A and **20**, at time t**3**, fourth solid-state switch **160** (i.e., trace **2020**) turns on adding a path between inductor **173** and ground **165**. The voltage at second junction **145** (i.e., trace **2025**) remains at the ground potential and current in inductor **173** (trace **2030**) continues to decrease as the inductor

dissipates its stored energy. Current in inductor **173** continues to decrease to a predetermined minimum current (Imin) that is non-zero in this particular embodiment. In some embodiments the minimum current (Imin) can be between 10 milliamps and 50 amperes, while in other embodiments it can be between 100 milliamps and 1 ampere and in another embodiment it can be between 200 milliamps and 400 milliamps. The controller then proceeds to step **1925** (see FIG. **21**) that is a second prefluxing state that can be used to increase current flowing through inductor **173**.

[0188] Now referring to FIG. **21**, in step **1925** first fourth solid-state switches, M**1** and M**4** remain on, second solid-state switch M**2** turns on, and third solid-state switches M**3** remains off. A simplified schematic of switched regulation circuit **125** in step **1925** is illustrated in FIG. **26**. This is the second inductor prefluxing stage where current in inductor **173** is increased at a substantially linear rate by applying voltage at first output terminal **120** (Vin) to the inductor. In this state the voltage at first terminal **120** (Vin) is applied directly across inductor **173**.

[0189] Now referring to timing diagram **2000**, the second prefluxing state (step **1925**) is shown at t**4**. The voltage at second junction **145** rapidly increases to the Vin voltage at first node **120** shown by trace **2025**. Current in inductor **170** (trace **2030**) increases rapidly, corresponding to the applied voltage and the characteristics of inductor **173**. In some embodiments the rate of current increase can be substantially similar to the rate of current increase in the time between t**1** and t**2**. The current in inductor **173** continues to increase until the switch state is changed, which in one embodiment, may be controlled by a delay shown in step **1930** that can be controlled by a timer, as discussed above.

[0190] Now referring to FIG. **21**, in step **1935** fourth solid-state switch M**4** remains on and second solid-state switch M**2** is turned on while first and third solid-state switches M**1**, M**3**, respectively, remain off. A simplified schematic of switched regulation circuit **125** in step **1935** is illustrated in FIG. **27**. Capacitor **170** is connected between inductor **173** and ground **165**, allowing the charge stored in the capacitor to discharge through the inductor to load **115** (see FIG. **1**). As capacitor **170** begins to discharge (with a time constant set by capacitor **170** and inductor **173**), current in inductor **173** increases. This condition is illustrated in timing diagram **2000** in FIG. **22** at time t**5** showing the voltage at second junction **145** (i.e., trace **2025**) at a voltage that is close to the voltage at Vin (**120**) as it is connected to fully charged capacitor **170**. As capacitor **170** resonates with inductor **173**, it discharges causing current to increase in inductor **173** (i.e., trace **2030**). The increase in current causes the voltage at Vout (node **176**) to increase. As the charge stored in capacitor **170** is reduced, current in inductor **173** peaks (Ipeak), then begins to decrease (trace **2030**).

[0191] The controller then proceeds to step **1940** (see FIG. **21**) which is a second "soft braking" configuration that can be used to transition the remaining current in inductor **173**. Soft braking can enable a higher current per phase and/or a smaller capacitor **170** per phase as discussed above.

[0192] More specifically, in step **1940** second, third and fourth solid-state switches M**2**, M**3** and M**4**, respectively, are on while first solid-state switch M**1** is turned off. A simplified schematic of switched regulation circuit **125** in step **1935** is illustrated in FIG. **28**. In this state inductor **173** is coupled to ground **165** through third and fourth solid-state switches, M**3** and M**4**, respectively, allowing the residual current in the inductor to continue to decrease down to a non-zero minimum current (Imin).

[0193] Step **1940** is illustrated in timing diagram **2000** (see FIG. **22**) at time t**6**. Now referring simultaneously to FIGS. **7**A and **20**, at time t**6**, third solid-state switch **150** (i.e., trace **2015**) turns on adding a path between inductor **173** and ground **165**. The voltage at second junction **145** (i.e., trace **2025**) remains at the ground potential and current in inductor **173** (trace **2030**) continues to decrease as the inductor dissipates its stored energy. Current in inductor **173** continues to decrease to a predetermined minimum current (Imin) that is non-zero in this particular embodiment. The controller then returns to step **1905** (see FIG. **21**) which is the first prefluxing state that can be used to increase current flowing through inductor **173**.

[0194] Timing diagram **2000** in FIG. **22** is for illustration only and is one example of the function of circuit **125** (see FIG. **7**A) operating with a non-zero inductor current. Other switching algorithms, control functions and features can be implemented without departing from this disclosure. To control the duration of any of steps **1905**-**1940** illustrated in FIG. **21** any type of timer or control circuit can be used, including those disclosed herein. For example, in some embodiments a comparator can be used to compare output voltage (Vout) to a commanded voltage. If the output voltage is too low the controller can shorten the soft brake duration and start the next preflux step early, leading to a higher output voltage and higher average output current delivered to load (see FIG. **7**A). This control algorithm can also provide a relatively fast response time to loads having high transient voltage requirements. In further embodiments a multi-phase architecture can be employed where multiple switched regulation circuits **125** (see FIG. **2**) are used together to provide power to load **115**.

[0195] In further embodiments alternative switching sequences **1900** can be used to provide additional features and functions of switched regulation circuit **125** (see FIG. **7**A). For example, wait states can be added after first and second soft brake steps (steps **1920** and **1940**, respectively) to provide light load performance. More specifically, when load **115** (see FIG. **7**A) requires a reduced amount of current and/or voltage, after first softbrake (step **1920**) a wait state can be commanded where first and fourth solid-state switches, M**1** and M**4**, respectively are on and second and third solid-state switches, M**2** and M**3** are off. This essentially halts current flow through circuit **125** to load **115** (see FIG. **7**A) until the subsequent preflux step **1925** is commanded. Similarly, after second soft brake (step **1940**) a second wait state can be commanded where second and third solid-state switches, M**2** and M**3**, respectively, are on and first and fourth solid-state switches, M**1** and M**4**, respectively, are off. This state essentially halts current flow through circuit **125** until the subsequent preflux step **1905** is commanded.

[0196] In some embodiments a comparator control circuit can be included as a portion of the phaser circuit. More specifically, a comparator control circuit can use Vout and the clock signal to only allow the phaser to execute a phase if Vout is below a predetermined voltage and a clock signal is received from the Voltage to Time circuit. This feature can protect against the phaser sending trigger signals to one or more phases if Vout is above the predetermined voltage but due to transients or bandwidth limitations of the control

circuit one or more clock signals are sent. Because Vout is above the predetermined voltage no phases will be triggered.

[0197] In the foregoing specification, embodiments of the disclosure have been described with reference to numerous specific details that can vary from implementation to implementation. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense. The sole and exclusive indicator of the scope of the disclosure, and what is intended by the applicants to be the scope of the disclosure, is the literal and equivalent scope of the set of claims that issue from this application, in the specific form in which such claims issue, including any subsequent correction. The specific details of particular embodiments can be combined in any suitable manner without departing from the spirit and scope of embodiments of the disclosure.

[0198] Additionally, spatially relative terms, such as "bottom or "top" and the like can be used to describe an element and/or feature's relationship to another element(s) and/or feature(s) as, for example, illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use and/or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as a "bottom" surface can then be oriented "above" other elements or features. The device can be otherwise oriented (e.g., rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0199] Various details are set forth herein as they relate to certain embodiments. However, the invention can also be implemented in ways which are different from those described herein. Modifications can be made to the discussed embodiments by those skilled in the art without departing from the invention. Therefore, the invention is not limited to particular embodiments disclosed herein.

[0200] Though the present invention is disclosed by way of specific embodiments as described above, those embodiments are not intended to limit the present invention. Based on the methods and the technical aspects disclosed herein, variations and changes may be made to the presented embodiments by those of skill in the art without departing from the spirit and the scope of the present invention.

1. (canceled)

2. A system comprising:

a substrate;

a first semiconductor die disposed on the substrate and including a load circuit;

a second semiconductor die disposed on the substrate and including a power converter circuit arranged to deliver power to the load circuit, the power converter circuit including a plurality of power switches coupled to a control circuit; and

wherein the control circuit is arranged to control a power delivered to the load circuit via the plurality of power switches.

3. The system of claim **2**, wherein the first semiconductor die further comprises an error signal generation circuit.

4. The system of claim **3**, wherein the control circuit is arranged to control the power delivered to the load circuit in response to receiving an error signal from the error signal generation circuit.

5. The system of claim **4**, wherein the power converter circuit is coupled to the load circuit at a node and wherein the error signal represents a difference between a regulated voltage at the node and a reference voltage.

6. The system of claim **4**, wherein the error signal is an analog voltage.

7. The system of claim **4**, wherein the error signal is a digital signal.

8. The system of claim **4**, wherein the error signal generation circuit comprises an analog-to-digital converter configured to generate the error signal.

9. The system of claim **4**, wherein the power converter circuit comprises a capacitor connected to the load circuit, wherein the capacitor is integrated on the first semiconductor die.

10. The system of claim **4**, wherein the power converter circuit comprises one or more inductors connected to the load circuit, wherein the inductors are formed on the substrate separate from the first and second semiconductor die.

11. The system of claim **4**, wherein the plurality of power switches are integrated on the second semiconductor die.

12. The system of claim **4**, further comprising a reference voltage generator configured to generate the reference voltage, wherein the error signal represents a difference and the reference voltage and wherein the reference voltage generator is integrated on the first semiconductor die.

13. The system of claim **4**, wherein the power converter circuit comprises:

a capacitor connected to the load circuit;

one or more inductors connected to the load circuit; and

wherein the plurality of power switches, the capacitor, and the one or more inductors collectively form a voltage regulator.

14. The system of claim **13**, wherein the voltage regulator is multiphase.

15. A method of forming a system, the method comprising:

attaching a first semiconductor die to a substrate, the first semiconductor die including a load circuit;

attaching a second semiconductor die to the substrate, the second semiconductor die including a power converter circuit arranged to deliver power to the load circuit, the power converter circuit including a plurality of power switches coupled to a control circuit; and

wherein the control circuit is arranged to control a power delivered to the load circuit via the plurality of power switches.

16. The method of claim **15**, wherein the first semiconductor die further comprises an error signal generation circuit.

17. The method of claim **16**, wherein the control circuit is arranged to control the power delivered to the load circuit in response to receiving an error signal from the error signal generation circuit.

18. The method of claim **17**, wherein the power converter circuit is coupled to the load circuit at a node and wherein the error signal represents a difference between a regulated voltage at the node and a reference voltage.

19. The method of claim **17**, wherein the error signal generation circuit comprises an analog-to-digital converter configured to generate the error signal.

20. The method of claim **17**, wherein the power converter circuit comprises a capacitor connected to the load circuit, wherein the capacitor is integrated on the first semiconductor die.

21. The method of claim **17**, wherein the power converter circuit comprises one or more inductors connected to the load circuit, wherein the inductors are formed on the substrate separate from the first and second semiconductor die.

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