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(54) **THREE-DIMENSIONAL RESERVOIR BASED ON VOLATILE THREE-DIMENSIONAL MEMRISTOR AND MANUFACTURING METHOD THEREFOR**

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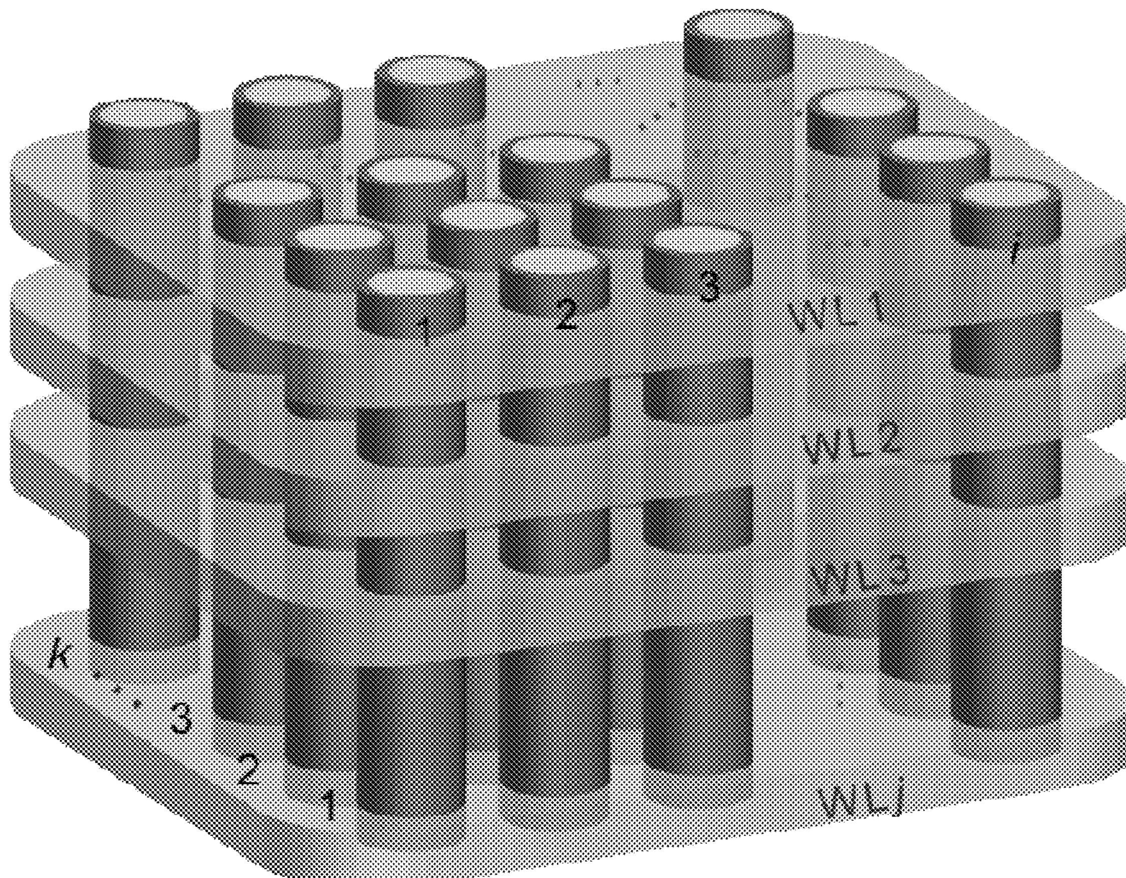
(57) **ABSTRACT**

A three-dimensional reservoir based on three-dimensional volatile memristors and a method for manufacturing the same. In the three-dimensional reservoir, a memory layer, a select layer, and an electrode layer in each via form a memristor which is a reservoir unit. The three-dimensional reservoir is formed based on a stacking structure and multiple vias. The three-dimensional reservoir is constructed by using virtual nodes generated from dynamic characteristics of the three-dimensional memristors. An interfacial memristor is first constructed, and its volatility is verified through electric tests. A vertical three-dimensional array is manufactured based on the volatile memristor. A dynamic characteristic of the memristor is adjusted through a Schottky barrier. Different layers in the three-dimensional reservoir correspond to different reservoirs, which are constructed by controlling memristors in the different layers, respectively.



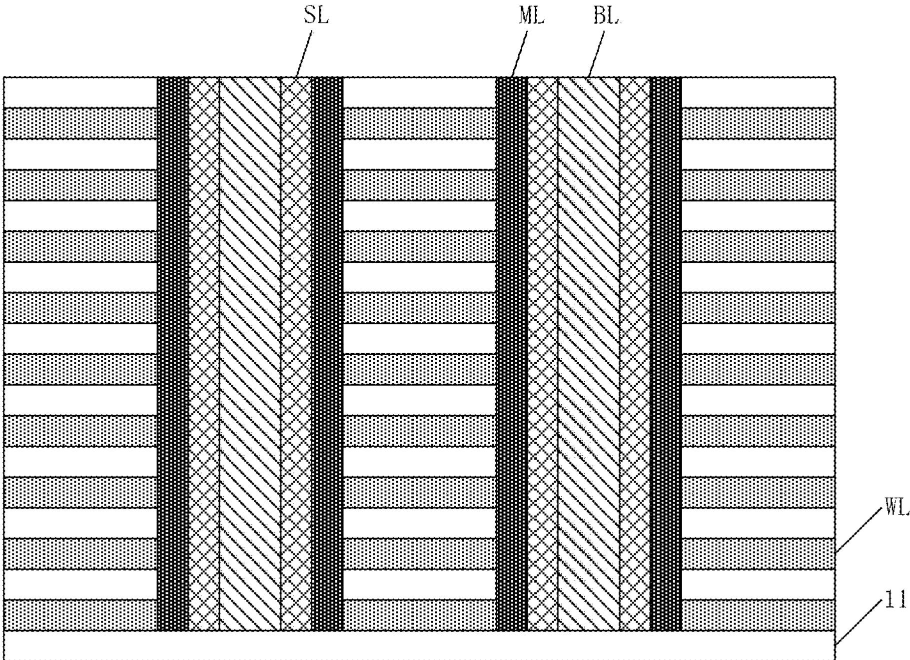


Figure 1

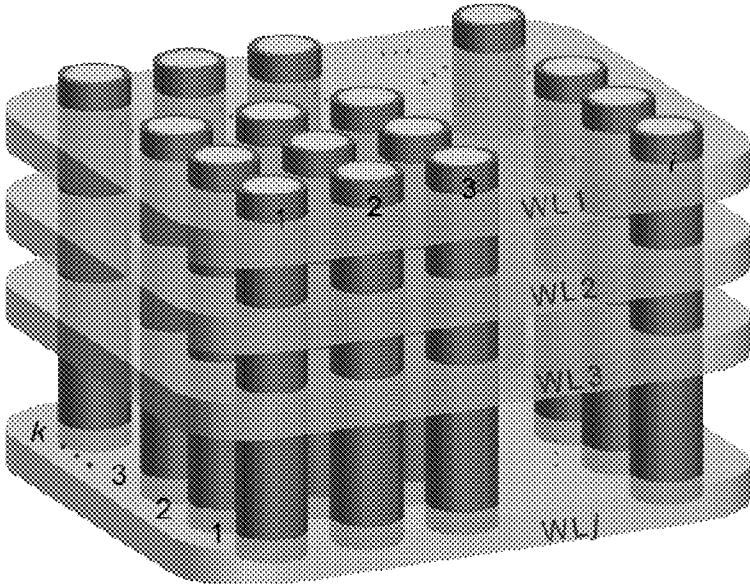


Figure 2

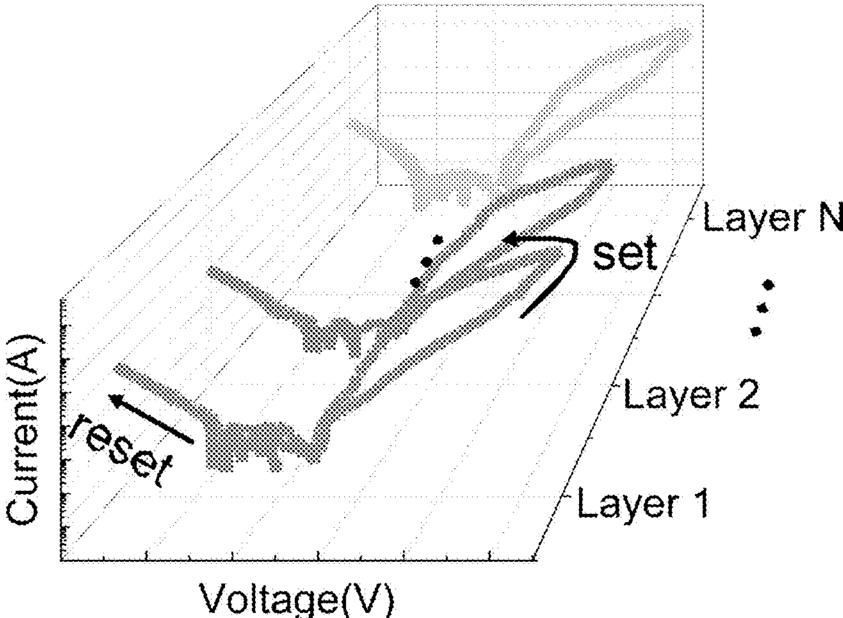


Figure 3

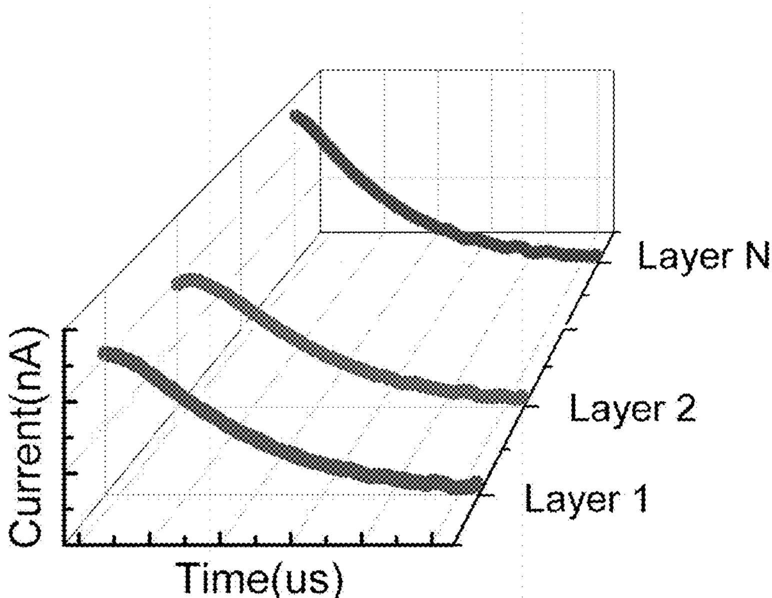


Figure 4

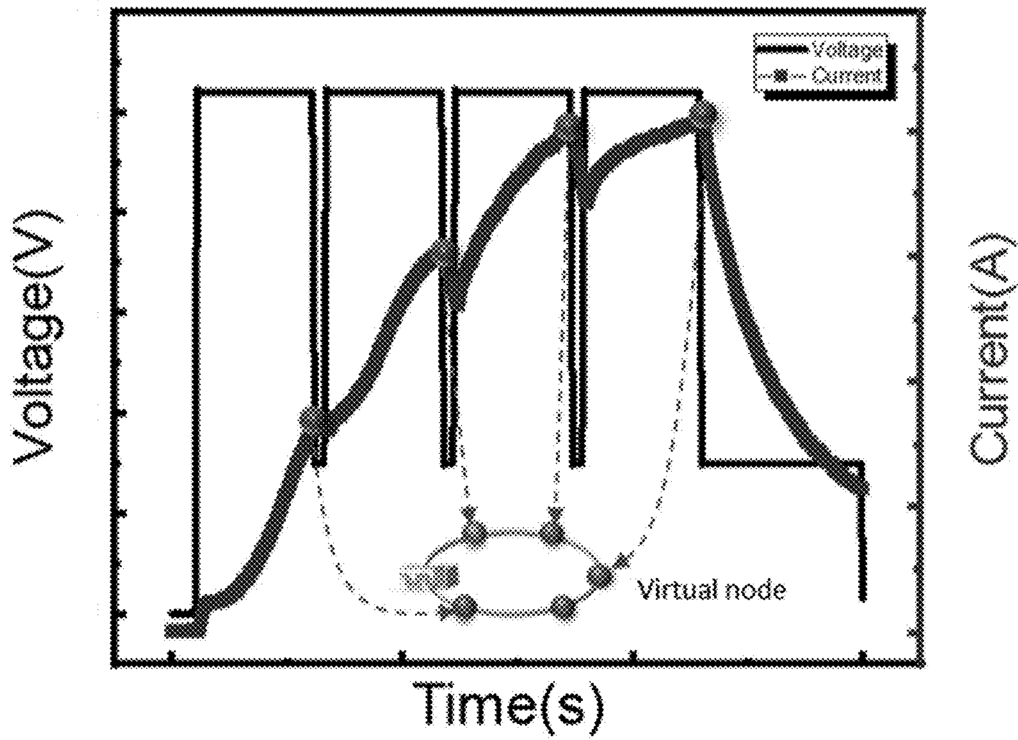


Figure 5

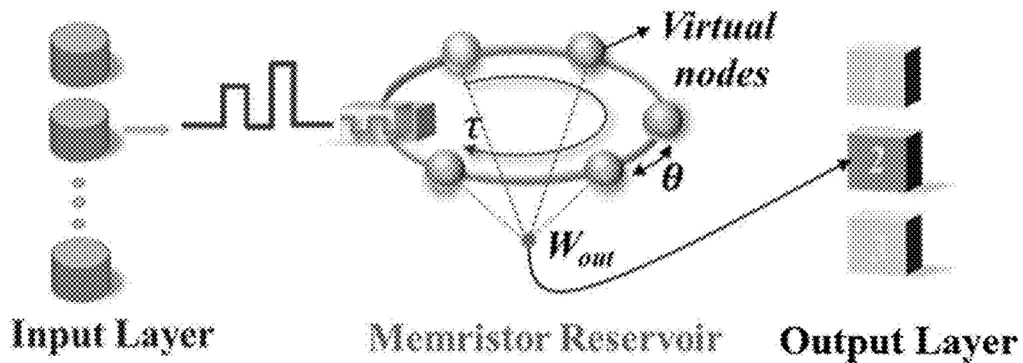


Figure 6

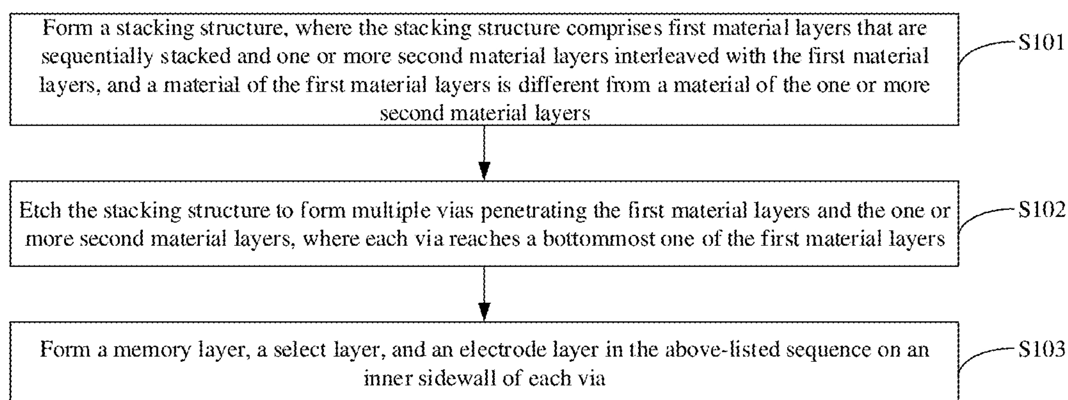


Figure 7

THREE-DIMENSIONAL RESERVOIR BASED ON VOLATILE THREE-DIMENSIONAL MEMRISTOR AND MANUFACTURING METHOD THEREFOR

[0001] This application claims priority to Chinese Patent Application No. 202210055435.0, titled "THREE-DIMENSIONAL RESERVOIR BASED ON VOLATILE THREE-DIMENSIONAL MEMRISTOR AND MANUFACTURING METHOD THEREFOR", filed on Jan. 18, 2022 with the China National Intellectual Property Administration, which is hereby incorporated by reference in its entirety.

FIELD

[0002] The present disclosure relates to the technical field of semiconductors, and in particular to a three-dimensional reservoir apparatus based on three-dimensional volatile memristors and a method for manufacturing the three-dimensional reservoir based on the three-dimensional volatile memristors.

BACKGROUND

[0003] Traditional computing paradigms are subject to the slowdown of Moore's Law and the von Neumann bottleneck with soaring development of artificial intelligence technology and applications, and computing paradigms having higher energy efficiency and a stronger computing capability have become an urgent need. The brain-inspired computing is one of the most potential computing paradigms.

[0004] Memristors have great advantages in hardware implementation of artificial neural networks due to their special characteristics. At present, most researches on memristors focus on how to use their analog resistive switching and non-volatility to implement addition and multiplication based on a memristor array. In comparison, few researches have been conducted on the dynamic characteristic and nonlinearity of the memristors.

[0005] Reservoir computing (RC) is a simple and efficient brain-inspired scheme that can process time-dependent signals reasonably. The reservoir computing originates from the echo state network proposed by H. Jaeger et al. in 2001, and the liquid state machine proposed by W. Maass et al. in 2002. The reservoir computing has drawn widespread academic attention in in recent years.

[0006] The reservoir computing utilizes inherent nonlinearity and volatility of the memristors to construct a "reservoir". Compared with a traditional recurrent neural network (RNN), the reservoir is a replacement of the intermediate layer, and it is only required to iterate weights of connections from the reservoir to the output layer in the training. Thereby, a process of training the network is significantly simplified.

[0007] In conventional technology, reservoir computing has been widely applied to time series prediction, pattern recognition, wireless communication, and other fields. In current researches, the reservoir computing based on memristors merely relate to constructing a reservoir network based on a planar memristor array.

[0008] The era of information explosion provides numerous and more complex tasks. Requirements of miniaturization, low power consumption, and high accuracy need to be met, and energy efficiency and a degree of parallelism of RC systems need to be improved, and information processing in the RC systems needs be accelerated to achieve real-time processing on input signals. Hence, there is a demand on devices of a higher density and an optimized combination of such devices with a network structure of the reservoir.

SUMMARY

[0009] In view of the above, a three-dimensional reservoir based on three-dimensional volatile memristors and a method for manufacturing the three-dimensional reservoir are provided according to embodiments of the present disclosure. The foregoing issue is addressed with following technical solutions.

[0010] A three-dimensional reservoir based on three-dimensional volatile memristors is provided, comprising: a stacking structure, comprising first material layers that are sequentially stacked, and one or more second material layers interleaved with the first material layers, where a material of the first material layers is different from a material of the one or more second material layers; multiple vias penetrating the first material layers and the one or more second material layers, where each via reaches a bottommost one of the first material layers; and a memory layer, a select layer, and an electrode layer, which are disposed in the above-listed sequence on an inner sidewall of each via.

[0011] In an embodiment, the multiple vias are arranged in an array.

[0012] In an embodiment, a thickness of each first material layer ranges from 10 nm to 200 nm.

[0013] In an embodiment, a thickness of each second material layer ranges from 5 nm to 100 nm.

[0014] In an embodiment, a thickness of the memory layer ranges from 2.5 nm to 6 nm.

[0015] In an embodiment, a thickness of the select layer ranges from 5 nm to 20 nm.

[0016] In an embodiment, each first material layer is made of SiO_2, and each second material layer is made of TiN or TaN.

[0017] A method for manufacturing a three-dimensional reservoir which is based on three-dimensional volatile memristors, comprising: forming a stacking structure, where the stacking structure comprises first material layers that are sequentially stacked and one or more second material layers interleaved with the first material layers, and a material of the first material layers is different from a material of the one or more second material layers; etching the stacking structure to form multiple vias penetrating the first material layers and the one or more second material layers, where each via reaches a bottommost one of the first material layers; and forming a memory layer, a select layer, and an electrode layer in the above-listed sequence on an inner sidewall of each via.

[0018] Compared with the conventional technology, the beneficial effects realized by the present disclosure are as follows.

[0019] According to embodiments of the present disclosure, the three-dimensional reservoir based on three-dimensional volatile memristors comprises: the stacking structure, comprising the first material layers that are sequentially stacked, and the one or more second material layers interleaved with the first material layers, where the material of the first material layers is different from the material of the one or more second material layers; the multiple vias penetrating the first material layers and the one or more second material layers, where each via reaches a bottommost one of the first material layers; and the memory layer, the

select layer, and the electrode layer, which are disposed in the above-listed sequence on the inner sidewall of each via.

[0020] The memory layer, the select layer, and the electrode layer in each via form a memristor, i.e., form a reservoir unit. The three-dimensional reservoir is formed based on the stacking structure and the multiple vias. Specifically, the three-dimensional reservoir is constructed by using virtual nodes generated from dynamic characteristics of the three-dimensional memristors. An interfacial memristor is first constructed, and its volatility is verified through electric tests. A vertical three-dimensional array is manufactured based on the volatile memristor. A dynamic characteristic of the memristor is adjusted through a Schottky barrier. Different layers in the three-dimensional reservoir correspond to different reservoirs, which are constructed by controlling memristors in the different layers, respectively. The virtual nodes are enriched, a degree of parallelism and recognition accuracy of a whole system are improved, and an area of the system is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] For clearer illustration of the technical solutions according to embodiments of the present disclosure or conventional techniques, hereinafter briefly described are the drawings to be applied in embodiments of the present disclosure or conventional techniques. Apparently, the drawings in the following descriptions are only some embodiments of the present disclosure and other drawings may be obtained by those ordinary skilled in the art based on the provided drawings without creative efforts.

[0022] FIG. **1** is a schematic section view of a three-dimensional volatile memristor according to an embodiment of the present disclosure.

[0023] FIG. **2** is a schematic diagram of a partial three-dimensional structure of a volatile three-dimensional memristor according to an embodiment of the present disclosure.

[0024] FIG. **3** is a schematic graph of characteristic I-V curves of different layers of a three-dimensional reservoir based on three-dimensional volatile memristors according to an embodiment of the present disclosure.

[0025] FIG. **4** is a schematic graph of dynamic characteristic curves of different layers of a three-dimensional reservoir based on three-dimensional volatile memristors according to an embodiment of the present disclosure.

[0026] FIG. **5** is a schematic diagram of virtual nodes based on a dynamic characteristic of a memristor according to an embodiment of the present disclosure.

[0027] FIG. **6** is a schematic diagram of operation of a reservoir having virtual nodes based on a dynamic characteristic of memristor according to an embodiment of the present disclosure.

[0028] FIG. **7** is a schematic flowchart of a method for manufacturing three-dimensional reservoir, which is based on three-dimensional volatile memristors, according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

[0029] Hereinafter the technical solutions in the embodiments of the present disclosure are described clearly and thoroughly in conjunction with the accompanying drawings in the embodiments of the present disclosure. Apparently, the described embodiments are only some rather than all of the embodiments of the present disclosure. Any other embodiments obtained based on the embodiments of the present disclosure by those ordinary skilled in the art without any creative effort fall within the scope of protection of the present disclosure.

[0030] In order to make the above objects, features and advantages of the present disclosure more comprehensible, hereinafter the present disclosure will be further described in detail in conjunction with the drawings and specific embodiments.

[0031] Reference is made to FIG. **1**, which is a schematic section view of a volatile three-dimensional memristor according to an embodiment of the present disclosure. Reference is made to FIG. **2**, which is a schematic diagram of a partial three-dimensional structure of a volatile three-dimensional memristor according to an embodiment of the present disclosure.

[0032] The three-dimensional reservoir comprises a stacking structure, multiple vias, a memory layer, a select layer, and an electrode layer.

[0033] The stacking structure comprises first material layers **11** that are sequentially stacked and one or more second material layers WL interleaved with the first material layers. A material of the first material layers **11** is different from a material of the one or more second material layers WL.

[0034] The multiple vias penetrate the first material layers **11** and the one or more second material layers WL. Each via reaches a bottommost one of the first material layers **11**.

[0035] The memory layer ML, the select layer SL, and the electrode layer EL are disposed in the above-listed sequence on an inner sidewall of each via.

[0036] The first material layers **11** are not depicted in FIG. **2**.

[0037] In this embodiment, the uppermost layer and the bottommost layer of the stacking structure are both first material layers **11**. Each second material layer WL is located between two adjacent ones of the first material layers **11**.

[0038] As an example, the first material layer **11** provides interlayer insulation. The first material layer **11** is made of insulating materials, including but not limited to SiO_2 or the like.

[0039] In an embodiment, a thickness of the first material layer **11** ranges from 10 nm to 200 nm. For example, the thickness of the first material layer **11** is 35 nm, 68 nm, 115 nm, 167 nm, or the like.

[0040] The second material layer WL serves as a word line of the three-dimensional reservoir. The second material layer is made of a material including but not limited to TiN or TaN.

[0041] In an embodiment, a thickness of the second material layer WL ranges from 5 nm to 100 nm. For example, the thickness of the second material layer WL is 8 nm, 35 nm, 76 nm, 88 nm, or the like.

[0042] Further, the vias penetrate all the first material layers **11**, except the bottommost one, and all the second material layers WL and reaches a surface of the bottommost first material layer, so as to separate a planar electrode.

[0043] In an embodiment as shown in FIG. **2**, the multiple vias are arranged in an array. That is, the multiple vias are equally separated in a row direction of the array, and/or equally separated in a column direction of the array. Thereby, a structure of the three-dimensional reservoir is optimized, and accordingly a characteristic of the three-dimensional reservoir is optimized.

[0044] Further, the memory layer ML may be grown through various techniques, which include but are not limited to, atomic layer deposition, magnetron sputtering, or ion beam sputtering. The memory layers ML cover the whole sidewall of the vias.

[0045] In an embodiment, the memory layer ML is made of a material including but not limited to HfO_2, TaOx, HZO, or the like.

[0046] In an embodiment, a thickness of the memory layer ML ranges from 2.5 nm to 6 nm. For example, the thickness of the memory layer ML is 2.8 nm, 4 nm, or 5.4 nm.

[0047] Concentration of ions may be controlled to adjust a height of the Schottky barrier.

[0048] Further, the self-aligned select layer SL is grown through a technique including but not limited to atomic layer deposition, oxygen plasma, or the like. The select layer SL is for suppressing interlayer leakage, and the select layer SL covers a whole of an inner sidewall of the memory layer ML.

[0049] In an embodiment, the select layer SL is made of a material including but is not limited to TiO_2, Al_2O_3, or the like.

[0050] In an embodiment, the thickness of the select layer SL ranges from 5 nm to 20 nm. For example, the thickness of the select layer SL is 6 nm, 12 nm, 17 nm, or the like.

[0051] In an embodiment, the electrode layer BL is deposited through a technique including but not limited to sputtering. The electrode layer BL serves as a bit line of the three-dimensional reservoir.

[0052] In an embodiment, the electrode layer BL is made of a material including but is not limited to TiN, W, Pt, Ru, or the like.

[0053] Reference is made to FIG. **3**, which is a schematic graph of characteristic I-V curves of different layers of a three-dimensional reservoir based on three-dimensional volatile memristors according to an embodiment of the present disclosure.

[0054] As shown in FIG. **3**, the scanned direct-current curves show that each layer of the three-dimensional reservoir has obvious nonlinearity.

[0055] Reference is made to FIG. **4**, which is a schematic diagram of dynamic characteristic curves of different layers of a three-dimensional reservoir based on three-dimensional volatile memristors according to an embodiment of the present disclosure.

[0056] As shown in FIG. **4**, the same excitation signal is applied to different layers, and the dynamic characteristic curves of different layers are obtained after the excitation signal disappears. It can be seen from FIG. **4** that there are differences among the dynamic characteristics of the different layers. On such basis, different pulse adjustment may be applied to different layers to obtain a sufficiently large difference among the dynamic characteristics, and such large difference can be used to construct different reservoirs.

[0057] Reference is made to FIG. **5**, which is a schematic diagram of virtual nodes based on a dynamic characteristic of a memristor according to an embodiment of the present disclosure. Reference is made to FIG. **6**, which is a schematic diagram of operation of a reservoir having virtual nodes based on a dynamic characteristic of a memristor according to an embodiment of the present disclosure.

[0058] An appropriate sequence of pulses may be applied based on the dynamic characteristic of the memristor as shown in FIG. **5**, in order to obtain virtual nodes (i.e., the virtual nodes as shown in FIG. **6**) that meet the requirement of an RC system. On a basis of such theory, the three-dimensional reservoir can be constructed with the virtual nodes based on the dynamic characteristic of the memristor.

[0059] In other words, the memory layer, the select layer, and the electrode layer in each via form a memristor, i.e., form a reservoir unit. The three-dimensional reservoir is formed based on the stacking structure and the multiple vias. Specifically, the three-dimensional reservoir is constructed by using virtual nodes generated from dynamic characteristics of the three-dimensional memristors. An interfacial memristor is first constructed, and its volatility is verified through electric tests. A vertical three-dimensional array is manufactured based on the volatile memristor. A dynamic characteristic of the memristor is adjusted through a Schottky barrier. Different layers in the three-dimensional reservoir correspond to different reservoirs, which are constructed by controlling memristors in the different layers, respectively. The virtual nodes are enriched, a degree of parallelism and recognition accuracy of a whole system are improved, and an area of the system is reduced.

[0060] In an embodiment on a basis of all foregoing embodiments, a method for manufacturing a three-dimensional reservoir which is based on three-dimensional volatile memristors is further provided. Reference is made to FIG. **7**, which is a schematic flowchart of a method for manufacturing a three-dimensional reservoir, which is based on three-dimensional volatile memristors, according to an embodiment of the present disclosure.

[0061] The method for manufacturing the three-dimensional reservoir based on the three-dimensional volatile memristors comprises steps S**101** to S**103**.

[0062] In S**101**, a stacking structure is formed, where the stacking structure comprises first material layers that are sequentially stacked and one or more second material layers interleaved with the first material layers, and a material of the first material layers is different from a material of the one or more second material layers.

[0063] In S**102**, the stacking structure is etched to form multiple vias penetrating the first material layers and the one or more second material layers, where each via reaches a bottommost one of the first material layers.

[0064] In S**103**, a memory layer, a select layer, and an electrode layer are formed in the above-listed sequence on an inner sidewall of each via.

[0065] In this embodiment, the first material layers and the second material layers are alternately deposited on the substrate through a technique including but not limited to physical vapor deposition or chemical vapor deposition, so as to form the stacking structure. Both the uppermost layer and the bottommost layer of the stacking structure are the first material layers.

[0066] As an example, the first material layer provides interlayer insulation. The first material layer is made of insulating materials, including but not limited to SiO_2 or the like.

[0067] In an embodiment, a thickness of the first material layer ranges from 10 nm to 200 nm. For example, the thickness of the first material layer is 35 nm, 68 nm, 115 nm, 167 nm, or the like.

[0068] The second material layer serves as a word line of the three-dimensional reservoir. The second material layer is made of a material including but not limited to TiN or TaN.

[0069] In an embodiment, a thickness of the second material layer ranges from 5 nm to 100 nm. For example, the thickness of the second material layer is 8 nm, 35 nm, 76 nm, 88 nm, or the like.

[0070] Further, the vias penetrate all the first material layers, except the bottommost one, and all the second material layers and reaches a surface of the bottommost first material layer, so as to separate a planar electrode.

[0071] In an embodiment as shown in FIG. **2**, the multiple vias are arranged in an array. That is, the multiple vias are equally separated in a row direction of the array, and/or equally separated in a column direction of the array. Thereby, a structure of the three-dimensional reservoir is optimized, and accordingly a characteristic of the three-dimensional reservoir is optimized.

[0072] Further, the memory layer may be grown through various techniques, which include but are not limited to, atomic layer deposition, magnetron sputtering, or ion beam sputtering. The memory layers ML cover the whole sidewall of the vias.

[0073] In an embodiment, the memory layer is made of a material including but not limited to HfO_2, TaOx, HZO, or the like.

[0074] In an embodiment, a thickness of the memory layer ML ranges from 2.5 nm to 6 nm. For example, the thickness of the memory layer ML is 2.8 nm, 4 nm, or 5.4 nm.

[0075] Concentration of ions may be controlled to adjust a height of the Schottky barrier.

[0076] Further, the self-aligned select layer SL is grown through a technique including but not limited to atomic layer deposition, oxygen plasma, or the like. The select layer SL is for suppressing interlayer leakage, and the select layer SL covers a whole of an inner sidewall of the memory layer ML.

[0077] In an embodiment, the select layer SL is made of a material including but is not limited to TiO_2, Al_2O_3, or the like.

[0078] In an embodiment, the thickness of the select layer SL ranges from 5 nm to 20 nm. For example, the thickness of the select layer SL is 6 nm, 12 nm, 17 nm, or the like.

[0079] In an embodiment, the electrode layer BL is deposited through a technique including but not limited to sputtering. The electrode layer BL serves as a bit line of the three-dimensional reservoir.

[0080] In an embodiment, the electrode layer BL is made of a material including but is not limited to TiN, W, Pt, Ru, or the like.

[0081] A principle of the three-dimensional reservoir manufactured by the method is identical to that of the three-dimensional reservoir according to the foregoing embodiments of the present disclosure, and is not repeated herein.

[0082] Hereinabove the three-dimensional reservoir based on three-dimensional volatile memristors and the method for manufacturing the same are described in detail according to embodiments of the present disclosure. Principles and implementations of the present disclosure are described by using specific embodiments herein. Description of the above embodiments is merely intended for helping understand the method and key concepts of the present disclosure. In addition, it should be noted that those skilled in the art may make some variations to specific implementations and application scopes based on the concepts of the present disclosure. Hence, the content of this specification should not be construed as a limitation to the present disclosure.

[0083] It should be noted that the embodiments of the present disclosure are described in a progressive manner, and each embodiment places emphasis on the difference from other embodiments. Therefore, one embodiment can refer to other embodiments for the same or similar parts. Since devices disclosed in the embodiments correspond to methods disclosed in the embodiments, the description of the devices is simple, and reference may be made to the relevant part of the methods.

[0084] It should be noted that, the relationship terms such as "first", "second" and the like are only used herein to distinguish one entity or operation from another, rather than to necessitate or imply that an actual relationship or order exists between the entities or operations. Furthermore, the terms such as "include", "comprise" or any other variants thereof means to be non-exclusive. Therefore, a process, a method, an article or a device including a series of elements include not only the disclosed elements but also other elements that are not clearly enumerated, or further include inherent elements of the process, the method, the article or the device. Unless expressively limited, the statement "including a . . . " does not exclude the case that other similar elements may exist in the process, the method, the article or the device other than enumerated elements.

[0085] According to the description of the disclosed embodiments, those skilled in the art can implement or use the present disclosure. Various modifications made to these embodiments may be obvious to those skilled in the art, and the general principle defined herein may be implemented in other embodiments without departing from the spirit or scope of the present disclosure. Therefore, the present disclosure is not limited to the embodiments described herein but conforms to a widest scope in accordance with principles and novel features disclosed in the present disclosure.

1. A three-dimensional reservoir based on three-dimensional volatile memristors, comprising:
- a stacking structure, comprising first material layers that are sequentially stacked, and one or more second material layers interleaved with the first material layers, wherein a material of the first material layers is different from a material of the one or more second material layers;
- a plurality of vias penetrating the first material layers and the one or more second material layers, wherein each via reaches a bottommost one of the first material layers; and
- a memory layer, a select layer, and an electrode layer, which are disposed in the above-listed sequence on an inner sidewall of each via.

2. The three-dimensional reservoir according to claim **1**, wherein the plurality of vias are arranged in an array.

3. The three-dimensional reservoir according to claim **1**, wherein a thickness of each first material layer ranges from 10 nm to 200 nm.

4. The three-dimensional reservoir according to claim **1**, wherein a thickness of each second material layer ranges from 5 nm to 100 nm.

5. The three-dimensional reservoir according to claim **1**, wherein a thickness of the memory layer ranges from 2.5 nm to 6 nm.

6. The three-dimensional reservoir according to claim **1**, wherein a thickness of the select layer ranges from 5 nm to 20 nm.

7. The three-dimensional reservoir according to claim **1**, wherein each first material layer is made of SiO_2, and each second material layer is made of TiN or TaN.

8. A method for manufacturing a three-dimensional reservoir, which is based on three-dimensional volatile memristors, comprising:

forming a stacking structure, wherein the stacking structure comprises first material layers that are sequentially stacked and one or more second material layers interleaved with the first material layers, and a material of the first material layers is different from a material of the one or more second material layers;

etching the stacking structure to form a plurality of vias which penetrate the first material layers and the one or more second material layers, wherein each via reaches a bottommost one of the first material layers; and

forming a memory layer, a select layer, and an electrode layer in the above-listed sequence on an inner sidewall of each via.

* * * * *