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(54) **LINEAR FILTER CIRCUIT**

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(57) **ABSTRACT**

In the linear filter circuit, a right shift circuit derives $A\times2^{-n}$ by shifting the input pixel value A rightward by n bits. A selector selects either the input pixel value A or an input pixel value B according to an n-bit blending factor α, conducts computation of $(A\times\alpha\_+B\times\alpha)$, and outputs n partial products. A Wallace adder adds up a total of (n+1) partial products output from the selector and the right shift circuit, and thereby derives an output value $Y=A\times(1-\alpha)+B\times\alpha$ of the linear filter circuit.

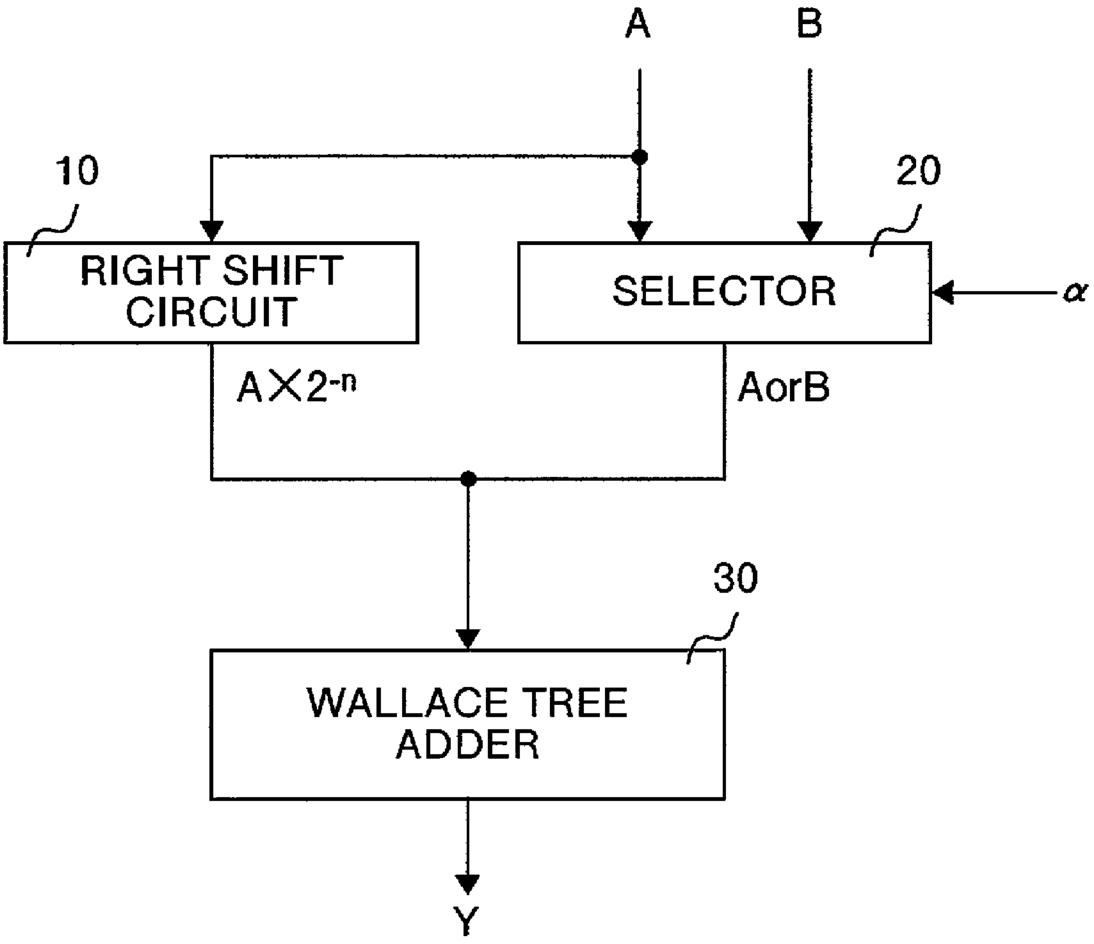


FIG.1

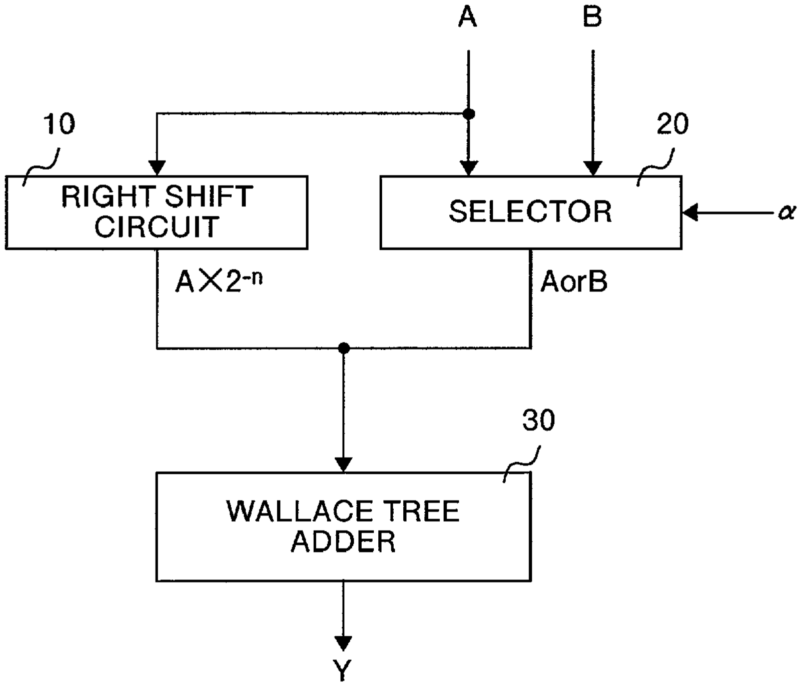

A
B
10
20
RIGHT SHIFT CIRCUIT
SELECTOR
α
A×2^-n
AorB
30
WALLACE TREE ADDER
Y

FIG.2

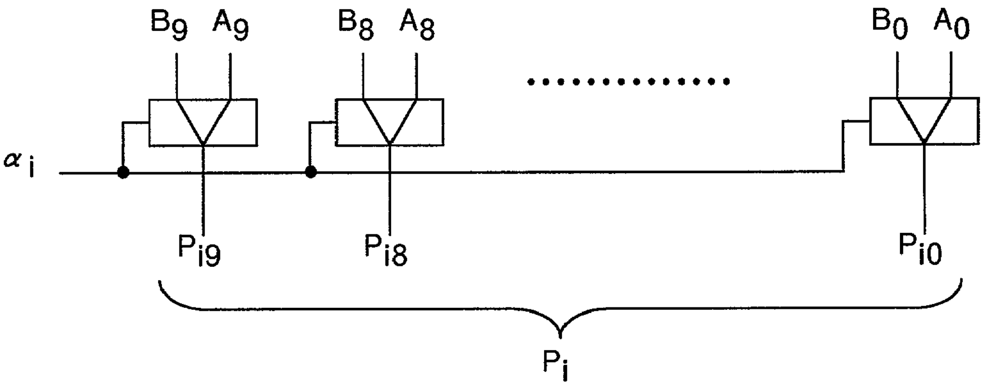

B9 A9
B8 A8
B0 A0
αi
Pi9
Pi8
Pi0
Pi

FIG.3

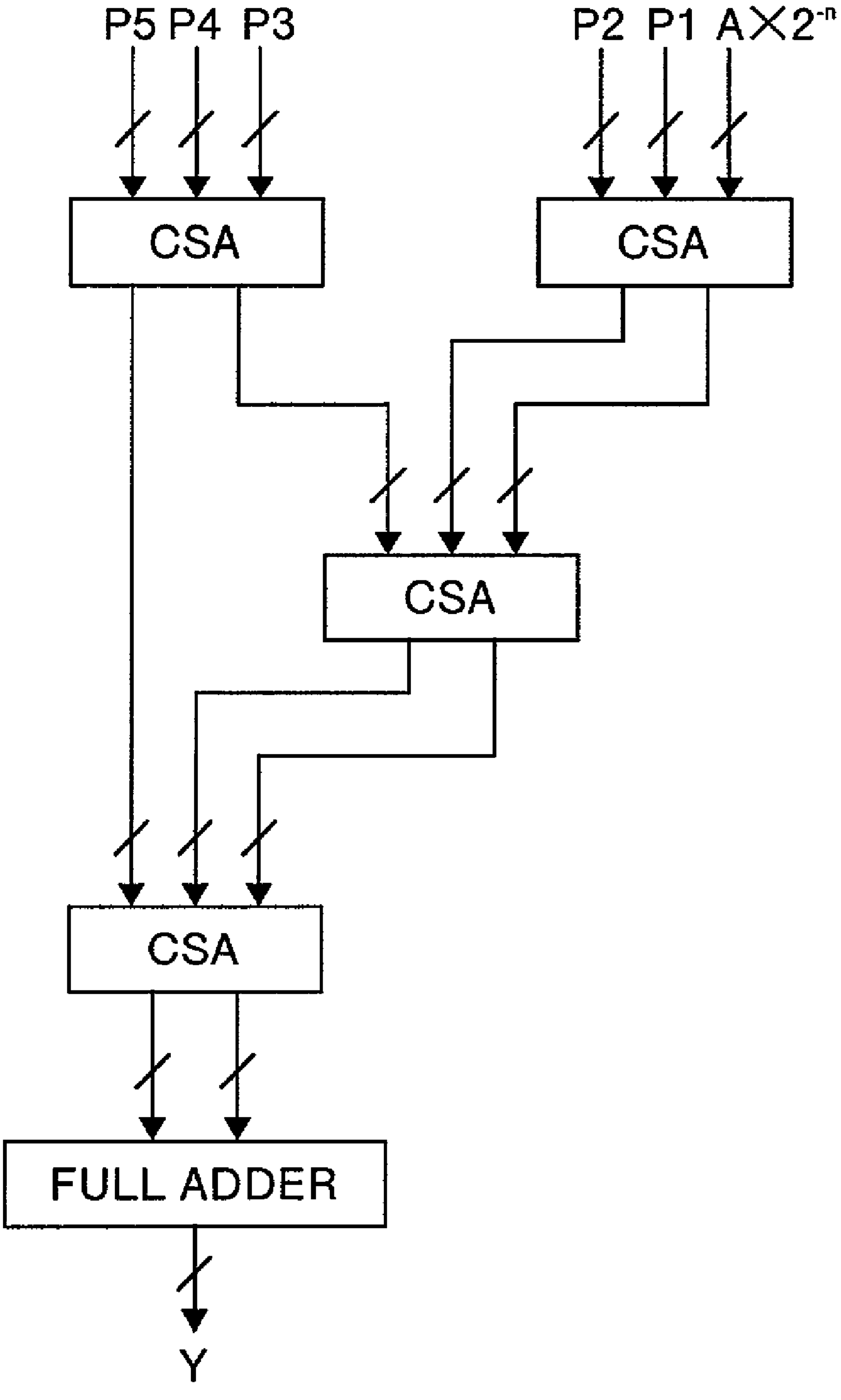
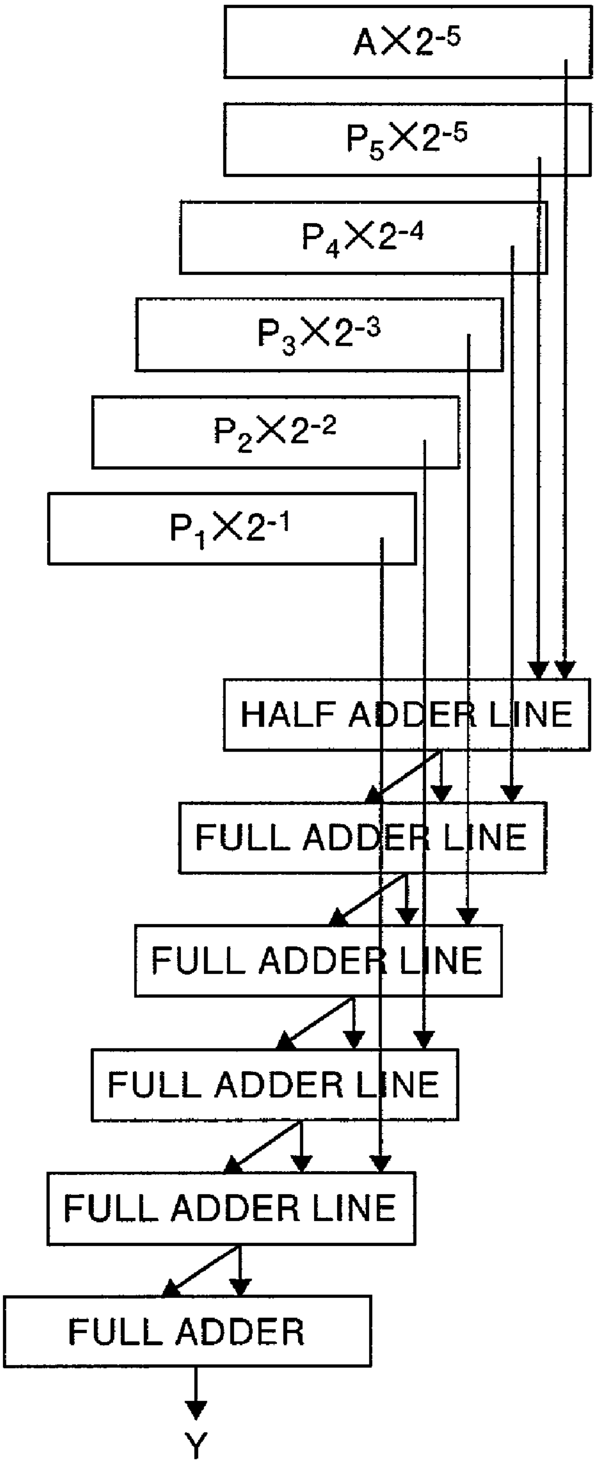


FIG.4



A×2-5
P5×2-5
P4×2-4
P3×2-3
P2×2-2
P1×2-1
HALF ADDER LINE
FULL ADDER LINE
FULL ADDER LINE
FULL ADDER LINE
FULL ADDER LINE
FULL ADDER
Y

FIG.5

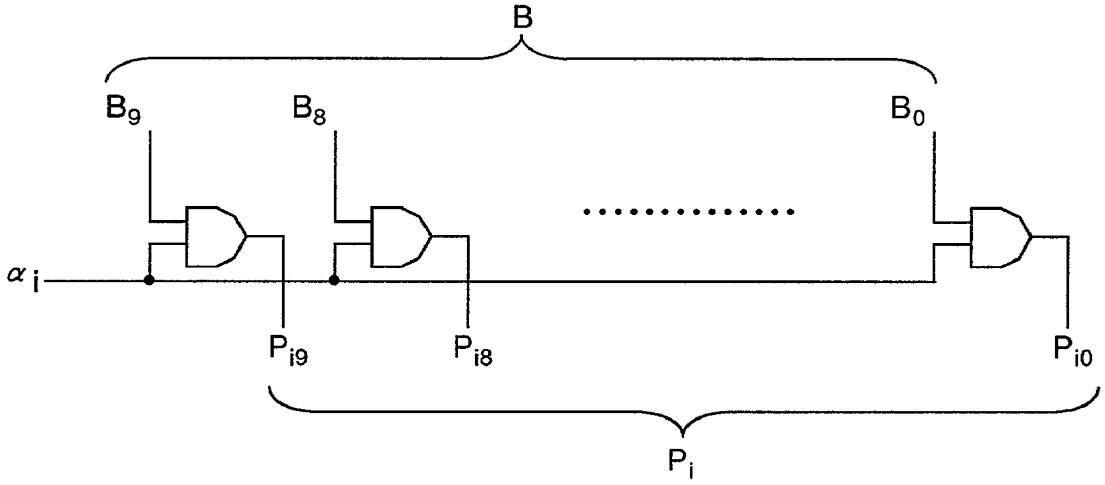

B
B_9
B_8
B_0
α_i
P_{i9}
P_{i8}
P_{i0}
P_i

FIG.6

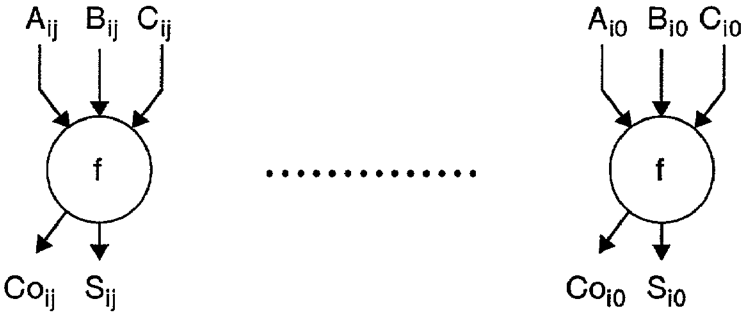
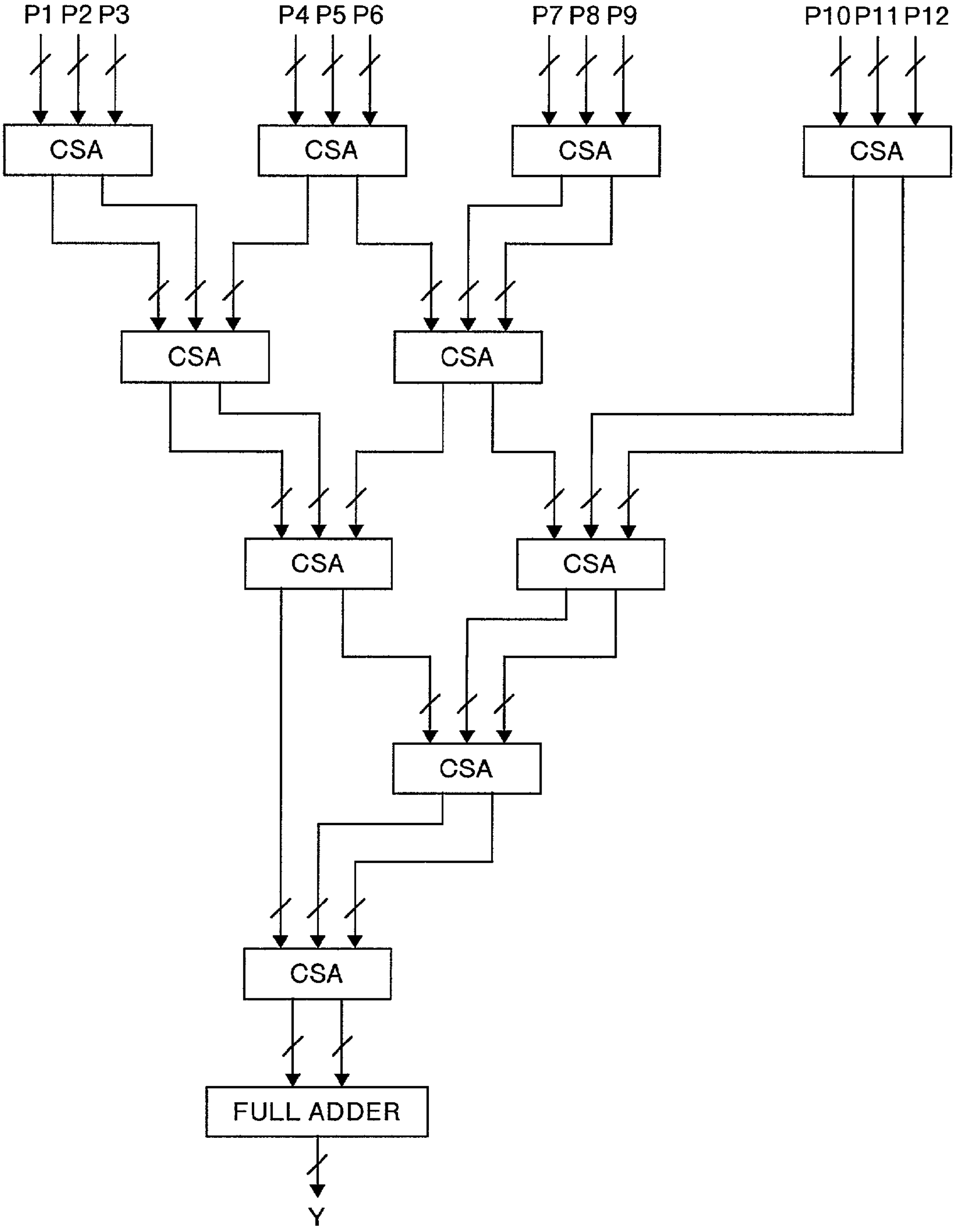

A_{ij} B_{ij} C_{ij}
f
Co_{ij} S_{ij}
A_{i0} B_{i0} C_{i0}
f
Co_{i0} S_{i0}

FIG.7


P1 P2 P3
P4 P5 P6
P7 P8 P9
P10 P11 P12
CSA
CSA
CSA
CSA
CSA
CSA
CSA
CSA
CSA
CSA
FULL ADDER
Y

LINEAR FILTER CIRCUIT

FIELD OF THE INVENTION

[0001] The present invention relates to a linear filter circuit used in image processing such as 3D graphics. In particular, this invention relates to the linear filter circuit in which the number of adders and the number of stages used to add partial products can be reduced.

BACKGROUND OF THE INVENTION

[0002] In the field of image processing, such as 3D graphic processing, processing (alpha blending) of blending color data for a transparent substance located on this side on the screen with color data for a substance located on the further side on the screen is executed in order to conduct semitransparent processing of displaying the transparent substance located on this side on the screen. Supposing color data (a pixel value) of the substance located on this side to be A, color data (a pixel value) of the substance located on the further side to be B, and a blending value (alpha value) which represents transparency to be α, the blending processing is implemented by executing processing represented by the following equation (1) in a linear filter circuit

$$Y=A\times(1-\alpha)+B\times\alpha \qquad (1)$$

[0003] where A and B are integers, and α is a decimal represented as 0.xxxx.

[0004] As for A, B, α and Y, specifications, such as the number of bits, handling only positive numerical values as A, B and α, and handling both positive and negative numerical values as A, B and α, depend on the graphic system to be used. Assuming that 10-bit positive integers are used as A, B and Y and a decimal having five bits after the decimal point is used as α, and 10 high-order bits are output as Y, a conventional linear filter circuit will now be explained.

[0005] The equation (1) is rewritten as

$$Y=A-A\times\alpha+B\times\alpha \qquad (2)$$

[0006] A circuit according to the equation (2) may be implemented by using two multipliers and two adders (including subtracters). However, since the area of the circuit and the delay value of signal transmission typically increase, letting

$$\alpha=\alpha_1 2^{-1}+\alpha_2 2^{-2}+\alpha_3 2^{-3}+\alpha_4 2^{-4}+\alpha_5 2^{-5}$$

[0007] the equation (2) is further rewritten as represented by equation (3). "A_" denotes bit inverted data of A.

$$\begin{aligned}Y &= A+(\mathrm{A\_}+1)\alpha+B\times\alpha \qquad (3)\\ &= A+\alpha+\mathrm{A\_}\times(\alpha_1 2^{-1}+\alpha_2 2^{-2}+\alpha_3 2^{-3}+\alpha_4 2^{-4}+\alpha_5 2^{-5})+\\ &\quad B\times(\alpha_1 2^{-1}+\alpha_2 2^{-2}+\alpha_3 2^{-3}+\alpha_4 2^{-4}+\alpha_5 2^{-5})\\ &= A+\alpha+\mathrm{A\_}\alpha_1 2^{-1}+\mathrm{A\_}\alpha_2 2^{-2}+\mathrm{A\_}\alpha_3 2^{-3}+\mathrm{A\_}\alpha_4 2^{-4}+\\ &\quad \mathrm{A\_}\alpha_5 2^{-5}+B\times\alpha_1 2^{-1}+B\alpha_2 2^{-2}+B\alpha_3 2^{-3}+B\alpha_4 2^{-4}+B\alpha_5 2^{-5}\end{aligned}$$

[0008] In the equation (3), for example, B×α_1 becomes 0 when. α_1 is 0, whereas B×α_1 becomes B when α_1 is 1. In other words, B×α_1 is implemented by logically AND-ing each of bits B_9 to B_0 of B and α_1 as shown in **FIG. 5**, and these are called partial products. If all of twelve partial products in the equation (3) are added up with due regard to figure alignment and an eleventh bit is discarded, then the value of Y to be derived is obtained.

[0009] As the method of adding the partial products, for example, the Wallace tree scheme using the carry save adder (CSA) can be mentioned. By adding up the generated partial products by using the Wallace tree scheme, a faster speed and a reduced area can be accomplished. As shown in **FIG. 6**, the carry save adder (CSA) has a logical structure which adds up three inputs to be added (an augend sequence A_{ij} to A_{i0}, an addend sequence B_{ij} to B_{i0}, and a carry-in sequence C_{ij} to C_{i0}), by using a full adder, and thereby narrows down them to two numbe, i.e., a sum sequence S_{ij} to S_{i0} ic and a carry-out sequence Co_{ij} to Co_{i0}.

[0010] If the Wallace tree scheme using such a carry save adder (CSA) is used, and twelve partial products **P1** to **P12** exist as represented by the equation (3), then the configuration of the Wallace tree becomes as shown in **FIG. 7**.

[0011] With reference to **FIG. 7**, in a fit stage, twelve partial products **P1** to **P12** can be narrowed down to eight partial products by using four CSAs. In a second stage, two CSAs are used for six partial products among the eight partial products obtained by the narrowing down, and thus the eight partial products are narrowed down to 4+2 partial products. In a third stage, the six partial products are narrowed down to four partial products by using two CSAs. In a fourth stage, the four partial products are narrowed down to 1+2 partial products by using one CSA. In a fifth stage, the three partial products are narrowed down to two partial products by using one CSA. A final sum is obtained by using an ordinary full adder for the two numbe. By taking 10 high-order bits of the resultant sum, Y to be derived is obtained.

[0012] In this way, when a linear filter circuit is formed by using the equation (3), the circuit which generates twelve partial products, the five-stage Wallace tree using ten CSAs, and the full adder are needed.

[0013] In the conventional art, however, partial products such as B×α_1 are derived by logically AND-ing two inputs B and α_1. When α has n bits, at least 2 n partial products are generated and these 2 n partial products need be added up. Therefore, the number of CSAs and the number of stages in the Wallace tree become large. This results in a problem that fast operation is hindered and the area of the circuit is increased.

SUMMARY OF THE INVENTION

[0014] It is an object of the present invention to provide a linear filter circuit capable of achieving fast processing and reduction of the area of the circuit.

[0015] The linear filter circuit according to one aspect of this invention uses two input pixel values A and B and an n-bit blending factor a (decimal), computes Y=A×(1−α)+B×α (where A and B are integers), and thereby blends the two input pixel values. This linear filter circuit comprises a shift circuit which shifts the input pixel value A rightward by n bits, a selector which selects either the input pixel value A and the input pixel value B according to the n-bit blending factor α and outputs n partial products, and an adder which adds up a total of (n+1) partial products between output from the selector and output from the shift circuit.

[0016] The equation Y=A×(1−α)+B×α (where A and B are integers) can be rewritten as $Y=A\times(\alpha\_+2^{-n})+B\times\alpha=A\times 2^{-n}+(A\times\alpha\_+B\times\alpha)$, where α_ is bit inverted data of α. According to the first aspect, the shift circuit derives $A\times2^{-n}$ by shifting the input pixel value A rightward by n bits. The selector selects either the input pixel value A or the input pixel value B according to the n-bit blending factor α, and conducts computation of (A×α_+B×α) to output n partial products. The adder adds up a total of (n+1) partial products output from the selector and the shift circuit, and thereby derives the output value Y of the equation. As a result, the number of generated partial products becomes (n+1), and the number is reduced as compared with the conventional art. Accordingly, a linear filter circuit having a faster speed and a reduced area can be implemented.

[0017] In the above-mentioned linear filter circuit, carry save adders of multiple stages of a Wallace tree scheme are used in the adder.

[0018] According to the above aspect, a plurality of partial products are added up by using the carry save adders of multiple stages of the Wallace tree scheme. By the number of partial products reduced as compared with the conventional art, the number of carry save adders and the number of stages thereof can be reduced.

[0019] Other objects and features of this invention will become apparent from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] **FIG. 1** is a block diagram showing an embodiment of the linear filter circuit according to the present invention,

[0021] **FIG. 2** is a diagram showing an internal configuration of a selector,

[0022] **FIG. 3** is a diagram showing an internal configuration of a Wallace tree adder,

[0023] **FIG. 4** is a diagram showing a configuration example of another adder,

DETAILED DESCRIPTIONS

[0027] An embodiment of the linear filter circuit according to the present invention will be explained in detail by referring to the accompanying drawings.

[0028] **FIG. 1** is a diagram showing the embodiment of the linear filter circuit according to the present invention. The linear filter circuit shown in **FIG. 1** is applied to blending processing having A as color data (a pixel value) of a substance located on this side, B as color data (a pixel value) of a substance located on the further side, and α as a blending value (alpha value) which represents transparency. The processing represented by the following equation (1) is conducted to obtain a blending output value Y.

$$Y=A\times(1-\alpha)+B\times\alpha \tag{1}$$

[0029] where A and B are integers, and a is a decimal.

[0030] In the present embodiment, the equation (1) is rewritten as heretofore explained. A decimal having five bits after the decimal point (n=5) is used as α. It is assumed that 10-bit positive integers are used as A, B and Y and 10 high-order bits are output as Y.

[0031] As for (1−α), the following relation is utilized,

$$(1-\alpha)=\alpha_{1}\_2^{-1}+\alpha_{2}\_2^{-2}+\alpha_{3}\_2^{-3}+\alpha_{4}\_2^{-4}+\alpha_{5}\_2^{-5}+2^{-5} \tag{4}$$

[0032] where "α_" is bit inverted data of α.

[0033] This can be confirmed by making sure that 1 is obtained if α is added to the right side. That is,

$$\begin{aligned}
&\alpha+\alpha_{1}\_2^{-1}+\alpha_{2}\_2^{-2}+\alpha_{3}\_2^{-3}+\alpha_{4}\_2^{-4}+\alpha_{5}\_2^{-5}+2^{-5}= \\
&\qquad(\alpha_{1}2^{-1}+\alpha_{2}2^{-2}+\alpha_{3}2^{-3}+\alpha_{4}2^{-4}+\alpha_{5}2^{-5})+ \\
&\qquad(\alpha_{1}\_2^{-1}+\alpha_{2}\_2^{-2}+\alpha_{3}\_2^{-3}+\alpha_{4}\_2^{-4}+\alpha_{5}\_2^{-5}+2^{-5})= \\
&\qquad(\alpha+\alpha_{1}\_)2^{-1}+(\alpha_{2}+\alpha_{2}\_)2^{-2}+(\alpha_{3}+\alpha_{3}\_)2^{-3}+(\alpha_{4}+\alpha_{4}\_)2^{-4}+ \\
&\qquad(\alpha_{5}+\alpha_{5}\_)2^{-5}+2^{-5}=2^{-1}+2^{-2}+2^{-3}+2^{-4}+2^{-5}+2^{-5}=1
\end{aligned}$$

[0034] Substituting the equation (4) into the equation (1) and rewriting a resultant equation, we get the following equation.

$$\begin{aligned}
Y&=A\times(1-\alpha)+B\times\alpha \qquad (5)\\
&=A\times(\alpha_{1}\_2^{-1}+\alpha_{2}\_2^{-2}+\alpha_{3}\_2^{-3}+\alpha_{4}\_2^{-4}+\alpha_{5}\_2^{-5}+2^{-5})+ \\
&\quad B\times(\alpha_{1}2^{-1}+\alpha_{2}2^{-2}+\alpha_{3}2^{-3}+\alpha_{4}2^{-4}\alpha_{5}\_2^{-5}) \\
&=A\times2^{-5}+(A\alpha_{1}\_+B\alpha_{1})2^{-1}+(A\alpha_{2}\_+B\alpha_{2})2^{-2}+(A\alpha_{3}\_+B\alpha_{3})2^{-3}+ \\
&\quad(A\alpha_{4}\_+B\alpha_{4})2^{-4}+(A\alpha_{5}\_+B\alpha_{5})2^{-5}
\end{aligned}$$

[0024] **FIG. 5** is a circuit diagram which derives a partial product in the conventional art,

[0025] **FIG. 6** is a diagram showing a carry save adder, and

[0026] **FIG. 7** is a diagram showing the Wallace tree adder according to the conventional art.

[0035] The equation (5) becomes a logical equation which forms a linear filter circuit of the present embodiment shown in **FIG. 1**.

[0036] In the equation (5), $A\times2^{-n}$ can be implemented by shifting A rightward by n bits. In this case, n=5. A right shift circuit **10** shown in **FIG. 1** shifts the input pixel value A rightward by n bits. The operation of $A\times2^{-n}$ is implemented by this right shift.

[**0037**] In the equation (5), $(A\alpha_{i}\_\_+B\alpha_{i})$ can be interpreted as a selector which selects A when α_i is 0 and selects B when α_i 1, where i=1 to n. A selector **20** shown in **FIG. 1** selects either an input pixel value A or B according to a blending coefficient α_i. $(A\alpha_{i}\_\_+B\alpha_{i})$ is implemented by this selection operation.

[**0038**] **FIG. 2** shows an internal configuration of the selector **20** which selects one of the input pixel values A (A_0 to A_9) and B (B_0 to B_9) each having 10 bits according to a 1-bit blending coefficient α_i. A selected 9-bit output P_{i0} to P_{i9} is output as one partial product P_i.

[**0039**] Then, n partial products P_1 to P_n output from the selector **20** and one partial product $A\times2^{-n}$ output from a right shift circuit **10** are input to a Wallace tree adder **30** serving as an adder which adds the partial products.

[**0040**] In the Wallace tree adder **30**, n+1 input partial products P_1 to P_n and $A\times2^{-n}$ are added up with due regard to figure alignment. **FIG. 3** shows an internal configuration of the Wallace tree adder **30** in a case of n=5. The Wallace tree adder **30** executes addition processing of six partial products with a Wallace tree of three stages using four carry save adders (CSAs) and one full adder.

[**0041**] According to the Wallace tree adder **30** of **FIG. 3**, in a first stage, six partial products can be narrowed down to four partial products by using two CSAs. In a second stage, one CSA is used for three partial products among the four partial products, and thus the four partial products are narrowed down to 2+1 partial products. In a third stage, the three partial products are narrowed down to two partial products by using one CSA. A final sum is obtained by performing full addition on the two numbers in an ordinary full adder. By taking 10 high-order bits of the resultant sum, a linear filter output Y to be derived is obtained.

[**0042**] In this way, when a linear filter circuit is logically formed on the basis of the equation (5), the number of partial products derived by using the one right shift circuit **10** and the selector **20** becomes (n+1) . By the way, the number of partial products in the case of the conventional art is 2n. Therefore, addition of the partial products can be conducted by using the three-stage Wallace tree using four CSAs, and one full adder. In other words, according to the present embodiment, the number of CSAs in the Wallace tree can be reduced from ten (conventional art) to four and the number of stages of the CSAs can be reduced from five (conventional art) to three, by adopting the right shift circuit **10** and the selector **20** in the configuration which generates partial products of the multiplier. Therefore, it is possible to obtain a linear filter circuit which is reduced in circuit area and which operates fast.

[**0043**] In the embodiment, partial products derived by the right shift circuit **10** and the selector **20** are added by the Wallace tree adder. An arbitrary adder other than the Wallace tree adder may also be used so long as the adder can add up the partial products. For example, if a multiplier using the carry save method is applied to the present invention, the configuration of the adder becomes as shown in **FIG. 4**. In **FIG. 4**, derived partial products $P_1\times2^{-1}$ to $P_5\times2^{-5}$ and $A\times2^{-5}$ are added by using a half adder line of a first stage, full adder lines of four stages, and a full adder. In this case, modifications, such as alteration of the half adder line of the first stage which adds two numbers to a full adder line which adds three numbers, are also possible.

[**0044**] In this embodiment, an arbitrary number of bits can be adopted for A, B, Y and α. Both numbers having signs and numbers having no signs can be coped with by the same logical configuration as that explained above. Further, the linear filter circuit can also be applied to processing of finding an interior division point of two coordinates (a point which divides a distance between two points into α and 1−α).

[**0045**] As heretofore explained, according to the first aspect of the present invention, the shift circuit derives A×2¯n by shifting the input pixel value A rightward by n bits. The selector selects either the input pixel value A or the input pixel value B according to the n-bit blending factor α, conducts computation of $(A\times\alpha\_+B\times\alpha)$, and outputs n partial products. The adder adds up a total of (n+1) partial products output from the selector and the shift circuit, and thereby derives the output value $Y=A\times(1-\alpha)+B\times\alpha$. As a result, the number of generated partial products is reduced as compared with the conventional art. Accordingly, a linear filter circuit having a faster speed and a reduced area can be implemented.

[**0046**] Moreover, a plurality of partial products are added up by using the carry save adders of multiple stages of the Wallace tree scheme. By the number of partial products reduced as compared with the conventional art, the number of carry save adders and the number of stages thereof used in the adder can be reduced.

[**0047**] Although the invention has been described with respect to a specific embodiment for a complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modifications and alternative constructions that may occur to one skilled in the art which fairly fall within the basic teaching herein set forth.

What is claimed is:

1. A linear filter circuit which uses two input pixel values A and B and an n-bit blending factor α, where α is a decimal, computes $Y=A\times(1-\alpha)+B\times\alpha$, where A and B are integers, and thereby blends the two input pixel values, the linear filter circuit comprising:

a shift circuit which shifts the input pixel value A rightward by n bits;

a selector which selects either the input pixel value A or the input pixel value B according to the n-bit blending factor α, and outputs n partial products; and

an adder which adds up a total of (n+1) partial products output from said selector and said shift circuit.

2. The linear filter circuit according to claim 1, wherein carry save adders of multiple stages of a Wallace tree scheme are used in said adder.

* * * * *