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(54) **GOA CIRCUIT AND DISPLAY PANEL**

(71) Applicant: **Shenzhen China Star Optoelectronics Semiconductor Display Technology Co., LTD.**, Shenzhen, Guangdong (CN)

(72) Inventor: **Xiaobin HU**, Shenzhen, Guangdong (CN)

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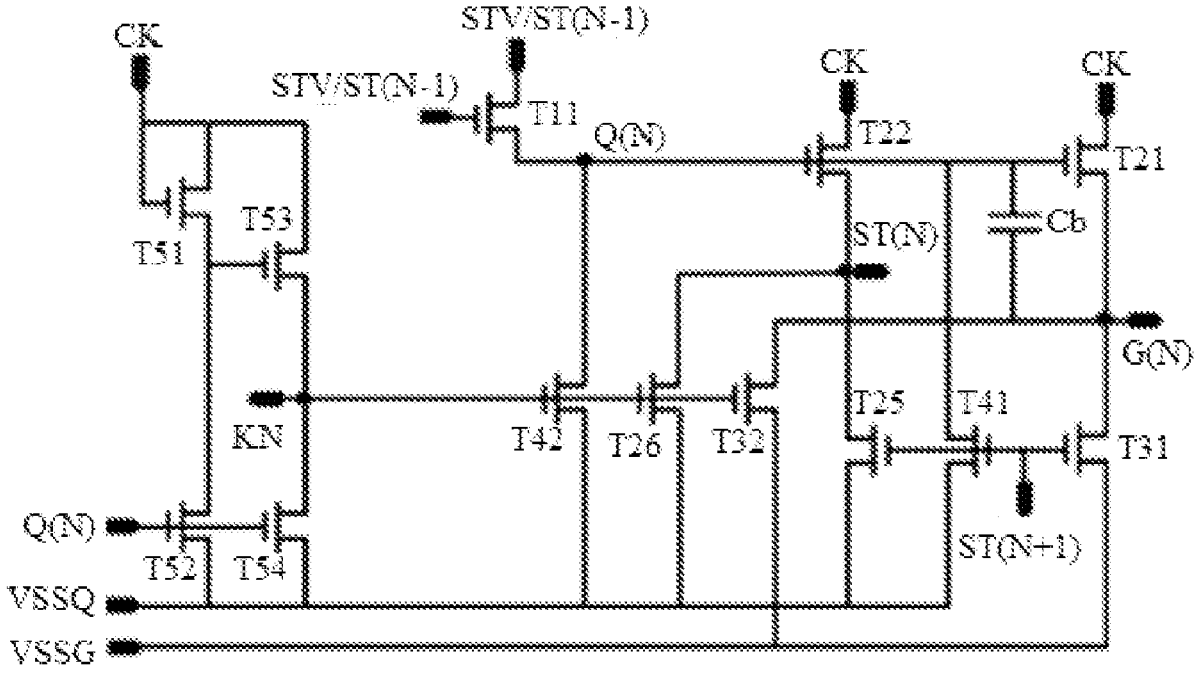
(57) **ABSTRACT**

A GOA circuit and a display panel are provided. The GOA circuit and the display panel decrease thin film transistors required by an inverter in a circuit structure. A thin film transistor number is decreased, and an area occupied by a GOA space can be effectively decreased, which facilitates decreasing of border sizes of panels. Gates of thin film transistors of the GOA circuit are controlled by clock signals that have not been attenuated, which can prevent failure resulting from an attenuated cascaded signal caused by threshold voltage drifting of thin film transistors.



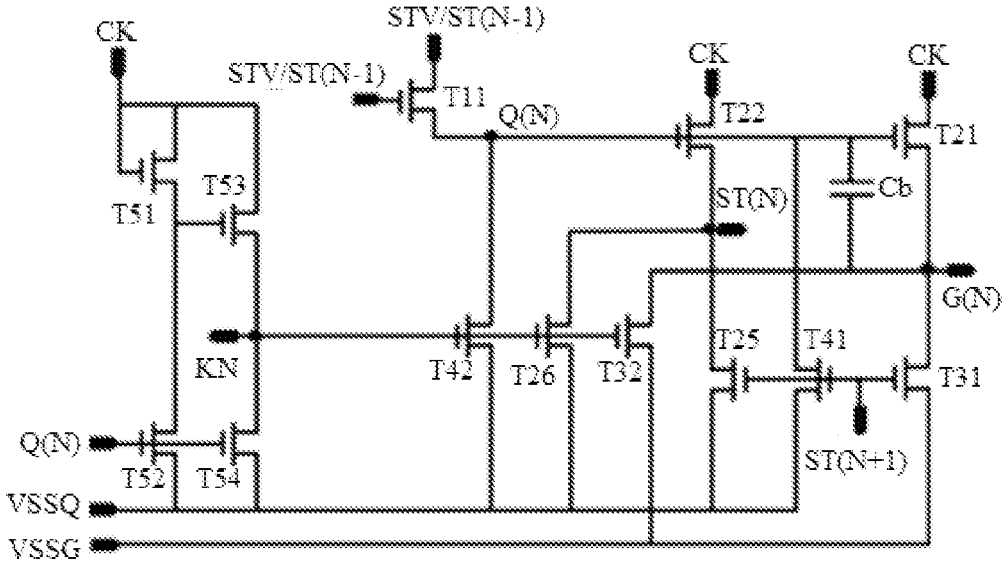

CK
STV/ST(N-1)
STV/ST(N-1)
T11
Q(N)
CK
T22
CK
T21
T53
T51
ST(N)
Cb
G(N)
KN
T42
T26
T32
T25
T41
T31
Q(N)
T52
T54
ST(N+1)
VSSQ
VSSG

FIG. 1

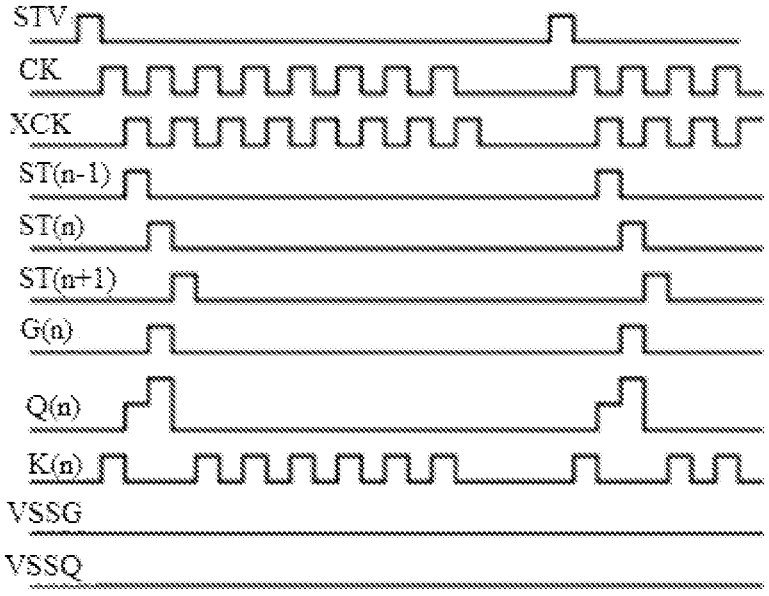

STV
CK
XCK
ST(n-1)
ST(n)
ST(n+1)
G(n)
Q(n)
K(n)
VSSG
VSSQ

FIG. 2

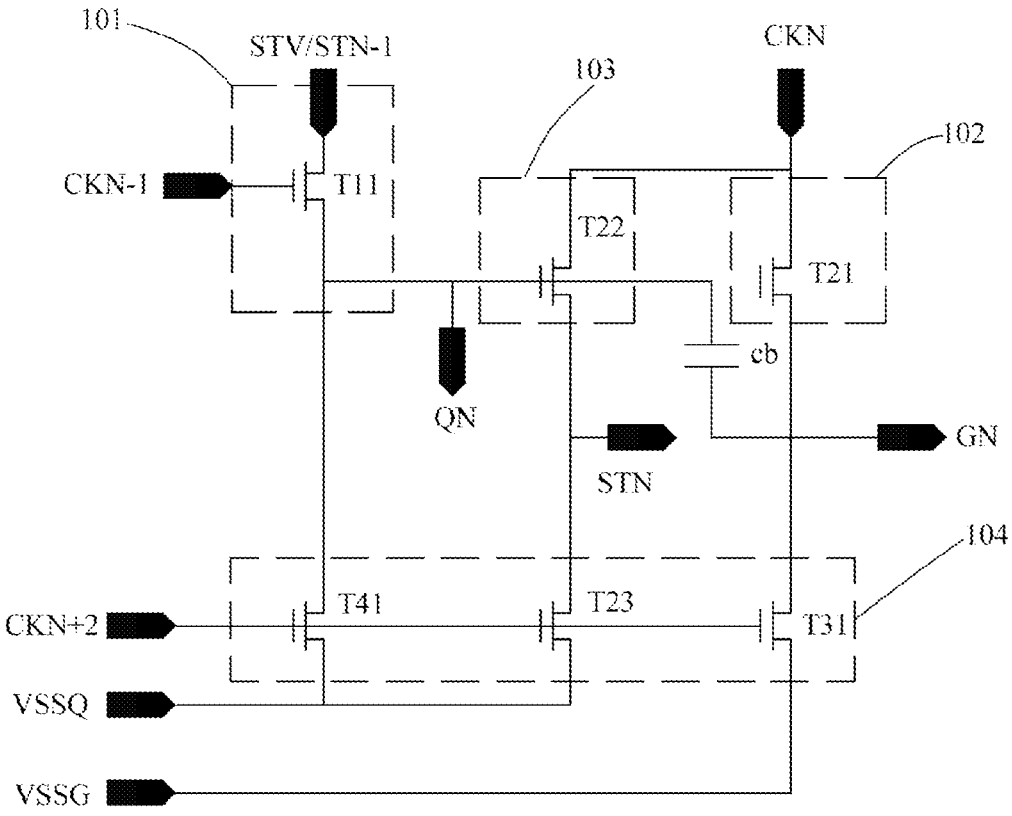

101
STV/STN-1
103
CKN
102
CKN-1
T11
T22
T21
cb
QN
GN
STN
104
CKN+2
T41
T23
T31
VSSQ
VSSG

FIG. 3

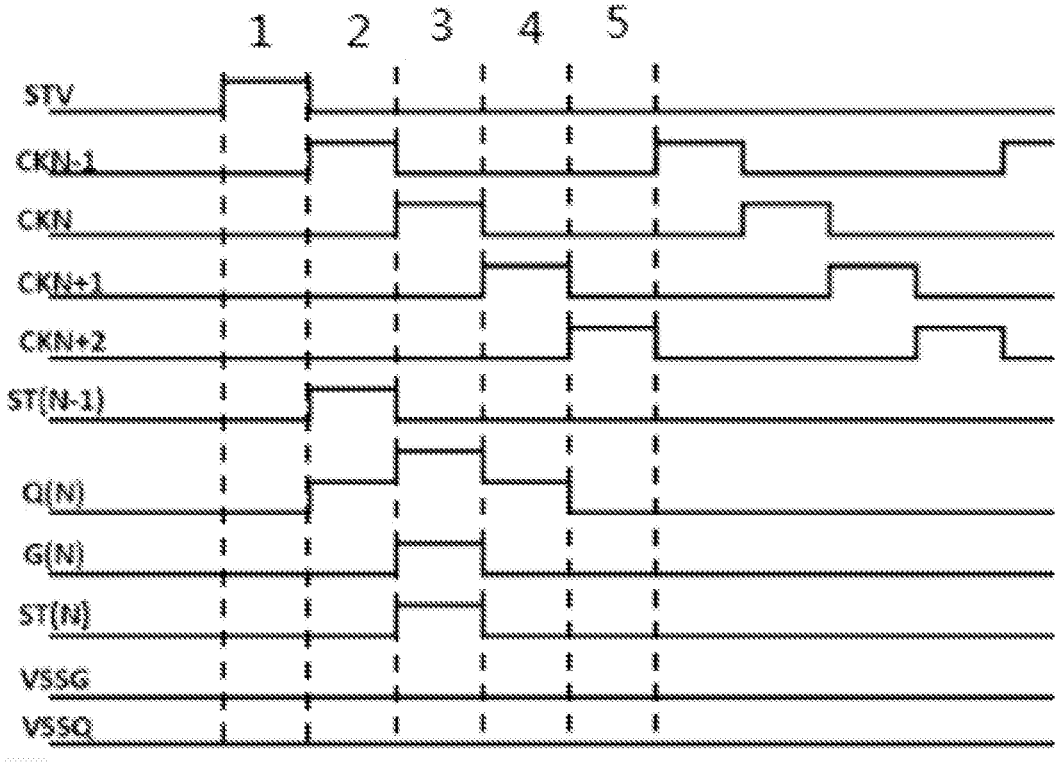


FIG. 4

GOA CIRCUIT AND DISPLAY PANEL

FIELD OF INVENTION

[0001] The present invention relates to the field of display technology, and especially to a gate driver on array (GOA) circuit and a display panel.

BACKGROUND OF INVENTION

[0002] Gate driver on array (GOA) technology is advantageous to a narrow-border display screen design and decreases costs. It has extensive researches and wide applications.

SUMMARY OF INVENTION

[0003] FIG. **1** is a general single stage GOA circuit. FIG. **2** is a timing diagram of the GOA circuit. In the GOA circuit, a threshold voltage of thin film transistors drifts after operating for a long time, which leads to attenuation of output signals ST(N), Q(N), and G(N). Wherein, a conducting state and a turn-off state of thin film transistors having gates controlled by attenuated signals (such as T**11**, T**31**, T**41**, T**25**, T**52**, and T**54** in FIG. **1**) will further deteriorate, which leads to further attenuation of the output signals. Such kind of unstable state will be reduced to a vicious circle, leading to a failure of the GOA circuit. In order to increase reliability of the circuit, an inverter consisting of thin film transistors in FIG. **1** (T**51**, T**52**, T**53**, T**54**) and a node voltage will be added to maintain thin film transistor T**42**, T**26**, and T**32**. However, on the one hand, this approach increases many thin film transistors, resulting in a larger area occupied by the GOA circuit and a wider border of the panel. On the other, gates of T**52** and T**54** of the inverter are also controlled by an attenuated signal Q(N), and a vicious circle results from electric potential competition of node KN and node Q(N) in FIG. **1** still exists, which easily leads to a failure.

[0004] The present invention is to provide a GOA circuit that decreases a thin film transistor number of the GOA circuit and increases stability of the GOA circuit as well.

[0005] The present invention provides a GOA circuit that includes a plurality of cascaded GOA circuit units, wherein an n-stage GOA circuit unit includes a pull-up control circuit unit **101**, a pull-up circuit unit **102**, a transfer circuit unit **103**, a pull-down circuit unit **104**, and a capacitor Cb; wherein the pull-up control circuit unit **101**, the pull-up circuit unit **102**, the transfer circuit unit **103**, the pull-down circuit unit **104**, a pull-down maintenance circuit unit **105**, and the capacitor Cb are all electrically connected to a first node Q(n); the pull-up circuit unit **101** receives a clock signal CKN−1 of an (n−1)-stage GOA circuit unit, and a start trigger signal STV or a cascaded signal STN−1 of the (n−1)-stage GOA circuit unit to charge the first node Q(n) to a high electric potential; the pull-up circuit unit **102** receives a clock signal CKN to pull up an output signal GN of the n-stage GOA circuit unit to a high electric potential of the clock signal CKN; the transfer circuit unit **103** receives the clock signal CKN and outputs a cascaded signal STN of the n-stage GOA circuit unit to control a pull-up control circuit unit of an (n+1)-stage GOA unit to turn on or turn off; the pull-down circuit unit **104** receives a clock signal CKN+2 of an (n+2)-stage GOA circuit unit, a first low-electric-potential direct current signal VSSQ, and a second low-electric-potential direct current signal VSSG to pull down a precharge electric potential of the first node Q(n), an electric potential of the cascaded signal STN of the n-stage GOA circuit unit, and an electric potential of the n-stage scan driving signal G(n) to a low electric potential; and the capacitor Cb is configured to provide and maintain the precharge electric potential of the first node Q(n), and the capacitor Cb is connected to the output signal GN of the n-stage GOA circuit unit.

[0006] Furthermore, the pull-up control circuit unit **101** includes:

[0007] A first thin film transistor T**11**, wherein a gate of the first thin film transistor T**11** is connected to the clock signal CKN−1 of the (n−1)-stage GOA circuit unit, a drain of the first thin film transistor T**11** is connected to the start trigger signal STV or the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit, and a source of the first thin film transistor T**11** is connected to the first node QN.

[0008] Furthermore, the pull-up circuit unit **102** includes:

[0009] A second thin film transistor T**21**, wherein a gate of the second thin film transistor T**21** is connected to the first node QN, a drain of the second thin film transistor T**21** is connected to the clock signal CKN, and a source of the second thin film transistor T**21** is connected to the output signal GN of the n-stage GOA circuit unit.

[0010] Furthermore, the transfer circuit unit **103** includes:

[0011] A third thin film transistor T**22**, wherein a gate of the third thin film transistor T**22** is connected to the first node QN, a drain of the third thin film transistor T**22** is connected to the clock signal CKN, and a source of the third thin film transistor T**22** outputs the cascaded signal STN of the n-stage GOA circuit unit.

[0012] Furthermore, the pull-down circuit unit **104** includes:

[0013] A fourth thin film transistor T**23**, wherein a gate of the fourth thin film transistor T**23** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the fourth thin film transistor T**23** is connected to the cascaded signal STN of the n-stage GOA circuit unit, and a source of the fourth thin film transistor T**23** is connected to the first low-electric-potential direct current signal VSSQ;

[0014] A fifth thin film transistor T**31**, wherein a gate of the fifth thin film transistor T**31** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the fifth thin film transistor T**31** is connected to the output signal GN of the n-stage GOA circuit unit, and a source of the fifth thin film transistor T**31** is connected to the second low-electric-potential direct current signal VSSG; and

[0015] A sixth thin film transistor T**41**, wherein a gate of the sixth thin film transistor T**41** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the sixth thin film transistor T**41** is connected to the first node QN, and a source of the sixth thin film transistor T**41** is connected to the first low-electric-potential direct current signal VSSQ.

[0016] Furthermore, if n is equal to 1, then the drain of the first thin film transistor T**11** is connected to the start trigger signal STV;

[0017] If n is greater than 1, then the drain of the first thin film transistor T**11** is connected to the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit.

[0018] Furthermore, duty ratios of high electric potential of the clock signals CKN−1, CKN, CKN+1, and CKN+2 are 25%, the clock signals sequentially delay, and a delay time between adjacent clock signals is 25% of a clock cycle time;

the high electric potential of the clock signals is identical to a high electric potential of the start trigger signal STV; and a low electric potential of the clock signals is identical to a low electric potential of the start trigger signal STV.

[0019] Furthermore, an electric potential of the first low-electric-potential direct current signal VSSQ is identical to a low electric potential of the start trigger signal STV; and an electric potential of the second low-electric-potential direct current signal VSSG is greater than the electric potential of the first low-electric-potential direct current signal VSSQ.

[0020] Furthermore, the GOA circuit includes phase 1 to phase 5 in one period;

[0021] In phase 1, the start trigger signal STV rises, and the circuit is activated;

[0022] In phase 2, the clock signal CKN−1 and the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit are simultaneously at the high electric potential, while CKN+2 is at the low electric potential, T**41**, T**31**, and T**23** are turned off, and therefore the first node QN of a current stage is charged to the high electric potential, thereby turning on transistors T**21** and T**22**;

[0023] In phase 3, the clock signal CKN−1 is at the low electric potential to turn off T**11**, and simultaneously the clock signal CKN changes into the high electric potential to charge output signals STN and GN to the high electric potential, wherein the output signal GN is configured to drive a current row load of a panel (driving of gate lines), and the output signal STN is cascaded to a next stage (cascaded signal) to charge a first node QN+1 of the next stage to the high electric potential;

[0024] In phase 4, the clock signal CKN changes into the low electric potential and pulls down the output signals STN and GN to the low electric potential; and

[0025] In phase 5, the clock signal CKN+2 is at the high electric potential to turn on T**41**, and to pull the first node QN to the low electric potential, thereby turning off transistors T**21** and T**22**.

[0026] The present invention further provides a display panel that includes the GOA circuit.

[0027] The present invention provides a GOA circuit and a display panel that decrease thin film transistors required by an inverter in a circuit structure. A thin film transistor number is decreased, and an area occupied by a GOA space can be effectively decreased, which facilitates decreasing of border sizes of panels. Gates of thin film transistors of the GOA circuit are controlled by clock signals that have not been attenuated, which can prevent failure resulting from an attenuated cascaded signal caused by threshold voltage drifting of thin film transistors.

DESCRIPTION OF DRAWINGS

[0028] FIG. **1** is a circuit diagram of a gate driver on array (GOA) circuit of conventional technology.

[0029] FIG. **2** is a waveform of timing control and signal output of the GOA circuit of conventional technology.

[0030] FIG. **3** is a circuit diagram of a GOA circuit according to the present invention.

[0031] FIG. **4** is a waveform of timing control and signal output of the GOA circuit according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0032] In order to make a purpose, technical approach, and effect of the present application more clear and definite, the following describes the present application in detail using embodiments with reference to accompanying drawings. It should be understood that specific embodiments described here are merely used to explain the present application and not intended to limit the present application.

[0033] As shown in FIG. **3**, the present invention provides a gate driver on array (GOA) circuit that includes a plurality of cascaded GOA circuits.

[0034] Wherein, an n-stage GOA circuit unit includes a pull-up control circuit unit **101**, a pull-up circuit unit **102**, a transfer circuit unit **103**, a pull-down circuit unit **104**, and a capacitor Cb.

[0035] The pull-up control circuit unit **101**, the pull-up circuit unit **102**, the transfer circuit unit **103**, the pull-down circuit unit **104**, a pull-down maintenance circuit unit **105**, and the capacitor Cb are all electrically connected to a first node Q(n).

[0036] The pull-up circuit unit **101** receives a clock signal CKN−1 of an (n−1)-stage GOA circuit unit, and a start trigger signal STV or a cascaded signal STN−1 of the (n−1)-stage GOA circuit unit, to charge the first node Q(n) in the circuit to a high electric potential.

[0037] The pull-up control circuit unit **101** includes a first thin film transistor T**11**, wherein a gate of the first thin film transistor T**11** is connected to the clock signal CKN−1 of the (n−1)-stage GOA circuit unit, a drain of the first thin film transistor T**11** is connected to the start trigger signal STV or the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit, and a source of the first thin film transistor T**11** is connected to the first node QN.

[0038] The pull-up circuit unit **102** receives a clock signal CKN to pull up an output signal GN of the n-stage GOA circuit unit to a high electric potential of the clock signal CKN.

[0039] The pull-up circuit unit **102** includes a second thin film transistor T**21**, wherein a gate of the second thin film transistor T**21** is connected to the first node QN, a drain of the second thin film transistor T**21** is connected to the clock signal CKN, and a source of the second thin film transistor T**21** is connected to the output signal GN of the n-stage GOA circuit unit.

[0040] The transfer circuit unit **103** receives the clock signal CKN and outputs a cascaded signal STN of the n-stage GOA circuit unit, to control turning on or turning off of a pull-up control circuit unit of an (n+1)-stage GOA unit.

[0041] The transfer circuit unit **103** includes:

[0042] A third thin film transistor T**22**, wherein a gate of the third thin film transistor T**22** is connected to the first node QN, a drain of the third thin film transistor T**22** is connected to the clock signal CKN, and a source of the third thin film transistor T**22** outputs the cascaded signal STN of the n-stage GOA circuit unit.

[0043] The pull-down circuit unit **104** receives a clock signal CKN+2 of an (n+2)-stage GOA circuit unit, a first low-electric-potential direct current signal VSSQ, and a second low-electric-potential direct current signal VSSG, to pull down precharge of the first node Q(n), and pull down electric potential of the cascaded signal STN of the n-stage GOA circuit unit and of the n-stage scan driving signal G(n) to a low electric potential.

[0044] The pull-down circuit unit **104** includes:

[0045] A fourth thin film transistor T**23**, wherein a gate of the fourth thin film transistor T**23** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the fourth thin film transistor T**23** is connected to the cascaded signal STN of the n-stage GOA circuit unit, and a source of the fourth thin film transistor T**23** is connected to the first low-electric-potential direct current signal VSSQ;

[0046] A fifth thin film transistor T**31**, wherein a gate of the fifth thin film transistor T**31** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the fifth thin film transistor T**31** is connected to the output signal GN of the n-stage GOA circuit unit, and a source of the fifth thin film transistor T**31** is connected to the second low-electric-potential direct current signal VSSG; and

[0047] A sixth thin film transistor T**41**, wherein a gate of the sixth thin film transistor T**41** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the sixth thin film transistor T**41** is connected to the first node QN, and a source of the sixth thin film transistor T**41** is connected to the first low-electric-potential direct current signal VSSQ.

[0048] The capacitor Cb is configured to provide and maintain a precharge electric potential of the first node Q(n), and the capacitor Cb is connected to the output signal GN of the n-stage GOA circuit unit.

[0049] Furthermore, if n is equal to 1, then the drain of the first thin film transistor T**11** is connected to the start trigger signal STV; if n is greater than 1, then the drain of the first thin film transistor T**11** is connected to the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit.

[0050] FIG. **4** is a timing control diagram according to the present invention. Wherein, duty ratios of high electric potential of the clock signals CKN−1, CKN, CKN+1, and CKN+2 are 25%. The clock signals sequentially delay, and a delay time between adjacent clock signals is 25% of a clock cycle time.

[0051] The high electric potential of the clock signals is identical to a high electric potential of the start trigger signal STV, and a low electric potential of the clock signals is identical to a low electric potential of the start trigger signal STV.

[0052] An electric potential of the first low-electric-potential direct current signal VSSQ is identical to a low electric potential of the start trigger signal STV, and an electric potential of the second low-electric-potential direct current signal VSSG is greater than the electric potential of the first low-electric-potential direct current signal VSSQ.

[0053] Referring again to FIG. **2**, in one period, in phase 1, the start trigger signal STV rises, and the circuit is activated; in phase 2, the clock signal CKN−1 and the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit are simultaneously at the high electric potential, while CKN+2 is at the low electric potential, T**41**, T**31**, and T**23** are turned off, and therefore the first node QN of a current stage is charged to the high electric potential, thereby turning on transistors T**21** and T**22**; in phase 3, the clock signal CKN−1 is at the low electric potential and turns off T**11**, and simultaneously the clock signal CKN changes into the high electric potential and charges output signals STN and GN to the high electric potential, wherein the output signal GN is configured to drive a current row load of a panel (driving of gate lines), and the output signal STN is cascaded to a next stage (cascaded signal) to charge a first node QN+1 of the next stage to the high electric potential; in phase 4, the clock signal CKN changes into the low electric potential and pulls down the output signals STN and GN to the low electric potential; and in phase 5, the clock signal CKN+2 is at the high electric potential, turns on T**41**, and pulls the first node QN to the low electric potential, thereby turning off transistors T**21** and T**22**.

[0054] Afterward, in each period, the clock signal CKN+2 turns on T**31**, T**41**, and T**23** once, and maintains GN, QN, and STN at a corresponding low electric potential, thereby contributing to a pull-down maintenance effect.

[0055] The present invention provides a GOA circuit that decreases thin film transistors required by an inverter in a circuit structure. A thin film transistor number is decreased, and an area occupied by a GOA space can be effectively decreased, which facilitates decreasing of border sizes of panels. Gates of thin film transistors of the GOA circuit are controlled by clock signals that have not been attenuated, which can prevent failure resulting from an attenuated cascaded signal caused by threshold voltage drifting of thin film transistors.

[0056] The GOA circuit is for a low temperature poly-silicon (LTPS) panel or for an organic light-emitting diode (OLED) panel.

[0057] The first to twelfth thin film transistors are all p-channel thin film transistors or all n-channel thin film transistors.

[0058] The present invention further provides a display panel that includes the above-mentioned GOA circuit. The display panel includes an OLED display panel or a LTPS display panel.

[0059] On the one hand, the GOA circuit decreases thin film transistors required by an inverter in a circuit structure. A number of the thin film transistors is decreased, and an area occupied by a GOA space can be effectively decreased, which facilitates decreasing of border sizes of panels, and facilitates realizing of narrow border designs of the display panel.

[0060] On the other hand, gates of thin film transistors of the GOA circuit are controlled by clock signals that have not been attenuated, which can prevent failure resulting from an attenuated cascaded signal caused by threshold voltage drifting of thin film transistors, thereby increasing reliability of the display panel.

[0061] It can be understood that a person of ordinary skill in the art can make equivalent alternations or changes according to technical approaches of the present application and the invention spirit, and all the changes or alternations are within the protection scope of the appended claims of the present application.

What is claimed is:

1. A gate driver on array (GOA) circuit, comprising a plurality of cascaded GOA circuit units, wherein an n-stage GOA circuit unit comprises a pull-up control circuit unit **101**, a pull-up circuit unit **102**, a transfer circuit unit **103**, a pull-down circuit unit **104**, and a capacitor Cb;

wherein the pull-up control circuit unit **101**, the pull-up circuit unit **102**, the transfer circuit unit **103**, the pull-down circuit unit **104**, a pull-down maintenance circuit unit **105**, and the capacitor Cb are all electrically connected to a first node Q(n);

the pull-up circuit unit **101** receives a clock signal CKN−1 of an (n−1)-stage GOA circuit unit, and a start trigger

signal STV or a cascaded signal STN−1 of the (n−1)-stage GOA circuit unit to charge the first node Q(n) to a high electric potential;

the pull-up circuit unit **102** receives a clock signal CKN to pull up an output signal GN of the n-stage GOA circuit unit to a high electric potential of the clock signal CKN;

the transfer circuit unit **103** receives the clock signal CKN and outputs a cascaded signal STN of the n-stage GOA circuit unit to control a pull-up control circuit unit of an (n+1)-stage GOA unit to turn on or turn off;

the pull-down circuit unit **104** receives a clock signal CKN+2 of an (n+2)-stage GOA circuit unit, a first low-electric-potential direct current signal VSSQ, and a second low-electric-potential direct current signal VSSG to pull down a precharge electric potential of the first node Q(n), an electric potential of the cascaded signal STN of the n-stage GOA circuit unit, and an electric potential of the n-stage scan driving signal G(n) to a low electric potential; and

the capacitor Cb is configured to provide and maintain the precharge electric potential of the first node Q(n), and the capacitor Cb is connected to the output signal GN of the n-stage GOA circuit unit.

2. The GOA circuit as claimed in claim **1**, wherein the pull-up control circuit unit **101** comprises:

a first thin film transistor T**11**, wherein a gate of the first thin film transistor T**11** is connected to the clock signal CKN−1 of the (n−1)-stage GOA circuit unit, a drain of the first thin film transistor T**11** is connected to the start trigger signal STV or the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit, and a source of the first thin film transistor T**11** is connected to the first node QN.

3. The GOA circuit as claimed in claim **1**, wherein the pull-up circuit unit **102** comprises:

a second thin film transistor T**21**, wherein a gate of the second thin film transistor T**21** is connected to the first node QN, a drain of the second thin film transistor T**21** is connected to the clock signal CKN, and a source of the second thin film transistor T**21** is connected to the output signal GN of the n-stage GOA circuit unit.

4. The GOA circuit as claimed in claim **1**, wherein the transfer circuit unit **103** comprises:

a third thin film transistor T**22**, wherein a gate of the third thin film transistor T**22** is connected to the first node QN, a drain of the third thin film transistor T**22** is connected to the clock signal CKN, and a source of the third thin film transistor T**22** outputs the cascaded signal STN of the n-stage GOA circuit unit.

5. The GOA circuit as claimed in claim **1**, wherein the pull-down circuit unit **104** comprises:

a fourth thin film transistor T**23**, wherein a gate of the fourth thin film transistor T**23** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the fourth thin film transistor T**23** is connected to the cascaded signal STN of the n-stage GOA circuit unit, and a source of the fourth thin film transistor T**23** is connected to the first low-electric-potential direct current signal VSSQ;

a fifth thin film transistor T**31**, wherein a gate of the fifth thin film transistor T**31** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the fifth thin film transistor T**31** is connected to the output signal GN of the n-stage GOA circuit unit, and a source of the fifth thin film transistor T**31** is connected to the second low-electric-potential direct current signal VSSG; and

a sixth thin film transistor T**41**, wherein a gate of the sixth thin film transistor T**41** is connected to the clock signal CKN+2 of the (n+2)-stage GOA circuit unit, a drain of the sixth thin film transistor T**41** is connected to the first node QN, and a source of the sixth thin film transistor T**41** is connected to the first low-electric-potential direct current signal VSSQ.

6. The GOA circuit as claimed in claim **2**, wherein if n is equal to 1, then the drain of the first thin film transistor T**11** is connected to the start trigger signal STV; if n is greater than 1, then the drain of the first thin film transistor T**11** is connected to the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit.

7. The GOA circuit as claimed in claim **1**, wherein

duty ratios of high electric potential of the clock signals CKN−1, CKN, CKN+1, and CKN+2 are 25%, the clock signals sequentially delay, and a delay time between adjacent clock signals is 25% of a clock cycle time;

the high electric potential of the clock signals is identical to a high electric potential of the start trigger signal STV; and

a low electric potential of the clock signals is identical to a low electric potential of the start trigger signal STV.

8. The GOA circuit as claimed in claim **1**, wherein

an electric potential of the first low-electric-potential direct current signal VSSQ is identical to a low electric potential of the start trigger signal STV; and

an electric potential of the second low-electric-potential direct current signal VSSG is greater than the electric potential of the first low-electric-potential direct current signal VSSQ.

9. The GOA circuit as claimed in claim **1**, wherein the GOA circuit comprises phase 1 to phase 5 in one period;

in phase 1, the start trigger signal STV rises, and the circuit is activated;

in phase 2, the clock signal CKN−1 and the cascaded signal STN−1 of the (n−1)-stage GOA circuit unit are simultaneously at the high electric potential, while CKN+2 is at the low electric potential, a sixth thin film transistor T**41**, a fifth thin film transistor T**31**, and a fourth thin film transistor T**23** are turned off, and therefore the first node QN of a current stage is charged to the high electric potential, thereby turning on a second thin film transistor T**21** and a third thin film transistor T**22**;

in phase 3, the clock signal CKN−1 is at the low electric potential to turn off T**11**, and simultaneously the clock signal CKN changes into the high electric potential to charge output signals STN and GN to the high electric potential, wherein the output signal GN is configured to drive a current row load of a panel (driving of gate lines), and the output signal STN is cascaded to a next stage (cascaded signal) to charge a first node QN+1 of the next stage to the high electric potential;

in phase 4, the clock signal CKN changes into the low electric potential and pulls down the output signals STN and GN to the low electric potential; and

in phase 5, the clock signal CKN+2 is at the high electric potential to turn on the sixth thin film transistor T**41**,

and to pull the first node QN to the low electric potential, thereby turning off the second thin film transistor T**21** and the third thin film transistor T**22**.

10. A display panel, comprising the GOA circuit as claimed in claim **1**.

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