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Forbes

(54) **MEMORY ARRAY WITH ULTRA-THIN ETCHED PILLAR SURROUND GATE ACCESS TRANSISTORS AND BURIED DATA/BIT LINES**

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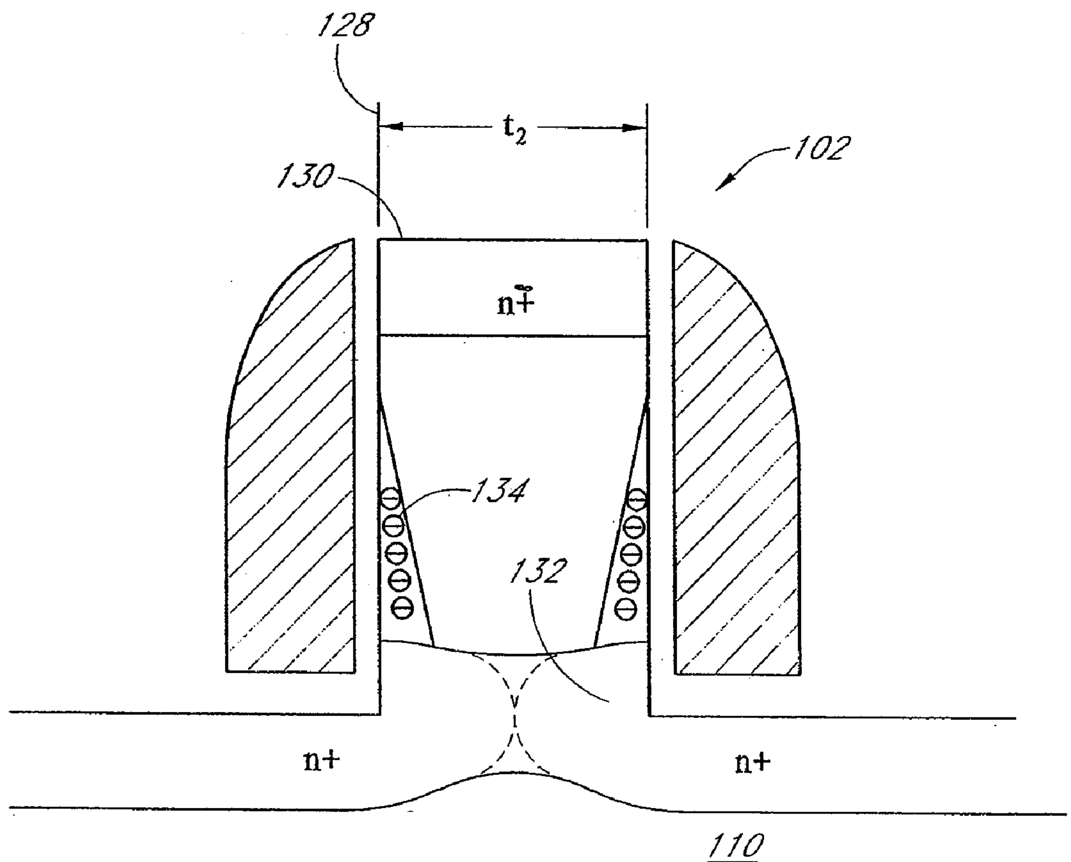
(57) **ABSTRACT**

A memory array with data/bit lines extending generally in a first direction formed in an upper surface of a substrate and access transistors extending generally upward and aligned generally atop a corresponding data/bit line. The access transistors have a pillar extending generally upward with a source region formed so as to be in electrical communication with the corresponding data/bit line and a drain region formed generally at an upper portion of the pillar and a surround gate structure substantially completely encompassing the pillar in lateral directions and extending substantially the entire vertical extent of the pillar and word lines extending generally in a second direction and in electrical contact with a corresponding surround gate structure at at least a first surface thereof such that bias voltage applied to a given word line is communicated substantially uniformly in a laterally symmetric extent about the corresponding pillar via the surround gate structure.



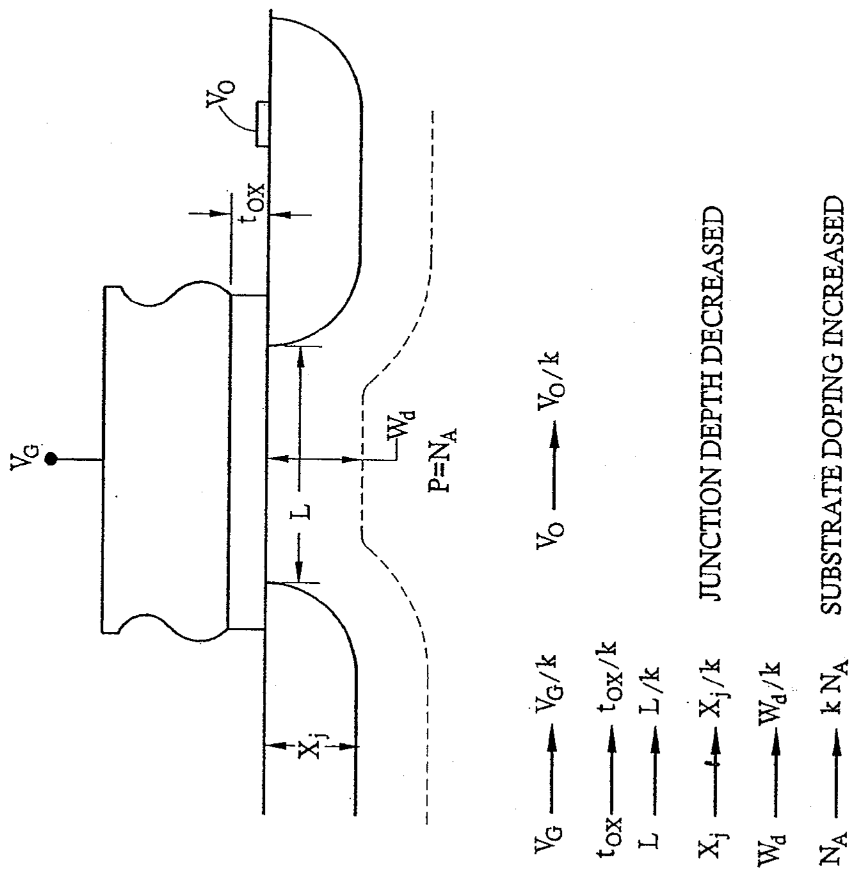


FIG. 1
(PRIOR ART)

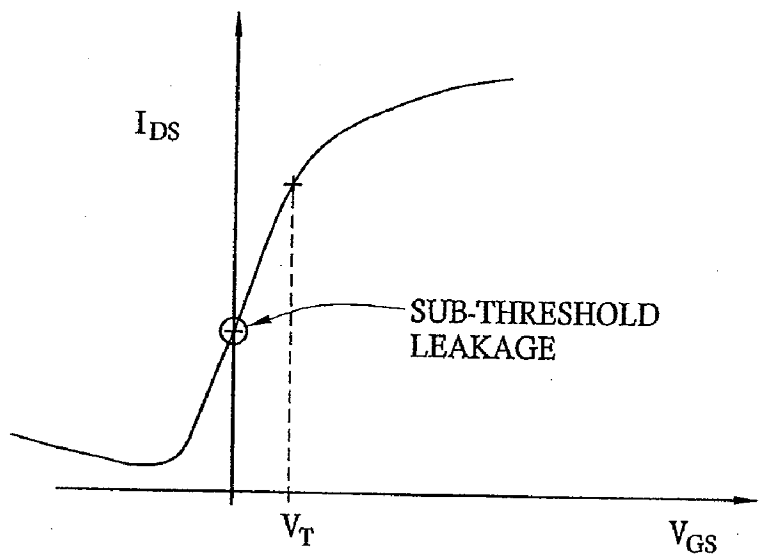


FIG. 2
(PRIOR ART)

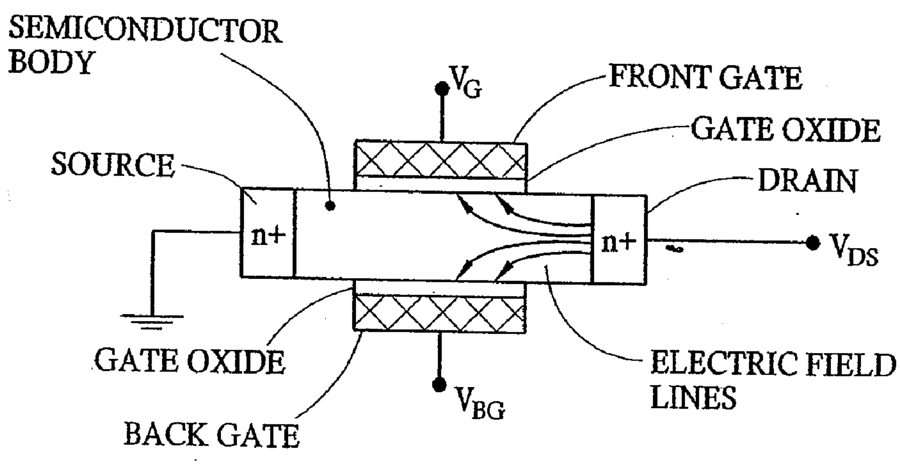


FIG. 3
(PRIOR ART)

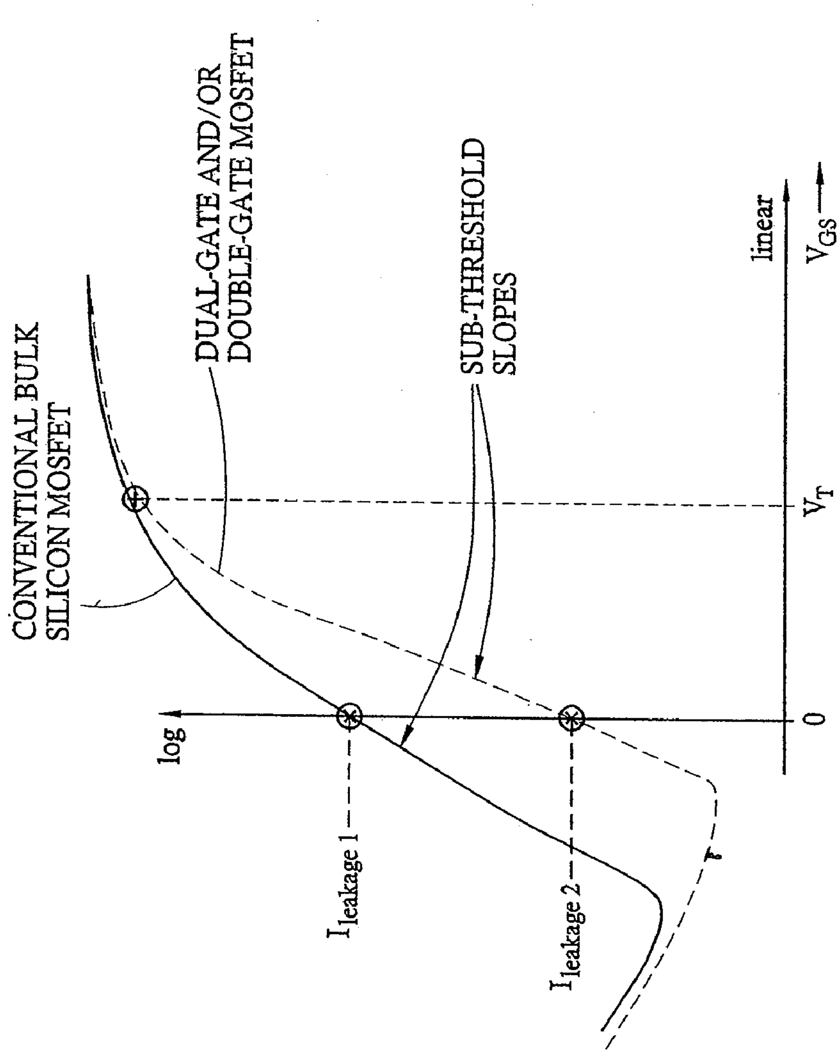


FIG. 4
(PRIOR ART)

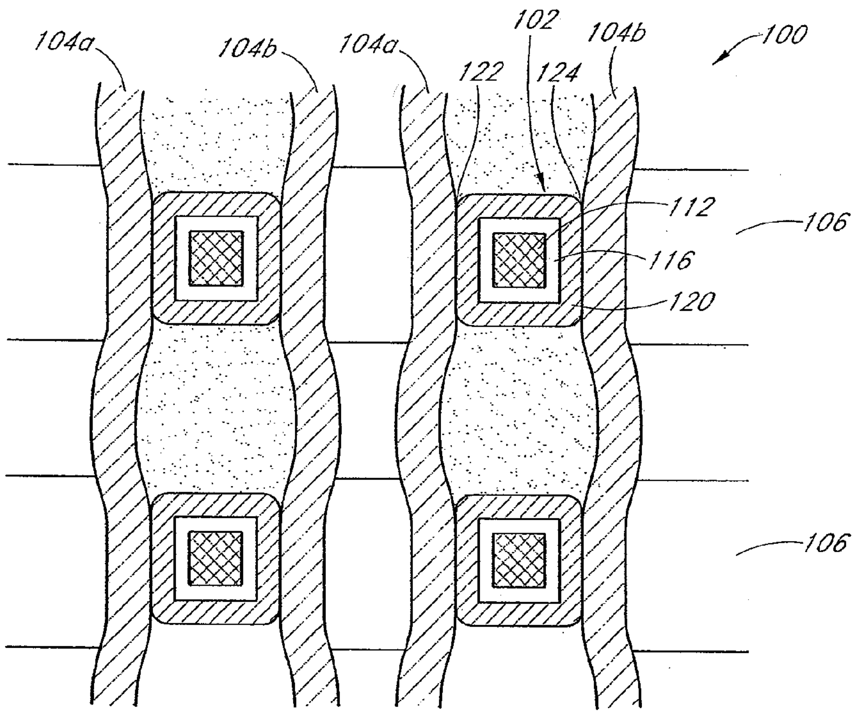

104a
104b
104a
102
104b
100
122
124
112
106
116
120
106

FIG. 5A

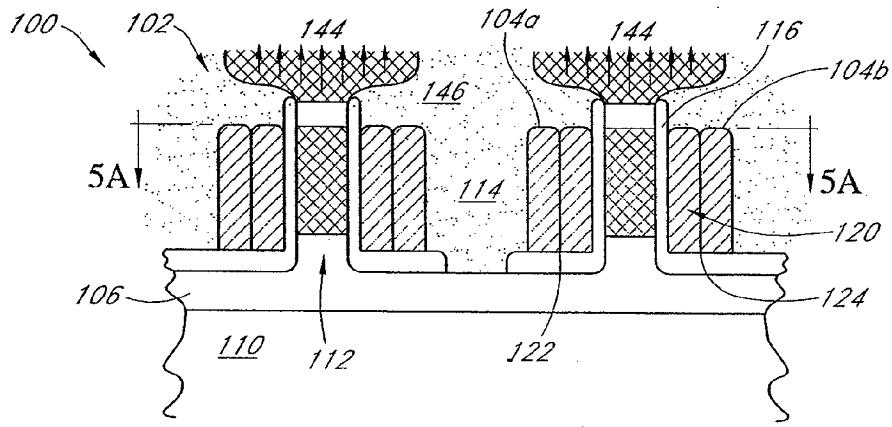

100
102
144
104a
144
116
104b
146
5A
114
5A
120
106
124
110
112
122

FIG. 5B

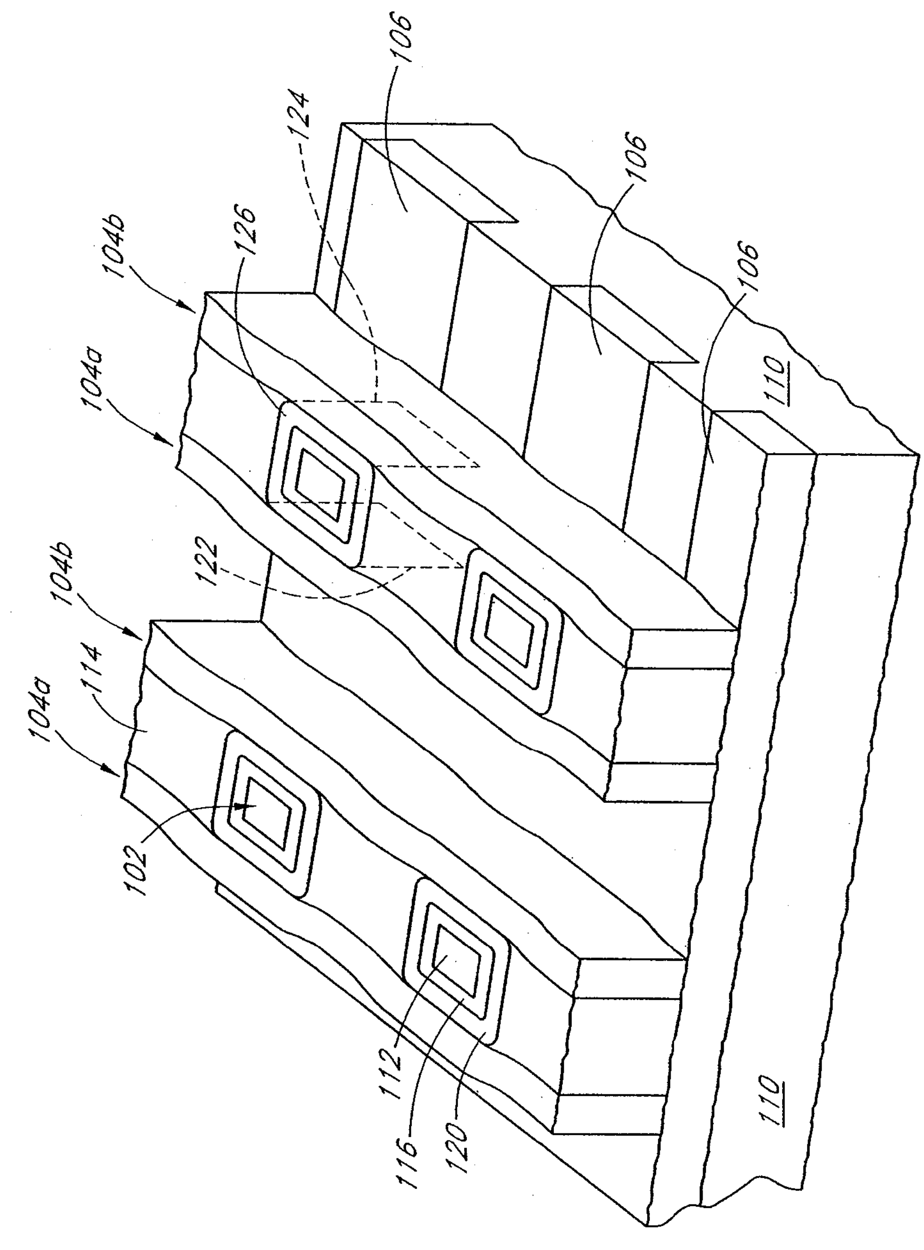

104a
104b
104a
104b
126
124
106
106
106
106
110
114
102
122
112
116
120
110

FIG. 6

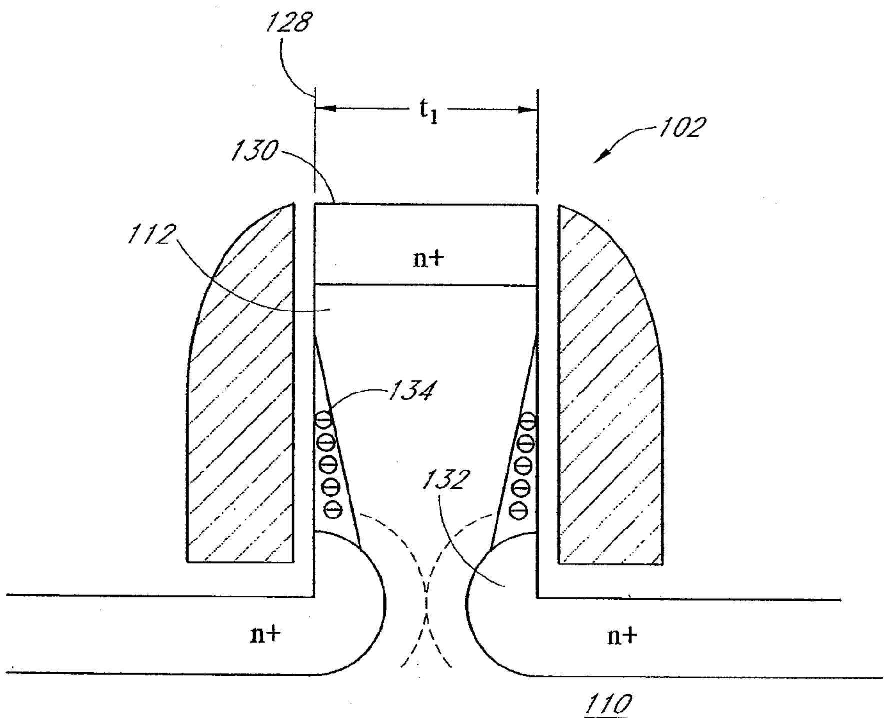


FIG. 7A

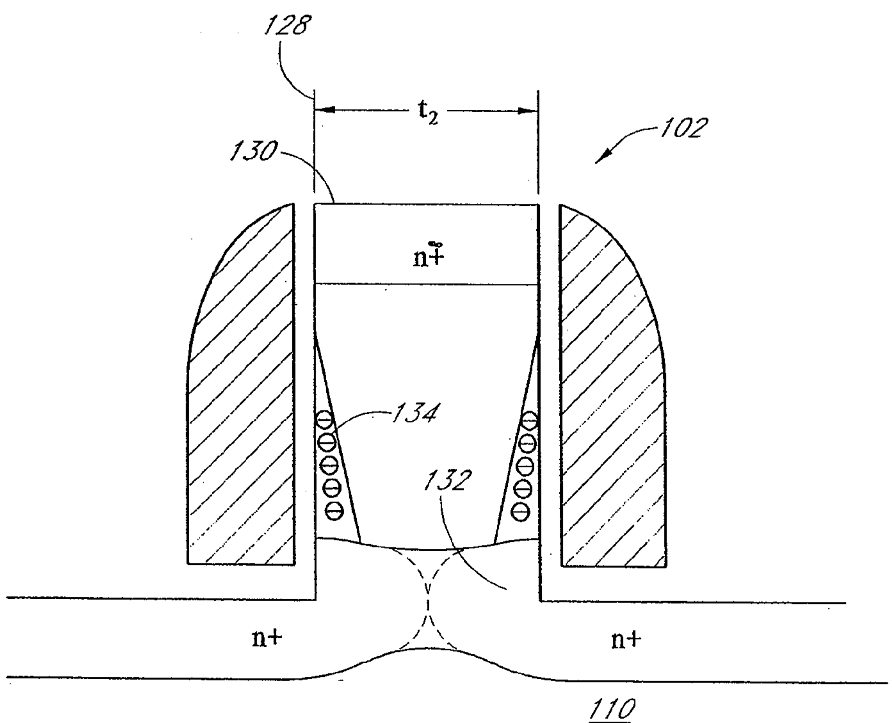


FIG. 7B

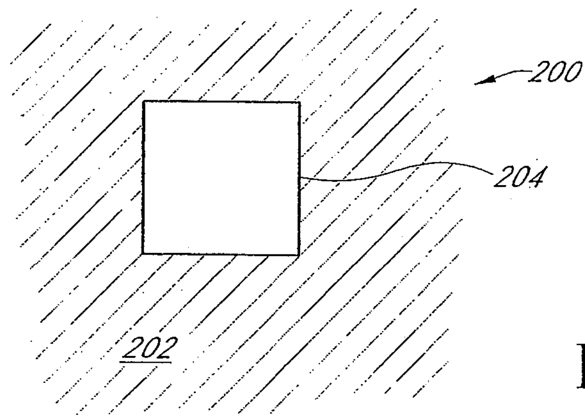


FIG. 8A

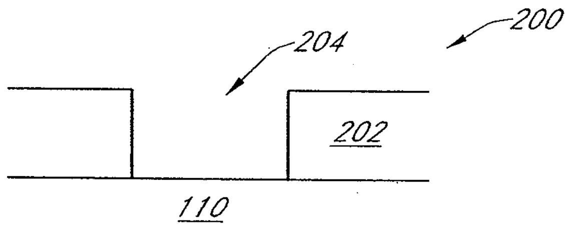


FIG. 8B

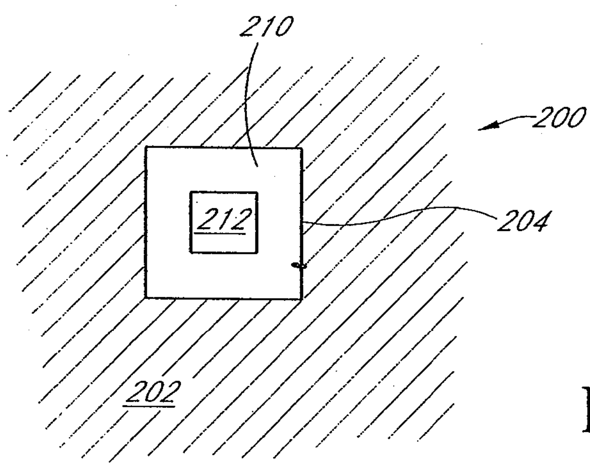


FIG. 9A

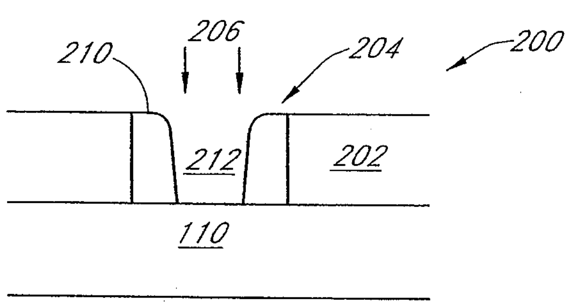


FIG. 9B

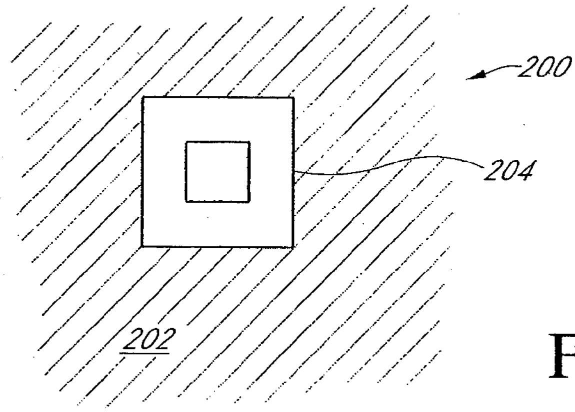


FIG. 10A

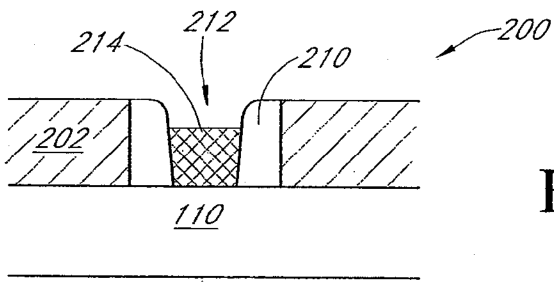


FIG. 10B

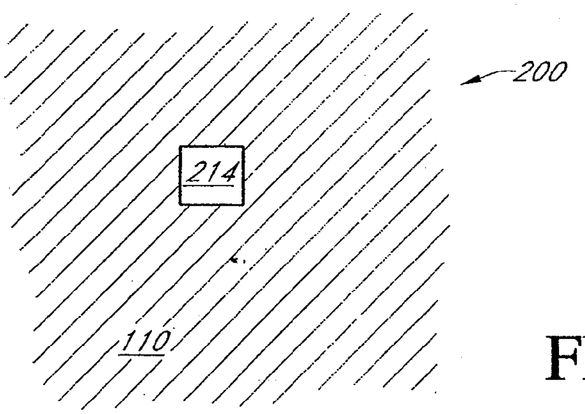


FIG. 11A

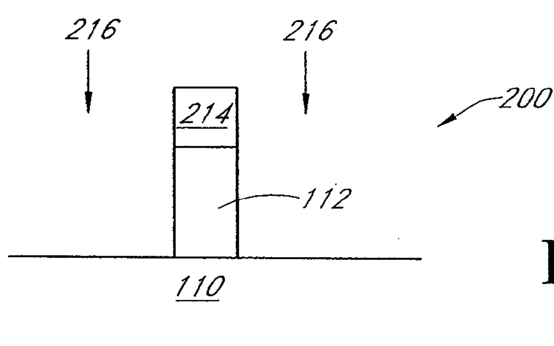


FIG. 11B

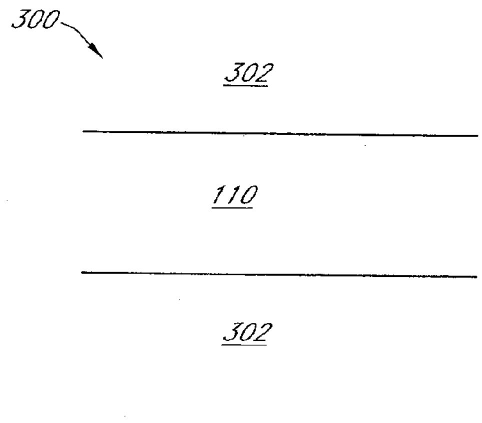


FIG. 12A

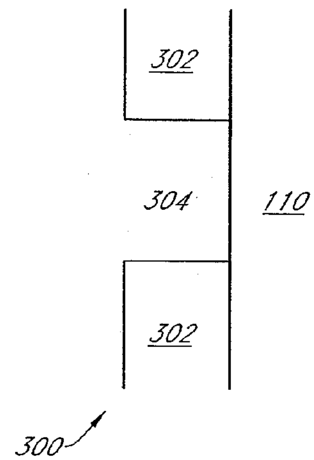


FIG. 12B

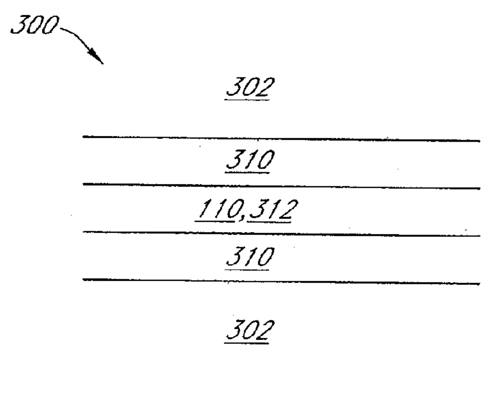


FIG. 13A

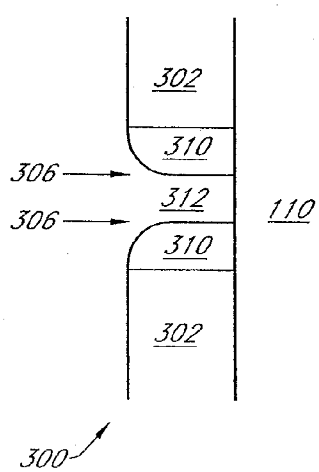


FIG. 13B

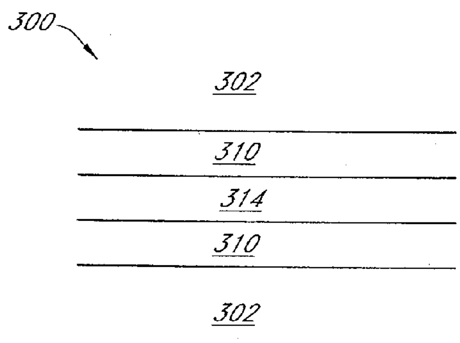


FIG. 14A

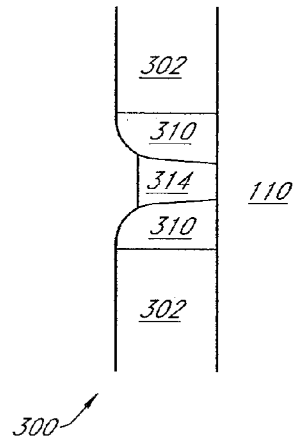


FIG. 14B

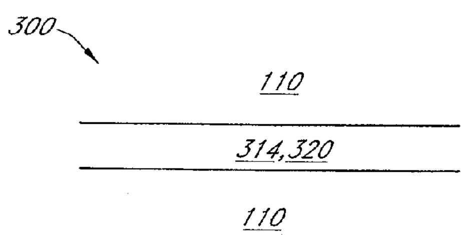


FIG. 15A

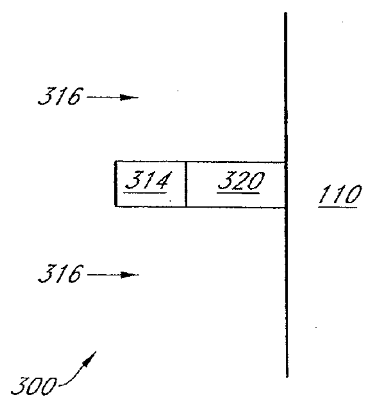


FIG. 15B

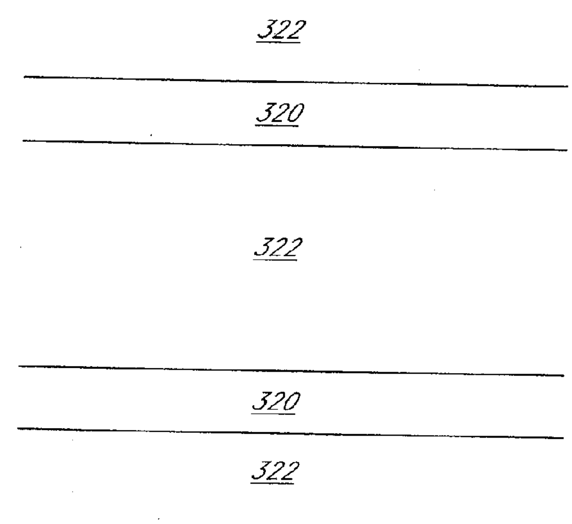


FIG. 16A

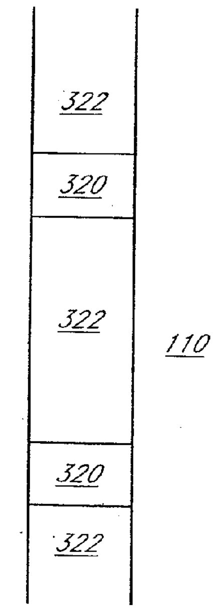


FIG. 16B

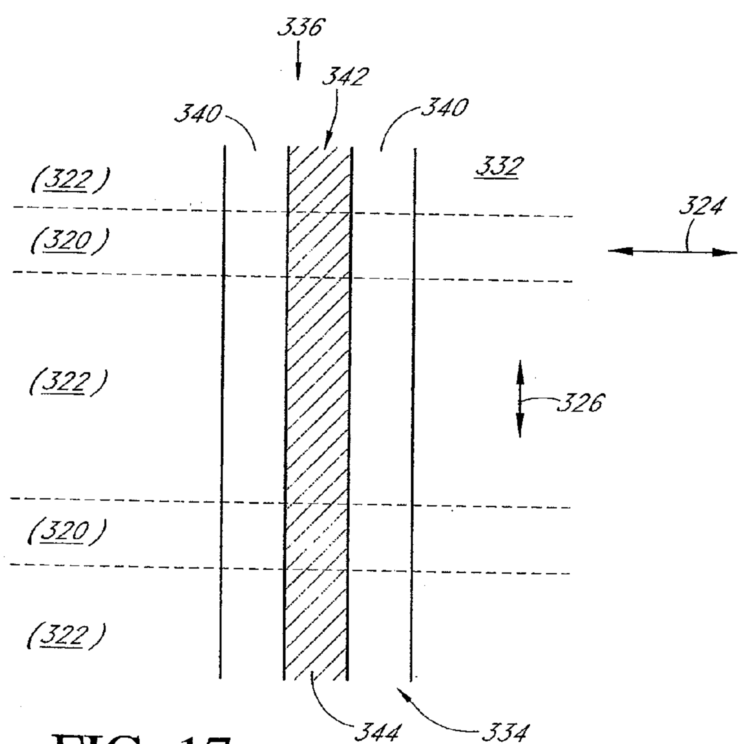


FIG. 17

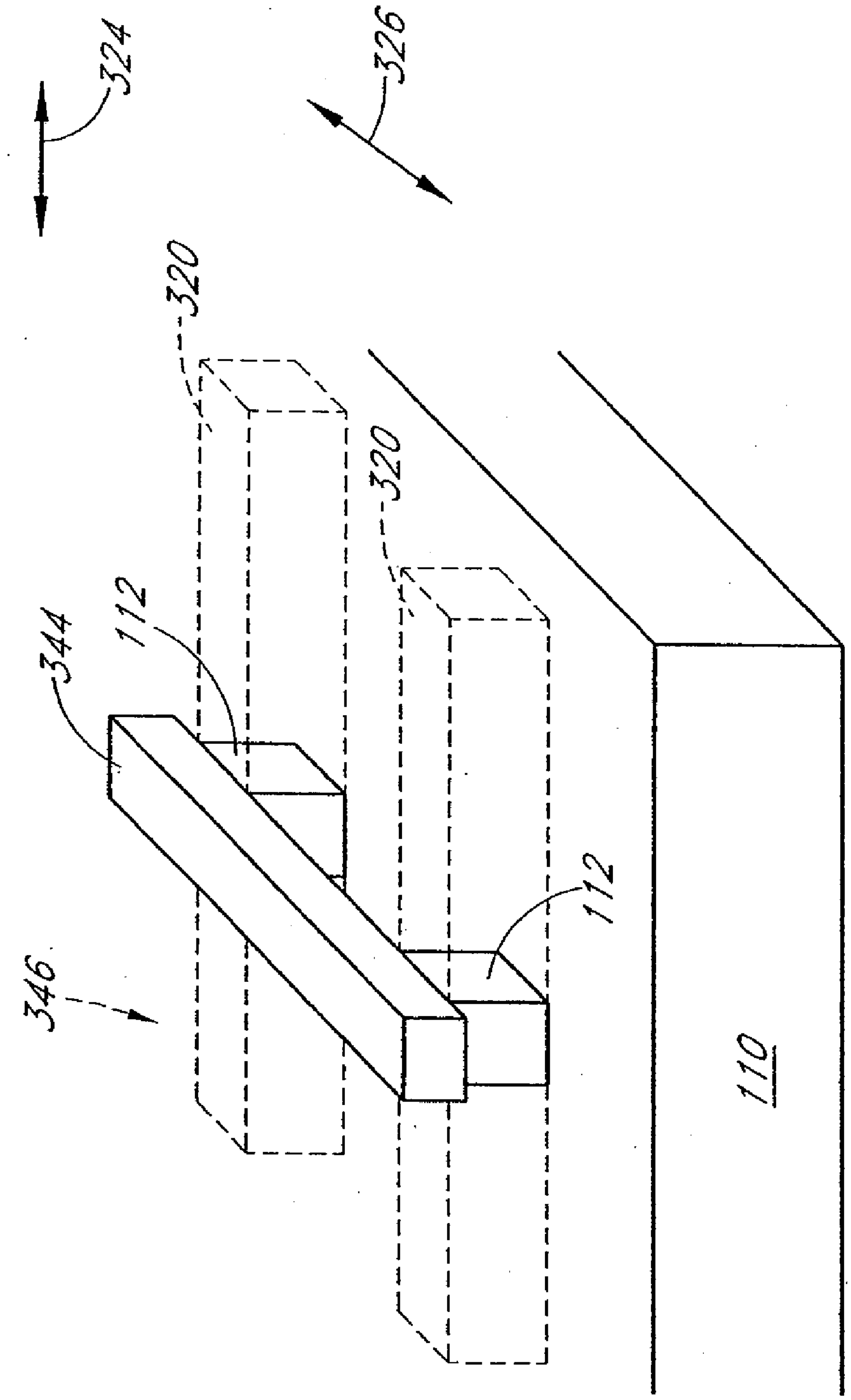


FIG. 18

FIG. 19A

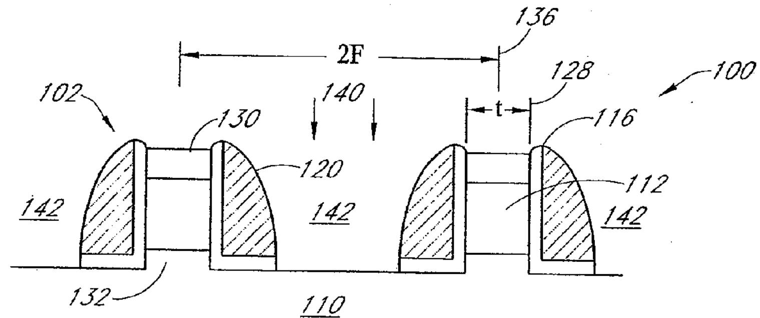


FIG. 19B

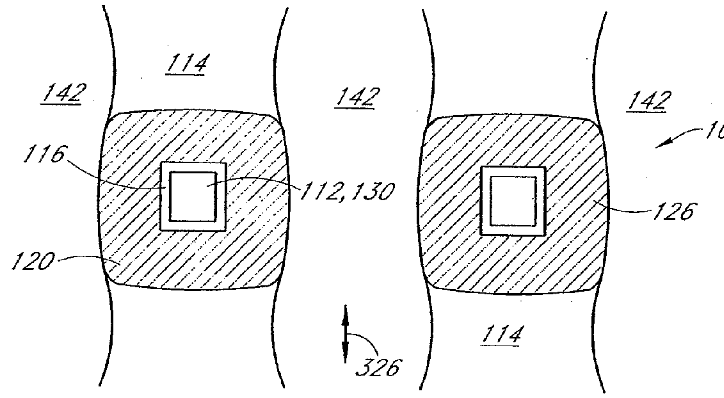


FIG. 20A

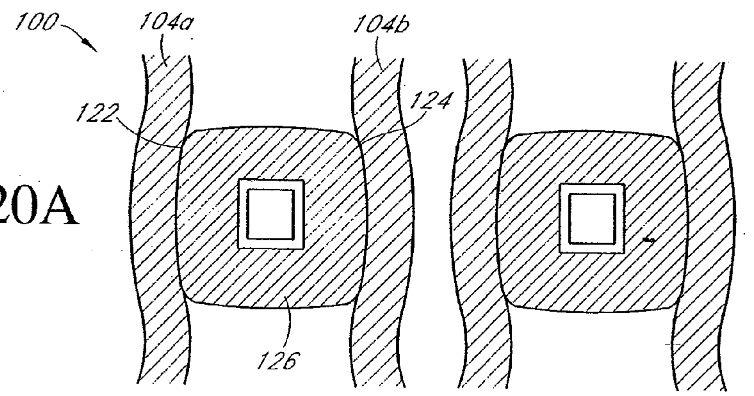
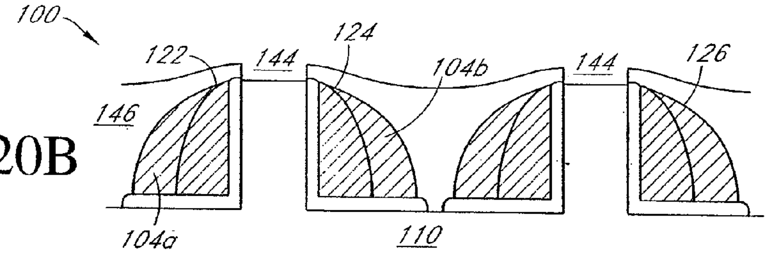


FIG. 20B



MEMORY ARRAY WITH ULTRA-THIN ETCHED PILLAR SURROUND GATE ACCESS TRANSISTORS AND BURIED DATA/BIT LINES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 13/050,819, filed Mar. 17, 2011, which is a continuation of U.S. application Ser. No. 12/407,615, filed Mar. 19, 2009, now U.S. Pat. No. 7,8910,972, which is a continuation of U.S. application Ser. No. 11/457,423, filed Jul. 13, 2006, now U.S. Pat. No. 7,525,141, which is a divisional application of U.S. patent application Ser. No. 11/129,502, filed May 13, 2005, now U.S. Pat. No. 7,371,627, the entireties of which are hereby incorporated herein by reference to be considered part of this specification.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates to the field of high density semiconductor memory arrays and more particularly to arrays with vertical transistors having sub-photolithographic device dimensions with ultra-thin pillars and substantially fully surrounding gates suitable for use as access transistors, such as for DRAM arrays.

[0004] 2. Description of the Related Art

[0005] Ongoing scaling of metal oxide semiconductor field effect transistor (MOSFET) technology to the deep sub-micron region where channel lengths are less than 0.1 micron (100 nanometers or 1,000 Å) causes significant problems in conventional transistor structures. Generally, junction depth should be much less than the channel length, and thus for a channel length of, for example, 1,000 Å, this implies junction depths on the order of a few hundred Angstroms. Such shallow junctions are difficult to form by conventional implantation and diffusion techniques.

[0006] FIG. **1** illustrates general trends and relationships for a variety of device parameters with scaling by a factor k. As another example, with an aggressive scaling factor, extremely high levels of channel doping are required to suppress undesirable short channel effects, such as drain induced barrier lowering (DIBL), threshold voltage roll off, and sub-threshold conduction. Sub-threshold conduction is particularly problematic in dynamic random access memory (DRAM), as it significantly reduces the charge storage retention time of the capacitor cells. Extremely high doping level generally results in increased leakage and reduced carrier mobility, thus making the channel shorter to improve performance is offset or negated by the lower carrier mobility and higher leakage. This leakage current is a significant concern and problem in low voltage and low power battery operated complimentary metal oxide semiconductor (CMOS) circuits and systems, particularly in DRAMs.

[0007] This is shown in FIG. **2** as that if low voltages are used for this low power operation, then there is a problem with threshold voltages and standby leakage current being of large enough value to degrade overall circuit performance. For example, to achieve significant overdrive and reasonable system switching speeds, the threshold voltage magnitudes are desirably small, in this example near 0 volts, however then the transistor, such as an access transistor, will always have a large sub-threshold leakage current. Various technologies have been employed to allow low voltage operation with deep sub-micron CMOS transistors that can have relatively large variations in threshold voltage, yet still have relatively low sub-threshold leakage currents at standby.

[0008] For example, one technique used in scaling down transistors is referred to as dual-gated or double-gated transistor structures. The terminology generally employed in the industry is "dual-gate" if the transistor has a front gate and a back gate which can be driven with separate and independent voltages and "double-gated" to describe structures where both gates are driven with the same potential. In certain aspects, a dual-gated and/or double-gated MOSFET offers better device characteristics than conventional bulk silicon MOSFETs. Because a gate electrode is present on both sides of the channel, rather than only on one side as in conventional planar MOSFETs, the electrical field generated by the drain electrode is better screened from the source end of the channel than in conventional planar MOSFETs, as illustrated schematically by the field lines in FIG. **3**.

[0009] This can result in an improved sub-threshold leakage current characteristic, as illustrated schematically in FIG. **4**. The dual-gate and/or double-gate MOSFET turns off and the sub-threshold current is reduced more quickly as the gate voltage is reduced. However, even though dual gate and/or double gate structures offer advantages over conventional bulk silicon MOSFETs, there remains a desire for continued improvement in device performance, for example, reduced sub-threshold leakage current, particularly with continued scaling.

SUMMARY OF THE INVENTION

[0010] The above referenced needs are satisfied by the invention which in one embodiment is a memory array comprising a semiconductive substrate, a plurality of conductive data/bit lines extending generally in a first direction and formed in an upper surface of the substrate, a plurality of access transistors extending generally upward from the upper surface of the substrate and aligned generally atop a corresponding data/bit line, wherein the access transistors comprise a pillar extending generally upward from the upper surface of the substrate and generally aligned atop the corresponding data/bit line wherein a source region is formed generally at a lower portion of the pillar so as to be in electrical communication with the corresponding data/bit line and a drain region is formed generally at an upper portion of the pillar, wherein the pillar intermediate the source and drain regions is substantially fully depleted and a surround gate structure substantially completely encompassing the pillar in lateral directions and extending substantially the entire vertical extent of the pillar, and a plurality of conductive word lines extending generally in a second direction and in electrical contact with a corresponding surround gate structure at at least a first surface thereof such that bias voltage applied to a given word line is communicated substantially uniformly in a lateral extent about the corresponding pillar via the surround gate structure.

[0011] Another embodiment is a method of fabricating a memory array comprising forming a plurality of data/bit lines in a surface of a substrate so as to extend in a first direction, forming a first mask layer on the surface of the substrate, forming first elongate openings in the first mask layer so as to be aligned generally with and extending along corresponding data/bit lines, depositing sidewall material in the first openings of the first mask layer, directionally etching the sidewall material so as to form first sidewall spacers arranged against inner surfaces of the first openings and defining generally centrally arranged first trenches in the first sidewall spacers between opposed sidewall spacers, forming first plug strips in corresponding first trenches, performing a directional etch with the first plug strips as masking structures so as to define a corresponding plurality of pillar strips extending generally vertically from the surface of the substrate and substantially conforming to the contour and position of the first plug strips, filling interstitial spaces between the pillar strips with fill material, forming a second mask layer on the surface of the substrate, forming second elongate openings in the second mask layer so as to overlie in an intersecting manner and extend in a second direction across corresponding data/bit lines and the pillar strips, depositing sidewall material in the second openings of the second mask layer, directionally etching the sidewall material so as to form second sidewall spacers arranged against inner surfaces of the second openings and defining generally centrally arranged second trenches in the second sidewall spacers between opposed sidewall spacers, forming second plug strips in corresponding second trenches, performing a directional etch with the second plug strips as masking structures so as to define a corresponding plurality of pillars extending generally vertically from the surface of the substrate and substantially conforming to the contour and position of intersections of the first and the second plug strips, and forming gate structures about the pillars such that the gate structures substantially completely laterally encompass corresponding pillars.

[0012] A further embodiment is a method of fabricating a memory array comprising forming a plurality of data/bit lines in a surface of a substrate, forming a mask layer on the surface of the substrate, forming openings in the mask layer so as to be aligned generally with corresponding data/bit lines, depositing sidewall material in the openings of the mask layer, directionally etching the sidewall material so as to form sidewall structures arranged against inner surfaces of the openings and defining a generally centrally arranged hole in the sidewall structures, forming a plug structure in the holes, performing a directional etch with the plug structures as masking structures so as to define a plurality of pillars extending generally vertically from the surface of the substrate and substantially conforming to the contour and position of the plug structures, and forming gate structures about the pillars such that the gate structures substantially completely encompass corresponding pillars.

[0013] Thus, various embodiments provide a memory array including access transistors over buried data/bit lines which include substantially surrounding gate structures which provide improved sub-threshold performance and relatively high device density. Certain embodiments provide the ability to fabricate relatively precisely defined device features of sub-photolithographic dimensions. Embodiments also provide word lines that contact surround gate structures for improved control of the conduction channel. These and other objects and advantages of the invention will be more apparent from the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. **1** is schematic illustration of general relationships of various device parameters/characteristics for a scaling factor k;

[0015] FIG. **2** is a graph illustrating sub-threshold leakage in a conventional silicon MOSFET;

[0016] FIG. **3** is a schematic illustration of a known dual-gate MOSFET;

[0017] FIG. **4** is a graph illustrating sub-threshold conduction characteristics of conventional bulk silicon MOSFETs and of dual-gate and/or double gate MOSFETs;

[0018] FIG. **5**A is a top section view along A-A' of FIG. **5**B which is a side section view both of one embodiment of an array of ultra-thin etched pillar access transistors;

[0019] FIG. **6** is a perspective view of the embodiments shown in section in FIGS. **5**A and **5**B;

[0020] FIG. **7**A is a side section view of one embodiment of an access transistor in a memory array and illustrating schematically electrical operation thereof;

[0021] FIG. **7**B is a side section view of another embodiment of an access transistor in a memory array and illustrating schematically electrical operation thereof;

[0022] FIGS. **8**A-**11**A are top views and FIGS. **8**B-**11**B are side section views respectively of one embodiment of fabricating an ultra-thin body transistor;

[0023] FIGS. **12**A-**16**A are top views and FIGS. **12**B-**16**B are end section views respectively of another embodiment of fabricating an ultra-thin body transistor;

[0024] FIG. **17** is a top view of a further fabrication step in one embodiment of fabricating an ultra-thin body transistor;

[0025] FIG. **18** is a perspective view of yet a further step in one embodiment of fabricating an ultra-thin body transistor;

[0026] FIGS. **19**A and **19**B are side section and top views respectively of one embodiment of a method of forming surround gate structures; and

[0027] FIGS. **20**A and **20**B are side section and top views respectively of one embodiment of a method of forming word/address lines in enclosing contact with the surround gate structures.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] Reference will now be made to the drawings of the various embodiments of the invention wherein like reference numerals will refer to like parts/structures throughout. FIGS. **5**A, **5**B, and **6** illustrate a top section view, side section view, and perspective view respectively of one embodiment of a memory circuit access array **100**, which in following will be referred to as the array **100** for brevity. The array **100** provides access with a plurality of memory cells, in certain embodiments an array of DRAM cells, which can be utilized for storage and access of information. The array **100** comprises a plurality of access transistors **102**, each of which is in electrical communication with a corresponding word line **104** and data/bit line **106**. In this particular embodiment of the array **100**, the word lines **104** are arranged generally parallel to each other. The data/bit lines are as well arranged substantially in parallel with each other, and also extending generally transversely with respect to the word lines **104**. In this particular embodiment, a pair of word lines **104***a* and **104***b* are provided for any given access transistor **102** and are arranged on opposite sides of each access transistor **102**.

[0029] The array **100** is formed on top of a semiconductive substrate **110**, in one particular embodiment comprising silicon. As can be seen in the side section view of FIG. **5**B, the data/bit lines **106** extend across an upper surface of the substrate **110**. In certain embodiments, the data/bit lines **106** comprise doped silicon regions of the substrate **110** and in one particular embodiment, n+ doped silicon. The array **100** also comprises a plurality of generally vertically extending ultra thin semiconductive pillars **112** forming a part of the structure of each access transistor **102** and positioned generally aligned with and atop corresponding buried data/bit lines **106**. An insulator layer **114** is positioned atop the substrate **110** and interposed portions of the data/bit lines **106** and includes gate insulator regions **116** which, in this embodiment, extend generally upward and substantially circumferentially enclose or encompass each of the semiconductive pillars **112**. Thus, the semiconductive pillars **112** are generally configured as ultra-thin vertically extending posts, cylinders, prisms, or the like, and the respective gate insulator regions **116** are configured as corresponding hollow posts, pillars, cylinders, prisms, or the like with the inner surface of the gate insulator region **116** conforming in cross-section to the outer surface of the respective semiconductive pillar **112** such that the two are in contact with each other.

[0030] Similarly, the array **100** comprises a corresponding plurality of gate conductor structures **120** which are also configured as generally vertically extending structures substantially encompassing or encircling and overlaid about the respective gate insulator region **116** with the enclosed semiconductive pillar **112**. In one particular embodiment, the gate conductors **120** comprise polycrystalline silicon (polysilicon). The gate conductors **120** are arranged with respect to corresponding word lines **104***a* and **104***b*, such that the gate conductor **120** is in electrical contact with the respective word line **104***a* along a first contact surface **122**, and such that the gate conductor **120** is in electrical contact with the respective word line **104***b* along a second contact surface **124** which is arranged substantially opposite the first contact surface **122**.

[0031] Thus, as the word lines **104***a* and **104***b* comprise conductive material which is in electrical contact with the gate conductor **120**, also comprising electrically conductive material, along the opposed first and second contact surfaces **122**, **124**, electrical potential which is provided via the word lines **104***a*, **104***b* will thus be conducted via the gate conductor **120** so as to substantially encompass or encircle the gate insulator region **116** and semiconductive pillar **112** which are arranged within the interior of the gate conductor **120**. The electric potential/field within the pillars **112** will be substantially laterally or horizontally symmetric at a given vertical position of the pillar **112** (see FIGS. **7**A and **7**B). Thus, a surround gate structure **126** is defined wherein an electrical potential can be provided substantially encircling or encompassing the enclosed semiconductive pillar **112**, however wherein the gate insulator region **116** inhibits electrical conduction therebetween.

[0032] This surround gate structure **126** (FIG. **6**), by providing regulated electrical potential via the word lines **104***a* and **104***b* and further via the gate conductor **120** about substantially all lateral sides, faces, directions of the generally vertically extending semiconductive pillar **112**, provides even more control of a gate potential applied to/removed from the pillar **112** as opposed to only a single side of a gate as in conventional bulk silicon processes and devices or the opposed sides of a dual gate and/or double gate MOSFET structure. In one embodiment, the doping of the pillars **112** is such that the transistors **102** operate from a substantially fully depleted state. Thus, in this embodiment, absence of an applied potential to the surround gate structure **126** substantially removes a conduction channel **134** (FIGS. **7**A and **7**B) thereby avoiding the need to apply a potential to turn off the transistors **102**. This embodiment provides simplified and more convenient operation of the array **100** and facilitates integration with other systems.

[0033] FIGS. **7**A and **7**B illustrate in side section view in greater detail embodiments of portions of the array **100** including the access transistors **102** thereof. FIG. **7**A illustrates one embodiment of the access transistor **102**, wherein the pillar **112** has a thickness **128** indicated as t_1 and similarly for FIG. **7**B the pillar **112** having a pillar thickness **128** t_2. While the illustrations herein are schematic in nature and should not be interpreted as being to scale, in these embodiments, the pillar thickness **128** t_1 is greater than the pillar thickness **128** t_2. It will be further appreciated that the pillar thickness **128** referred to can comprise multiple laterally-extending thickness measurements, such as in embodiments wherein the pillar **112** defines generally a rectangular prism structure, or generally a single lateral diameter dimension in embodiments wherein the pillar **112** defines generally a cylindrical vertically-extending structure.

[0034] In the embodiments illustrated in FIGS. **7**A and **7**B, drain regions **130** are defined generally adjacent the upper extent of the pillars **112** and source regions **132** positioned generally adjacent the lower extent of the pillars **112**. In one particular embodiment, the drain region **130** and source region **132** comprise regions of the semiconductive pillar **112** which are doped n+. In these embodiments, when the access transistor **102** is in an off condition, the surround gate structure **126** will be at substantially a zero or a negative bias. In this case, the access transistor **102** of these embodiments offers better device characteristics than conventional bulk silicon MOSFETs. These improved device characteristics arise because the thin physical dimensions of the ultra-thin semiconductive pillars **112** facilitate full depletion of the transistor **102** with relatively low doping levels. In one embodiment, a major pillar thickness **128** of approximately 100 nm with doping density of approximately $1\times10^{15}/cm^3$ provides the transistor **102** with substantially full depletion characteristics. Thus, embodiments of the array **100** offer increased circuit density with individual transistors **102** having relatively low doping densities in the pillars **112** thereof which reduces the aforementioned problems with relatively high doping levels which would otherwise be indicated to mitigate short channel effects.

[0035] Further, because the surround gate structure **126** encloses all lateral sides of a conduction channel **134** rather than only on one side as in conventional MOSFETs or separate opposed sides as in a dual gate and/or double gate MOSFET, more effective control of the channel is provided. The conduction channels **134** of these embodiments will describe generally a vertically extending annulus or ring structure conforming generally to the cross-sectional contour of the corresponding semiconductive pillar **112**. As previously noted, the conduction channels **134** are substantially horizontally symmetric at a given vertical position of the pillars **112**. With the surrounding gate structure **126** combined with the ultra thin semiconductive pillar **112**, electric field generated by the drain region **130** is better screened from the source region **132** at the opposite end of the conduction channel **134** region, thereby reducing subthreshold and standby leakage current therebetween. As previously indicated, this leakage current is a significant device parameter of the memory array **100**, particularly when the array **100** is configured as an array of DRAMs. The subthreshold and leakage current is a significant variable in determining the maximum retention time and the corresponding requirements for refreshing of logic states stored in the array **100** and the corresponding time or intervals between required refresh operations.

[0036] During read and write operations to the various cells of the array **100**, the surround gate structure **126** is biased positive to a value based on the particular application, however generally on the order of a few tenths of a volt. Depending upon the pillar thickness **128**, as well as the implantation and diffusion parameters employed for the particular application of the array **100**, the source region **132** may or may not substantially extend across the lower extent of the semiconductive pillar **112**. Thus, in the embodiment of FIG. **7**A, wherein the pillar thickness **128** is somewhat thicker as indicated by t_1, the source region **132** would not extend entirely across the lower extent of the semiconductive pillar **112**. In contrast, in the embodiment illustrated by FIG. **7**B, the pillar thickness **128** is relatively thinner or narrower indicated as T_2, and in this embodiment, the source region **132** would extend substantially across the bottom or lower extent of the semiconductive pillar **112**. As the source region **132** of the embodiment illustrated in FIG. **7**B extends across the base of the pillar **112** and thus provides a full p/n junction across the lower extent of the pillar **112**, this embodiment is generally preferred. Because the pillar thickness **128** is relatively small, application of high temperature processes to induce lateral diffusion of implanted dopants to form the source regions **132** is reduced, thereby avoiding the problematic aspects of more extreme high temperature parameters such as would be required with wide pillar structures. For example, in one embodiment, the array **100** is formed with high temperature process parameters not exceeding approximately 800° C. and 10 minutes. Embodiments of fabrication of the array **100** will be described in greater detail below.

[0037] FIGS. **8**A and **8**B through **11**A and **11**B illustrate schematically one embodiment of methods **200** of forming ultra thin body transistors, such as the access transistors **102** previously described, wherein the transistors **102** have sublithographic dimensions. In this particular embodiment, the transistors **102** are formed by a side wall spacer technique described in greater detail below. As shown in FIGS. **8**A and **8**B, in top and side section views respectively, a mask material **202** is formed on top of the underlying substrate **110** and an opening **204** is formed in the mask layer **202** so as to expose a portion of the underlying substrate **110**. The opening **204** is formed generally to conform to the desired cross-sectional shape of the surround gate structure **126** and semiconductive pillar **112**. Thus, while a generally square-shaped opening **204** is illustrated, this is for ease of illustration and is only one of many possible shapes of the opening **204**.

[0038] Following as shown in FIGS. **9**A and **9**B, again in top and side section views respectively, spacer material, in one embodiment comprising silicon oxide, is deposited within the opening **204** of the mask layer **202**. This spacer material is subjected to an anisotropic etch **206** so as to form a sidewall spacer structure **210** positioned generally against inner surfaces of the opening **204** formed in the mask layer **202** and further so as to form a generally centrally positioned hole **212** generally in the center of the sidewall spacer structure **210** and the opening **204**. Then as shown in FIGS. **10**A and **10**B, again in top and side section views respectively, a pillar plug **214** is formed within the generally centrally located hole **212** in the sidewall spacer structure **210**. In one embodiment, the pillar plug **214** comprises silicon nitride which is deposited, planarized, and etched so as to partially recess the pillar plug **214** within the hole **212**. This pillar plug **214** is subsequently utilized as a masking structure for etching of the underlying substrate **110** so as to define the semiconductive pillars **112**. Thus, the profile and dimensions of the pillar plug **214** generally corresponds to the subsequently formed semiconductive pillars **112**.

[0039] Then, as shown in FIGS. **11**A and **11**B, the mask **202** and side wall spacer structure **210** are removed so as to leave the pillar plug **214**. An etch **216** is performed to remove portions of the upper surface of the substrate **110** with the pillar plug **214** as a masking structure. Thus, the vertically extending pillar **112** is defined extending upwards from the upper surface of the substrate **110**.

[0040] FIGS. **12**A-**16**A, **12**B-**16**B, **17**, and **18** illustrate steps of another embodiment of a method **300** for forming pillars **112** for the ultra thin body transistors **102**. In this embodiment, a mask layer **302** is formed on top of the underlying substrate **110** and a generally elongate first mask opening **304** is formed therein. For ease of illustration and understanding, certain steps of the method **300** will be illustrated with respect to formation of a single semiconductive pillar **112**, however, it will be understood that generally the method **300** would be employed to fabricate a plurality of the pillars **112** so as to subsequently define the array **100**.

[0041] As shown in FIGS. **12**A and **12**B in top and end section view respectively, a first mask layer **302** is formed on the substrate **110** with a plurality of first openings **304** formed therein so as to expose generally parallel elongate trenchlike structures. Following as illustrated in FIGS. **13**A and **13**B, sidewall material is formed within the first opening **304** and exposed to an anisotropic etch **306** so as to define first sidewall spacers **310** which also extend in an elongate manner generally along the sides of the first opening **304** formed in the mask layer **302**. The anisotropic etch **306** further defines a first central trench **312** which similarly extends in an elongate manner between opposed sidewall spacers **310**.

[0042] As shown in FIGS. **14**A and **14**B in top and end section views respectively, a first plug strip **314** is formed within the first central trench **312** and in one particular embodiment comprises silicon nitride which is deposited, planarized, and etched so as to form the first plug strip **314** generally in a similar manner to that previously described for the pillar plug **214** of the method **200**.

[0043] Following as illustrated in FIGS. **15**A and **15**B, again in top and end section views respectively, an etch **316** is performed employing the first plug strip **314** as a masking structure so as to define a plurality of underlying generally vertically extending pillar strips **320**, which are elongate extending generally upward from the substrate **110** and corresponding generally to the contour and dimensions of the first plug strips **314**. As further illustrated in FIGS. **16**A and **16**B, again in top and end section views respectively, the first plug strips **314** are removed, and the spaces between the first pillar strips **320** and above the substrate **110** are formed with a fill material **322** which, in one embodiment, comprises a back filling with silicon oxide.

[0044] Following as illustrated in FIG. **17** in top view, the preceding steps of the method **300** are repeated substantially as previously described, however with the difference that the structures previously described, such as the first pillar strips **320**, are formed aligned generally along a first direction **322** and the following structures are fabricated oriented generally along a perpendicularly arranged second direction **326**. Thus, as illustrated in FIG. **17**, a second mask layer **332** is formed with a second opening **334** formed to extend generally in the second direction **326**. These structures are formed to overly the previously formed pillar strips **320** and fill material **322** which are illustrated in dashed lines and with parenthetical reference numbers. Similarly, a sidewall material is formed within the second opening **334** and exposed to an anisotropic etch **336** so as to define second sidewall spacers **340** and a second central trench **342** positioned generally between the opposed sidewall spacers **340**, again with these structures oriented generally in the second direction **326**. The second central trench **342** is again filled with material so as to form a second plug strip **344**, again extending generally along the second direction **326**.

[0045] Then as illustrated in perspective view in FIG. **18**, an etch **346** is performed employing the second plug strip **344** as a masking structure. As the second plug strip **344** extends generally along the second direction **326** and overlies the previously formed pillar strips **320** extending generally in the first direction **324**, the excess material of the first pillar strips **320** not masked by the intersecting second plug strip **344** is removed during the etch process **346** so as to define a corresponding plurality of generally vertically extending semiconductive pillars **112** extending generally vertically upward from the underlying substrate **110**. Thus, in these embodiments, the size and configuration of the resultant semiconductive pillars **112** corresponds to the intersection envelope between the first plug strips **314** and second plug strips **344**. In certain applications, the embodiments of the method **300** may provide advantages compared to the embodiments of the method **200** as the profile of the resultant semiconductive pillars **112** is defined by the intersection of the edges of the first plug strip **314** and second plug strip **344** which are configured as elongate strips rather than the single pillar plugs **214** of the method **200**. In certain applications, edges may be more precisely defined than the contour of individual holes, such as the central hole **212**.

[0046] FIGS. **19**A, **19**B, **20**A, and **20**B illustrate the further fabrication of the surround gate structures **126** and word lines **104** in this embodiment in a side wall spacer based process. As shown in FIG. **19**A, the respective pillars **112** define a device to device spacing **136**, separated by a distance **2**F as shown. The pillars **112** also define a pillar thickness **128** indicated by t in FIG. **15**. In these embodiments, the pillar thickness **128** is much less than the photolithographic dimension limit F, and thus the array **100** defines device features, such as the pillar thickness **128**, which are below the photolithographic dimension F.

[0047] As shown in FIG. **19**A, the gate insulator region **116** is grown or deposited and then polysilicon is further deposited on the gate insulator regions **116**. An anisotropic etch **140** is then performed so as to define sidewall structures of the encompassing gate insulator region **116** and surrounding gate conductor **120**. Then, as shown in FIG. **19**B, in one embodiment, this structure is back filled, such as with the insulator layer **114** comprising oxide. Trenches **142** are formed in this back fill material, such as the insulator layer **114**, wherein the trenches are interposed between adjacent transistors **102** and in one particular embodiment, extending generally in the second direction **326**.

[0048] As shown in FIG. **20**A, polysilicon or metal is deposited and anisotropically etched so as to be in contact generally at the first surface **122** and opposed second surface **124** defining the word/address lines **104***a* and **104***b*. The remainder of the process to form the array **100**, for example, establishment of capacitor contacts **144** and formation of cap/passivation structures **146** as shown in FIG. **20**B (also FIG. **5**B) can be formed using conventional techniques well understood by one of ordinary skill in the art. It will also be understood that certain intermediate processes, such as implants/diffusion processes for example to dope the pillars **112** and form the drain **130** and source **132** regions to form the array **100** will also be well understood by one of ordinary skill.

[0049] Thus, the aforementioned embodiments describe methods **200** and **300** for forming an array **100** of memory cells, such as an array of DRAM cells, having access transistors **102** with semiconductive pillars **112** of ultra thin dimensions. In certain embodiments, the device dimensions, such as the pillar thickness **128**, are much less than a photolithographic process limit F providing particularly efficient and densely packed components of the array **100**. Further advantages of the embodiments described herein are the formation of a surround gate structure **126** which provides more effective control of the conduction channel **134** with the aggressive scaling provided by these embodiments. Furthermore, certain embodiments provide a substantially fully depleted pillar **112** structure of ultra-thin dimensions which reduces the need for extremely high doping levels to reduce short channel effects and the attendant problems of high doping levels.

[0050] Although the foregoing description of the preferred embodiment of the present invention has shown, described, and pointed out the fundamental novel features of the invention, it will be understood that various omissions, substitutions, and changes in the form of the detail of the apparatus as illustrated, as well as the uses thereof, may be made by those skilled in the art without departing from the spirit of the present invention.

What is claimed is:

1. A method of fabricating a memory array comprising:

forming a pillar extending generally upward from an upper surface of a semiconductive substrate and generally aligned atop a corresponding data/bit line;

forming a source region generally at a lower portion of the pillar so as to be in electrical communication with the corresponding data/bit line;

forming a drain region generally at an upper portion of the pillar, wherein the pillar intermediate the source and drain regions is substantially fully depleted;

forming a gate structure substantially about the pillar in lateral directions, the pillar, the source region, the drain region, and the gate structure comprising an access transistor, the access transistor being substantially off with no applied gate potential; and

forming at least one conductive word line extending generally transversely to the corresponding data/bit line and in electrical contact with the gate structure along at least a first surface thereof such that bias voltage applied to the conductive word line is communicated about the pillar via the gate structure.

2. The method of claim **1** further comprising forming a second wordline in electrical contact with the gate structure along at least a second surface which is arranged substantially opposite the first surface.

3. The method of claim **1** wherein the corresponding data/bit line comprises n+ doped silicon regions of the substrate.

4. The method of claim **1** wherein a pair of wordlines is provided for the access transistor and the wordlines are arranged on opposite sides of the access transistor.

5. The method of claim 1 wherein the pillar defines generally a rectangular prism structure.

6. The method of claim 1 wherein the pillar defines generally a cylindrical vertically-extending structure.

7. The method of claim 1 wherein the drain region and the source region comprise regions of the pillar which are doped n+.

8. The method of claim 1 wherein the gate structure substantially encloses all lateral sides of a conduction channel.

9. The method of claim 1 wherein the source region substantially extends across a base of the pillar to provide a substantially full p/n junction.

10. The method of claim 1 further comprising interconnecting the upper portion of the pillar to a storage capacitor contacts to form at least a portion of a dynamic random access memory (DRAM) array.

11. A method of fabricating a memory array comprising:

forming a pillar extending generally upward from an upper surface of a semiconductor substrate and aligned in association with a corresponding data/bit line;

forming a source region generally at a lower portion of the pillar so as to be in electrical communication with the corresponding data/bit line;

forming a drain region generally at an upper portion of the pillar, wherein at least a portion of the pillar intermediate the source and drain regions is depleted; and

forming a gate structure substantially about the pillar, the pillar, the source region, the drain region, and the gate structure comprising an access transistor, the access transistor being substantially off with no applied gate potential; and

forming at least one conductive word line in electrical contact with the gate structure along at least a first surface thereof such that bias voltage applied to a given word line is communicated about the corresponding pillar via the gate structure.

12. The method of claim 11 further comprising forming a second wordline in electrical contact with the gate structure along at least a second surface which is arranged substantially opposite the first surface.

13. The method of claim 11 wherein the corresponding data/bit line comprises n+ doped silicon regions of the substrate.

14. The method of claim 11 wherein a pair of wordlines is provided for the access transistor and the wordlines are arranged on opposite sides of the access transistor.

15. The method of claim 11 wherein the pillar defines generally a rectangular prism structure.

16. The method of claim 11 wherein the pillar defines generally a cylindrical vertically-extending structure.

17. The method of claim 11 wherein the drain region and the source region comprise regions of the pillar which are doped n+.

18. The method of claim 11 wherein the gate structure substantially encloses all lateral sides of a conduction channel.

19. The method of claim 11 wherein the source region substantially extends across a base of the pillar to provide a substantially full p/n junction.

20. The method of claim 11 further comprising interconnecting the upper portion of the pillar to a storage capacitor contact to form at least a portion of a dynamic random access memory (DRAM) array.

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