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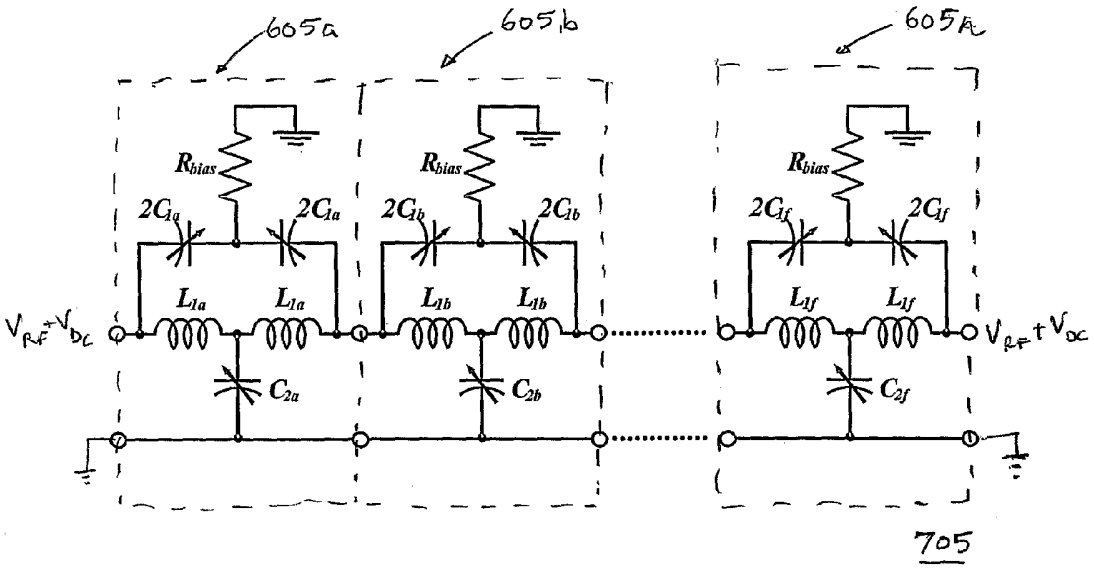
(54) **Title:** ANALOG PHASE SHIFTER USING CASCADED VOLTAGE TUNABLE CAPACITOR



(57) **Abstract:** A circuit topology is configured to flatten out a phase- and amplitude-response over a specified range of frequencies. The circuit topology also provides a large cumulative phase- shift. In one embodiment, the circuit topology cascades a plurality of all-pass sections, with the center-frequencies of each all-pass section staggered to create a substantially flat phase- response over a frequency range. Further, in one embodiment the plurality of all-pass sections has at least one all-pass section that is different from another all-pass section. Each all-pass section includes a tunable capacitor and has a center- frequency that can be varied by electronically tuning the capacitor. Each center frequency is selected to obtain substantially constant amplitude and phase response over a desired frequency range and capacitance tuning range.

WO 2006/130712 A2

ANALOG PHASE SHIFTER USING CASCADED VOLTAGE TUNABLE CAPACITOR

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims a benefit of, and priority under 35 USC § 119(e) to, U.S. Provisional Patent Application No. 60/690,452, filed June 13, 2005, titled "Analog Phase Shifters Using Voltage-Tunable Capacitors", and U.S. Provisional Application No. 60/686,100, filed May 31, 2005, titled "Broadband and Compact Analog Phase-Shifters Using Voltage-Tunable Capacitors," and U.S. Utility Patent Application No. 11/288,723, filed November 28, 2005, titled "Analog Phase Shifter Using Cascaded Voltage Tunable Capacitor," the contents of these applications which are herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0002] The present invention generally relates to the field of analog phase shifters and more specifically, to analog phase shifters using voltage variable capacitors.

2. DESCRIPTION OF THE RELATED ART

[0003] All-pass networks are used in communication electronics for phase-compensation and phase-shifting networks. The transfer function for a simple fourth-order all-pass network has the form

$$H(\omega)=\frac{\omega^2+aj\omega-b^2}{\omega^2-aj\omega-b^2} \quad (1)$$

[0004] Consequently, the amplitude response is a constant and only the signal phase is affected. Fourth-order lumped-element all-pass networks can be constructed from "bridged-tee" circuits. Figures 1a and 1b illustrate conventional bridged-tee circuits and design equations for realizing all-pass transfer functions. Specifically, Figures 1a illustrates a conventional bridged low-pass tee and Figure 1b illustrates a conventional bridged high pass tee.

[0005] The relevant design equations are also given with these figures, where R is the desired input/output impedance of the circuit. Note that

$$C_2 = 4C_1 \quad \text{and} \quad R = \sqrt{\frac{2L_1}{C_2}}.$$

[0006] Two related conventional all-pass sections are shown in Figures 2a and 2b. These sections include a shunt resonator element to achieve a more rapid variation in phase near the center frequency, specified by the Q-factor in the design equations. In Figures 1a and 2b, the conventional all-pass networks are illustrated with $Q \geq 1$. These circuits reduce to that of Figures 1a and 1b when Q = 1.

[0007] The phase response of a conventional phase shifter circuit using bridged-tee networks can be varied electronically by making the capacitive elements voltage-tunable Figure 3a illustrates a conventional bridged low-pass tee with a voltage tunable capacitive element and Figure 3b illustrates a conventional bridged high pass tee with a voltage tunable capacitive element.

[0008] Figure 4 illustrates a response of a single, ideal all-pass section with $R = 1$ and $\omega_0 = 1$ and Q=1 as the capacitors are varied by a factor of two around the nominal design values specified in Figures 1a and 1b. Note that the maximum phase-shift occurs at the "center-frequency" of the design. Thus by properly choosing the inductor and capacitor values, the circuit can be designed for a prescribed center-frequency and characteristic impedance. Usually (but not always) the characteristic impedance is set at 50 Ohms for an RF circuit.

[0009] Phase-shifters based on lumped-element all-pass sections such as those in Figures 2a and 2b have been demonstrated with several different technologies for tunable capacitors. The article "A precise analog phase-shifter for SHF SATCOM phased arrays (N. E. Hodges and M. H. Yam, 1992 IEEE GaAs IC Symposium Digest, pp. 29-32) describes a phase-shifter using diode varactors. The article "A MMIC active phase shifter using variable resonant circuit" (A. Hayashi and M. Muraguchi, IEEE Transactions Microwave Theory Tech., vol. 47, Oct. 1999, pp. 2021-2026) and the article "A tunable all-pass MIC active phase shifter (D. Viveiros, D. Consonni, and A. K. Jastryebski, IEEE Transactions Microwave Theory Tech., vol. 50, August 2002, pp. 1885-1889) describes an all-pass phase-shifter using GaAs MESFETs. The article "2.4 GHz Continuously Variable Terroelectric Phase Shifters Using All-Pass Networks" (D. Kim et al., IEEE Microwave and Wireless Components Left, vol. 13, Oct. 2003, pp. 434-436) describes an all-pass phase-shifter using capacitors made from tunable dielectric materials. However, electronic phase-shifters using

all-pass section are not common, and at least one prominent textbook in this field fails to mention the topology (see, S. Koul and B. Bhat, Microwave and Millimeter-wave Phase Shifters, vol. II: Semiconductor and Delay-Line Phase Shifters, Artech House: Boston, MA, 1991.

[0010] One reason for the lack of interest in all-pass phase-shifter is that in many applications such as phased-array antennas, a voltage-variable phase-shift of up to 360 degrees is desirable. This is not practical with a single all-pass section, because extremely large capacitance tuning ratios are required, and the resulting changes in the characteristic impedance of the circuit result in severe impedance mismatches with the host system and consequently poor insertion-loss characteristics. In particular, conventional a single-all pass section provides a phase-shift of barely up to 90 degrees.

[0011] One attempt at solving this problem has been described in the Hodges and Yam and the Kim et al. articles previously referenced, where two identical all-pass sections have been cascaded to increase the phase-shift. However, this approach suffers from several drawbacks. First, the phase-versus-frequency response is not constant, as is desired in many applications. Second, the variation in characteristic impedance as the capacitors are tuned has an increasingly pronounced effect as the number of sections increases. This is severely exacerbated by non-idealities in the lumped elements, such as interwinding capacitance in the inductive elements, mutual inductive coupling between the inductive elements, or parasitic inductance in the interconnecting lines between adjacent all-pass sections.

[0012] From the above, there is a need for a phase shifter that provides phase shift over almost 360 degrees (or greater) and is relatively constant over a wider frequency range with a limited amplitude modulation over the range.

SUMMARY OF THE INVENTION(S)

[0013] To address the shortcomings in the related arts, a circuit topology is configured to flatten out a phase- and amplitude-response over a specified range of frequencies. The circuit topology also provides a large cumulative phase-shift.

[0014] In one embodiment, the circuit topology of a plurality of all-pass sections (or circuits) forms a cascaded configuration when coupled together. Each all-pass section has a center-frequency. The frequencies are staggered to create a substantially flat phase-response over a predetermined frequency range. Further, in one embodiment the plurality of all-pass sections has at least one all-pass section that is different from another all-pass section. Each

all-pass section includes a tunable capacitor and a center-frequency. Each center frequency is selected to obtain substantially constant amplitude and phase response over a desired frequency range and capacitance tuning range.

[0015] The circuit topology beneficially provides compact and broadband phase-shifters for phased-arrays using tunable capacitors. In one embodiment, the circuit topology provides a phase-shift to an RF signal over a desired range of frequencies. An advantage of the circuit topology is a flat phase versus frequency response over a wide range of frequencies. Further, the circuit topology also includes an advantage of little amplitude modulation over the frequency range and the bias states of the device. Moreover, the circuit topology can be configured as a device having a suitably small size.

[0016] The circuit topology overcomes many previous limitations of conventional varactor-based phase-shifters, particularly those requiring large phase-shifts in excess of 360-degrees. A conventional phase shifter with a single all-pass circuit does not provide greater than a 90-degree phase shift so such a device is inconsequential for configurations requiring a large phase-shift. Large phase-shifts are useful in certain applications, for example, phase-array antennas where theoretically 360-degree phase shifts are needed. However, due to conventional manufacturing and mechanical tolerances and errors in some instances more than a 360-degree phase shift is required, for example, a phase shift of up to 400-degrees.

[0017] In addition, the circuit topology may include a DC biasing circuit. Generally, a composite phase-shifter has numerous tunable capacitors so that direct current (DC) control biasing becomes complicated if control wires are run to each tunable capacitor. Thus, in one embodiment, capacitors and inductors are preferably connected so that all sections can be biased from a single DC control line that is resistively coupled to the input or output. This configuration beneficially reduces complexity and may provide other benefits such as reduced circuit layout size, which would allow for smaller device sizes.

[0018] The features and advantages described in the specification are not all inclusive and, in particular, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification, and claims. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and may not have been selected to delineate or circumscribe the inventive subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The invention has other advantages and features which will be more readily apparent from the following detailed description of the invention and the appended claims, when taken in conjunction with the accompanying drawings, in which:

[0020] Figures (FIGS.) 1a and 1b illustrate conventional bridged-tee circuits and design equations for realizing all-pass transfer functions.

[0021] Figures 2a and 2b illustrate conventional all-pass sections.

[0022] Figure 3a illustrates a conventional bridged low-pass tee with a voltage tunable capacitive element.

[0023] Figure 3b illustrates a conventional bridged high pass tee with a voltage tunable capacitive element.

[0024] Figure 4 illustrates a conventional response of a single, ideal all-pass section with R=1 and ω_0=1 and Q=1 as the capacitors are varied by a factor of two around the nominal design values specified in Figures 1a and 1b.

[0025] Figure 5 illustrates one embodiment of a response of an all-pass section with R=1 and ω_0=1 and Q=1 as the capacitors are varied, e.g., by a factor of two around the nominal design values illustrated in Figure 2.

[0026] Figure 6a illustrates one embodiment of a bridged low-pass with DC biasing circuit.

[0027] Figure 6b illustrates one embodiment of a bridged-high pass with a DC biasing circuit.

[0028] Figure 7a illustrates one embodiment of a cascade of bridged low-pass with DC biasing circuit sections.

[0029] Figure 7b illustrates one embodiment of a cascade of bridged low-pass and bridged high-pass with DC biasing circuit sections.

[0030] Figure 8 illustrates one embodiment of a cascade of bridged low-pass circuit sections.

[0031] Figure 9 illustrates one embodiment of an implementation (die photo) of a six-section all-pass phase shifter cascade, e.g., shown in Figure 8, using spiral inductors, thin-film resistors, and dielectric varactors.

[0032] Figure 10 illustrates one embodiment of an implementation (die photo) of solder bumps for flip-chip packaging.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0033] The Figures ("FIGS.") and the following description relate to preferred embodiments of the present invention by way of illustration only. It should be noted that from the following discussion, alternative embodiments of the structures and methods disclosed herein will be readily recognized as viable alternatives that may be employed without departing from the principles of the claimed invention.

[0034] Reference will now be made in detail to several embodiments of the present invention(s), examples of which are illustrated in the accompanying figures. It is noted that wherever practicable similar or like reference numbers may be used in the figures and may indicate similar or like functionality. The figures depict embodiments of the present invention for purposes of illustration only. One skilled in the art will readily recognize from the following description that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles described herein.

[0035] The disclosed embodiments include a circuit topology that flattens out a phase- and amplitude-response over a specified range of frequencies, and provides a large cumulative phase-shift. In one embodiment a circuit topology is configured to cascade three or more all-pass sections (circuits), with the center-frequencies of the all-pass sections staggered in such a way as to create a flat phase-response over a frequency range.

[0036] Figure 5 illustrates one example of a phase response of an all-pass section with R=1 and ω_0=1 and Q=1 as the capacitors are varied, e.g., by a factor of two around the nominal design values associated with circuit designs such as those illustrated in Figures 6a and 6b. In one embodiment, a circuit topology (configuration) to achieve the benefits drawn out in Figure 5 (e.g., constant or substantially constant phase response and/or amplitude) can be attained through a set of all-pass sections as further described herein, for example, with reference to Figures 7 and 8. It is noted that the actual number of sections that are needed is determined by the required total phase-shift and the bandwidth.

[0037] The circuit topologies as described herein provide compact and broadband phase-shifters for phased-arrays using tunable capacitors. The device provides a phase-shift to radio-frequency (RF) signal over a desired range of frequencies. One advantage of such a circuit topology is a flat phase versus frequency response over a wide range of frequencies, as well as little amplitude modulation over this frequency range and the bias states of the device. Moreover, the circuit topology can be packaged as a device having a small size. This

overcomes many previous limitations of varactor-based phase-shifters, particularly for those requiring large phase-shifts in excess of 360 degrees.

[0038] A composite phase-shifter typically includes numerous tunable capacitors so that DC control biasing can become complicated if control wires are run to each capacitor. Figure 6a illustrates one embodiment of a bridged low-pass with DC biasing circuit 605 which reduces such conventional complexity. The bridged low-pass with DC biasing circuit 605 has a topology that includes a modified bridge low-pass circuit 610, a shunt bias 620 and a ground 630. The shunt bias 620 includes a shunt resistance R_{bias} 620a coupled to a shunt ground 620b.

[0039] The modified bridge low-pass circuit 610 is derived from a conventional bridge low-pass circuit configuration, e.g., as shown in Figure 3a, by splitting a varactor (or tunable capacitor) C_1 into a series combination, $2C_1$ 610a, $2C_1$ 610b, and adding the shunt bias 620. The modified bridge low-pass circuit 610 couples a DC bias voltage signal (e.g., $V_{RF} + V_{DC}$) an input 615a and/or an output 615b that is then delivered to the varactors $2C_1$ 610a, $2C_1$ 610b, C_2 610c. It is noted that when symmetry is sought with respect to application of the DC bias voltage to the circuit 605, the DC bias voltage can be applied simultaneously to both terminals rather than to one terminal 615a or the other 615b.

[0040] Figure 6b illustrates one embodiment of a bridged-high pass with direct current (DC) biasing circuit 645. The bridged-high pass with DC biasing circuit 645 includes a bridged high-pass circuit 640 with an input 655a and an output 655b. In contrast to the bridged low-pass with DC biasing circuit 605 configuration, the bridged-high pass with DC biasing circuit 645 is less complex with respect to biasing. In particular, the DC bias voltage signal (e.g., $V_{RF} + V_{DC}$) at the input 655a and/or output 655b is applied across each varactor C1 665a, C1 665b by virtue of the inductor elements, which are DC shorts. Again, it is noted that when symmetry is sought with respect to application of the DC bias voltage signal to the circuit 645, the DC bias voltage can be applied simultaneously to both terminals rather than to one terminal 655a or the other 655b.

[0041] Thus, in configurations of the bridged low-pass with DC biasing circuit 605 or the bridged high-pass with DC biasing circuit 645, the varactors and inductors preferably are connected so that the circuit section can be biased from a single DC control line. In the bridged low-pass with DC biasing circuit 605, the DC biasing is resistively coupled to the input 615a, 655a or output 615b, 655b, while no additional resistance coupling is necessary for the high-pass with DC biasing circuit 645. In alternative embodiments, DC biasing

circuits such as those described in U.S. Patent No. 6,674,321, which is assigned to the same assignee as the present invention and the contents of which is hereby incorporated by reference, also can be used in the configurations disclosed.

[0042] The configurations for each bridged circuit 605, 645 described above can be used to create a topology that comprises two or more circuits 605, 645 of the same type assembled in a cascaded configuration. For example, Figure 7a illustrates one embodiment of a cascaded circuit 705 comprised of more than two bridged low-pass with DC biasing circuit 605a-*n* (generally 605) sections, where *n* references a last section.

[0043] In the illustrated configuration, each section of the cascaded circuit 705 generates a frequency-phase response curve with a center frequency as illustrated in Figure 5. For example, the first section 605a generates a frequency-phase response curve with a center frequency of f_1 in Figure 5. The second section 605b generates a frequency-phase response curve with a center frequency of f_2, and the nth section 605n generates a frequency-phase response curve with a center frequency of f_n. The cumulative frequency-phase response curves result in a composite frequency-phase response curve that provides a relatively flat phase over a variety of frequencies.

[0044] It is noted that as the DC biasing voltage (e.g., $V_{RF} + V_{DC}$) across the varactors ($2C_{1a}$) in the cascaded circuit 705 changes, the curve amplitude changes up or down. In turn, these changes correspond to a change in phase. Further, in the configuration illustrated in Figure 7a, at least some of the all-pass sections have different center frequencies. In the example shown, if the center frequencies are f_1, f_2 and f_3, and there are two all pass sections for each center frequency, there are many different combinations for the order of each all pass section (e.g., 605a, 605b, 605c (not shown)). In one embodiment, orders that "mix up" the different center frequencies (e.g., f_1, f_2, f_3, f_1, f_2, f_3) are generally preferred over those that do not (e.g., f_1, f_1, f_2, f_2, f_3, f_3). The staggering of center frequencies helps ensure sufficient peak values that allow for a composite frequency-phase response curve that is relatively flat over a particular frequency range.

[0045] As an illustrative example of the flexibility of the configuration disclosed, if a relatively flat phase is desired from 18 GHz to 22 GHz, the first section 605a of the cascaded circuit 705 could have a center frequency f_1 of just under 18 GHz while the nth section 605*n* of the cascaded circuit 705 could have a center frequency f_n of just over 22 GHz. As another illustrative example, a wider range for a flat phase the first section 605a could have a center frequency f_1 of just under 17 GHz, the nth section 605*n* could have a center frequency f_n of

just over 23 GHz and another section 605*x* (not shown) may have a center frequency f_x that is a geometric mean of 17 GHz and 23 GHz so that a relatively flat phase can be ensured from 18 GHz to 22 GHz. Thus, the claimed invention provides a relatively flat phase over predetermined wide (or narrow) frequency range.

[0046] The configuration described with respect to Figure 7a illustrates an example of a cascaded topology using modified bridged low-pass section 605. The principle disclosed and describe with respect to that configuration are also applicable to a modified bridged high-pass section 645. In these configurations, the same type of all-pass sections are used n the cascaded topology with schemes for staggering the center frequencies, for example, f_1- f_2- f_1- f_2- f_1- f_2 or f_1- f_1- f_2- f_2- f_1- f_1, etc.

[0047] In alternative embodiments, the cascaded topology can be configured to have a configuration that includes alternating types of all-pass sections, e.g., the modified bridged low-pass section 605 is followed by a different all-pass section, e.g., the modified bridged high-pass section 645, before repeating. The alternating type of all-pass section, along with their respective center frequencies, provides an advantage of amplitude flatness. The characteristic impedance of the two types of sections vary in opposite ways as the varactors are tuned so that the impedance mismatches average out to some extent.

[0048] By way of example, in one embodiment for a 18 GHz to 22 GHz frequency range, one section made from a bridged low-pass with a center frequency of f_1, and a another section using a bridged high-pass with a center-frequency of f_2. The cascade would then involve an alternating sequence of both sections. The configuration can have as few as one of each section 605, 645 or multiples of each section in an alternated configurations. An example of such a configuration is shown in Figure 7b with a modified bridge low-pass section 605 alternated with a modified bridge high-pass section 645.

[0049] Figure 8 illustrates an example embodiment of a cascade of bridged low-pass with DC biasing circuit in a dual ground configuration. In particular, for some monolithic implementations of an all-pass cascade topology using spiral inductors, the inductive elements may occupy a large area on the chip so that additional transmission-line sections may be inserted between adjacent elements. Although this may introduce series inductance between the sections leading to an undesired low-pass cutoff frequency in the structure, its effects can be reduced through multiple ground conductors that are electrically connected in off-chip packaging. This enables the all-pass sections to be clustered more closely together,

which allows for smaller device sizes. An example using two ground rails on opposite sides of the chip is shown in Figure 8.

[0050] In Figure 8, each section 815a-n is a bridged low pass with DC biasing circuit includes a modified bridge low-pass circuit 825 tied to a one ground rail 820 through varactor C_{2a} and shunt bias portion tied to another ground rail 810 through a bias resistance R_b. The DC bias voltage signal (e.g., $V_{RF} + V_{DC}$) traverses the cascaded circuit along the modified bridged low pass circuit 825. Topologically, the cascaded configuration appears as one section flipped (e.g., upside down or toggled) relative to its adjacent section. As with the configurations illustrated in Figures 6a, 6b, and 7, when symmetry is sought with respect to application of the DC bias voltage signal to the circuit, the DC bias voltage signal can be applied simultaneously to both terminals rather than to one terminal or the other.

[0051] As noted, the cascaded circuit configuration (topology) illustrated in Figure 8 beneficially allows for more compact circuit designs. For example, Figure 9 illustrates one embodiment of an implementation (e.g., die photo showing physical layout) of a six-section all-pass phase shifter cascade, e.g., as shown in Figure 8, using spiral inductors, thin-film resistors, and dielectric varactors. The configuration illustrated in Figure 9 shows a relatively large layout footprint for a bias resistance R_b 935, but, a relatively very small layout footprint for the modified bridge low pass circuit 825 ($L + 2C_{1a}$ 825a and C_{2a} 825b). Further, the illustrated die shows compactness with respect to how all the components fit together with minimal "open space" on the die.

[0052] Figure 10 illustrates one embodiment of an implementation (die photo) of solder bumps 1010 for flip-chip packaging. The illustrated embodiment allows for small solder bump 1010 sizes, e.g., 100 micrometers.

[0053] The bridged low-pass with DC biasing circuit beneficially allows for more compact circuit designs and layouts. The bridged high pass with DC biasing circuit beneficially allows for simpler DC voltage biasing. Hence, the disclosed all pass circuits in a cascaded configuration also advantageously provides flexibility in circuit designs.

[0054] In general, it is noted that for the cascaded configurations, monolithic implementations are preferred for small-size and low-cost. For example, on-chip spiral inductors are a preferred method for implementing the inductive elements in each section. Multiple-layer spirals are preferred for minimizing the die area occupied by the inductors. Monolithic varactor technologies that can be easily integrated with spiral inductors are preferred. Some examples are dielectric varactors using BST materials or other voltage-

variable dielectrics (strontium titanate (STO), barium titanate (BTO), barium strontium titanate (BST), bismuth zinc niobate (BZN), etc.), or semiconductor diodes using silicon (Si), gallium arsenide (GaAs), silicon germanium (SiGe), etc., or micro-electro-mechanical (MEMS) devices. Tunable capacitors can be made using BST-based technology, for example as described in U.S. Patent Application No. 10/822,563, "Fabrication of Parallel Plate Capacitors Using BST Thin Films," which is incorporated herein by reference.

[0055] By way of example, one embodiment of a phase shifter in accordance with the principles disclosed herein is a 42 GHz phase shifter using thin-film BST on sapphire technology. The phase shifter can be configured for use in a 40 GHz to 44 GHz range with a 360 degree minimum phase shift using a control voltage range from 0 V to 20 V. In such configurations, the maximum insertion loss is 10 dB and a return loss is greater than or equal to 6 dB. Hence, such a configuration would provide continuous and precise analog control with a highly uniform group delay, good power handing (e.g., greater than +20 dBm), all within a compact die size (e.g., 1.0 mm x 0.85 mm size). Moreover, configurations such as this example would have virtually no control-circuit power consumption due to its single control line configuration as previously described.

[0056] Upon reading this disclosure, those of skill in the art will appreciate still additional alternative structural and functional designs for a system and a process for an analog phase shifter using voltage tunable capacitor (varactor) through the disclosed principles of the present invention. Thus, while particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and components disclosed herein and that various modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present invention disclosed herein without departing from the spirit and scope of the invention as defined in the appended claims.

CLAIMS

WHAT IS CLAIMED IS:

1. A phase shifter comprising:

a plurality of all-pass sections, each all-pass section including a first tunable capacitor and having a center-frequency different from another all-pass section, each center frequency selected to provide a composite response corresponding to a substantially constant phase response over a predetermined frequency range.

2. The phase shifter of claim 1, wherein the first tunable capacitor of an all-pass section of the plurality of all-pass sections comprises a dielectric varactor.

3. The phase shifter of claim 2, wherein the dielectric varactor comprises a material from a group consisting of strontium titanate (STO), barium titanate (BTO), barium strontium titanate (BST), and bismuth zinc niobate (BZN).

4. The phase shifter of claim 1, wherein the first tunable capacitor of an all pass section of the plurality of all-pass sections comprises a semiconductor diode varactor.

5. The phase shifter of claim 4, wherein the semiconductor diode varactor comprises a material from a group consisting of silicon, gallium arsenide, and silicon germanium.

6. The phase shifter of claim 1, wherein the first tunable capacitor of an all pass section of the plurality of all-pass sections comprises a micro-electro-mechanical (MEMS) device.

7. The phase-shifter of claim 1, wherein each all-pass section further comprises:

an input and an output, the first tunable capacitor connected between the input and the output;

a plurality of series-connected inductors connected between the input and output; and

a second tunable capacitor connected between a junction of the plurality of series-connected inductors and a ground.

8. The phase-shifter of claim 7, wherein the first tunable capacitor between the input and output comprises:

a plurality of series-connected tunable capacitors; and

a biasing resistor connected between a junction of the series-connected tunable capacitors and the ground.

9. The phase-shifter of claim 7, wherein the series inductors comprise an on-chip spiral inductor.

10. The phase-shifter of claim 7, wherein the series inductors comprise a distributed element.

11. The phase-shifter of claim 10, wherein the distributed element comprises a transmission-line segment.

12. The phase-shifter of claim 7, wherein the ground comprises a common ground conductor.

13. The phase-shifter of claim 7, wherein the ground comprises a plurality of ground conductors.

14. The phase-shifter of claim 13, wherein the plurality of ground conductors is configured for electrical coupling during packaging of the phase shifter.

15. The phase-shifter of claim 7, further comprising direct current (DC) blocking capacitors at the input and output.

16. The phase-shifter of claim 15, further comprising a bias voltage source configured to apply a bias voltage to the tunable capacitors in the circuit.

17. The phase-shifter of claim 15, further comprising a resistor coupled with a DC control voltage to one of the input, the output, and a signal path between the input and the output.

18. The phase-shifter of claim 7, where an inductor is included in series with the second shunt tunable capacitance.

19. The phase-shifter of claim 1, wherein each all-pass section further comprises:
an input and an output, the first tunable capacitor comprising a plurality of tunable capacitors connected in series between the input and output;
a first inductor connected between the input and the output; and
a second inductor connected between a ground and a junction of two tunable capacitors of the plurality of tunable capacitors connected in series.

20. The phase-shifter of claim 19, wherein the series inductors comprise an on-chip spiral inductor.

21. The phase-shifter of claim 19, wherein the series inductors comprise a distributed element.

22. The phase-shifter of claim 21, wherein the distributed element comprises a transmission-line segment.

23. The phase-shifter of claim 19, wherein the ground comprises a common ground conductor.

24. The phase-shifter of claim 19, wherein the ground comprises a plurality of ground conductors.

25. The phase-shifter of claim 24, wherein the plurality of ground conductors is configured for electrical coupling during packaging of the phase shifter.

26. The phase-shifter of claim 19, further comprising direct current (DC) blocking capacitors at the input and output.

27. The phase-shifter of claim 26, further comprising a resistor coupled with a DC control voltage to one of the input, the output, and a signal path between the input and the output.

28. The phase-shifter of claim 19, further comprising a third inductor connected in series with the first inductor between the input and the output.

29. A phase shifter comprising:

a low-pass bridged section, including a tunable capacitor and having a first center-frequency;

a high-pass bridged section, including a tunable capacitor and having a second center frequency, the high-pass bridged section coupled with the low-pass bridged section, the first and the second center frequencies selected to provide composite response corresponding to a substantially constant phase response over a predetermined frequency range.

30. The phase shifter of claim 29, wherein the high-pass bridged section couples with a second low-pass bridged section including a tunable capacitor and having a third center frequency, the third center frequency selected to provide a composite response corresponding to a substantially constant phase response over a predetermined frequency range.

31. The phase shifter of claim 30, wherein the second low-pass bridged section couples with a second high-pass bridged section including a tunable capacitor and having a fourth center frequency, the fourth center frequency selected to provide a composite response corresponding to a substantially constant phase response over a predetermined frequency range.

32. The phase shifter of claim 29, wherein the tunable capacitor of the bridged low-pass section and the tunable capacitor of the bridged high-pass section each comprises a tunable dielectric.

33. The phase shifter of claim 32, wherein the tunable dielectric comprises one from a group consisting of strontium titanate (STO), barium titanate (BTO), barium strontium titanate (BST), and bismuth zinc niobate (BZN).

34. The phase shifter of claim 29, wherein the tunable capacitor of the bridged low-pass section and the tunable capacitor of the bridged high-pass section each comprises a semiconductor diode varactor.

35. The phase shifter of claim 34, wherein a semiconductor diode varactor comprises a material from a group consisting of silicon, gallium arsenide, and silicon germanium.

36. The phase shifter of claim 29, wherein the tunable capacitor of the bridged low-pass section and the tunable capacitor of the bridged high-pass section each comprises a micro-electro-mechanical (MEMS) device.

$$L_1 = \frac{R}{\omega_0}$$
$$C_1 = \frac{1}{2R\omega_0}$$
$$C_2 = \frac{2}{R\omega_0}$$

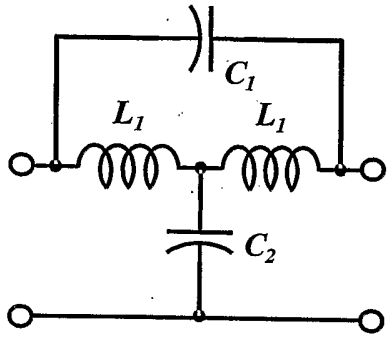
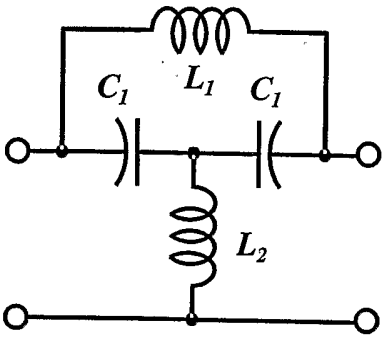


FIG. 1a



$$L_1 = \frac{2R}{\omega_0}$$
$$C_1 = \frac{1}{R\omega_0}$$
$$L_2 = \frac{R}{2\omega_0}$$

FIG. 1b

$$L_1 = \frac{RQ}{\omega_0}$$
$$C_1 = \frac{Q}{2R\omega_0}$$
$$L_2 = \frac{R\left(Q^2-1\right)}{2Q\omega_0}$$
$$C_2 = \frac{2}{RQ\omega_0}$$

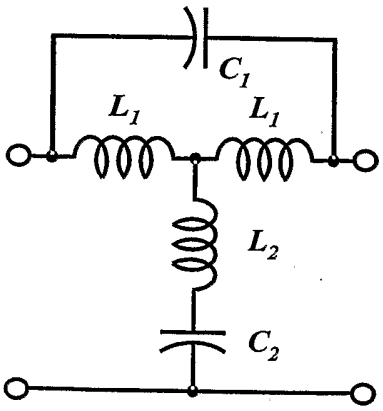
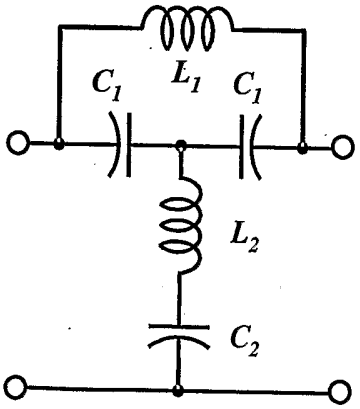


FIG. 2a



$$L_1 = \frac{2R}{Q\omega_0}$$
$$C_1 = \frac{Q}{R\omega_0}$$
$$L_2 = \frac{QR}{2\omega_0}$$
$$C_2 = \frac{2Q}{R\left(Q^2-1\right)\omega_0}$$

FIG. 2b

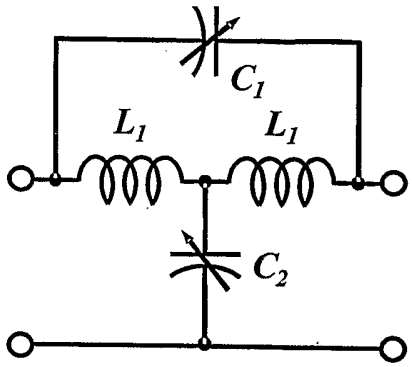


FIG. 3a

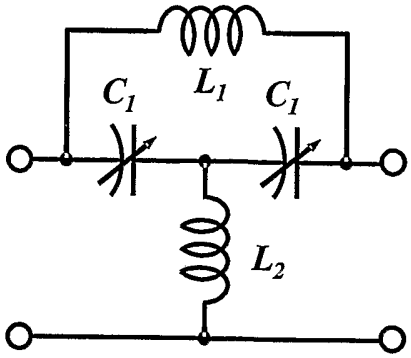


FIG. 3b

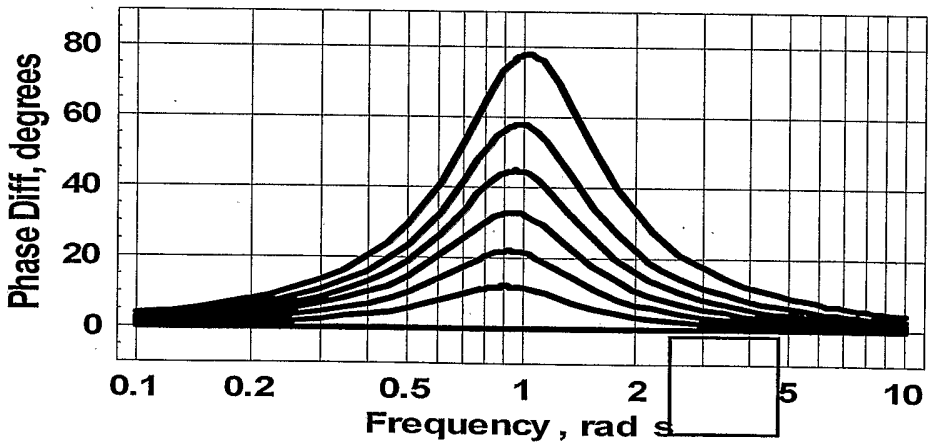


FIG. 4

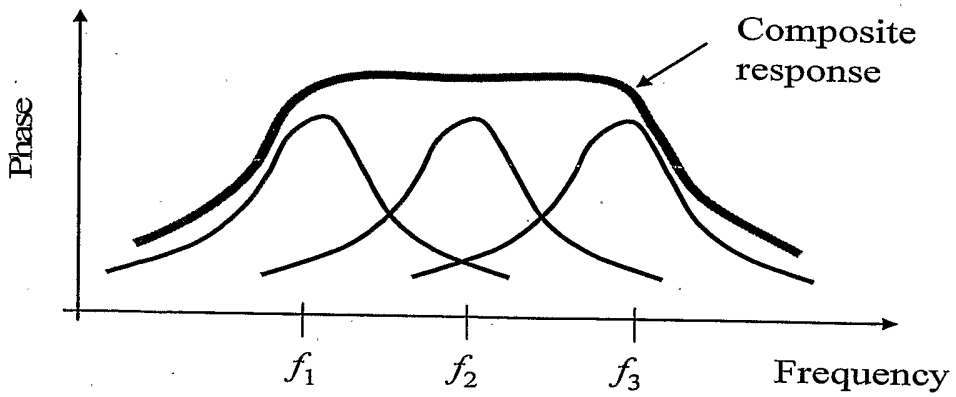


FIG. 5

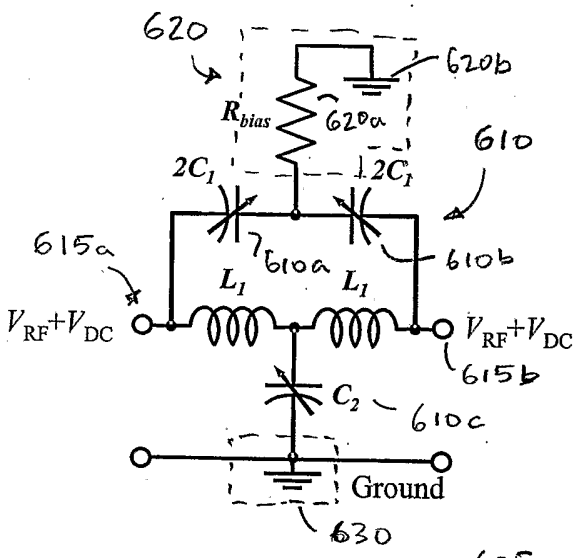


FIG. 6a

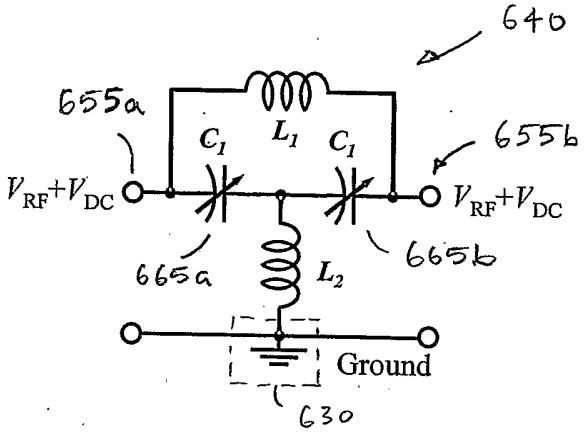


FIG. 6b

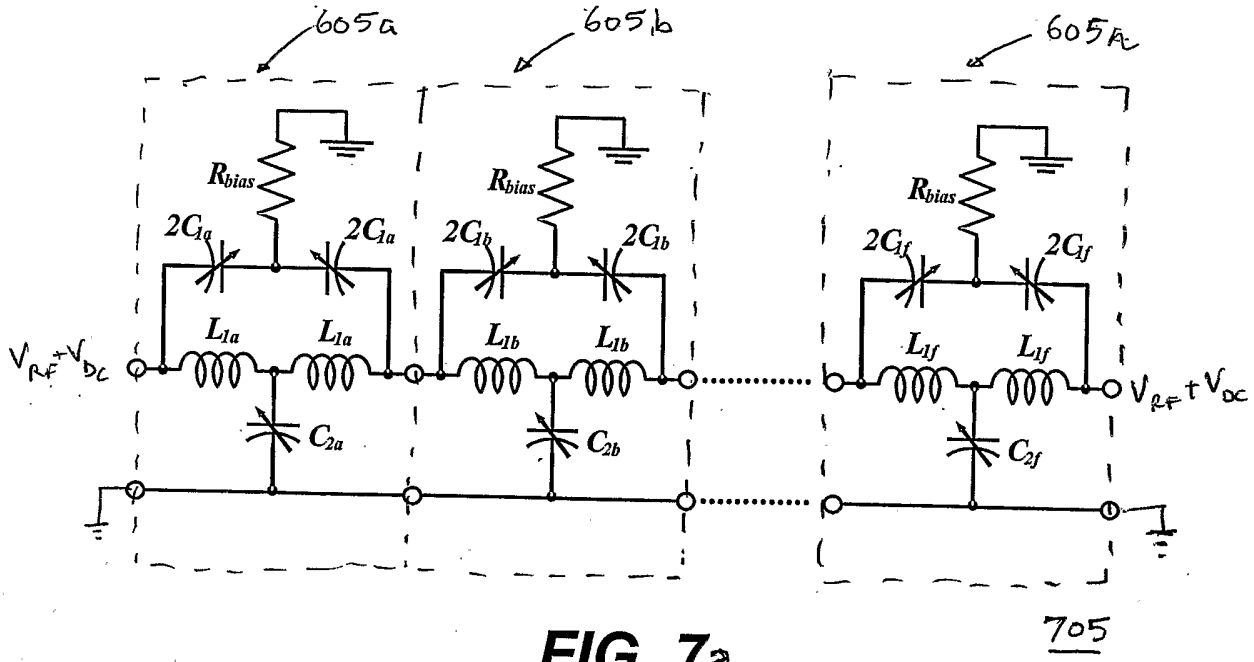

605a
605b
605c
R_{bias}
$2C_{1a}$
$2C_{1b}$
$2C_{1f}$
L_{1a}
L_{1b}
L_{1f}
$V_{RF}+V_{DC}$
C_{2a}
C_{2b}
C_{2f}
705

FIG. 7a

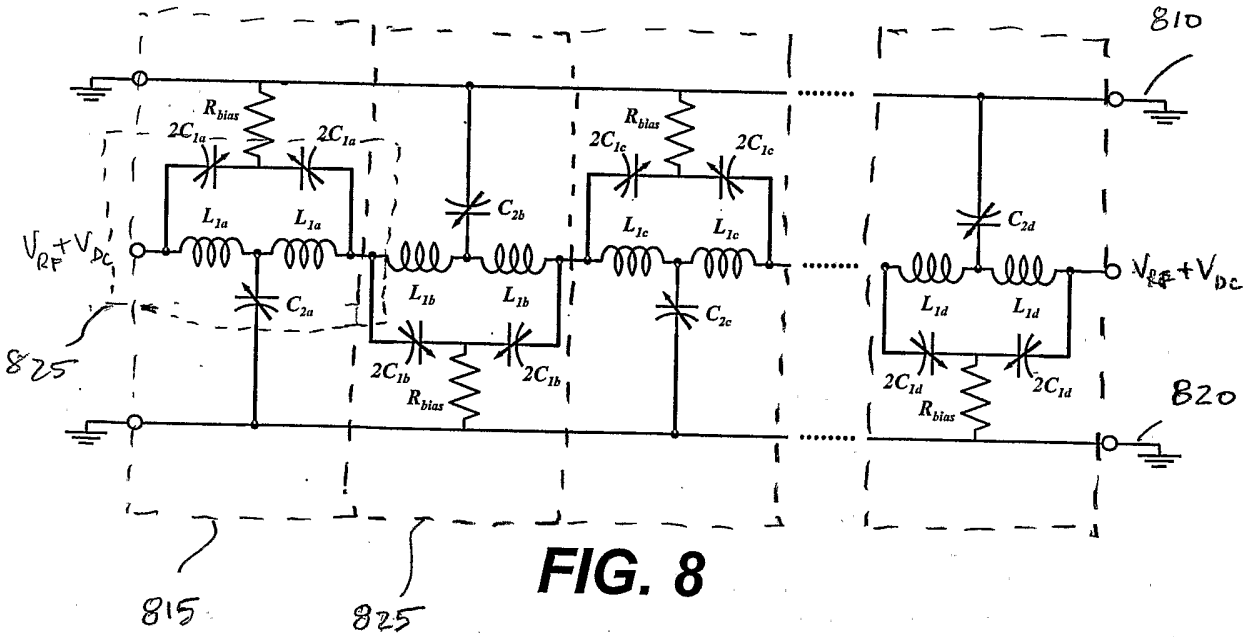

810
R_{bias}
$2C_{1a}$
$2C_{1b}$
$2C_{1c}$
$2C_{1d}$
L_{1a}
L_{1b}
L_{1c}
L_{1d}
C_{2a}
C_{2b}
C_{2c}
C_{2d}
$V_{RF}+V_{DC}$
825
820
815
825
805

FIG. 8

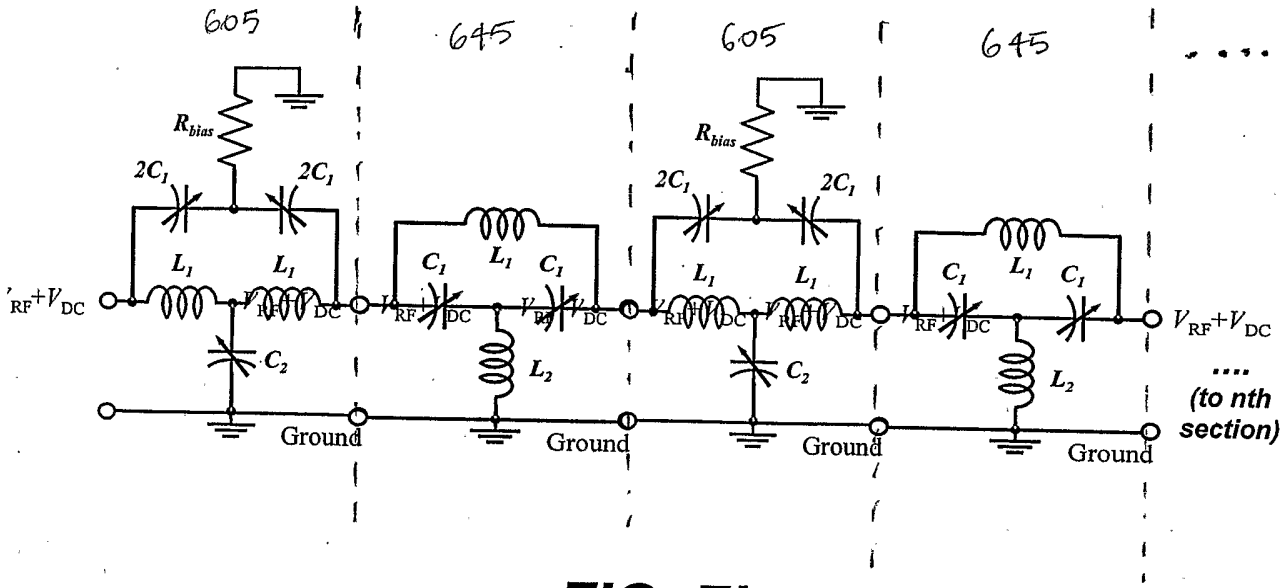

605
645
605
645
R_{bias}
$2C_1$
$2C_1$
L_1
L_1
C_1
L_1
C_1
$V_{RF}+V_{DC}$
C_2
L_2
Ground
Ground
Ground
Ground
$V_{RF}+V_{DC}$
....
(to nth section)

FIG. 7b

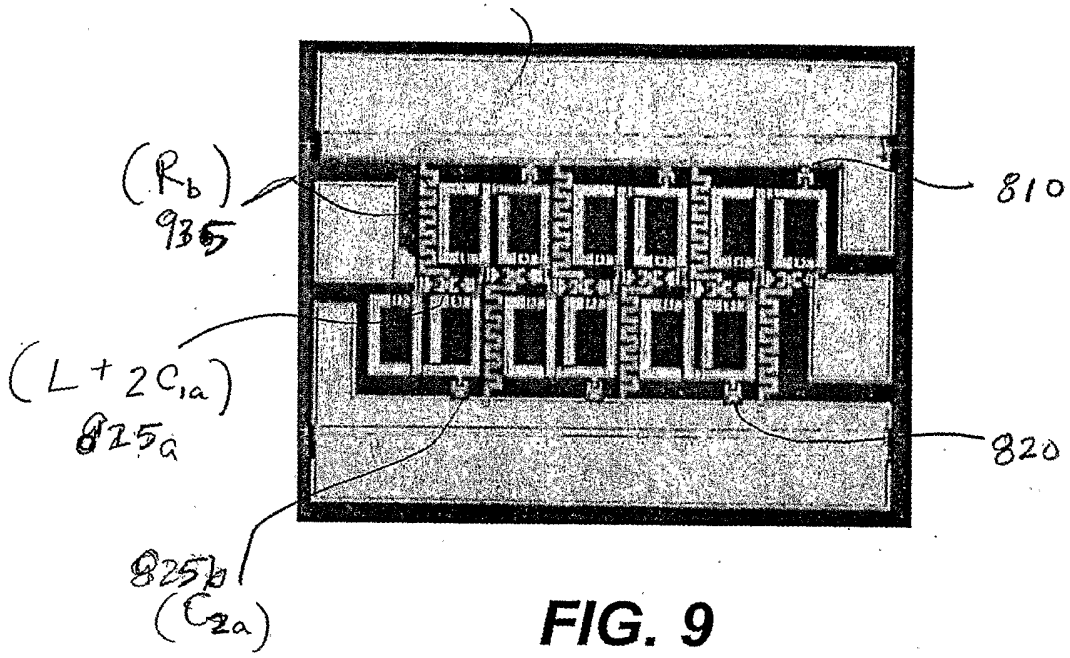


FIG. 9

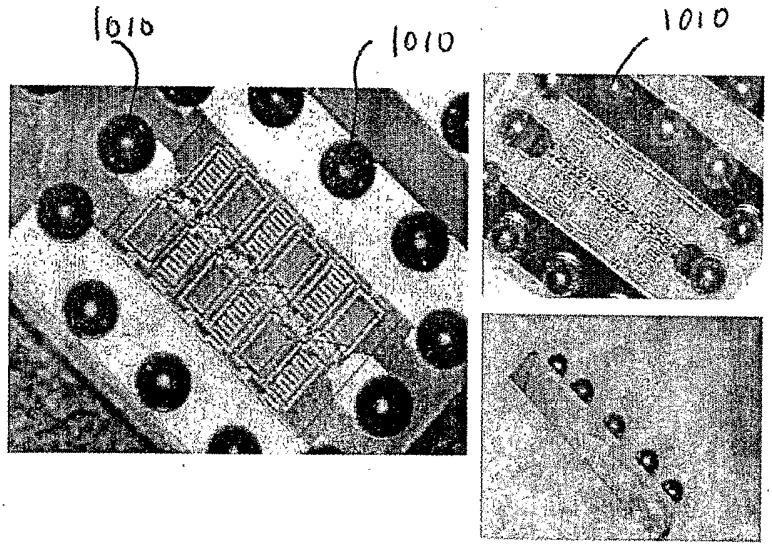


FIG. 10